Three Phase PFC Converter With Multilevel Inductive Switching Network

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***Abstract*—The rising power requirement of the on-board charger demands high efficiency and high power density in the three-phase power factor correction (PFC) converters. However, due to the large volume of boost inductors and filters of the conventional two-level converters, their power density is limited. In this article, multilevel inductive switching network (MISN) modules based on low-voltage switches are arranged in series at the ac-side to reduce the large size of inductors and filters. Besides, the operating principle and control strategy of the three-phase MISN-PFC converter are analyzed. In addition, to determine the multiple variables of the MISN module, the design methodology is proposed based on the loss model and volume model for the multilevel converter. Finally, a 10 kW prototype has been established to verify the analysis, where 99% efficiency at full load and 430 W/in^3 power density are achieved.**

***Index Terms*—High power density, multilevel inductive switching network (MISN), multilevel converter, three-phase power factor correction (PFC).**

I. Introduction

DRIVEN by the trend of low-carbon transportation, electric vehicles (EVs) entered the climax of development [1], [2]. The manufacturers of EVs are continually upgrading the batteries' capacity and charging power to alleviate the problem of range anxiety. Meanwhile, the power of OBCs has been upgraded from 3.3 kW [3] to more than 6 kW [4], and further to 10 or 20 kW through three-phase charging [5]. Although the charging process can be completed more quickly by fast dc charging or replacing batteries, considering the inadequate infrastructure, the cost-effective high power three-phase OBCs are more attractive to the market [6].

Owing to the limited space in EVs, high efficiency and high power density have become important requirements for the high power OBCs. In conventional applications, the two-level [7], [8] and three-level converters [9] are widely used as the front-end PFC converter. However, their bulky filters and boost inductors usually occupy half the size of the converters, resulting in limited power density. To pursue higher efficiency and density, the switching frequency was increased through the ZVS soft switching technique in [10], [11], [12], [13], and [14]. But, the power density is less than 300 W/in^3, because the volume of filters and inductors are still dominantly in large size.

In recent years, multilevel converters have shown the advantages of high efficiency and high density. In [15], a unified switch loss model for the multilevel converter was proposed. It is revealed that low-voltage switches can easily realize high efficiency of the converter for the lower new figure-of-merit (NFoM) [16], [17]. Besides, the multilevel converter could reduce the volt-second of inductor, and significantly cut down its volume. The flying-capacitor (FC) multilevel converter has been used in single-phase ac–dc [18], [19], and dc–ac [20], [21] for kW-level applications, which improves the power density to 500–1000 W/in^3 (excluding the bus capacitors), and maintaining over 99% peak efficiency. However, because of the nested connection between cells, the transient voltage stress will increase by 50%–100% [22] when a short-circuit fault happens, and it is also inconvenient to bypass the faulty cells. Moreover, the cascaded H-bridge (CHB) converter also attracts some attentions [23], which is modularized with several full-bridge cells, and has similar performance in loss and volume. Through detecting and simply bypassing the faulty cell [24], the reliability of CHB converter can be promoted. A 2 kW 1400 W/in^3 (excluding bus capacitors) CHB-PFC prototype was presented in [25] and its efficiency reached 99% from half to full load. Nevertheless, the CHB converter requires multiple isolated dc–dc converters to realize single output, which makes the system complex. The multibus structure means multiple common-mode conduction paths, resulting in severe EMI problems [26]. A low-cost PFC converter is proposed in [27], which uses a series filter circuit to reduce the bulky inductor for the single-phase diode rectifier in 110 V power system. There are some problems in this topology. Due to the diode based rectifier bridge, its output voltage is unregulated. And when it is applied to high bus voltage applications, the voltage stress of the filter circuit will be increased, leading to larger switching loss of the filter circuit. But it is worth noting that [27] presented a possibility for multilevel converters to be compatible with single output bus and modularization. For example, in the medium and high power system [28], [29], similar ideal has been adopted to build multilevel converter for its smaller footprint structure and dc fault blocking capability. However, since the existing works only concentrate on the operating principle and control method, there is a lack of

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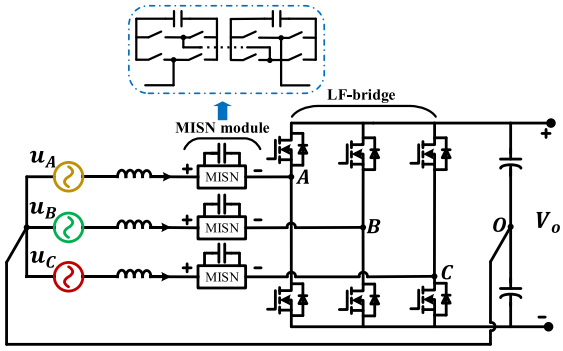

Fig. 1. Schematic of three-phase MISN-PFC converter.

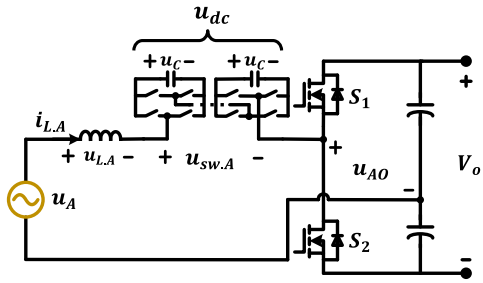

Fig. 2. Equivalent circuit for phase-A.

design methodology to achieve high efficiency and high power density.

This article presents a three-phase multilevel PFC converter with single output bus and good modularization capability, which can be used in the EV system in demand for high efficiency and high power density. As shown in Fig. 1, three multilevel inductive switching network (MISN) modules, which are constructed with H-bridge cells, are arranged in series to reduce the volt-second of the inductors. Thanks to the low NFoM of low-voltage switches of MISN modules, the loss of the designed MISN-PFC converter can be reduced compared with traditional two-level counterparts with high-voltage switches. Besides, the modified current loops with transient compensation are proposed to realize the cooperative operation for the three-phase MISN modules and LF-bridge, so that the current distortion can be avoided. And independent voltage control loops are utilized to keep all of the capacitors' average voltage identical. In addition, design methodology for the MISN-PFC converter is also provided based on the loss and volume models. Finally, a 10 kW prototype has been built to verify the effectiveness of the proposed control strategy and design method. More details about the MISN-PFC converter and the experimental results are presented in this article.

II. Operating Principle of the MISN-PFC Converter

A. Single-Phase Equivalent Circuit

When connected with the three-phase grid, the MISN-PFC converter is configured with the three-phase four-wire connection, and its related single-phase equivalent circuit (e.g., phase-A) can be easily derived in Fig. 2. The MISN module is composed of several low-voltage H-bridge cells and driven by the carrier-phase-shift pulsewidth modulation (PWM) modulation [30]. Consequently, increasing the cell number of the MISN module will reduce the inductor's volt-second, resulting in a smaller size of the inductor and filter. Additionally, the high voltage bridge on the right is used for line-frequency rectification, known as the line-frequency bridge (LF-bridge).

Detailed operating waveforms at steady state are shown in Fig. 3. The input voltage of phase-A u_A and the mid voltage of LF-bridge u_{AO} are presented in the first row. In order to achieve the minimum inductor voltage level, the MISN module generates

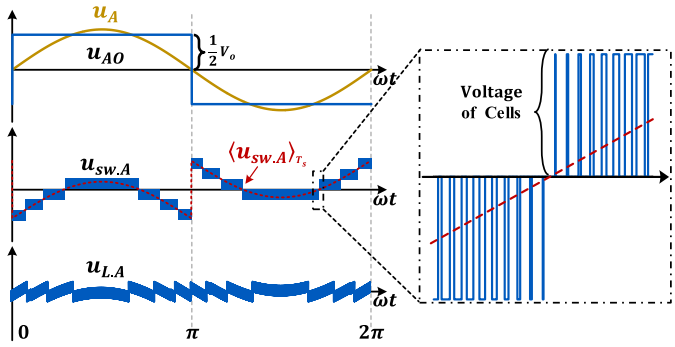

Fig. 3. Voltage waveforms of phase-A, including input voltage u_A, LF-bridge mid voltage u_{AO}, MISN module port voltage $u_{\mathrm{sw}.A}$, and inductor voltage $u_{L.A}$.

the multilevel voltage $u_{\mathrm{sw}.A}$ to cancel the voltage difference between u_A and u_{AO} and the switching cycle average of $u_{\mathrm{sw}.A}$ satisfies (1), which is shown as the red dashed line in the second row

$$\langle u_{\mathrm{sw}.A}\rangle_{T_s} \approx u_A - u_{AO}. \tag{1}$$

The behavior of the MISN module is similar to the CHB converter with no load, and its multilevel port voltage $u_{\mathrm{sw}.A}$ is constructed with the voltage of cells' capacitors. From the enlarged position in Fig. 3, the amplitude of each voltage level is clamped by the capacitors, and the frequency of $u_{\mathrm{sw}.A}$ is increased to $2N_C$ times of the switching frequency, in which N_C is the cell number of the MISN module. Therefore, the volt-second of the inductor is limited, as shown in the third row of Fig. 3. Compared with the two-level converter, smaller inductor and filter are needed under the same input current total harmonic distortion (iTHD) restriction.

B. Steady Condition for the MISN Module

In essence, the MISN module helps the inductor store the energy and diminish its volume, thus it can be equivalent to an inductor, which is made of semiconductors and capacitors. This is the reason why this multilevel module is named after MISN.

Similar to the volt-second balance of the inductor, keeping the MISN module in a charge-discharge balanced state is necessary. This means that the input power from the grid is transmitted to the load directly. Assuming an ideal power factor correction, the power is mainly delivered by the line-frequency voltage and

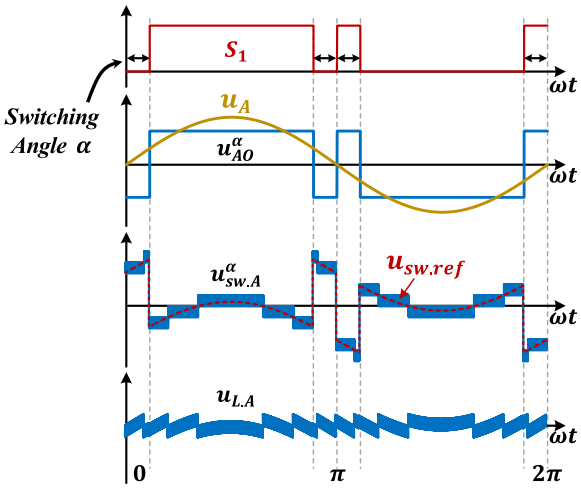

Fig. 4. Voltage waveforms of phase-A with switching angle α.

current, so the power $P_{\text{MISN}.A}$ absorbed by the MISN module is derived as

$$P_{\text{MISN}.A} = \left(U_A - U_{AO}^{1st}\right) \cdot I_{L.A} \tag{2}$$

where U_A, $I_{L.A}$ are the RMS value of u_A, $i_{L.A}$, respectively. U_{AO}^{1st} is the RMS value of the fundamental component of u_{AO}.

When the power is balanced in the MISN module, $P_{\text{MISN}.A} = 0$, and U_{AO}^{1st} should be equaled to U_A. Based on the Fourier series decomposition, the fundamental component of u_{AO} is

$$u_{AO}^{1st} = \frac{2V_o}{\pi} \sin(\omega t) \tag{3}$$

in which V_o is the output voltage.

By combining (2) and (3), the condition for power balance of MSIN module is

$$V_o = \frac{\sqrt{2}\pi}{2} U_A. \tag{4}$$

According to (4), for the steady operation of the MISN module, the output voltage is unregulated. To obtain a regulated output voltage, the duty cycle of u_{AO} should be adjusted according to the input voltage. Here, a switching angle α is added to u_{AO} to change the amplitude of U_{AO}^{1st}, and the control signal for S_1 are shown in the first row of Fig. 4. Due to the central symmetry of the switching angle in line cycle, there are only odd components in u_{AO}^{α}

$$u_{AO}^{\alpha} = \sum_{n=13,5\ldots} \frac{2V_o}{n\pi} \left(2\cos\alpha - 1\right) \sin(n\omega t). \tag{5}$$

The MISN module operates in the same way to cancel the voltage difference, and the waveform of $u_{\text{sw}.A}^{\alpha}$ is presented in the second row in Fig. 4. At this time, $P_{MISN.A}^{\alpha}$ and the steady condition are influenced by α, which are given as

$$P_{\text{MISN}.A}^{\alpha} = \frac{\sqrt{2}I_{L.A}}{\omega_0} \left[\sqrt{2}\pi U_A - V_o\left(4cos\alpha - 2\right)\right] \tag{6}$$

$$V_o = \frac{\sqrt{2}\pi}{4\cos\alpha - 2} U_A \tag{7}$$

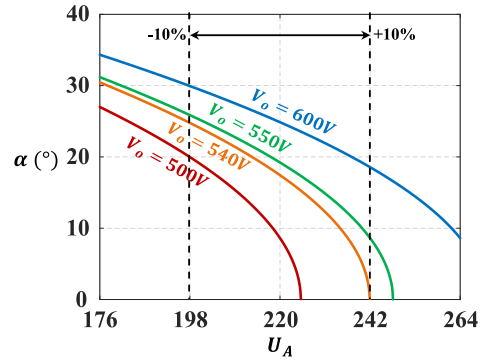

Fig. 5. Requirement for input voltage and switching angle under different output voltage. (red: $V_o = 500\,\text{V}$, orange: $V_o = 540\,\text{V}$, green: $V_o = 550\,\text{V}$, blue: $V_o = 600\,\text{V}$).

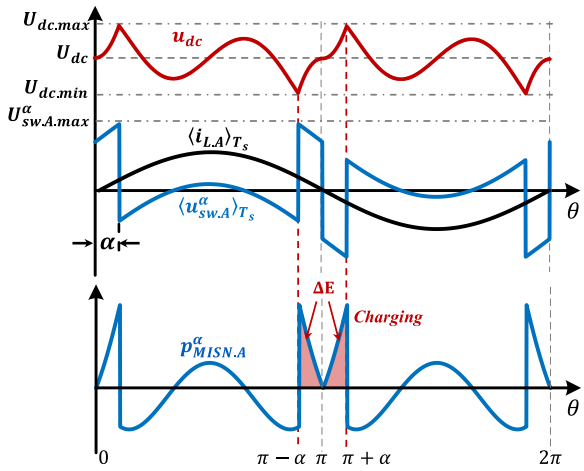

Fig. 6. DC-side voltage and input power of the MISN module.

where ω_0 is the angular frequency of the grid.

According to (7), the limitation for input voltage and switching angle is shown in Fig. 5 under the given output voltage. In the picture, the x-axis represents the RMS value of the input phase voltage, and y-axis is the switching angle. Combined with (6), it can be known that the operation points on the curve in Fig. 5 represents the balanced state for the MISN module, the operation points above the curve is the charging state, and the operation points below the curve is the discharging state.

C. Voltage Limitation for the MISN Module

As mentioned before, the MISN module is similar to the CHB circuit, thus, its dc-side voltage u_{dc} should be higher than the ac-side voltage to avoid losing control of the inductor current. As shown in Fig. 6, the input power p_{MISN}^{α} of the MISN module is given in the third row based on the switching cycle average of $u_{sw.A}^{\alpha}$ and $i_{L.A}$ in the second row. Therefore, the dc-side voltage u_{dc} can be derived with the conversation of energy, and drawn in the first row. The capacitor is charged from $U_{\text{dc.min}}$ to $U_{\text{dc.max}}$ with the energy ΔE in the interval of $[\pi - \alpha,\ \pi + \alpha]$

$$\Delta E = \frac{1}{\omega_0} \int_{\pi-\alpha}^{\pi+\alpha} p_{\text{MISN}}^{\alpha}(\theta)\, d\theta. \tag{8}$$

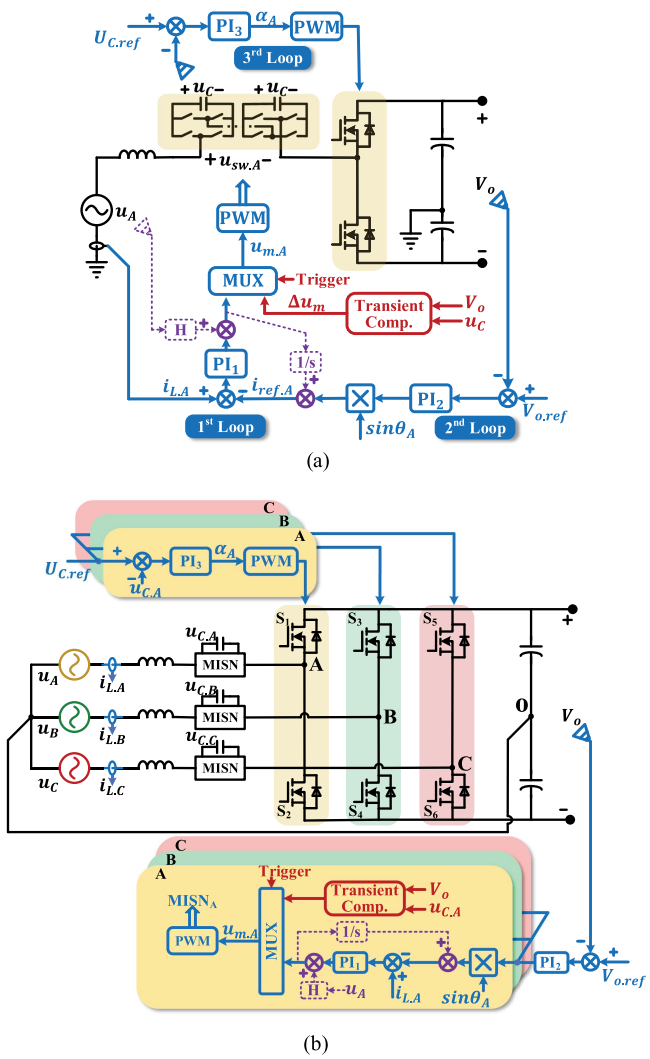

Fig. 7. Schematic of the MISN-PFC converter. (a) Control diagram for phase-A equivalent circuit. (b) Control diagram for 3-phase converter.

Consequently, the voltage limitation is

$$\begin{cases} U_{\text{dc.min}} \geq U^{\alpha}_{\text{sw}.A.\text{max}} \\ U^{\alpha}_{sw.A.\text{max}} = u_A(\alpha) + \frac{1}{2}V_o \end{cases} \tag{9}$$

where $U_{\text{dc.min}}$ is the minimum value of u_{dc}, while $U^{\alpha}_{\text{sw}.A.\text{max}}$ is the maximum value of the ac-side voltage.

III. Control Strategy for the MISN-PFC Converter

In this part, the current tracking for the power factor correction and the voltage control of capacitors for the output bus as well as the MISN module are discussed. The control diagram of MISN-PFC converter is shown in Fig. 7, where Fig. 7(a) is for the single-phase equivalent circuit to illustrate the control method, and Fig. 7(b) is the complete control system.

A. Three-Loop Control Strategy for the MISN-PFC Converter

The control system is basically constructed with three loops: first current loop for PFC, second voltage loop for output voltage regulation, and third voltage loop for MISN voltage balance, which are drawn in blue color in Fig. 7(a).

In the first current loop, the inductor current is controlled by the high-frequency switching network, i.e., MISN module. The duty cycle of $u^{\alpha}_{\text{sw}.A}$ is determined by the output value of the PI_1, so that the inductor current can be forced to follow the reference. In order to obtain a regulated output voltage, the second voltage loop adjusts the amplitude of reference current to manage the power flow. For example, if V_o is smaller than the normal value, the second voltage loop will increase the current amplitude, then more energy will be delivered to the output bus to boost the voltage, and vice versa. As illustrated in Fig. 5, to keep the MISN module stable under a regulated V_o, the switching angle α needs to be modified according to the input voltage. Furthermore, the dc-side voltage u_{dc} of the MISN module should be controlled to meet with (9). Therefore, the third voltage loop is added to control the charging and discharging of the MISN module by α to realize the normal operation of the converter.

B. Transient Compensation

For the purpose of a good voltage cancellation, $u^{\alpha}_{sw.A}$ should be altered quickly when the LF-bridge switches, as demonstrated in Fig. 4. However, due to the inertia of PI compensator in the current loop, the slope of the modulation signal $u_{m.A}$ is limited, which will cause large current distortion and even make the inductor saturated. Therefore, a transient compensation control is added to modify $u_{m.A}$ rapidly, as shown in red line in Fig. 7(a). According to Fig. 4, to minimize the current distortion, the voltage jumps of $u^{\alpha}_{sw.A}$ should be same as that of u^{α}_{AO}, which equals to V_o. Then the value of the transient compensation signal can be calculated:

$$\Delta u_m = \pm \frac{V_m V_o}{2N_C u_C} \tag{10}$$

where V_m is the peak value of the triangular carrier, u_C is the voltage of the sampled cell of the MISN module, and the polarity is dependent on the direction of the voltage jumps.

As shown in Fig. 7, the red part represents the transient compensation, V_o and u_C is sampled to calculate the compensation value Δu_m. The transient compensation is triggered based on the driving signal of the LF-bridge, and Δu_m will be added to the output of PI_1 every time the edge of u^{α}_{AO} is detected.

C. Other Auxiliary Control

As revealed in [31], the small inductance of the multilevel converter results in difficulties for achieving unity PF. Some efforts, such as feedforward compensation [32], have been taken to solve this problem. Besides, influenced by the zero order current, the voltage of the split output capacitors is unbalanced, and a novel control method in [33] is adopted to reduce the zero order current and balance the output voltage. These two modifications are presented with purple dashed line in Fig. 7, and the detailed analysis is neglected since they're not the key points in this article.

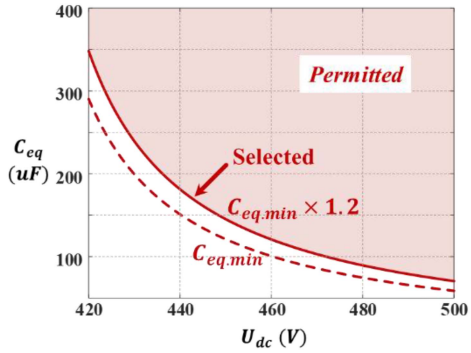

Fig. 8. Feasible combinations of C_{eq} and U_{dc}, when $P = 10\,\text{kW}$, and $V_o = 550\,\text{V}$.

IV. Design Methodology for the MISN-PFC Converter

In this section, the design method of the MISN-PFC converter is presented, and a 10 kW three-phase PFC with $\pm 10\%$ input voltage range is taken as an example to explain the design process. The variables to be designed are output voltage V_o, and several parameters of the MISN module, including capacity C_C, average dc-side voltage U_{dc}, cell number N_C, and frequency f_s.

A. Output Voltage Selection

Based on the steady condition in (7), the switching angle α is inversely proportional to the input voltage under the given V_o. Considering $\alpha > 0$, the minimum value of the regulated output voltage V_o is 540 V for the $\pm 10\%$ input voltage range, as illustrated by orange line in Fig. 5. If a larger V_o is selected, the range of α is increased, and the energy ΔE absorbed by the MISN module will also be increased. As a result, larger size capacitors are needed to restrict the voltage ripple of u_{dc}. So, the bus voltage should be set close to the minimum limitation. In this example, $V_o = 550\,\text{V}$ is selected for $\pm 10\%$ input voltage range.

B. Capacity Requirement of the MISN Module

Considering the minimum voltage limitation in (9), the capacity C_C of each cell in the MISN module should be selected carefully. To simplify the analysis, the multiple cells of the MISN module are equivalent to a single cell, whose voltage is U_{dc}, and capacitance is C_{eq} ($C_{\text{eq}} = C_C/N_C$). Combining (8) and (9), the requirement for the equivalent series capacity C_{eq} of the MISN module can be derived as

$$\begin{cases} C_{\text{eq}}\left(U_{\text{dc}}\right) \geq \frac{K_1(\alpha)\cdot P}{3\omega_0\left[U_{dc}^2-\left(K_2(\alpha)\cdot U_A\right)^2\right]} \\ K_1\left(\alpha\right) = 2\alpha - \sin\left(2\alpha\right) - \frac{\pi(\cos\alpha-1)}{2\cos\alpha-1} \\ K_2\left(\alpha\right) = \frac{\sqrt{2}\pi}{8\cos\alpha-4} + \sqrt{2}sin\alpha \end{cases} \tag{11}$$

in which P is the rated power.

According to (11), the suitable combinations of C_{eq} and U_{dc} is restricted in the red area in Fig. 8, and the dashed line represents the minimum capacity $C_{\text{eq.min}}$. To achieve the smallest capacitor volume, C_{eq} is selected based on the solid-line with 20% margin.

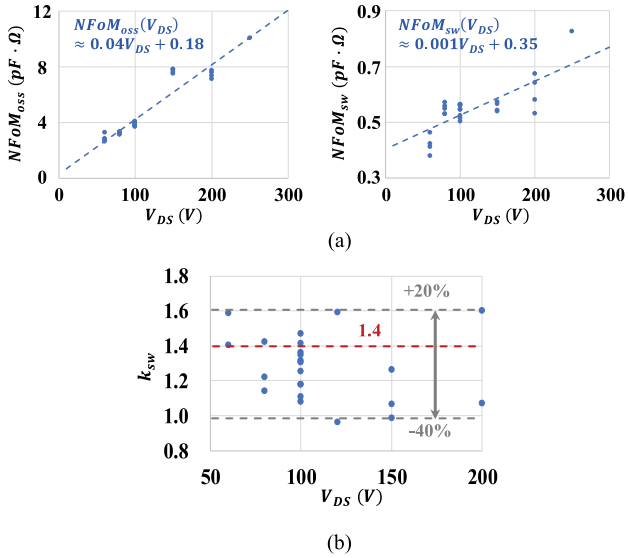

Fig. 9. Statistical data for different voltage Si MOSFETs (the data is calculated with the datasheet from infineon). (a) The value of NFoM_{oss} and NFoM_{sw}. (b) The value of k_{sw}.

C. Loss and Volume Optimization

In terms of the efficiency, the loss of the MISN module occupies a large percentage of the total loss, which is mainly affected by average dc-side voltage U_{dc}, cell number N_C, and switching frequency f_s. Referring to [15], the minimum loss of the MISN module can be estimated in (12) based on the NFoM of switches, and the $P_{\text{loss.min}}$ can be realized when the $R_{ds.on}$ of switches meets with (13)

$$\begin{aligned} &P_{\text{loss.min}} \\ &= 4U_{\text{dc}}I_L \cdot \sqrt{k_{\text{temp}}\left(k_{sw}I_L\text{NFoM}_{\text{sw}} + \text{NFoM}_{\text{oss}}\right)f_s} \end{aligned} \tag{12}$$

$$R_{ds.on} = \frac{U_{\text{dc}}}{N_C I_L}\sqrt{\frac{\left(k_{\text{sw}}I_L NFoM_{\text{sw}} + NFoM_{\text{oss}}\right)f_s}{k_{\text{temp}}}} \tag{13}$$

$$\begin{cases} \text{NFoM}_{\text{sw}} = C_{gd.tr}\, R_{ds.on} = f_{\text{sw}}\left(V_{DS}\right) \\ \text{NFoM}_{\text{oss}} = C_{oss.er}\, R_{ds.on} = f_{\text{oss}}\left(V_{DS}\right) \\ V_{DS} = 1.3 \cdot U_{dc.max}/N_c \end{cases} \tag{14}$$

where k_{temp} is the temperature coefficient, k_{sw} is the coefficient of the switching loss, I_L is the RMS value of the inductor current, and V_{DS} is the breakdown voltage of switches. $C_{gd.tr}$ is a fixed capacitance that gives the same charging time as C_{gd} from 0 to $70\%V_{DS}$, and $C_{\text{oss.er}}$ is a fixed capacitance that gives the same stored energy as C_{oss} from 0 to $70\%V_{DS}$.

It's found that $P_{\text{Loss.min}}$ is positively correlated to NFoM_{sw} and NFoM_{oss}, which are determined by the breakdown voltage V_{DS} and device manufacturing technology. In Fig. 9(a), the NFoM_{sw} and NFoM_{oss} of Si MOSFETs are investigated, and it can be seen that NFoM is approximately proportional to V_{DS}. As shown in Fig. 9(b), the value of k_{sw} of different switches is different. In order to simplify the calculation, all devices use the same $k_{\text{sw}} = 1.4$ described in red dashed line, which results in less than $+20\%$ deviation of switching loss in the worst case [25].

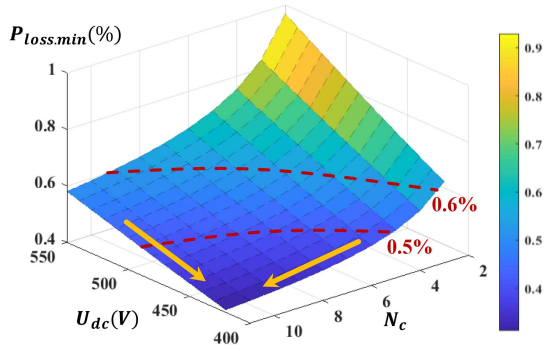

Fig. 10. Minimum loss of the MISN module versus $U_{\rm dc}$ and N_c under 10 kW and 20 kHz of switching frequency.

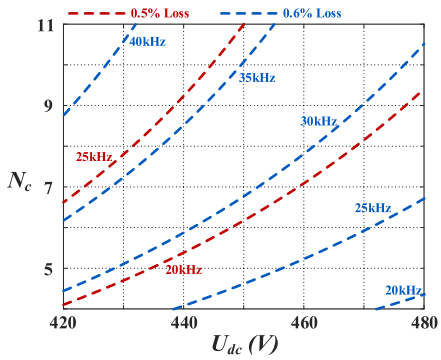

Fig. 11. f_s contour map for 0.5% (red) and 0.6% (blue) loss limitation at 10 kW.

By the way, -40% deviation can be regarded as over design and will not do damage to the converter.

With (12) and (14), the minimum loss of the MISN module can be calculated at a certain load. For a constant switching frequency f_s, the relationship between $P_{\rm Loss.min}$ and $U_{\rm dc}$, N_c is drawn in Fig. 10, where the loss has been normalized by the power. To begin with, the higher $u_{\rm dc}$, the larger $P_{\rm Loss.min}$ of the MISN module. This is because the switching loss and capacitive loss of the MISN module is increased by the high U_{dc}. Besides, under the same $U_{\rm dc}$, the more cells of the MISN module, the less $P_{\rm Loss.min}$, since lower voltage switches can be used. Moreover, the switching loss and capacitive loss are approximately proportional to f_s, thus $P_{\rm loss.min}$ can also be increased by the increasing of f_s, moving the loss surface upward.

According to the expected loss restriction, a contour line can be obtained as shown in red dashed line in Fig. 10, which represents the eligible combinations of $U_{\rm dc}$ and N_C under the given f_s. When the switching frequency changes, a contour map can be got, as shown in Fig. 11. Therefore, there are only two degrees of freedom for $U_{\rm dc}$, N_C, and f_s with the expected loss limitation. The definition for the contour map can be derived from (12) with the expected loss $P_{\rm loss.exp}$, i.e.,

$$f_s = \frac{1}{k_{\rm temp}\left(k_{sw} I_L {\rm NFoM_{sw}} + {\rm NFoM}_{oss}\right)} \left(\frac{P_{\rm loss.exp}}{4U_{\rm dc} I_L}\right)^2. \quad (15)$$

To further determine the value of $U_{\rm dc}$ and N_c, the volume of the converter is taken into consideration. Since the deigned variables have no effect on the LF-bridge and bus capacitors,

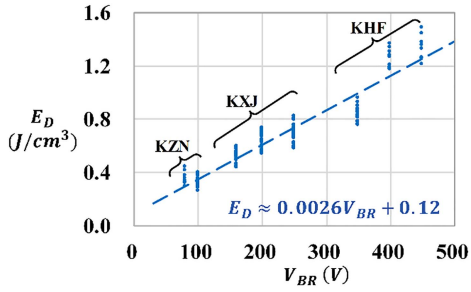

Fig. 12. Energy density of the electrolytic capacitors in the series KHF, KXJ, KZN from NCC.

the volume model just counts volume of inductor, and MISN module.

At first, the volume of the inductor can be estimated with AP method [34], which uses the product of the winding area A_w and the cross-sectional area A_e to calculate the inductor volume

$${\rm Vol_L} \approx k_L (A_e A_W)^{\frac{3}{4}} = k_L \left(\frac{L I_{\rm peak} I_{\rm RMS}}{k_w J B_{\rm max}}\right)^{\frac{3}{4}} \quad (16)$$

where the const k_L is related to the type of core, k_w is window utilization rate, J is current density, and the inductance L satisfies: [25]

$$L = \frac{U_{dc}}{8 N_c^2 f_s \Delta i_{pp}} \quad (17)$$

where Δi_{pp} is the current ripple of the inductor current.

The MISN module is composed of electrolytic capacitors and circuit boards. The volume of capacitors can be evaluated by their energy density ED

$${\rm ED} = \frac{\frac{1}{2} C V_{\rm BR}^2}{{\rm Vol_{Cap}}} \quad (18)$$

where $V_{\rm BR}$ is the breakdown voltage of capacitors and ${\rm Vol_{Cap}}$ represents the capacitors' volume. Fig. 12 shows the capacitors' energy density for different breakdown voltage.

Thus, the volume of the MISN capacitors, ${\rm Vol}_C$, can be obtained

$${\rm Vol_C} \approx \frac{\frac{1}{2} C_{eq} (1.2 U_{\rm dc.max})^2}{E_D}. \quad (19)$$

Then, the circuit board of MISN module is constructed with several modularized cells, whose volume is nearly constant (e.g., $3\,{\rm cm}^3$). So, the volume of the circuit board (${\rm Vol_{Cell}}$) is approximately proportional to N_C.

Finally, the total volume is

$${\rm Vol_{Total}} = {\rm Vol}_L + {\rm Vol}_C + {\rm Vol_{Cell.}} \quad (20)$$

Combing (15) and (20), the frequency contour map for the expected loss limitation and the corresponding volume contour map are depicted in the same picture in Fig. 13, where the red dashed lines are related to f_s, and the color represents different value of ${\rm Vol_{Total}}$. The total volume ${\rm Vol_{Total}}$ is calculated with $20\%\, I_{\rm RMS}$ ripple current, $k_L \approx 11.9$, $k_w = 0.3$, $J = 10\,{\rm A/mm^2}$, and $B_{\rm max} = 0.3T$.

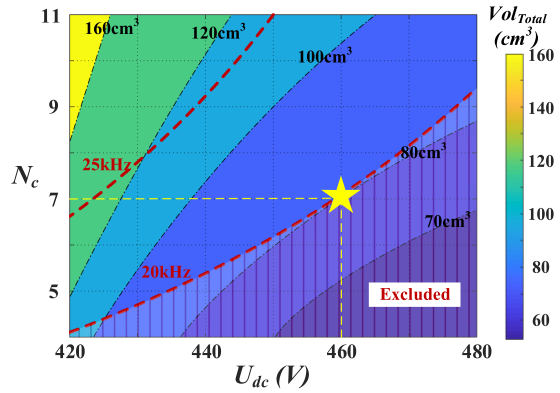

Fig. 13. Contour map of f_s and $\text{Vol}_{\text{Total}}$ under 0.5% loss limitation of the MISN module at 10 kW.

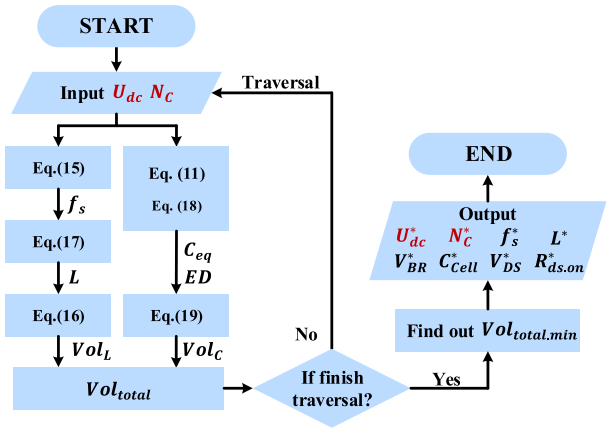

Fig. 14. Design flowchart for the MISN converter.

To avoid $f_s < 20$ kHz, which is in the hearing range of human, the shadow area in Fig. 13 is excluded from the selection. Therefore, in order to realize the minimum value of $\text{Vol}_{\text{Total}}$, $U_{dc} = 460$ V, $N_C = 7$, $f_s = 20$ kHz is adopted. Based on (11) and (13), 80 V 1000 uH electrolytic capacitor and 100 V 2 mΩ Si MOSFET are selected. It should be noted that $N_C = 6$ is discarded for the bad performance of the commercial 120 V switches.

The design flowchart is presented in Fig. 14, the independent variables are cell number N_C and dc-side voltage U_{dc}, which are marked red. It can be seen that the main ideal of the proposed design methodology is to reduce the volume of the MISN module as much as possible under the expected loss limit.

V. Hardware and Experimental Verification

A. Hardware Prototype

A 10 kW 430 W/in^3 prototype with 7cells is built and the specifications of the converter are given in Table I. As shown in Fig. 15, the hardware constitutes of three parts: input filter (EMI filters and inductors), MISN module (cell circuits and capacitors), LF-bridge (including output capacitors) and control board. The MISN module is constructed with 100 V Si MOSFETs to realize 0.5% loss limitation at full load, and the LF-bridge is designed with 1200 V SiC MOSFETs to reduce conduction loss. The detailed information of devices in prototype is given in Table II.

TABLE I
Prototype Specifications

Parameter	Symbol	Value
Power	P	$10kW$
Input phase voltge	U_s	$220V_{RMS}$ (±10%)
Output voltage	V_o	$550V$
Output Cap.	C_o	$198uF \times 2$
Inductor	L	$9.7uH$ ($\Delta i_{pp} \leq 6A$)
Cell Voltage	U_C	$65V$
Cell Cap.	C_C	$1000uF$ ($80V$)
Switching frequency	f_s	$20kHz$
Cell number	N_C	7

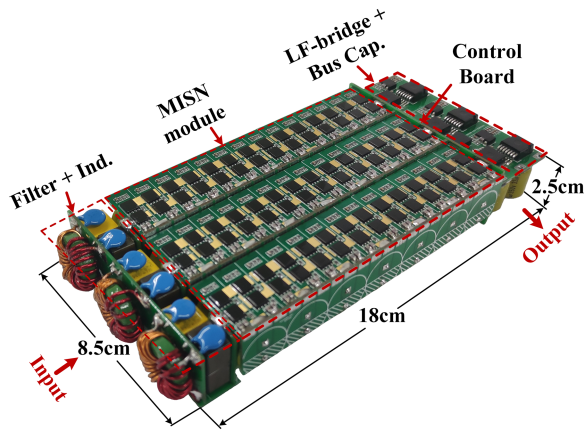

Fig. 15. Hardware implementation.

TABLE II
Prototype Devices

Description	Value
MOSFETs of MISN cells	ISC022N10NM6
Drivers of MISN cells	UCC20225A-Q1
Capacitors of MISN cells	LKMJ2501K102MF
MOSFETs of LF-bridge	IMBG120R030M1H
Bus capacitors	VKML1702V330V
Inductors	XAL1510-472ME (2PCS in series)
DSP	TMS320F280049CRSH
FPGA	EG4S20NG88

The schematic as well as the top and bottom views of the MISN cell is given in Fig. 16. Since the MISN cells are floating, two isolated half-bridge drivers are used to realize PWM driving. The primary side of the isolated driver is connected to the controller, which can be powered easily; the secondary side is powered by the additional isolated power supply module. The size of MISN cell is 26 mm × 18 mm × 5 mm.

The digital control system is constructed with DSP and FPGA, and its schematic is presented in Fig. 17. The sampled signals are converted by DSP for the calculation of three-loop control strategy. Then, the results are transmitted to FPGA to generate the PWM driving signals of MISN module as well as LF-bridge.

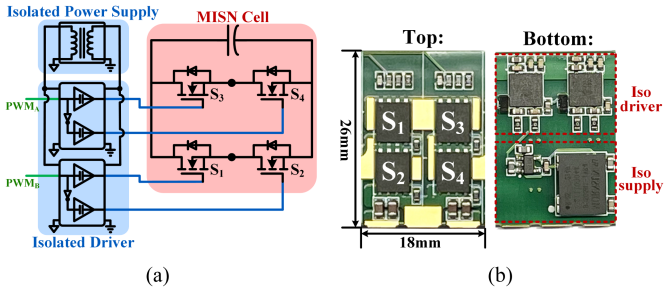

Fig. 16. Implementation of the MISN cells. (a) Schematic diagram. (b) Hardware diagram.

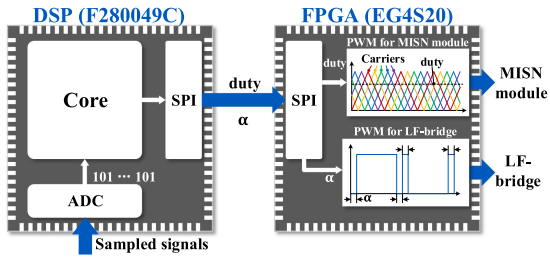

Fig. 17. Schematic of the digital control system.

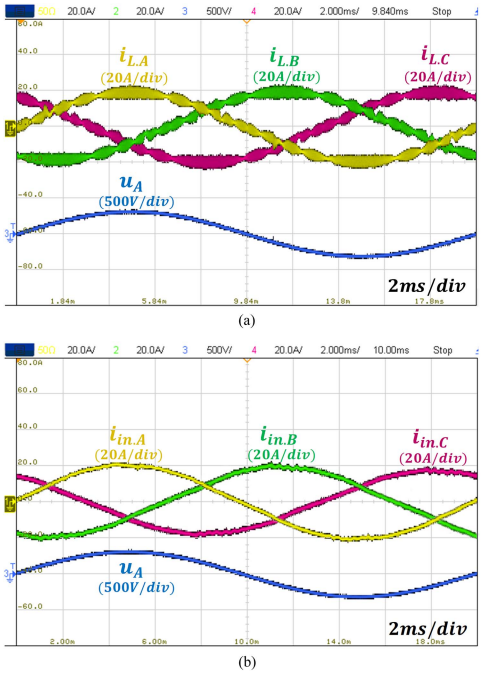

Fig. 18. Three-phase full-load currents. (a) 3-phase inductor currents. (b) 3-phase input currents.

B. Experimental Results

When connected with the three-phase gird, the MISN-PFC converter operates in three-phase mode, and the three-phase inductor currents ($i_{L.A}$, $i_{L.B}$, $i_{L.C}$) at full load condition are shown in Fig. 18(a). Due to the high frequency current ripple of inductor currents, purified input currents can be easily obtained with smaller size of filter. The waveforms of input currents ($i_{in.A}$, $i_{in.B}$, $i_{in.C}$) are presented in Fig. 18(b), with the help of the first current loop, the input currents are forced to track the input voltage for power factor correction, and the power factors are nearly unit, the iTHD is less than 2%.

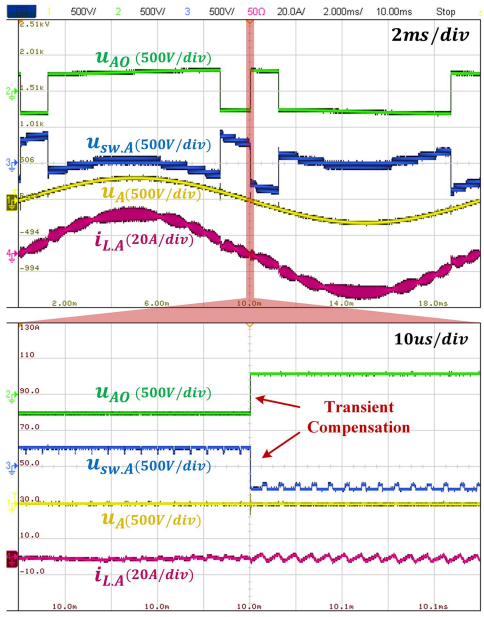

Fig. 19. Transient compensation for phase-A.

The transient compensation is employed to inverse the port voltages of the three-phase MISN modules ($u_{sw.A}$, $u_{sw.B}$, $u_{sw.C}$) at the switching time of LF-bridge. As shown in Fig. 19, some key waveforms of phase-A and the detailed process during the LF-bridge switching are given. It can be seen that the duty cycle of $u_{sw.A}$ is compensated at the edge of u_{AO}, and there is only little current distortion of $i_{L.A}$.

The MISN capacitors' voltages are controlled by the third voltage loop for voltage balance. In Fig. 20(a), the cells' voltages of three-phase MISN modules are measured, including voltage of cell-1 in phase-A ($u_{C1.A}$), phase-B ($u_{C1.B}$), and phase-C ($u_{C1.C}$). Thanks to three independent MISN voltage control loops, the average values of them are identical and good voltage balance has been achieved. Besides, the common-duty-cycle control is adopted, and all cells in the same phase have identical charging and discharging time in every switching period, so that the cell voltage in the same phase is also balanced, as shown in Fig. 20(b).

The dynamic performance at 220 Vac are presented in Fig. 21, including the output voltage and dc-side voltage of MISN module during the load changing. No matter stepping up or stepping down load by 50%, the transient process of output voltage is about two line frequency period, and the overshoot is about 8%. As for the dc-side voltage of MISN module, the transient process is longer about 5–8 periods. In addition, due to the nonlinear relationship between switching angle α and P^{α}_{MISN}, described in (6), the dynamic performance is different under different input voltages. As shown in Fig. 22, the transient process of MISN voltage at 198 Vac is faster than that at 242 Vac.

The efficiency of the prototype with rated input voltage is drawn in Fig. 23. The peak efficiency of the MISN-PFC converter is 99.2% near the half load, and the full-load efficiency can reach 99%. The loss breakdown at full load is presented

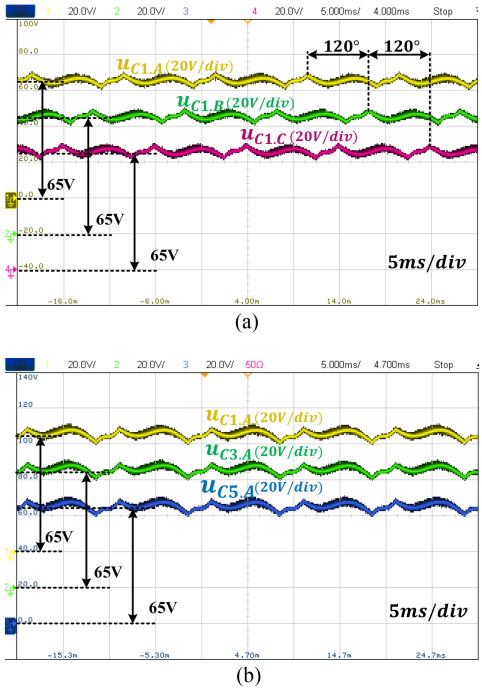

Fig. 20. Capacitor voltage of MISN module. (a) In the different phase. (b) In the same phase.

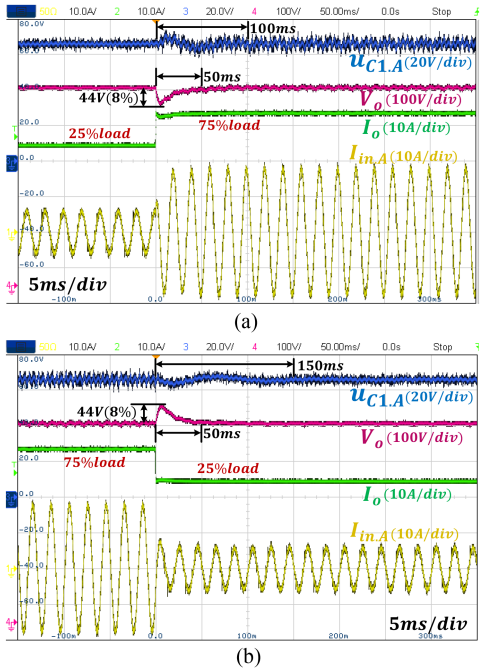

Fig. 21. Dynamic performance during load changing at 220 Vac. (a) From 25% to 75% load. (b) From 75% to 25% load.

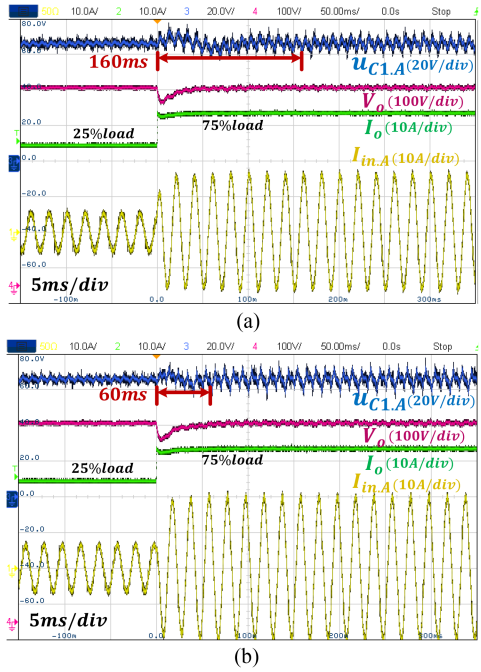

Fig. 22. Dynamic performance under different input voltages. (a) From 25% to 75% load at 242 Vac phase voltage. (b) From 25% to 75% load at 198 Vac phase voltage.

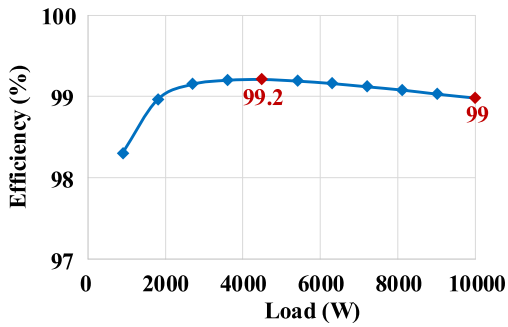

Fig. 23. Measured efficiency of 3-phase MISN-PFC converter.

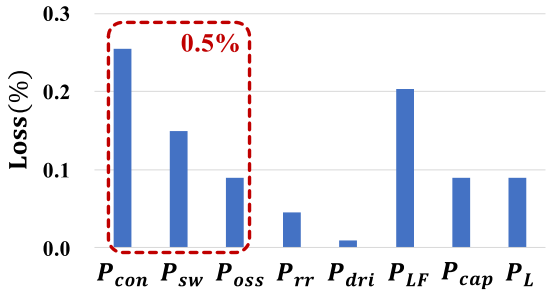

Fig. 24. Loss breakdown at full load.

in Fig. 24, the summary of conduction loss (P_{con}), switching loss (P_{sw}), and capacitive loss (P_{oss}) for the MISN module is around 0.5%, which is satisfied with expected limitation. Considering the diode reverse recovery loss (P_{rr}) and driving loss (P_{dri}), the total loss of MISN module is slightly higher than the expected loss limitation. Besides, as a result of the low frequency operating of the LF-bridge, the related loss (P_{LF}) is 0.2%, mainly composed of conduction loss.

The power factor and iTHD for three-phase input currents are almost the same, and the experimental results of phase-A are presented in Fig. 25. By means of the feedforward control, the power factor is larger than 0.95 for the whole load range, while the iTHD is less than 8%. Besides, the results of FFT analysis for the input current at full load and 30% load are presented in Fig. 26. The input current is mainly composed of fundamental

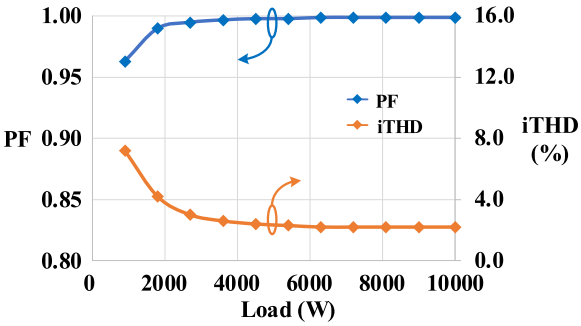

Fig. 25. Measured power factor and iTHD.

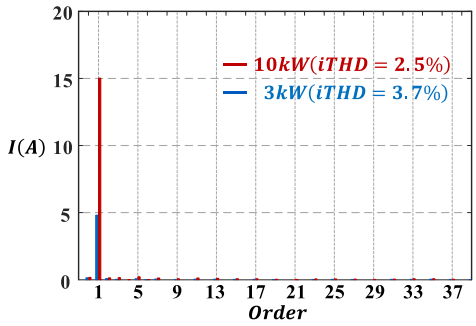

Fig. 26. FFT analysis for the input current.

TABLE III
STATE-OF-THE-ART THREE-PHASE PFC CONVERTERS

	[8]	[13]	[12]	[14]*	Proposed
Type	2LB6 CCM	2LB6 CRM	2LB6 ZVS	T-type	MISN
Spec.	22kW 750V	25kW 800V	20kW 600V	2kW 800V	10kW 550V
f_s/kHz	48	300~530	300	150	20
THD/%	3.2	2	-	-	2.5
Eff/%	98.4	98.9	98.5	>99	99
W/in^3	160	230	120	250	430

* no hardware prototype.

component, and the low frequency harmonics of input current is very small.

In Table III, the performance of different types of three-phase PFC converters is compared, including the full load efficiency, power density, and current THD of the converter. The power density is calculated with the heatsink removed, which usually occupies 20%–30% of the converter. Therefore, it can be seen that the multilevel MISN topology can achieve high efficiency and high power density of the converter simultaneously.

VI. Conclusion

In this article, a three-phase MISN-PFC converter with single output bus and good modularization capability is presented for OBC application and its operation principle has been analyzed. To guarantee the normal operation, the three-loop control system with transient compensation is proposed, which helps to realize good current quality and voltage balance. Besides, the design method is proposed to determine the variables of the MISN module under the expected loss limitation, including average dc-side voltage $U_{\rm dc}$, cell number N_C, and switching frequency f_s. Finally, based on the proposed design methodology, a 7cells 10 kW prototype has been built, and 99% efficiency at full-load and power density of more than 430 W/in^3 are achieved.

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