Static and Dynamic Characteristics of a 1200-V/22-mΩ Normally-Off SiC/GaN Cascode Device Built With Parallel-Connected SiC JFETs Controlled by a Single GaN HEMT

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***Abstract*—A silicon carbide junction field effect transistors (SiC-JFETs) /gallium-nitride high electron mobility transistor (GaN-HEMT) hybrid power switch is proposed with scaled-up current rating enabled by parallel-connected high-voltage (HV, i.e., 1200 V) SiC-JFETs controlled by a single low-voltage enhanced-mode GaN-HEMT in a cascode configuration. Only one set of gate driver (for the GaN HEMT) is required by the cascode device and therewith higher efficiency is achieved regarding the gate-driver loss compared with a board-level parallel connection of several standalone devices (e.g., SiC MOSFETs or SiC/Si cascode devices). Key factors that affect the current-sharing balance between the parallel-connected SiC JFETs and associated matching method are systematically investigated by taking into account the specific transient behaviors of the cascode device. It is found that the variation in SiC JFETs' threshold voltages plays the most important role in current balancing when the GaN HEMT drives the SiC JFETs internally with superior fast speed. A 1200-V/22-mΩ proof-of-concept prototype of the proposed device with two SiC JFETs in parallel is demonstrated and characterized in a comparative study considering the matching of JFETs. By matching the SiC JFETs according to their transfer curves, the current-sharing imbalance among the SiC JFETs can be limited to be less than 1.5%. This all-wide-bandgap device exhibits high-temperature stability of threshold voltage, extremely small gate-driver loss, and low interelectrode capacitances, of which features are promising for high-frequency applications.**

***Index Terms*—Cascode device, current-sharing balance, gallium-nitride (GaN) high electron mobility transistor (HEMT), hybrid switch, normally-off, parallel connection, silicon carbide (SiC) junction field effect transistors (JFETs).**

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I. Introduction

Wide bandgap (WBG) power semiconductor devices, e.g., silicon carbide (SiC) and gallium nitride (GaN) devices, are promising candidates for the next-generation power converters with higher power density and higher efficiency, thanks to their superior device properties, such as low specific ON-resistance, high frequency, and high operation temperature [1], [2].

SiC power switches with a rated voltage of 650–1700 V, such as SiC junction field effect transistors (JFETs) and MOSFETs, are favored by power conversion system (e.g., photovoltaic inverters and on-board chargers) with higher efficiency and reduced converter size, owing to the relatively mature material and processing techniques [3], [4]. GaN high electron mobility transistor (HEMT) with voltage rating ranging from 200 to 650 V are capable of operating at higher frequency (e.g., 100kHz–10 MHz) and are emerging in consumer electronics, such as compact fast chargers for mobile phones [5], [6].

Recently, a hybrid switch in the form of a SiC/GaN cascode device is proposed where the HV SiC JFET delivers the high-voltage blocking capability and the low-voltage (LV) GaN HEMT offers the normally-off control [7], [8]. This hybrid switch combines the advantages of SiC and GaN devices, such as the thermal stability of threshold voltage delivered by a GaN HEMT, high voltage rating and avalanche capability provided by a SiC JFET [9].

For power converters (e.g., motor drive of electric vehicle and power system of all-electric aircraft) that are in pursuit of higher power (e.g., 10 kW or above), power devices are being required to achieve higher current ratings (e.g., >80 A) [10], [11], [12]. It is straightforward to apply a board-level parallel connection of the SiC/GaN cascode devices or SiC MOSFETs [13], [14] to overcome the low-yield issue during manufacturing to scale up current ratings. However, although the parallel connection of standalone SiC JFETs have been studied comprehensively and possible remedies were suggested [15], it is still challenging to use several cascode devices directly in parallel. With several cascode devise directly in parallel, except for the SiC JFETs, there would be several LV GaN HEMTs, which will induce additional device variations that make it more complex to match cascode devices. On the other hand, multiple gate drivers for each of the

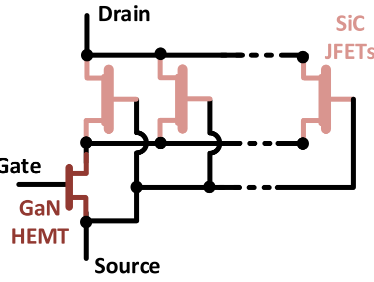

Fig. 1. Proposed cascode device with parallel-connected SiC JFETs controlled by a single GaN HEMT.

individual cascode device would induce extra gate-driver losses. Furthermore, the gate-driver mismatch and gate-circuitry variations would aggravate the current-sharing imbalance [13], [15].

An alternative method is to adopt a single LV GaN HEMT that enables the internal gate control for parallel SiC JFETs in a cascode configuration, as depicted in Fig. 1. Only one set of gate driver is required by the GaN HEMT and, thus, there is no gate-driver mismatch issue in this case. Besides, an LV GaN HEMT could deliver lower gate charge required to switch [16] and hence reduce the gate-driver loss [17].

Meanwhile, SiC JFETs are preferred for parallel connection compared with SiC MOSFETs, as SiC JFETs deliver better thermal stability of threshold voltage due to the junction-type gate stack. SiC JFETs are free of gate-oxide induced channel-mobility degradation, which exits in SiC MOSFETs [18], [19]. Besides, ON-resistance (R_{ON}) of SiC JFETs exhibit positive temperature coefficient and could enable naturally current-sharing balance during ON-state.

In this article, we propose a cascode device adopting parallel SiC JFETs controlled by a single GaN HEMT. The relevant matching method and device characteristics are investigated. In Section II, key factors (e.g., device parameters and circuitry ones) that limit the current-sharing behaviors among the parallel JFETs are theoretically analyzed. In Section III, a proof-of-concept 1200-V/22-mΩ prototype is implemented with SiC JFETs according to the matching method as investigated in Section II. Static and dynamic behaviors of the prototype are characterized systematically and compared with conventional SiC MOSFETs in parallel operation, in order to validate the feasibility and advantages of the proposed cascode device. Finally, conclusions are drawn in Section IV.

II. Key Factors Affecting the Current-Sharing Balance Among SiC JFETs in Parallel

The transient behaviors of the cascode device are first analyzed in theory. Generally, an LV E-mode GaN-HEMT features higher switching speed owing to its higher transconductance (g_{GaN}) and smaller output capacitance compared with SiC JFETs used in this work [20]. Therefore, in an SiC/GaN cascode device, the LV GaN HEMT behaves in a manner analogous to an inner gate-drive ICs for the HV SiC JFETs.

Key factors that affect the transient behaviors of the proposed SiC/GaN cascode device are analyzed at first. A schematic diagram of the turn-ON transient waveforms is depicted in Fig. 2(a). During the time interval [t_1-t_2], the GaN HEMT's gate capacitor, $C_{GS\text{-}G}$, is charged by the gate driver until $v_{GS\text{-}G}$ (GaN-HEMT's gate voltage) reaches the value of $V_{TH\text{-}G}$ (GaN-HEMT's threshold voltage), as shown by the current path in Fig. 2(b). At [t_2 and t_3], the GaN-HEMT's drain voltage ($v_{DS\text{-}G}$) falls and the GaN HEMT's output capacitance ($C_{GD\text{-}G}$+$C_{DS\text{-}G}$), and SiC JFET's gate-to-source capacitance ($C_{GS\text{-}J}$) discharge simultaneously through the GaN-HEMT's enhanced channel, as depicted in Fig. 2(c). The time interval [t_1 and t_3] is defined as the turn-ON delay time ($t_{d\text{-}ON}$). $t_{d\text{-}ON}$ is calculated by (1), where R_G refers to the gate resistor, $V_{G\text{-}ON}$ the gate driver's turn-ON voltage, $C_{GD\text{-}G}$+$C_{GS\text{-}G}$ the GaN device's input capacitance, $V_{TH\text{-}G}$ the threshold voltage of the GaN device, $V_{DS\text{-}G}$ the OFF-state drain-to-source voltage of the GaN device, $V_{TH\text{-}J}$ the threshold voltage of the JFET, and R_G the gate driver resistance [20]

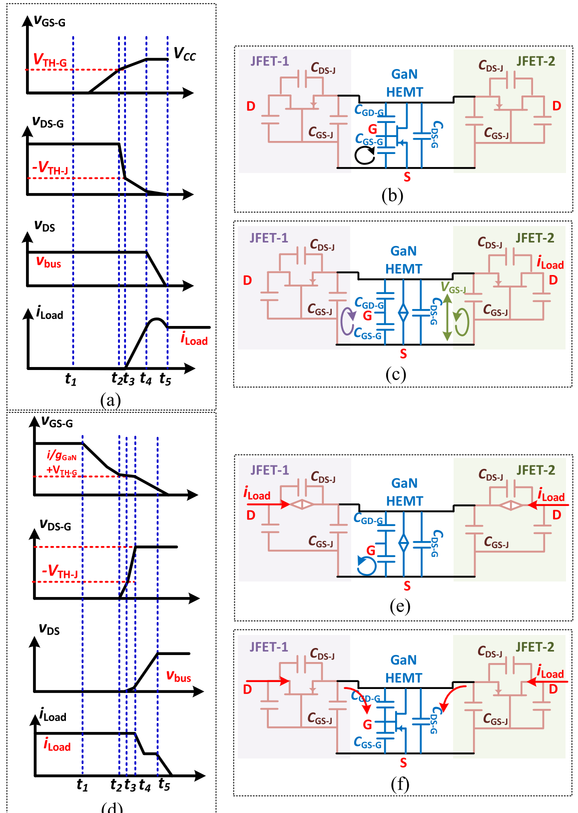

Fig. 2. (a) Schematic diagrams of the transient turn-ON waveforms of the cascode device. The current paths in the SiC/GaN cascode device during turn-ON at time interval of (b) t_1 and t_2 or (c) t_2 and t_3. (d) Schematic diagrams of the transient turn-OFF waveforms of the cascode device. The current paths in the cascode device during turn-OFF at time interval of (e) t_1-t_2 and (f) t_2-t_3.

$$t_{d-ON} = -R_G(C_{GS-G}+C_{GD-G})\ln\left(1-\frac{V_{TH-G}}{V_{G-ON}}\right) + \frac{(V_{DS-G}+V_{TH-J})R_G C_{GD-G}}{V_{G-ON}-V_{TH-G}}. \quad (1)$$

There is a chance that temperature would induce variations in $V_{TH\text{-}G}$. Based on the abovementioned analysis, the variations in $V_{TH\text{-}G}$ would only influence $t_{d\text{-}ON}$. After a duration of $t_{d\text{-}ON}$, the LV GaN HEMT is about to be fully turned ON as the GaN device has a relatively faster switching speed. Starting from t_3,

it is the turn-ON speed of the two SiC JFETs that determine the transient turn-ON behaviors of the cascode device.

The analysis on the device turn-OFF is analogous to the device turn-ON, as illustrated by the schematic diagram in Fig. 2(d). In the beginning, $C_{\text{GS-G}}$ (i.e., gate-to-source capacitor of the GaN HEMT) and $C_{\text{GD-G}}$ are discharged by the outer gate driver till $v_{\text{GS-G}}$ reaches $V_{\text{TH-G}}+i_{\text{Load}}/g_{\text{GaN}}$, where g_{GaN} refers to the small-signal value of the transconductance of a GaN HEMT. At this time instant ([t_1-t_2]), the GaN HEMT starts to be pinched off and then get saturated. $v_{\text{DS-G}}$ rises when the capacitors (i.e., $C_{\text{GD-G}}$, $C_{\text{DS-G}}$, and $C_{\text{GS-J}}$) of the inner gate driver loop are charged by i_{Load}. In this scenario ([t_2-t_3]), $v_{\text{DS-G}}$ and i_{Load} work as the inherent gate-control voltage and current, respectively, for the SiC JFETs. When $v_{\text{DS-G}}$ approximates $-V_{\text{TH-J}}$, SiC JFETs are pinched off. The turn-OFF delay time ($t_{\text{d-off}}$) during, which $v_{\text{DS-G}}$ rises to $-V_{\text{TH-J}}$ is derived as [20]

$$t_{\text{d-off}} = -R_{\text{G}}\left(C_{\text{GS-G}} + C_{\text{GD-G}}\right)\ln\left(\frac{V_{\text{TH-G}} + i_{\text{Load}}/g_{\text{GaN}}}{V_{\text{G-ON}}}\right) + \frac{-V_{\text{TH-J}}R_{\text{G}}C_{\text{GD-G}}}{-V_{\text{G-OFF}} + V_{\text{TH-G}} + i_{\text{Load}}/g_{\text{GaN}}}. \quad (2)$$

Thereafter, starting from t_3, it is the turn-OFF speed of the two SiC JFETs that determine the transient behaviors of the cascode device. Then, the SiC JFETs get pinched off and its drain voltage-rising slew rate is determined by

$$\frac{dv}{dt} = \frac{i_{\text{Load}}}{C_{\text{GD-J}} + C_{\text{DS-J}}} \quad (3)$$

where $C_{\text{GD-J}}$ refers to the JFET's gate-to-drain capacitor, $C_{\text{DS-J}}$ the JFET's drain-to-source capacitor.

During the turn-OFF transient, the SiC JFETs in parallel bare the same voltages and are simultaneously controlled by the GaN HEMT through the inner gate driver loop. Therefore, the first term at the right-hand side of (2) is the same for all the SiC JFETs. The variations in $V_{\text{TH-J}}$ counts for the spreads in $t_{\text{d-OFF}}$ of each SiC JFET and will leads to current redistribution among them during switching transient.

Therefore, simulations in *LTSpice* are first carried out to study the effects of variations in device parameters (i.e., $V_{\text{TH-J}}$ and g_{JFET}) with respect to current sharing behaviors in an SiC/GaN cascode device. Besides, variations in parasitic inductances (i.e., inductances along the power loop or gate driver loop), are also analyzed regarding the transient performances.

A. Effects of Variations in $V_{TH\text{-}J}$

1200-V/35-mΩ SiC JFETs from UnitedSiC Inc (i.e., UJ3N120035K3S [21]) and an 80-V/2.2-mΩ GaN E-mode HEMT from EPC Inc (i.e., EPC2206 [22]) are selected to build an SiC/GaN cascode device with two paralleled SiC JFETs, as depicted in Fig. 3. The SiC JFET and GaN HEMT models are based on field effect transistor (FET) models developed by Shichman and Hodges [23] in *LTSpice*. In those FET models, the channel-length modulation is adopted and the pinch-OFF region of the FET channel is treated as one-sided abrupt junction. Therefore, the drain current ($i_{\text{D-J}}$) of the SiC JFET at linear region and saturation region is expressed as

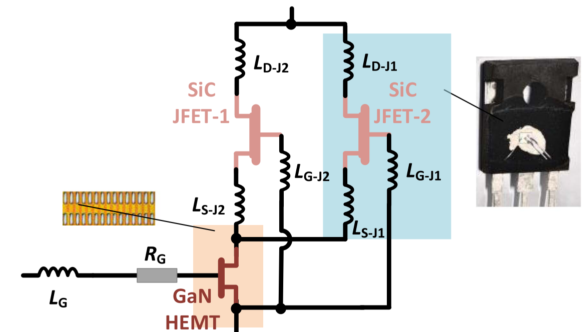

Fig. 3. Schematic diagram of the SPICE model of an SiC/GaN cascode device with parallel-connected SiC JFETs controlled by one single GaN HEMT.

$$\begin{cases} i_{\text{D-J}} = \beta(1+\lambda v_{\text{DS-J}})v_{\text{DS-J}}\times \\ [2(v_{\text{GS-J}} - V_{\text{TH-J}}) - v_{\text{DS-J}}] \\ \quad (v_{\text{DS-J}} < v_{\text{GS-J}} - V_{\text{TH-J}}) \\ i_{\text{D-J}} = \beta(1+\lambda v_{\text{DS-J}})(v_{\text{GS-J}} - V_{\text{TH-J}})^2 \\ \quad (v_{\text{DS-J}} \geq v_{\text{GS-J}} - V_{\text{TH-J}}) \end{cases} \quad (4)$$

where β and λ are parameters defined by device characteristics during processing (e.g., the junction depth and doping concentration of the channel region of the JFETs).

On the other hand, as presented in Fig. 3, the parasitic inductances (e.g., $L_{\text{D-J1}}$) distributed along the bonding wires as well as the leads of a TO-247 housing (where a SiC JFET is packaged) cannot be neglected, as they are several or tens of nanohenries, which could affect the device's fast switching behaviors [24]. At the subscript part of the inductance's designator, the first upper-case letter refers to the terminals of the devices (D for drain, G for gate, and S for drain); J1 or J2 refers to JFET-1 or JFET-2, respectively. The values of the inductances are given by UniteSiC Inc: $L_{\text{D-J}} = 5$ nH, $L_{\text{G-J}} = 10$ nH, and $L_{\text{S-J}} = 2$ nH. The GaN HEMT is packaged in a chip-scale linear grid array (LGA), which enables relatively lower parasitic inductances (lower than 1nH) [25] and extremely small footprint, i.e., a 6 mm × 2.3 mm rectangle-shape one. The size of the LGA package is relatively small compared with a TO-247 package housing and would not make a significant difference of the dimensions on board.

The selected SiC JFET (UJ3N120035K3S) exhibits a typical $V_{\text{TH-J}}$ of -11.5 V. Hard-switching waveforms of the two SiC JFETs with varied spread ($\Delta V_{\text{TH-J}}$) between their threshold voltages are simulated in a double pulse tester (DPT) circuitry with a load current of 80 A and a dc bus voltage of 800 V, as presented in Fig. 4(a)–(f). $\Delta V_{\text{TH-J}}$ between JFET-1 and JFET-2 (as indicated in Fig. 3) ranges in (0, 0.5, 1 V).

It is noted that the $\Delta V_{\text{TH-J}}$ will affect more on the current-sharing balance of the SiC JFETs during turn-ON in comparison with that of SiC JFETs during turn-OFF. This is because the spread of $V_{\text{TH-J}}$ determines the turn-OFF delay time of the SiC JFET. With a large load current (i_{Load}) providing the function of gate-control current, the spread in turn-OFF delay time of the two JFETs is limited as $v_{\text{DS-G}}$ will raised up to $V_{\text{TH-J}}$ in an extremely

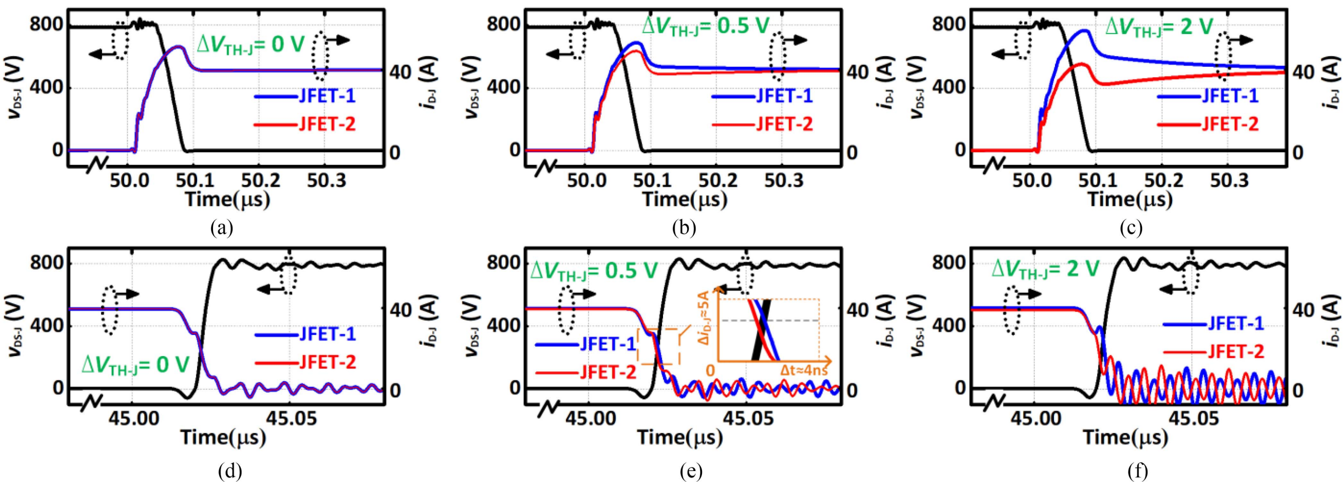

Fig. 4. Hard switching waveforms of the parallel-connected JFET-1 and JFET-2 with varied $V_{\text{TH-J}}$ spread ($\Delta V_{\text{TH-J}}$) within the SiC/GaN cascode device: (a) turn-ON and (b) turn-OFFwaveforms at $\Delta V_{\text{TH-J}} = 0$ V; (c) turn-ON and (d) turn-OFF waveforms at $\Delta V_{\text{TH-J}} = 0.5$ V; (e) turn-ON and (f) turn-OFF waveforms at $\Delta V_{\text{TH-J}} = 2$ V.

short period (Δt_{OFF}), of which the value can be calculated by

$$\Delta t_{\text{OFF}} \approx \frac{\int_0^{-V_{\text{TH-J}}} (C_{\text{DS-G}} + C_{\text{GS-J}})\, dv}{i_{\text{Load}}}. \tag{5}$$

As $C_{\text{DS-G}}$ and $C_{\text{GS-J}}$ are less than 2nF, Δt_{OFF} will be less than 1 ns with i_{Load} at 40 A, according to (5). Therefore, with a notable spread in $V_{\text{TH-J}}$, the current redistribution between the two JFETs can still be restricted to a low level during the turn-OFF transient, as indicated by the inset in Fig. 4(e).

B. Effects of Variations in g_{JFET}

The saturation region of the SiC JFET can be defined by (4) and hence the g_{JFET} during hard-switching transient can be derived by

$$g_{\text{JFET}} = 2\beta(1 + \lambda v_{\text{DS-J}})(v_{\text{GS-J}} - V_{\text{TH-J}}) \tag{6}$$

where β is treated as constant and identical as the SiC JFETs of the same ratings share similar parameters designed by the same company. However, there is still a chance that g_{JFET} be varied due to errors in process control, of which the errors can be reflected by the variation in β.

The voltage and current waveforms of JFET-1 and JFET-2 are simulated with a variation of 50% the value of β among their transconductances. It is noted that the variation in β can hardly affect the current-sharing behaviors during the switching transients (see Fig. 5). The rising or falling slew rate of the drain current of the SiC JFET is determined by g_{JFET} multiplied by the derivation of the JFET's gate voltage, i.e., $v_{\text{GS-J}}$. $v_{\text{GS-J}}$ can be derived from the inner gate driver circuit composed of the channel resistance of GaN HEMT (R_{GaN}), $C_{\text{DS-G}}$, and $C_{\text{GS-J}}$

$$v_{\text{GS-Ji}} \begin{cases} = V_{\text{GS-J}} e^{-t/R_{\text{GaN}}(C_{\text{DS-G}} + C_{\text{GS-J}})} (\text{turn} - \text{on}) \\ = i_{\text{Load}} t / C_{\text{DS-G}} + C_{\text{GS-J}} (\text{turn} - \text{off}). \end{cases} \tag{7}$$

As analyzed in Part A of this section, $C_{\text{DS-G}}$ and $C_{\text{GS-J}}$ deliver a value of less than 2 nF and hence the time constant of the inner gate driver (which determines the derivation of $v_{\text{GS-J}}$) is less than 1 ns. Therefore, the current-sharing imbalance is dominated by the short turn-ON or turn-OFF time interval despite of the notable variation in g_{JFET}.

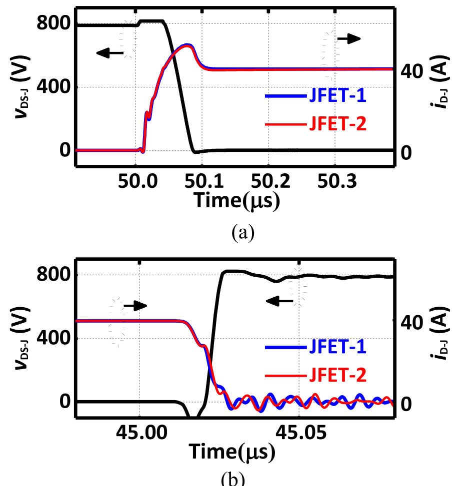

Fig. 5. (a) Turn-ON (b) and turn-OFF waveforms of JFET-1 and JFET-2 with a variation of 50% the value of β in g_{JFET}.

C. Effects of Variations in Parasitic Inductances

The parasitic inductance along the power-loop inductance could be cancelled by a symmetry design on the circuit layout. Another type of parasitic inductance that may affect the current-sharing balance is the outer gate-driver inductance. When two cascode devices are parallel connected in a conventional method and controlled individually by two sets of gate driver [see Fig. 6(a)], variations in the gate-driver inductances (e.g., $L_{\text{G-1}}$ and $L_{\text{G-2}}$ in Fig. 6) are easily produced due to unmatched gate driver circuitry and affect the gate-control delay time. For verification, the switching waveforms of two individual cascode devices in parallel are simulated with a variation of 5 nH between $L_{\text{G-1}}$ and $L_{\text{G-2}}$, as plotted by Fig. 6(b) and (c). It is noted that the

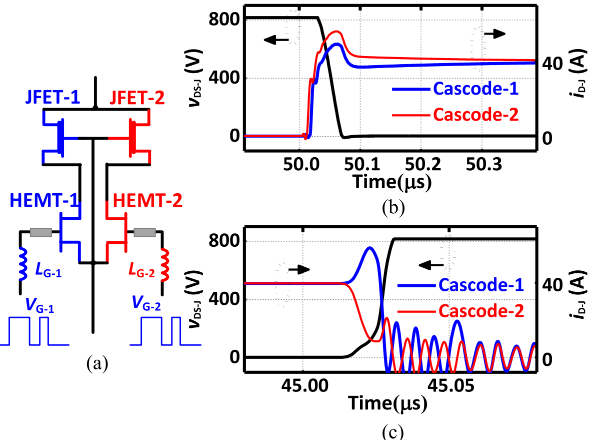

Fig. 6. (a) Schematic diagram of two paralleled standalone SiC/GaN cascode devices with variations in $L_{\text{G-1}}$ and $L_{\text{G-2}}$. (b) Turn-ON and (c) turn-OFF waveforms of JFET-1 and JFET-2 with a variation of 10 nH between $L_{\text{G-1}}$ and $L_{\text{G-2}}$.

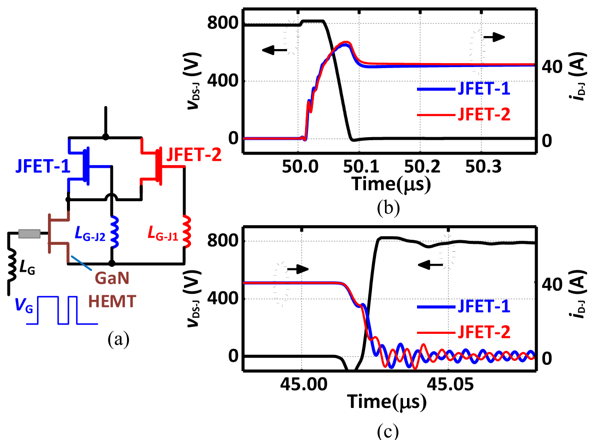

Fig. 7. (a) Schematic diagram of the proposed SiC/GaN cascode device with variations in inductances along the inner gate-driver loop. (b) Turn-ON and (c) turn-OFF waveforms of JFET-1 and JFET-2 with a variation of 10 nH between $L_{\text{G-J1}}$ and $L_{\text{G-J2}}$.

variation in the two sets of gate driver loop gives rise to severe current-sharing imbalance between the two cascode devices (i.e., the two JFETs). This is because the variation in L_{G} will directly affect the turn-ON or turn-OFF delay during switching.

On the contrary, the proposed SiC/GaN cascode device requires only one set of gate driver, as the LV GaN HEMT internally controls the paralleled SiC JFETs through the inner gate driver loop. There is still a chance that variation arises from the leads of inner gate driver. Hence switching performances are simulated with a variation of 10 nH between $L_{\text{G-J1}}$ and $L_{\text{G-J2}}$, as plotted in Fig. 7. It is noted that the influence of variation in $L_{\text{G-J}}$ is limited. As analyzed in *Part B* of this section, the current slew rates are dominated by the time constant of the inner gate driver loop. Therefore, a limited variation in $L_{\text{G-J}}$ will not effectively affect the current sharing behavior within a period of $\sim$1 ns. However, current ringing is observed due to $L_{\text{G-J}}$, as plotted by the current waveforms in Fig. 7(b) and (c).

In summary, it is observed that the variation in $V_{\text{TH-J}}$ is the most crucial factors that lead to current-sharing imbalance between the paralleled SiC JFETs during fast switching transients, especially during device turn-ON, the interval of which is longer than that of device turn-OFF. Other parameters such as g_{JFET} and $L_{\text{G-J}}$ have relatively weaker influence on the current-sharing balance, owing to the fast gate-control speed enabled by the GaN HEMT along the inner gate driver.

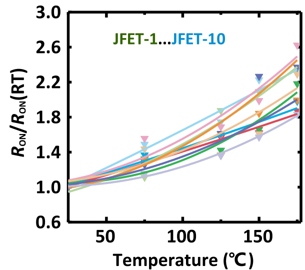

Fig. 8. Positive temperature coefficient of R_{ON} at an elevated temperature from 25 °C to 175 °C obtained by measuring the output curves of 10 SiC JFETs (numbered by JFET-1–JFET-10).

III. Implementation and Characterization of a 1200-V/22-mΩ SiC/GaN Cascode Device

A. Selection of SiC JFETs for the Proposed SiC/GaN Cascode Device

To match the SiC JFETs for parallel operation in a cascode device, ten SiC JFETs (i.e., UJ3N120035K3S) are first measured to validate their positive temperature coefficient of ON-resistance (R_{ON}) when temperature elevates from 25 °C to 175 °C, as plotted in Fig. 8. R_{ON} is extracted by derivation of the linear region of the output curves of the ten SiC JFETs (numbered by JFET-1–JFET-10) by an Agilent B1505A power device analyzer [26]. All SiC JFETs exhibit a positive temperature coefficient, as plotted by the relative value of R_{ON} with respect to R_{ON} at room temperature [(RT), i.e., 25 °C in this work]. With the temperature rising from RT to 175 °C, R_{ON} of the SiC JFETs is nearly tripled (as being enlarged to 2.6 times of R_{ON} at RT), suggesting the potential of restoring current balance between the SiC JFETs in parallel.

Meanwhile, the static transfer I–V characteristics of those ten SiC JFETs are measured using Agilent B1505A power device analyzer, as plotted in Fig. 9(a). Most of the JFETs exhibit a VTH-J of −10 V (at VDS = 0.5 V, ID = 5 mA) with a threshold voltage spread of less than 1 V. Among the ten JFETs, two JFETs deliver notable higher ON-state resistance and higher subthreshold swing compared with the other ones, suggesting defective devices existing in the samples chosen, presumably due to the yield rates of the device processing. The other eight SiC JFETs except the defective ones exhibit approximately identical R_{ON} and transconductances, which can be derived from the derivation of the transfer curves.

Meanwhile, the transfer curves of the SiC JFET under varied temperature from 25 °C to 250 °C are measured, as plotted in Fig. 9(b). The SiC JFETs adopted in this work delivers a thermally stable VTH-J with a slight negative shift of $\sim$0.2 V when the temperature is up to 250 °C, as plotted in Fig. 9(c). The thermal stability of SiC JFETs is owing to the PN-junction type gate stack where the gate is oxide free and, thus, there

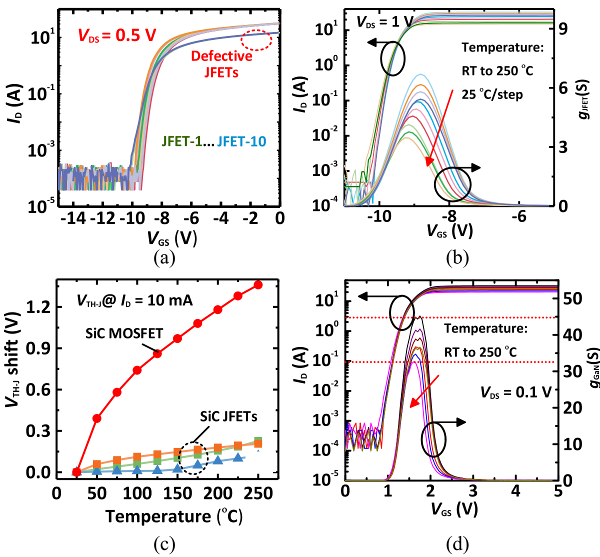

Fig. 9. (a) Transfer curves of JFET-1 to JFET-10 in semi-log plots at RT. (b) Transfer curves and transconductance ($g_{\rm JFET}$) of SiC JFET-1 under varied temperature from 25 °C to 250 °C. (c) $V_{\rm TH\text{-}J}$ shift (the value of which is negative) of SiC JFETs in comparison with a SiC MOSFET under varied temperature ranging from 25 °C to 250 °C. (d) Transfer curves and transconductance ($g_{\rm JFET}$) of the LV GaN HEMT under varied temperature from 25 °C to 250 °C.

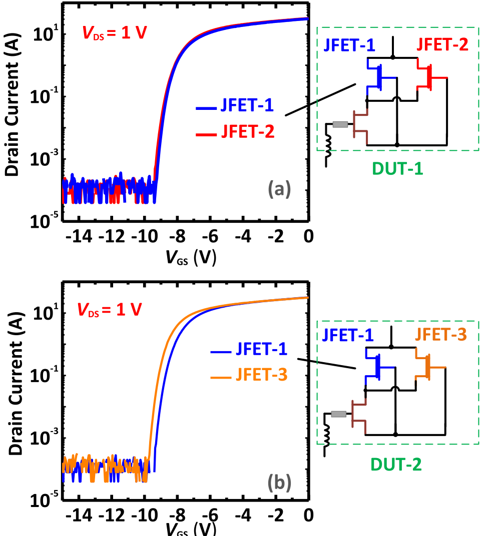

Fig. 10. (a) Transfer curves of JFET-1 and JFET-2 which are well matched. (b) Transfer curves of JFET-1 and JFET-3 with notable variation in $V_{\rm TH\text{-}J}$.

is no SiC/Oxide interface traps that affect the $V_{\rm TH\text{-}J}$ stability under high temperature. Meanwhile, the adopted SiC JFET (UJ3N120035K3S) provided by UnitedSiC features extremely narrow channel and lightly doped channel region as well as N drift region, leading to less sensitive VTH-J with respect to temperature [27]. In comparison, a 1200-V SiC MOSFET (C2M0025120D [28]) of the same power rating could deliver a large negative threshold voltage shift of above 1.3 V [see Fig. 9(c)] when the temperature rises to 250 °C, induced by the detrapping electrons from the SiC/Oxide interface traps along the channel region [29]. Compared with the increasing magnitude of $R_{\rm ON}$ at elevated temperature (see Fig. 8), the slight change in VTH-J due to temperature has a relatively weaker influence on the SiC JFET in parallel.

It is noted that the LV GaN HEMT exhibits a small negative $V_{\rm TH}$ shift (less than 0.15 V) when the temperature rises to 250 °C [see Fig. 9(d)], indicating the thermal stability of $V_{\rm TH\text{-}G}$ provide by the *p*-GaN gate stack. On the other hand, $g_{\rm GaN}$ is reduced from 45 to 30 S as the temperature rises. In comparison, $g_{\rm JFET}$ of the SiC JFET is significantly lower (the value of which is reduced from 7 to 3 S), indicating a relatively a higher gate overdrive required to conduct and a resultant slower turn-OFF speed [see Fig. 9(b)]. Therefore, although high temperature would lead to a slight negative shift in $V_{\rm TH\text{-}G}$ and reduce $g_{\rm GaN}$, $g_{\rm GaN}$ is still several times larger than $g_{\rm JFET}$. A smaller gate over-drive voltage would drive the GaN HEMT into fully turn-ON mode, and thus, the GaN HEMT works as a superiorly fast gate driver, which internally control the switching of the SiC JFETs. The temperature-induced variations in $V_{\rm TH\text{-}G}$ and $g_{\rm GaN}$ would impact the turn-ON or turn-OFF delay time of the SiC/GaN cascode device, much like how changes in temperature can impact power devices due to fluctuations in gate-drive ICs.

As indicated by the simulation results in Section II, the variation in VTH-J is the most crucial factor that affects the current-sharing balance between the SiC JFETs in an SiC/GaN cascode device. Meanwhile, although the parasitic inductances along the power loop can also effectively break the current-sharing balance during switching, the variation in inductances can be cancelled by a symmetry design of circuit layout.

Therefore, according to the transfer curves of the SiC JFETs in Fig. 9, two JFETs (i.e., JFET-1 and JFET-2), which deliver well-matched transfer characteristics [see Fig. 10(a)], are selected to compose a 1200-V SiC/GaN cascode device, namely, the first device under test (DUT-1). For the purpose of comparative studies, a second DUT (i.e., DUT-2) consisting of JFET-1 and JFET-3 with a variation of ∼0.5 V in VTH-J [see Fig. 10(b)] is built. Both DUTs employ the identical GaN HEMT (i.e., EPC2206) and the identical JFET-1.

B. *Static Characteristics of the 1200-V/22mΩ SiC/GaN Cascode Device*

Device-level characterizations are first conducted to evaluate the static performances of the DUTs by the Agilent B1505A power device analyzer, as plotted in Fig. 11(a) and (b). DUT-1 and DUT-2 exhibit almost identical transfer and output characteristics (i.e., $V_{\rm TH}$ = 1.6 V and $R_{\rm ON}$ = 22 mΩ at $V_{\rm GS}$ = 5 V) despite the variations in the SiC JFETs. This is because these two DUTs are measured with no quiescent drain bias ($V_{\rm DS}$ = 0 V) and therewith the SiC JFETs are in ON-state. As the JFETs exhibit similar $R_{\rm ON}$, the transfer and output curves are solely determined by the GaN HEMT, which is identical in both of the two DUTs.

Static OFF-state *I–V* currents results are plotted in Fig. 11(c) accordingly. The cascode device achieves a breakdown voltage of 1200 V with a criterion of 10^5 $I_{\rm ON}/I_{\rm OFF}$ ratio and $I_{\rm OFF}$ is mainly contributed by the drain-to-source leakage current path. This is

TABLE I
FIGURES-OF-MERIT OF THE CASCODE DEVICE IN THIS WORK AND STATE-OF-THE-ART SIC MOSFETS

Device technology	This Work	C2M0025120D [28]	SCT3022KL [30]	IMW120R020M1H [31]
Manufacturer	UnitedSiC/EPC	Cree	Rohm	Infineon CoolSiC
Voltage rating (V)	1200	1200	1200	1200
R_{ON}(mΩ)	22 (V_{GS} = 5 V)	25 (V_{GS} = 20 V)	22 (V_{GS} = 18 V)	19 (V_{GS} = 18 V)
C_{ISS} (pF) (V_{DS}=800 V)	1610	3140	2879	3460
C_{OSS} (pF) (V_{DS}=800 V)	138	224	237	159
C_{RSS} (pF) (V_{DS}=800 V)	2	9	108	23
Q_{GD} (nC)	3	71.5	80	24
R_{ON}*Q_{GD}(mΩ·nC)	66	1787.5	1760	456
V_{GS} limit (V)	−5/+6	−10/+20	−4/+22	−5/+18

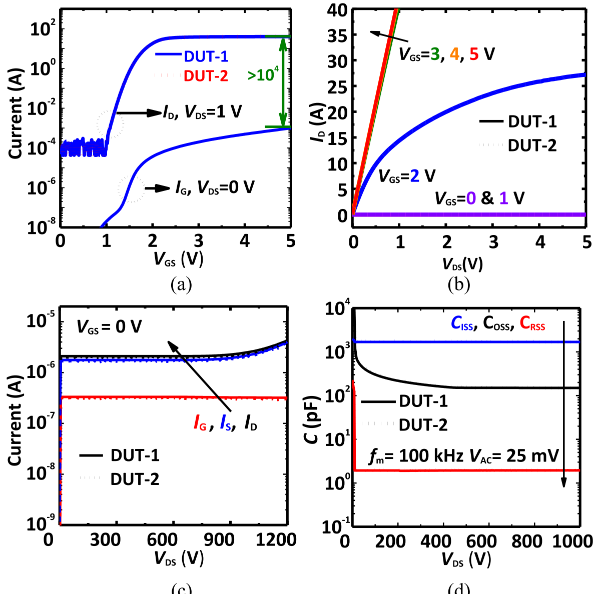

Fig. 11. (a) Semi-log plot of I_G-V_{GS} (V_D=0) and I_D-V_{GS} (V_{DS}=1). (b) I_D-V_D output characteristics in forward-conduction mode. (c) OFF-state leakage currents. (d) C–V curves in drain-voltage blocking state.

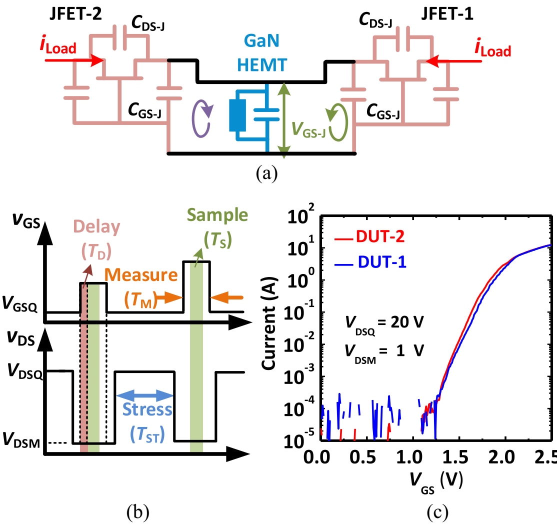

Fig. 12. (a) Equivalent circuit of the proposed cascode device during turn-ON. (b) Soft-switching waveforms for the measurement of transfer characteristics. (c) Transfer curves under dynamic switching operation.

because the GaN HEMT employed here features a Schottky-type gate contact, which is reverse biased during OFF-state.

C–V characteristics of the 1200-V/22-mΩ SiC/GaN cascode device are measured from the three inter-electrode capacitors (i.e., C_{GS}, C_{GD}, and C_{DS}). The measurement results along with other key figures-of-merit are compared with representative state of the art 1200-V SiC MOSFETs delivering a similar R_{ON} (i.e., ∼22mΩ), as summarized in Table I. The proposed 1200-V/22-mΩ SiC/GaN cascode device exhibits significantly lower terminal capacitances (i.e., C_{ISS}, C_{OSS}, and C_{RSS}), owing to the series connection of the LV GaN HEMT and the HV SiC JFETs. The small terminal capacitances suggest its potential of achieving high switching speed. In addition, the extremely small C_{RSS} could facilitate reduced Miller effect and thereof suppressed electromagnetic interference to the gate drive circuitry coupled from the drain terminal. However, the small gate voltage swing (V_{GS} limit in Table I) due to the usage of GaN HEMT would require careful design of gate driver circuitry regarding suppression of electromagnetic interference.

C. Dynamic Characteristics of the 1200-V/22 mΩ SiC/GaN Cascode Device

In order to investigate the impact of variations in SiC JFETs, dynamic performances of the DUTs are required to be measured. One possible method is to capture the subthreshold currents in microseconds during the device transient turned ON immediately after an OFF-state quiescent drain bias (V_{DSQ}). As illustrated by Fig. 12(a), with a V_{DSQ} larger than $-V_{TH\text{-}J}$ (the magnitude of the SiC-JFET's threshold voltage, which is around—9 V according to Fig. 10), $C_{GS\text{-}J}$ and $C_{DS\text{-}G}$ are charged in parallel to pinch off the SiC JFET. When the cascode device is turned ON, $C_{GS\text{-}J}$ and $C_{DS\text{-}G}$ are discharged along the JFET's internal gate driver loop through the GaN HEMT's channel, as illustrated by (1). When the device operates in subthreshold region, R_{GaN} is of several kilo-ohms, resulting in a time constant $\{R_{GaN}\times(C_{GS\text{-}J}+C_{DS\text{-}G})\}$ of a few microseconds (as $C_{GS\text{-}J}+C_{DS\text{-}G}$ is of several nanofarads) along the internal gate drive loop of the JFETs. A JFET would be turned ON immediately when $V_{GS\text{-}J}$ reaches $-V_{TH\text{-}J}$.

As JFET-3 exhibits a $-V_{TH\text{-}J}$ of 9.5 V which is 0.5 V higher than that of JFET-1, JFET-3 is turned ON earlier than JFET-1 in DUT-2. On the contrary, JFET-1 and JFET-2 are turned ON simultaneously within DUT-1 as JFET-1 and JFET-2 offer

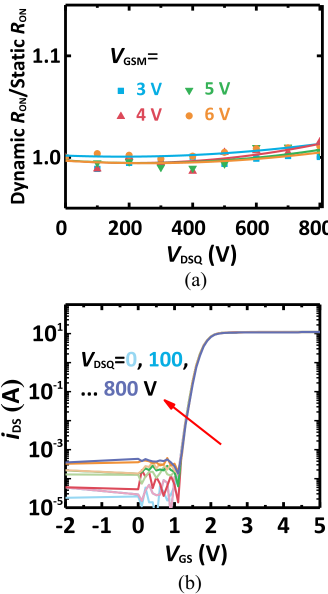

Fig. 13. (a) Dynamic R_{ON} of the proposed SiC/GaN cascode device (b) V_{TH} shift under varied drain voltage stress (V_{DSQ}).

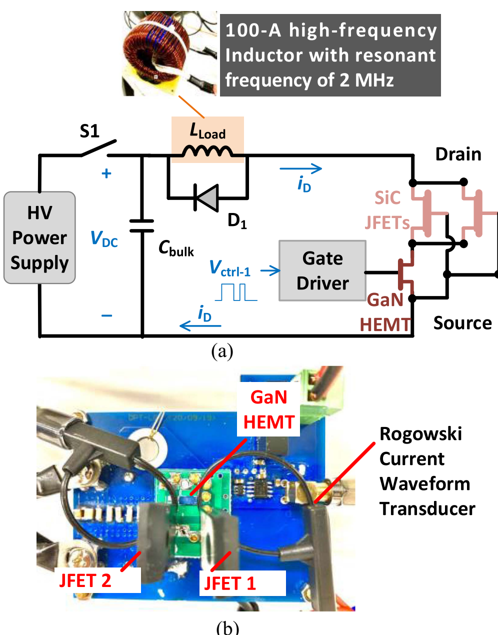

Fig. 14. (a) Circuit schematic diagram and (b) photograph of the DPT setup with a daughter board on which the SiC/GaN cascode device is implemented.

identical $V_{\mathrm{TH\text{-}J}}$. Therefore, there would be variations between DUT-1 and DUT-2 witnessed by the subthreshold drain current (i_{D}), which could reveal the impact of variation in $-V_{\mathrm{TH\text{-}J}}$.

For verification, a high-speed AMCAD pulsed *I-V* system [26] is employed to measure the subthreshold current with a time resolution of less than 1 μs, as illustrated by the soft-switching waveforms in Fig. 12(b). The measurement starts directly with OFF–ON soft-switching cycles. Within one cycle of switch, the device is first stressed at OFF-state ($V_{\mathrm{GSQ}} = 0$ V) with a quiescent drain bias ($V_{\mathrm{DSQ}} = 20$ V), and then switched to the ON-state ($V_{\mathrm{DSM}} = 1$ V and V_{GSM} rises from 0 to 2.5 V at a step of 0.0125 V by each cycle) in the linear region with i_{D} measured shortly after (delayed by $T_{\mathrm{D}} = 1$ μs) by averaging the values in the sample window (i.e., $T_{\mathrm{S}} = 0.5$ μs) at a sample rate of 50 MHz. The pulsewidth (T_{M}) is 4 μs, and the pulse period (one OFF–ON cycle) is 1 ms. As shown by the measurements results in Fig. 12(c), DUT-2 exhibits higher i_{D} than DUT-1 in their subthreshold region (at $V_{\mathrm{GSM}} < 1.7$ V), due to the earlier turn-ON of JFET-3 with a higher value of $-V_{\mathrm{TH\text{-}J}}$.

Dynamic R_{ON} and V_{TH} shift of the demonstrated cascode device is characterized using the AMCAD system [26], as plotted in Fig. 13. The 1200-V SiC/GaN cascode device delivers a stable dynamic R_{ON} at $V_{\mathrm{G\text{-}ON}} = 3$–6 V under $V_{\mathrm{DSQ}} = 800$ V. The V_{TH} shift is also negligibly small, because the HV SiC JFET shields most of the drain voltage for the LV GaN HEMT and therewith the voltage-drop induced storage charge is small in the *p*-GaN gate.

D. Hard-Switching Characteristics of the 1200-V/22 mΩ SiC/GaN Cascode Device

A DPT is deployed to investigate the switching characteristics of the SiC/GaN cascode device as well as the transient current-sharing behaviors among the two SiC JFETs. The two SiC JFETs are soldered in a symmetrical layout on a daughter board, realizing a uniform distribution of parasitic inductances along the power loop.

The schematic diagram of the experimental set-up and the daughter board is depicted in Fig. 14. The drain current (i_{D}) of both the SiC JFETs are measured by two Rogowski transducers with isolated outputs monitored by an oscilloscope. Two differential probes are applied to measure the drain-to-source voltage (v_{DS}) and the gate driver voltage ($v_{\mathrm{GS\text{-}G}}$) imposed on the gate electrode of the GaN HEMT.

Two 1200-V/50-A SiC Schottky diode are employed as the freewheeling diode of the load inductance to facilitate fast commutation and low reverse recovery charges. The 100-A load inductance features high frequency enabled by low parasitic capacitance between its windings.

Instead of a recommended turn-ON gate driver voltage of up to ~15 V in the case of 1200-V SiC power MOSFETs (see Table I), the suggested turn-ON gate voltage ($V_{\mathrm{G\text{-}ON}}$) of that *p*-GaN gate HEMTs are much lower, e.g., ranging from 3 to 6 V. A modest $V_{\mathrm{G\text{-}ON}}$ of 5 V is adopted to drive the cascode device to overcome the drain bias induced positive V_{TH}-shift while keeping $v_{\mathrm{GS\text{-}G}}$ below the upper limit.

The hard-switching behaviors of DUT-1 and DUT-2 under 800-V/80-A are characterized (at a gate resistance of 2 Ω, a load inductance of 100 μH), as plotted in Figs. 15 and 16. DUT-1 exhibits a balanced current-sharing among JFET-1 and JFET-2 during both turn-ON and turn-OFF transitions, as shown in Fig. 15. In contrary, DUT-2 exhibits noticeable transient current-sharing imbalance among JFET-1 and JFET-3. During the turn-ON transient, as JFET 3 exhibits a $-V_{\mathrm{TH\text{-}J}}$ of 9.5 V, which is 0.5 V higher than that of JFET-1, JFET-3 is turned ON earlier than JFET-1 and thereby bares larger portion of the

TABLE II
COMPARISON BETWEEN THE SiC/GaN CASCODE DEVICE AND STATE OF THE ART TWO PARALLEL SiC MOSFETs

Device technology	This Work	C3M0040120D [32]	SCT3040KL [33]	IMBG120R045M1H [34]
Manufacturer	UnitedSiC/EPC	Cree	Rohm	Infineon CoolSiC
Voltage Rating (V)	1200	1200	1200	1200
Number of devices	Two SiC JFETs and one GaN HEMT	Two devices in parallel		
R_{ON}(mΩ)	22 (V_{GS} = 5 V)	20 (V_{GS} = 20 V)	20 (V_{GS} = 20 V)	22 (V_{GS} = 20 V)
Gate-driver loss ($E_{G\text{-}OSS}$)	71 nJ	2900 nJ	2700 nJ	1100 nJ
Integration range of V_{GS} (V)	0/+5	0/+15	0/+15	0/+15
Switching loss* (E_{Total})	3 mJ	3.7 mJ	3.3 mJ	3.1 mJ
C_{ISS}（pF）(V_{DS}=800 V)	1610	5800	2674	3054
C_{OSS}（pF）(V_{DS}=800 V)	138	206	152	140
Cost of devices** in USD ($)	43.8	34.7	91.3	31.2

*The switching losses are measured under 800-V/80-A with a gate resistance (R_G) of 2 Ω, a load inductance of 100 μH and a SiC Schottky-barrier diode [35] as the freewheeling diode.
**The device prices refer to the online prices (at a sales volume of 500) at: www.digikey.com (3 January 2023).

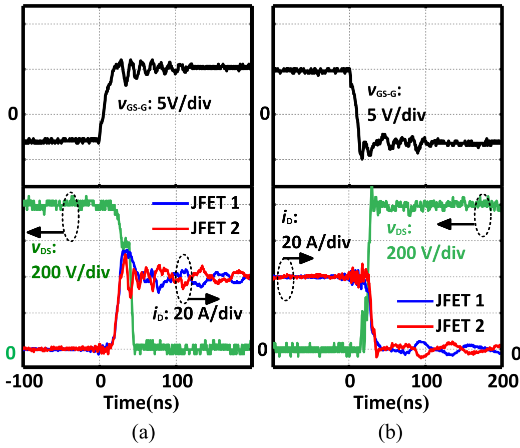

Fig. 15. Transient waveforms of DUT-1 built with well-matched JFET-1 and JFET-2 during (a) turn-ON and (b) turn-OFF under 800 V/80 A.

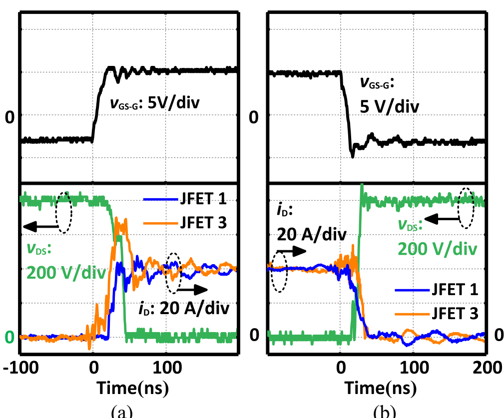

Fig. 16. Transient waveforms of DUT-2 built by JFET-1 and JFET-3 with varied transfer characteristics during (a) turn-ON and (b) turn-OFF under 800 V/80 A.

transient rising current. The currents are redistributed among the two JFETs until JFET-1 is fully turned ON within 50 ns. During the turn-OFF transient, JFET-1 is pinched off first due to its lower $-V_{TH\text{-}J}$ and JFET-3 still bares higher current diverted

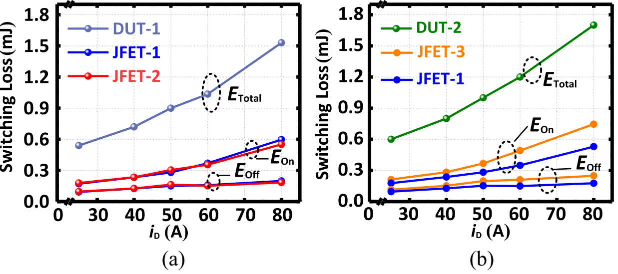

Fig. 17. (a) Switching losses of DUT-1 (E_{Total}), turn-ON and turn-OFF losses of JFET-1 and JFET-2 (E_{ON} and E_{OFF}). (b) Switching losses of DUT-2 (E_{Total}), turn-ON and turn-OFF losses of JFET-1 and JFET-3 (E_{ON} and E_{OFF}).

from JFET-1. Since the turn-OFF duration is shorter than the turn-ON duration, the turn-OFF current redistribution is alleviated compared to the device turn-ON.

Therefore, the SiC JFET with higher $-V_{TH\text{-}J}$ (corresponding to a lower $V_{TH\text{-}J}$, which is negative) bares larger switching stress during both turn-ON and turn-OFF transitions in a parallel connection within the cascode device, as indicated by the switching energy in Fig. 17. As plotted in Fig. 17(a), the switching loss imbalance among JFET-1 and JFET-2 in DUT-1 is less than 1.5%. However, as plotted in Fig. 17(b), the switching loss imbalance among JFET-1 and JFET-3 is over 25% when i_D rises to 80 A, due to the uneven current sharing induced by the variation of SiC JFETs.

In the meantime, a comparison is made regarding gate-driver loss, switching loss, and device cost between the proposed SiC/GaN cascode device and conventional parallel SiC MOSFETs. As the SiC/GaN cascode device demonstrated in this work adopts two SiC JFETs, which enables a rated voltage of 1200-V and a R_{ON} of 22-mΩ, two parallel 40-mΩ SiC MOSFETs are selected to achieve a R_{ON} of ~20 mΩ from state of the art products, including a planar gate SiC MOSFET, a double-trench gate one ,and an asymmetry trench gate one, as summarized in Table II. The proposed SiC/GaN cascode device features significantly lower gate-driver loss compared with a conventional parallel connection of two SiC MOSFETs, owing to the low gate charge required to switch offered by the

GaN HEMT. The switching losses of the four topologies are quite close to each other, with the cascode device delivering a slightly lower switching loss as a result of its lower C_{OSS}. The device cost would be higher according to the prices given by the distributor of *Digi-Key Electronics* (USA). This may be because of marketing issues, such as mass production and shipping fee (the device provided by Rohm is significantly more expensive than the others).

IV. Conclusion

An all-WBG SiC/GaN cascode device built with parallel SiC JFETs controlled by a single GaN HEMT is proposed and demonstrated by a 1200-V/22-mΩ prototype, which exhibits extremely small interelectrode capacitance, high-temperature threshold stability, and superior low gate-driver losses, of which features are promising for high-frequency applications. It is found that the variation in threshold voltages is the most important factor affecting the current-sharing balance among the paralleled SiC JFETs. By matching the transfer characteristics of the SiC JFETs and applying a symmetry circuit layout accordingly, the current imbalance between the paralleled SiC JFETs can be restricted below 1.5% under high-power hard-switching conditions. It is worthwhile to point it out that the proposed hybrid switch can be implemented in a multichip copackaged module for enhanced performances.

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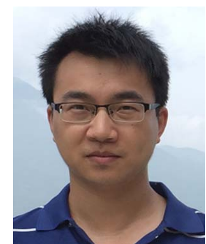

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