Single-Switch Discontinuous Current-Source Gate Driver With Voltage Boosting Capability and No Current Diversion

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***Abstract*—This article presents a novel single-switch discontinuous current-source gate driver (CSD)with voltage boosting capability appropriate for ultralow voltage applications. The power MOSFET gate current using this CSD does not deviate during both turn-ON and turn-OFF transitions. Thus, in comparison to the previous CSDs, the effective gate current is much higher and nearly constant during switching transitions, which would reduce both turn-ON and turn-OFF transient intervals and consequently the switching losses. Other advantages of this CSD are low number of components, high $C\frac{dv}{dt}$ immunity, and the ability to increase the gate-source voltage to more than the gate-drive source voltage, which reduces the drain-source ON-resistance($R_{DS(on)}$). The power MOSFET fast transition intervals and low $R_{DS(on)}$ have contributed to improved efficiency. The proposed CSD is analyzed and theoretical analysis is verified by the stimulation and experimental results at 1 MHz.**

***Index Terms*—Current diversion problem, current-source gate driver (CSD), voltage-source gate driver (VSD).**

I. Introduction

INCREASED power consumption of microprocessors has led to larger power supplies and urgent demand for higher power density. The practical approach to reach higher power density is raising the switching frequency, which contributes to higher switching losses and gate drive losses [1], [2], [3], [4].

DC–DC buck converters with the voltage-source gate driver (VSD) are extensively used as voltage regulator modules (VRMs) to supply the microprocessors as illustrated in Fig. 1 while the VSD circuit is shown in Fig. 2(a) [5], [6]. At higher switching frequencies, VRMs with conventional voltage-source drivers (VSDs) are no longer efficient because the effective gate current is low, and the power MOSFET gate energy is wasted in the gate resistance during the turn-OFF transition. Thus, increasing the switching frequency negatively affects the VRM efficiency [7]. Also, at switching transitions of VSD-driven power MOSFETs (as shown in Fig. 1), the induced voltage across the source inductance (L_s), gate resistance (r_g), and the gate drive supply voltage affect the gate current. The L_s and drain inductance (L_D) are produced by traces and interconnections inside and outside the package of a power MOSFET [8]. The induced voltage across L_s increases V_{gs} and reduces the gate current before the power MOSFET is completely turned ON or OFF, which increases the switching time intervals and consequently the switching loss [9].

In order to reduce the gate drive loss, resonant gate drivers (RGDs) are introduced [10], [11], [12]. RGDs recover the power MOSFET gate energy at the turn-OFF transition by employing an inductor. However, the power MOSFET gate capacitors charge and discharge with zero initial current, which limits the power MOSFET switching speed, and consequently, the RGDs cannot

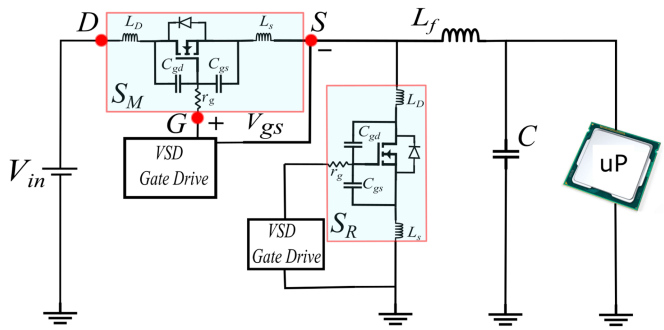

Fig. 1. Power MOSFET equivalent circuit in a buck VRM.

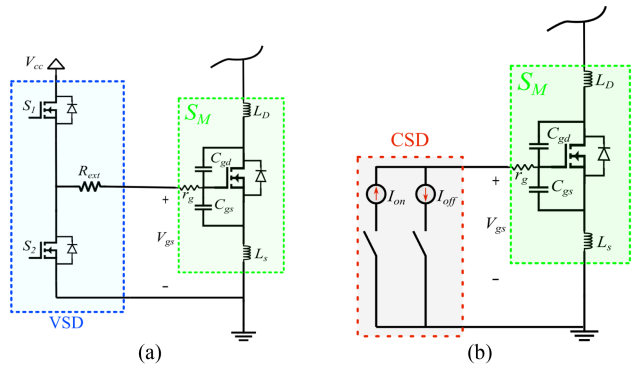

Fig. 2. (a) Voltage source gate driver (VSD). (b) Equivalent circuit of CSD.

Manuscript received 26 January 2023; revised 5 April 2023 and 17 June 2023; accepted 12 July 2023. Date of publication 24 July 2023; date of current version 1 September 2023. Recommended for publication by Associate Editor M. Ponce-Silva. *(Corresponding author: Hosein Farzanehfard.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3298091.

Digital Object Identifier 10.1109/TPEL.2023.3298091

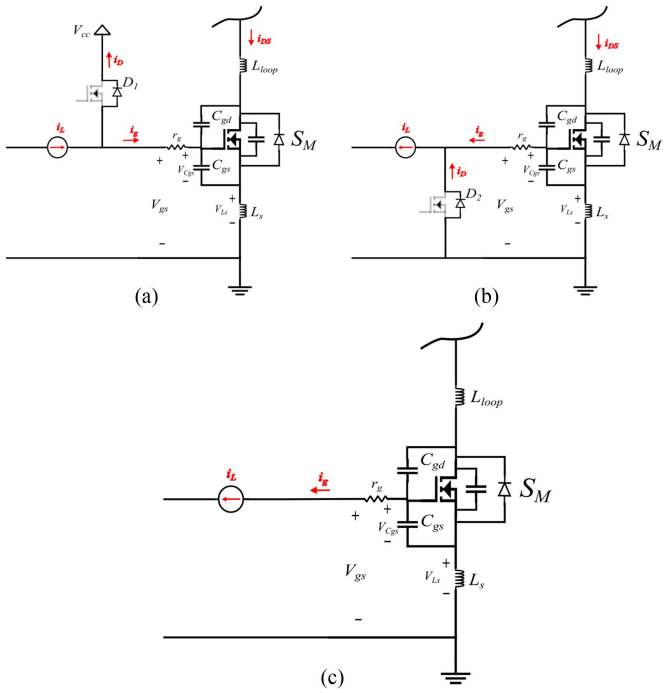

Fig. 3. Equivalent circuit of CSDs. (a) With current diversion during turn-ON. (b) With current diversion during turn-OFF. (c) Without current diversion.

reduce the switching losses [13]. RGDs are proper for applications where the switching losses are not predominant (e.g., synchronous rectifiers in buck VRMs) [14].

To turn the power MOSFET ON and OFF with a nearly constant nonzero initial current, current-source drivers (CSDs) [13], [15], [16] are introduced, with the equivalent circuit illustrated in Fig. 2(b), in order to reduce the switching and gate drive losses [15]. The main problem of CSDs is the gate current diversion during turn-OFF and turn-ON transitions due to the presence of parasitic components L_s and r_g[14].

The equivalent circuit of CSDs and the current diversion during turn-ON and turn-OFF transitions are illustrated in Fig. 3(a) and (b), respectively. When the power MOSFET S_M drain current is increased or decreased, the induced voltage across L_s turns ON the diodes D_1 and D_2 during turn-ON and turn-OFF transitions, respectively, and some of the gate current is deviated in diodes. Thus, due to the current diversion, the gate current decreases, which increases the switching time intervals and therefore switching loss. The solution to mitigate the current diversion is to use CSDs that act as an ideal current source, as shown in Fig. 3(c).

In ultralow voltage applications, due to the low input voltage level, the power MOSFET gate voltage should be raised to a higher level than the input voltage. This leads to lower MOSFET ON-resistance, which would considerably reduce the conduction loss [17], [18]. High-frequency applications with gate voltage boosting requirements are extensive, including class E low-power amplifiers, VRMs, cochlear implants, synchronous buck–boost converters used for portable applications, and tapped inductor buck converter [17].

The CSDs introduced in [7], [17], [19], [20], [21], [22], and [23] can reduce switching losses compared with RGDs, but cannot solve the current diversion problem and without voltage boosting capability are not suitable for ultralow voltage applications. In [15], some series diode were used to create negative gate-source voltage to solve the current diversion problem at the turn-OFFtransition; however, the current diversion at the turn-ON transition is not solved. This CSD has five control switches, and the negative gate-source voltage depends on the number of diodes, thus, it requires a higher number of components. This CSD is not able to provide the gate voltage higher than the drive supply voltage, hence, it is not proper for ultralow voltage applications. The proposed circuit in [13] can solve the current diversion at turn-ON and turn-OFF transitions but the gate capacitor is not clamped to any voltage. Thus, the CSDs inductor can have undesired resonance with gate capacitor and cause unsought triggering of the power MOSFET and increase the conduction loss. In addition, this CSD uses many components including four switches and two diodes. The circuit in [14] with two control switches was proposed to solve the current diversion in the turn-OFFtransition. This CSD acts like an ideal current source at the turn-OFF transition, and the inductor current does not deviate, but the at turn-ON transition cannot solve the current diversion problem. In addition, the negative gate-source voltage of this CSD is twice the positive voltage, thus, it is not appropriate for applications that require a gate-source voltage more than 10 V. Also, without voltage boosting capability, this CSD cannot be used for ultralow voltage applications. The CSDs presented in [7] and[17] have voltage boosting capability with two and four control switches, respectively, but they have the current diversion problem at the turn-OFF transition, which increases the switching losses.

In this article, a single-switch discontinuous CSD is introduced, which reduces the gate drive and switching losses with minimum number of components and simple control circuit. This CSD operates as an ideal current source during turn-OFFand turn-ON transitions, respectively. Thus, the current diversion problem is solved at turn-ON and turn-OFF transitions, and the power MOSFET switching losses are reduced. In addition, with voltage boosting capability, which increases the gate voltage to more than the gate drive supply voltage, the power MOSFET conduction loss is reduced.

II. Circuit Description and Operation

As shown in Fig. 4, the proposed CSD consists of a control switch S, a diode D, a pair of coupled inductors (L_1 and L_2) with the turns ratio determined as $n = N_1/N_2$, L_{lk_1} is the primary-side leakage inductance, and V_{cc} is the CSD power supply. This CSD drives the power MOSFET S_M where the key waveforms are illustrated in Fig. 5, and S is the gate signal for the control switch, I_{L_m} is the magnetizing inductance current, I_{n_1} and I_{n_2} are the primary- and secondary-side currents, respectively. Also, I_g is the power MOSFET (S_M) gate current, and $V_{\rm gs}$ is the gate-source voltage.

The operation of the proposed circuit is described in eight modes, as shown in Fig. 6. Before t_0, the power MOSFET S_M

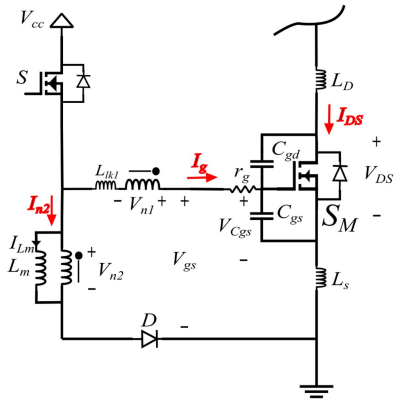

Fig. 4. Proposed discontinuous CSD.

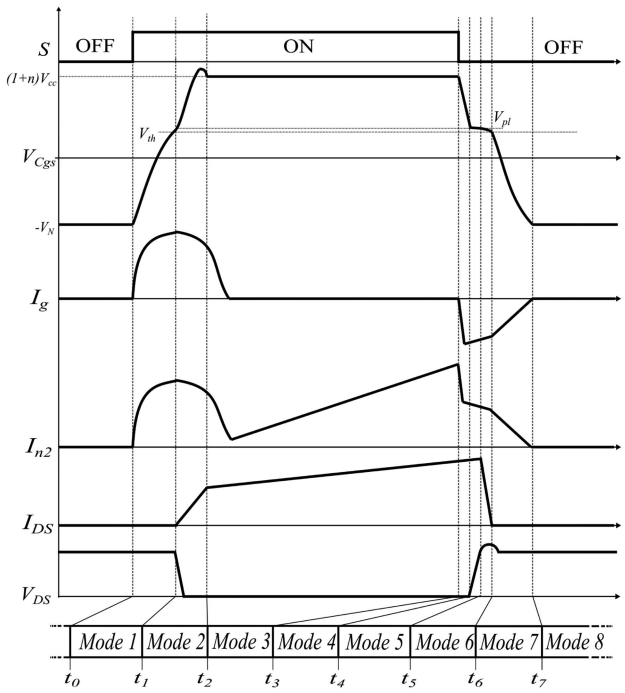

Fig. 5. Key waveforms of the proposed CSD.

is OFF,and the gate-source voltage (V_{gs}) is negative and equal to V_N.

1) Mode 1 $[t_0 - t_1]$ *[Fig. 6(a)]:* At t_0, the switch S is turned ON under zero-current switching (ZCS), and a resonance occurs between power MOSFET (S_M) gate capacitors and $L_{lk1} + L_s$, and thus, the gate capacitors start to charge from the final negative gate-source voltage (V_N). In this resonance, L_s is part of the resonant network and there is no path for the gate current to deviate in this mode. At the same time, the diode D turns ON, and the currents of the coupled inductors are the same. This mode is continuous until the voltage of gate-source capacitor $V_{C_{\text{gs}}}$ reaches the gate threshold voltage (V_{th}) of power MOSFET S_M. The relations for I_g and $V_{C_{\text{gs}}}$ are as follows:

$$V_{C_{\text{gs}}}(t) = e^{-\alpha_0 t}\left(A_0 \cos\left(\sqrt{\omega_0^2 - \alpha_0^2}\,t\right) + B_0 \sin\left(\sqrt{\omega_0^2 - \alpha_0^2}\,t\right)\right) \tag{1}$$

$$I_g(t) = (C_{\text{gs}} + C_{\text{gd}})\frac{d}{dt}V_{C_{\text{gs}}}(t) \tag{2}$$

$$A_0 = V_N + V_{cc}, \quad B_0 = \frac{\alpha_0 A_0}{\sqrt{\omega_0^2 - \alpha_0^2}} \tag{3}$$

$$R_{\text{on}} = R_{\text{DS}_S} + r_g + R_{\text{ac}} \tag{4}$$

$$\alpha_0 = \frac{R_{\text{on}}}{2(L_{lk1} + L_s)}, \quad \omega_0 = \frac{1}{\sqrt{(L_{lk1} + L_s)(C_{\text{gs}} + C_{\text{gd}})}} \tag{5}$$

where C_{gd} is the power MOSFET (S_M) gate-drain capacitor, R_{DS} is the ON-resistance of S, r_g is the power MOSFET (S_M) gate resistance, and R_{ac} is the primary winding (N_1) ac resistance.

2) Mode 2 $[t_1 - t_2]$ *[Fig. 6(b)]:* At t_1, the power MOSFET (S_M) drain-source current I_{DS} starts to increase from zero. The current through the L_{lk1} is charging the gate capacitors and there is no path for the gate current to divert. In this mode, depending on the induced voltage across L_s and L_D, the following two different operating states may happen.

A. V_{DS} in (2) remains greater than $V_{C_{\text{gs}}} - V_{\text{th}}$; thus, the power MOSFET S_M operates in saturation region.

B. V_{DS} decreases to a voltage value lower than $V_{C_{\text{gs}}} - V_{\text{th}}$, due to large enough induced voltage across L_s and L_D, and the power MOSFET S_M enters the ohmic region before drain-source current (I_{DS}) reaches the load current.

In low-voltage applications, such as VRMs due to low input voltage and high output current, V_{DS} reaches zero before I_{DS} reaches peak value. The power MOSFET S_M enters the ohmic region in a short time; thus, case B occurs, and this mode ends when V_{gs} reaches $V_{cc}(1 + n)$

$$V_{\text{DS}} = V_{\text{in}} - V_{L_s} - V_{L_D}. \tag{6}$$

3) Mode 3 $[t_2 - t_3]$ *[Fig. 6(c)]:* At t_2, V_{gs} is clamped to $V_{cc}(1 + n)$, and the I_{L_m} is increasing to reach the optimal designed current

$$I_{L_m} = \frac{V_{cc}(t_3 - t_2)}{L_m}. \tag{7}$$

4) Mode 4 $[t_3 - t_4]$ *[Fig. 6(d)]:* This mode begins by turning OFF S under zero-voltage switching (ZVS) due to the existence of power MOSFET S_M gate-source capacitor (C_{gs}), which behaves as a snubber capacitor for switch S, as shown in Fig. 7. Also, during this mode, I_{L_m} discharged the power MOSFET (S_M) gate capacitors until $V_{C_{\text{gs}}}$ reaches V_{pl}. I_g is obtained from (2), and other important relations are as follows:

$$V_{pl} = V_{\text{th}} + \frac{I_o}{g_{fs}} \tag{8}$$

$$V_{C_{\text{gs}}}(t) = V_{fD} + e^{-\alpha_1 t}\left(A_1 \cos\left(\sqrt{\omega_1^2 - \alpha_1^2}\,t\right)\right.$$

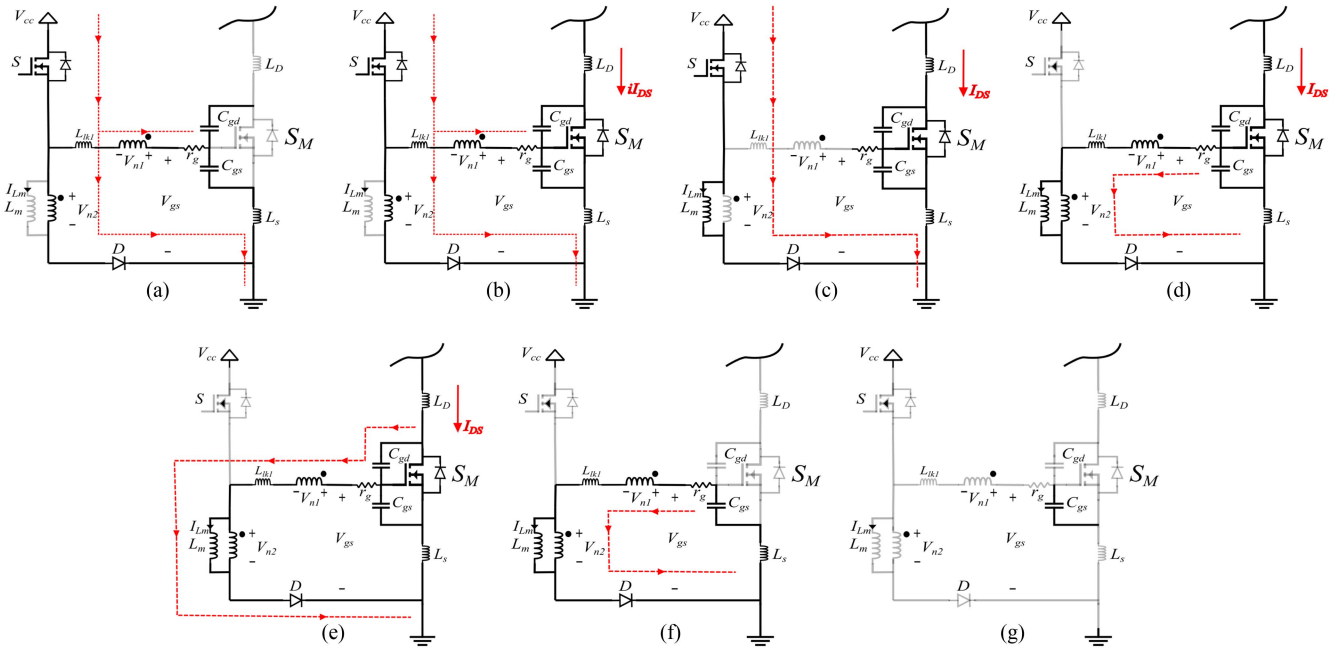

Fig. 6. Current path in each operating mode. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Modes 4 and 6. (e) Mode 5. (f) Mode 7. (g) Mode 8.

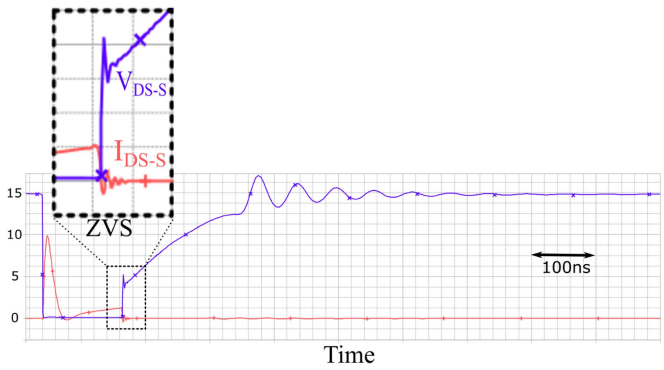

Fig. 7. Simulation waveforms of $I_{\mathrm{DS}-S}$ (drain-source current) and $V_{\mathrm{DS}-S}$ (drain-source voltage) of switch S.

$$+ B_1 \sin\left(\sqrt{\omega_1^2 - \alpha_1^2}\, t\right)\Bigg)$$

$$A_1 = V_{cc}(1+n) - V_{fD}$$

$$B_1 = \frac{\alpha_1 A_1 + \frac{I_{\mathrm{pre}}}{(C_{\mathrm{gs}}+C_{\mathrm{gd}})}}{\sqrt{\omega_1^2 - \alpha_1^2}} \tag{9}$$

$$\alpha_1 = \frac{R_{\mathrm{off}}}{2(L_m + L_s)} \tag{10}$$

$$R_{\mathrm{off}} = r_g + 2R_{\mathrm{ac}} \tag{11}$$

$$\omega_1 = \frac{1}{\sqrt{(L_m + L_s)(C_{\mathrm{gs}} + C_{\mathrm{gd}})}} \tag{12}$$

where V_{fD} is the diode D forward voltage bias, I_{pre} is the I_{L_m} value when S is turned OFF, and g_{fs} is the power MOSFET (S_M) transconductance.

5) Mode 5 $[t_4 - t_5]$ [Fig. 6(e)]: In this mode, $V_{C_{\mathrm{gs}}}$ remains constant and equal to V_{pl}, and I_{L_m} discharges the gate-drain capacitor (C_{gd}) while V_{DS} starts to increase from $R_{\mathrm{DS}(on)@V_{pl}} I_o$ to reach V_{in} and I_{ds} remains constant. When V_{DS} reaches V_{in}, this mode ends, and V_{DS} and I_g are derived as follows:

$$I_g(t) = \frac{V_{pl} - V_{fD}}{R_{\mathrm{off}}} + \left(I_g(t_4) - \frac{V_{pl} - V_{fD}}{R_{\mathrm{off}}}\right) e^{\frac{R_{\mathrm{off}}}{L_m + L_s} t} \tag{13}$$

$$V_{\mathrm{DS}}(t) = R_{\mathrm{DS}(on)@V_{pl}} I_o - \frac{1}{C_{\mathrm{gd}}} \int_0^{t_5 - t_4} I_g(t)\, dt \tag{14}$$

where $R_{\mathrm{DS}(on)@V_{pl}}$ is the power MOSFET (S_M) drain-source resistance when $V_{C_{\mathrm{gs}}}$ is equal to V_{pl}.

6) Mode 6 $[t_5 - t_6]$ [Fig. 6(d)]: At t_5, V_{DS} reaches V_{in}, and I_{L_m} has discharged C_{gs} to V_{th}. During this mode, I_{DS} starts to decrease from load current to zero, which produces a voltage across L_s and L_D, and thus, V_{DS} keeps increasing. In this mode, there is only one path for I_{L_m}, which discharges C_{gs}, and thus, the current diversion problem is solved. At the end of this mode, $V_{C_{\mathrm{gs}}}$ reaches V_{th}. In this mode, $V_{C_{\mathrm{gs}}}$, I_{DS}, and V_{DS} behave as follows:

$$V_{C_{\mathrm{gs}}} = V_{fD} + A_2 e^{-\alpha_2 - \sqrt{\alpha_2^2 - \omega_1^2}\, t} + B_2 e^{-\alpha_2 + \sqrt{\alpha_2^2 - \omega_1^2}\, t} \tag{15}$$

$$A_2 = \frac{(V_{pl} - V_{fD})(-\alpha_2 + \sqrt{\alpha_2^2 - \omega_1^2}) - \frac{I_g(t_5)}{C_{\mathrm{gs}}+C_{\mathrm{gd}}}}{2\sqrt{\alpha_2^2 - \omega_1^2}} \tag{16}$$

$$B_2 = \frac{(V_{pl} - V_{fD})(+\alpha_2 + \sqrt{\alpha_2^2 - \omega_1^2}) + \frac{I_g(t_5)}{C_{\mathrm{gs}}+C_{\mathrm{gd}}}}{2\sqrt{\alpha_2^2 - \omega_1^2}} \tag{17}$$

$$\alpha_2 = \frac{L_s g_{fs} + R_{\text{off}}(C_{\text{gs}} + C_{\text{gd}})}{2(L_m + L_s)(C_{\text{gs}} + C_{\text{gd}})} \tag{18}$$

$$I_{\text{DS}}(t) = g_{fs}(V_{C_{\text{gs}}} - V_{\text{th}}) \tag{19}$$

$$V_{\text{DS}}(t) = V_{\text{in}} + L_s\left(-\frac{dI_{\text{DS}}}{dt} + \frac{dI_g}{dt}\right) - L_D\frac{dI_{\text{DS}}}{dt} \tag{20}$$

where L_D is the drain parasitic inductance of power MOSFET S_M.

7) Mode 7 $[t_6 - t_7]$ [Fig. 6(f)]: At t_6, I_{DS} has reached zero and the power MOSFET (S_M) is OFF. I_{L_m} discharged C_{gs} from V_{th} to zero, and then, the rest of the CSD inductor current I_{L_m} causes C_{gs} voltage to reach its negative peak value V_N, and this mode ends. I_g is obtained from (2), and $V_{C_{\text{gs}}}$ is derived as follows:

$$V_{C_{\text{gs}}}(t) = V_{fD} + e^{-\alpha_1 t}\left(A_3\cos\left(\sqrt{\omega_1^2 - \alpha_1^2}t\right) + B_3\sin\left(\sqrt{\omega_1^2 - \alpha_1^2}t\right)\right) \tag{21}$$

$$A_3 = V_{\text{th}} - V_{fD}, \qquad B_3 = \frac{A_3\alpha_1 + \frac{I_g(t_6)}{C_{\text{gs}}+C_{\text{gd}}}}{\sqrt{\alpha_1^2 - \omega_1^2}}. \tag{22}$$

8) Mode 8 $[t_7 - t_8]$ [Fig. 6(g)]: At t_7, $V_{C_{\text{gs}}}$ reaches V_N, D is turned OFF, and I_{L_m} remains zero until S turns ON.

III. Loss Analysis

In VRMs, the power MOSFET switching losses are reduced by removing the current diversion problem and increasing the gate current, whose higher effective gate current increases the gate drive loss. Thus, there is a tradeoff between the switching and gate drive losses to obtain the optimal gate current (CSD current).

In order to reach the optimum design for CSD inductor current, $I_g, I_{\text{DS}}, V_{C_{\text{gs}}}$, and V_{DS} are derived in each mode to calculate the switching and gate drive losses.

The total losses of the proposed CSD include the conduction loss of diode P_D, the conduction loss of the control switch P_S, the gate driver coupled inductors losses P_{ind}, the gate resistance losses (P_{r_g}) of the power MOSFET S_M, and the gate losses of the control switch P_{gate}. The control switch in this CSD operates under ZCS at the turn-ON transition and ZVS at the turn-OFF transition, and hence, the switching losses of the control switch can be ignored.

A. Switching Losses

1) Turn-OFF Loss: At the turn-OFF transition, the switching loss occurs in *modes 5 and 6*, thus

$$P_{\text{loss-off}} = f_{\text{sw}}\left(\int_{t_4}^{t_5} I_o V_{\text{DS}}(t)dt + \int_{t_5}^{t_6} I_{\text{DS}}(t)V_{\text{DS}}(t)dt\right) \tag{23}$$

where f_{sw} is the switching frequency and I_o is the load inductor current in VRM.

2) Turn-ON Loss: In VRMs, during turn-ON transitions when $V_{\text{gs}} > V_{\text{th}}$, the drain-source voltage becomes zero before the drain-source current reaches a steady-state value but at light load in VRMs with VSDs, this may not occur. The proposed CSD, without current diversion in the turn-ON transition by higher effective gate current, guarantees that the drain-source voltage (V_{DS}) drops to zero before the drain-source current (I_{DS}) reaches the load current. Thus, I_{DS} is calculated from (19), and V_{DS} is obtained as follows:

$$V_{C_{\text{gs}}}(t) = A_0 + B_4 e^{-}\alpha_3 - \sqrt{\alpha_3^2 - \omega_0^2}t + C_0 e^{-\alpha_3 + \sqrt{\alpha_3^2 - \omega_0^2}t} \tag{24}$$

$$B_4 = \frac{V_{\text{th}}(-\alpha_3 + \sqrt{\alpha_3^2 - \omega_0^2}) - \frac{I_g(t_1)}{C_{\text{gs}}+C_{\text{gd}}}}{2\sqrt{\alpha_3^2 - \omega_0^2}} \tag{25}$$

$$C_0 = \frac{V_{\text{th}}(+\alpha_3 + \sqrt{\alpha_3^2 - \omega_0^2}) + \frac{I_g(t_1)}{C_{\text{gs}}+C_{\text{gd}}}}{2\sqrt{\alpha_3^2 - \omega_0^2}} \tag{26}$$

$$\alpha_3 = \frac{L_s g_{fs} + R_{\text{on}}(C_{\text{gs}} + C_{\text{gd}})}{(L_{\text{lk}} + L_s)(C_{\text{gs}} + C_{\text{gd}})} \tag{27}$$

$$I_{\text{DS}}(t) = g_{fs}(V_{\text{gs}} - V_{\text{th}}) \tag{28}$$

$$V_{\text{DS}}(t) = V_{\text{in}} - L_s\left(\frac{dI_{\text{DS}}}{dt} + \frac{dI_g}{dt}\right) - L_D\frac{dI_{\text{DS}}}{dt} \tag{29}$$

where L_D is the drain parasitic inductance of the power MOSFET. The switching loss during the turn-ON transition can be calculated as follows:

$$P_{\text{loss}-on} = f_{\text{sw}}\int_{t_1}^{t_2} V_{\text{DS}}(t)I_{\text{DS}}(t)dt. \tag{30}$$

Now, the total switching losses P_{sw} of power MOSFET S_M is attained as follows:

$$P_{\text{sw}} = P_{\text{loss-on}} + P_{\text{loss-off}}. \tag{31}$$

B. Gate Drive Losses

1) Conduction Loss of D: The diode is ON, in modes 1–7 in which P_D can be calculated as follows:

$$P_D = f_{\text{sw}}\left(\int_{t_0}^{t_2} nV_{fD}I_g(t)dt + \int_{t_2}^{t_7} V_{fD}I_g(t)dt\right). \tag{32}$$

2) Conduction Loss of S: The control switch S is ON, at modes 1–3; thus, P_S is calculated as follows:

$$P_S = f_{\text{sw}}\int_{t_0}^{t_3} R_{\text{DS}}(I_g(t) + nI_g(t))^2 dt. \tag{33}$$

3) Coupled Inductor Losses:

a) *Copper losses:* The total copper losses of coupled inductor P_{cop} is calculated as follows:

$$P_{\text{cop}} = f_{\text{sw}}\left(\int_{t_0}^{t_2} R_{\text{ac}}(I_g(t) + nI_g(t))^2 dt\right.$$

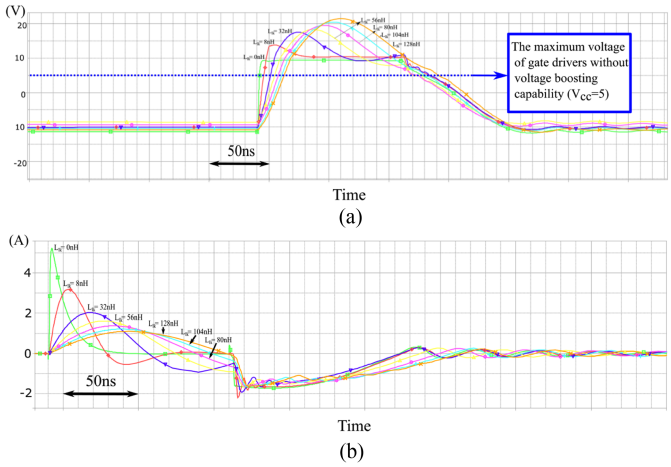

Fig. 8. Simulation waveforms of the proposed CSD with different leakage inductances and magnetizing inductance 160 nH. (a) V_{gs}. (b) I_g.

$$+ R_{ac} I_{L_m} + \int_{t_3}^{t_7} R_{ac}(I_g(t) + nI_g(t))^2 dt \Bigg) \quad (34)$$

where each pair of coupled inductor resistance is R_{ac}.

b) *Core loss:* The core loss is calculated in [17] as follows:

$$P_{core} = f_{sw}^x B^y k_1 v_e \quad (35)$$

where B is the peak flux density in the core, x is the frequency exponent, y is the flux density exponent, k_1 is the fixed coefficient, which depends on the core material, v_e is the effective volume of the core, and the total losses of the coupled inductor is derived as follows:

$$P_{ind} = P_{core} + P_{cop}. \quad (36)$$

4) Conduction Loss of r_g: The total losses of power MOSFET (S_M) gate resistance are given as follows:

$$P_{r_g} = f_{sw} \left(\int_{t_0}^{t_2} r_g I_g^2(t) dt + \int_{t_3}^{t_7} r_g I_g^2(t) dt \right). \quad (37)$$

IV. Design Considerations

The main component in the CSD design is the coupled inductors, which include the magnetizing and leakage inductances. The gate current is affected by the leakage and magnetizing inductances at turn-ON and turn-OFF transitions, respectively. As L_{lk} increases, the gate current is decreased and the time interval of the turn-ON transition is increased, and thus, to design the leakage inductance (L_{lk}), the maximum current rate of the control switch and the turn-ON time interval should be considered. To show the effect of L_{lk} on the gate current and gate-source voltage, these waveforms with different leakage inductances are shown in Fig. 8.

To obtain the minimum losses, the design of the CSD gate current is optimized by a tradeoff between the switching and gate drive losses. Considering that the optimal design for the inductor current of CSD depends on the application, the proposed CSD is designed to drive high-side (HS) switch (S_M) of a buck VRM, as shown in Fig. 9. The specifications for this design are given in Table II. In order to design the inductor current in the optimal point, P_{CSD}, P_{sw}, and P_{total} are illustrated in Fig. 10, where P_{total} is the sum of turn-OFF and turn-ON switching losses (P_{sw}), and gate drive losses (P_{CSD}). In order to reach the highest efficiency for VRM, I_{L_m} is selected as 1.85 A, which is at the minimum point of the P_{total} curve. However, I_{L_m} in this CSD depends on the duty cycle of the HS MOSFET, but P_{total}, as shown in Fig. 10, does not change much in a limited interval, such as $1\text{ A} < I_{L_m} < 3\text{ A}$. The value of L_m is calculated by considering an optimal design for I_{L_m} and V_N, where V_N must be smaller than the maximum negative gate voltage rate of the HS MOSFET. Thus, L_m can be derived from (7), where $(t_3 - t_2)$ is the HS MOSFET average pulsewidth, which is equal to 150 ns.

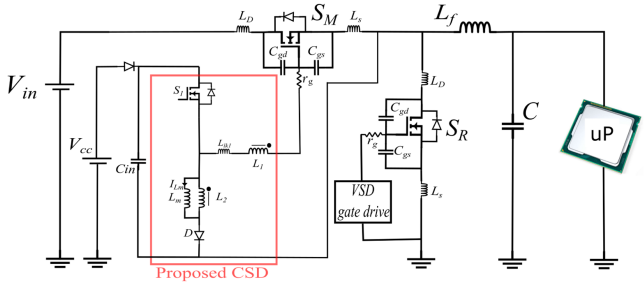

Fig. 9. Buck VRM with the proposed gate driver.

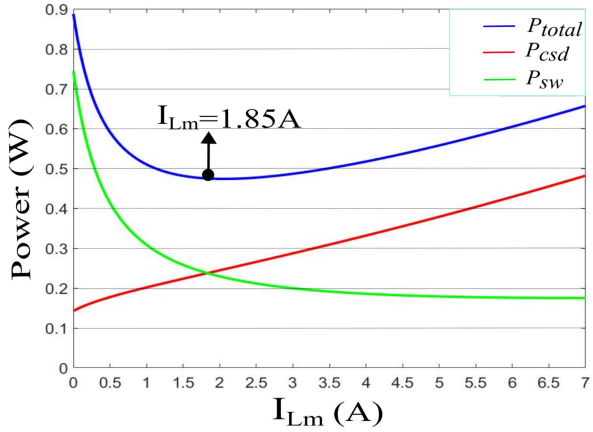

Fig. 10. Optimal design curves.

V. Results

In order to verify the circuit operation, the proposed CSD is used to drive the HS MOSFET in a buck VRM, while the low-side (LS) switch (S_R) is driven by a VSD (ISL6207) and the isolated voltage source V_{cc}, as illustrated in Fig. 9, and the experimental prototype is shown in Fig. 11. The design specifications of the implemented prototype are given in Table II. To drive the control switch S, an auxiliary pulse generator with MOSFET driver (ISL6207) is used. The gate signal is fed to the ISL6207 to deliver high-peak current pulses operating at 1 MHz into the gate of S.

TABLE I
COMPARISON BETWEEN THE PROPOSED GATE DRIVER AND OTHER COUNTERPARTS

Driver circuit	CSD type (DGC/CGC)	Number of switches	Total number of components	Voltage boosting capability	Mitigating current diversion turn-OFF	Mitigating current diversion turn-ON	Gate drive loss (W)	Gate current I_g (A)
Proposed	DGC	1	3	✓	Yes	Yes	0.24	1.85
[14]	DGC	2	3	x	Yes	No	0.25	2.12
[13]	DGC	4	7	x	Yes	Yes	0.38	0.8
[15]	DGC	4	11	x	partially	No	0.53	0.69
[19]	DGC	2	4	x	No	No	0.5	2.1
[17]	DGC	4	5	✓	No	Yes	0.32	1.8
[7]	CGC	2	4	✓	No	partially	1.2	1.85
[22]	CGC	4	5	x	No	No	1	1.7

TABLE II
DESIGN PARAMETERS

VRM	
Input voltage V_{in}	12 V
Output voltage V_{out}	1.3 V
Output current I_o	20 A
Switching frequency f_{sw}	1MHz
HS MOSFET (S_M)	IRF7811 AV
LS MOSFET (S_R)	SG40N01Q
LS MOSFET gate driver	ISL6207
L_f	2×650 nH
C	7.7 uF
CSD	
Gate drive voltage V_{cc}	5V
Control switch S	FDN335N
Diode D	MBR0520
L_m	400 nH
L_{lk}	60 nH

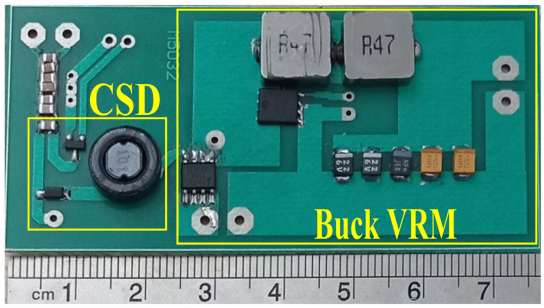

Fig. 11. Prototype of the proposed gate driver applied to a buck VRM.

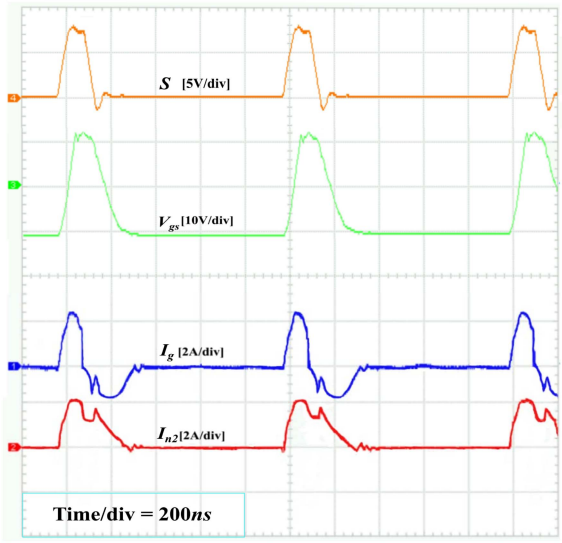

Fig. 12. Experimental waveforms: the gate signal of S, V_{gs}, I_g, and I_{n2}.

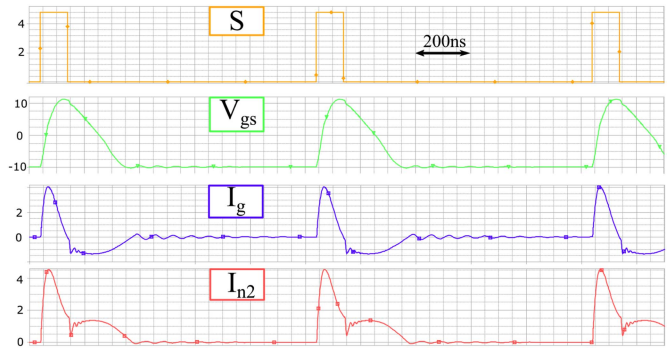

Fig. 13. Simulation waveforms of V_{gs}, I_g and I_{n2} with control signal of S.

The key experimental and simulation waveforms of the buck VRM are shown in Figs. 12 and 13, respectively, in which the first top waveform (S) is the gate signal of the control switch S, and the second and third waveforms (V_{gs} and I_g) are the gate-source voltage and the gate current of HS MOSFET, respectively, and the current I_{n2} is shown at the bottom of this figure. According to Fig. 12, even though the negative gate-source voltage value of the HS MOSFET in the proposed CSD is lower than that of the CSD in [14], the positive gate-source voltage of the proposed CSD is higher with the same gate drive source voltage. Thus, this CSD reduces the possibility of damage to the gate terminal at turn-OFF and decreases the conduction loss at turn-ON. Also, the voltage drop across the gate resistance and source inductance is compensated by changing the voltage across the magnetizing inductance, and thus, the CSD behaves like an ideal current source during the turn-OFF and turn-ON times. The experimental waveforms for the gate-source voltage and the drain-source voltage of the HS MOSFET are presented in Fig. 14.

It should be noted that the parasitic components of the printed circuit board (PCB), differential probe, and the current sensing resistors impact the gate-source voltage and gate current of the HS MOSFET. Thus, the experimental waveforms presented in Fig. 12 are a bit different from the actual and simulation waveforms. Also, the coupled inductors are hand wound with available materials for the laboratory prototype, resulting in higher leakage inductance and resistance.

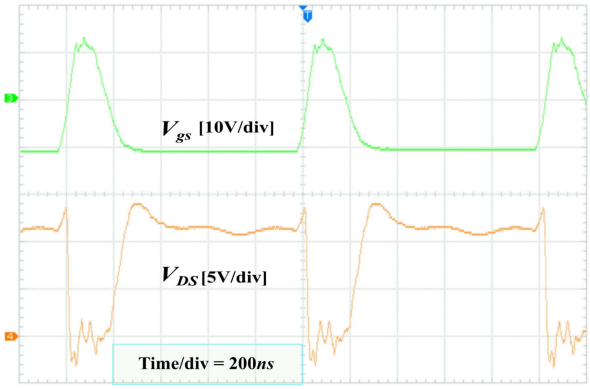

Fig. 14. Experimental $V_{\rm gs}$ and $V_{\rm DS}$ waveforms of the HS MOSFET (S_M).

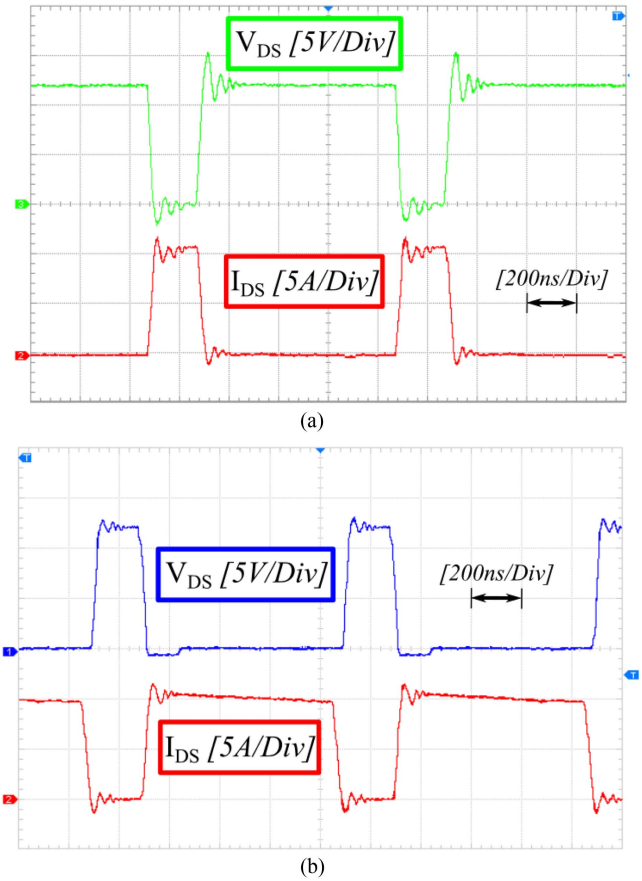

Fig. 15. Experimental voltage and current waveforms of (a) S_M and (b) S_R in a buck VRM.

The experimental waveforms of the voltage and currents of S_M and S_R are shown in Fig. 15. Also, to compare the proposed CSD with a conventional gate driver (VSD), the S_M switch is driven by a VSD, and the simulation waveforms are illustrated in Fig. 16. As shown in Fig. 16(a), the S_M switch driven by the proposed CSD is turned ON and OFF faster than the S_M switch driven by a VSD in Fig. 16(b). Whereas the proposed CSD recovers the gate energy during the turn-OFF transition and has a lower gate drive loss.

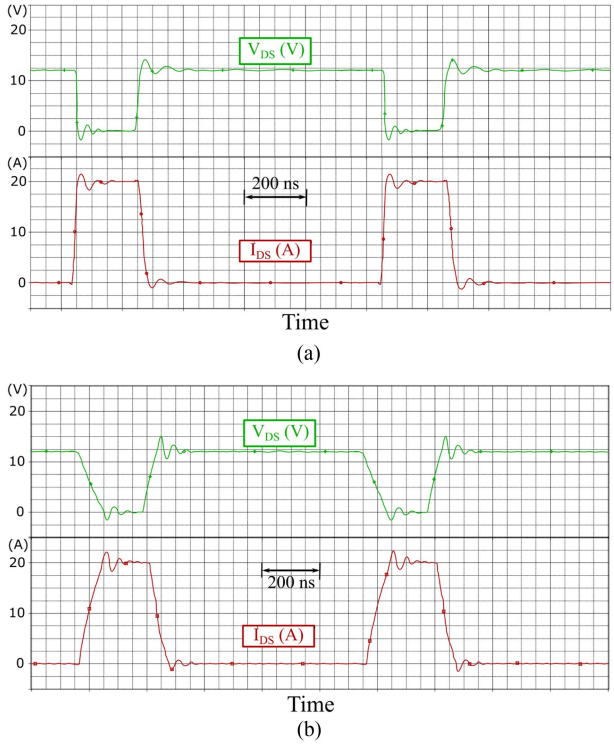

Fig. 16. Simulation voltage and current waveforms of S_M switch (L_s = 2 nH) driven by (a) proposed CSD and (b) VSD.

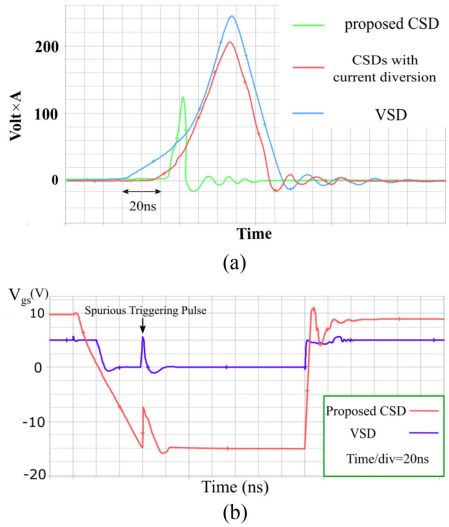

Fig. 17. Simulation results: (a) instantaneous turn-OFF switching losses, (b) LS switch gate-source voltage of the proposed CSD and a VSD in the presence of a spurious triggering pulse.

The instantaneous turn-OFF switching losses are shown in Fig. 17(a). As observed, due to solving the current diversion problem at the turn-OFF transition, the proposed CSD has lower turn-OFF switching losses compared with CSDs with current diversion and VSD.

As given in Table I, the gate drive losses of CSDs are calculated with the optimal gate current. The proposed CSD has

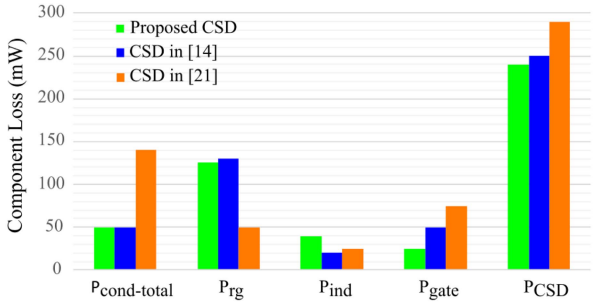

Fig. 18. Loss breakdown and the total loss of the proposed CSD in comparison with the CSDs presented in [14] and [21].

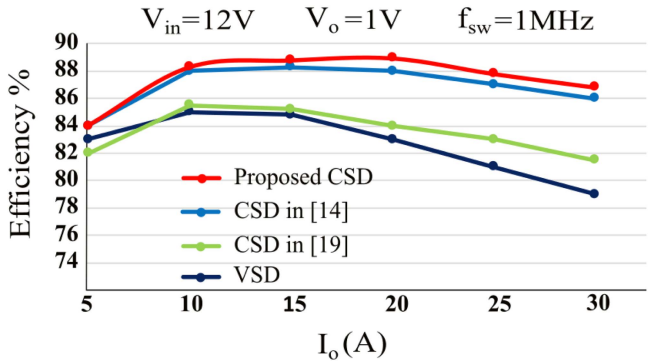

Fig. 19. Buck VRM efficiency comparison with the proposed CSD and other prominent counterparts.

a lower number of components and due to the discontinuous gate current (DGC), the energy circulating loss is decreased in comparison to continuous gate current (CGC) CSDs.

The proposed CSD is applied to the LS switch of a buck VRM to show the immunity against the spurious triggering pulse. As shown in Fig. 17(b), the gate-source voltage of the LS switch driven by the proposed CSD has a negative gate voltage when the power MOSFET is OFF. The spurious pulse created by the HS switch at turn-ON cannot raise the LS switch gate voltage beyond the threshold for turn-ON. Thus, the proposed CSD has higher $C\frac{dv}{dt}$ immunity compared with VSDs.

The loss breakdown and the total losses of the proposed CSD, and those of CSDs in [14] and [21] are calculated with the optimal gate current, as depicted in Fig. 18. As observed, the proposed CSD has a lower gate drive loss compared with that of other CSDs because of DGC and a lower number of components.

In order to compare the buck converter efficiency with the proposed CSD and other gate drivers, PSpice software is used to simulate the buck converter shown in Fig. 19. Unlike the CSD in [14], the proposed CSD has the gate voltage boosting capability, which decreases $R_{\mathrm{DS(on)}}$ and consequently the HS MOSFET conduction loss. Therefore, at $I_o = 30$ A, the proposed CSD improves the buck converter efficiency by 1% in comparison to [14], and by 5.4% in comparison to [19] due to having lower HS MOSFET switching losses at both turn-ON and turn-OFF transitions.

VI. Conclusion

A new single switch discontinuous CSD with voltage boosting capability, which eliminates the current diversion problem during the switch turn-ON and turn-OFF transitions, due to its performance as an ideal current source is introduced in this article. The presented gate driver has only one switch and other attractive features, such as low-energy circulating loss, gate energy recovery, and high $C\frac{dv}{dt}$ immunity. The simulation results indicate that the turn-OFF and turn-ON losses of the HS MOSFET driven by the proposed CSD are lower than those of the most CSDs with the current diversion problem. This CSD with voltage boosting capability reduces $R_{\mathrm{DS(on)}}$ and consequently the conduction loss in comparison to most counterparts CSDs. As shown in the experimental results, at the switch turn-OFF time, the negative gate-source voltage of the HS MOSFET driven by the proposed CSD is equal to the positive voltage at turn-ON time, which reduces the possibility of damage to the HS MOSFET. The proposed CSD is applied to a buck VRM, which demonstrates improved efficiency in comparison to other gate drivers. A prototype of the CSD at 1 MHz is implemented, and the experimental results verify the simulation and the theoretical analysis.

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