Self-Powered Synchronous Electric Charge Extraction Rectifier for Rotational Electret Energy Harvester With Dual-Stage Electrodes

Yiran Liu, Zehan Shi, Adrien Badel, Tomoya Miyoshi, *Member, IEEE*, and Yuji Suzuki, *Fellow, IEEE*

***Abstract*—This article presents for the first time the development of a self-powered synchronous electric charge extraction (SECE) circuit for an in-plane rotational electret kinetic energy harvester (EH) with a cold start function. As an electret EH features low source current and high output impedance, its output power is sensitive to the leakage current and the parasitic capacitance. A novel dual-stage electrode design is proposed, with the control stage providing a sub-5V supply to the control circuit and triggering a synchronous switch in the high-voltage main circuit. Compared to a conventional buck converter, the power harvested on a 5-V load was doubled with the present synchronous electric charge extraction (SECE) prototype. Based on the circuit simulations, the achievable power increase at the generator output with the proposed circuit is mainly constrained by the impedance introduced by itself. The experimental results show that the circuit can be cold-started and directly powered by electret EHs.**

***Index Terms*—Dual-stage electrode, electret, energy harvesting, power management circuit, synchronous electric charge extraction (SECE).**

I. Introduction

ENERGY harvesting, which generates electricity from ambient energy sources, offers an opportunity to free wireless sensor nodes from batteries, which limit the operating time under small volume requirements [1], [2], [3]. In wearable applications [4], [5], body heat and human motion [6], [7] are two major energy sources. Motion-driven kinetic energy harvesters (EHs), such as arm-equipped or shoes-embedded ones, are more powerful than a bandage-type EH pasted on the skin, thereby attracting much attention. As human motion is characterized by multiaxis, low frequency ($\sim$1 Hz) and large amplitude, rotational EHs [8], [9] are more appropriate, when compared with its linear-vibrational counterparts, where the travel range of the proof mass is limited [10].

To date, various miniatured rotational EHs with different transduction mechanisms have been proposed based on piezoelectric [11], electromagnetic [12], [13], [14], and electrostatic [15], [16]. In the present study, we focus on the in-plane rotational electret EH, in which a precharged electret layer is used as a quasi-permanent charge source [17]. Miyoshi et al. [16] have demonstrated that a wrist-worn rotational electret EH has the potential to harvest much more energy at low frequencies in a low-profile configuration than the electromagnetic counterparts.

Unlike electromagnetic EHs, the output impedance of electret EHs is as high as tens of MΩ, so that the output current is limited to 1$\sim$10 μA [18], [19]. Therefore, high output voltage is necessary for high output power.

On the other hand, since dc sub-5 V is usually required for driving circuits, stepping-down the output voltage of electret EH and regulating the output voltage is not a straightforward process considering a total power budget at the μW level. In this regard, previous studies have mainly focused on the design of an efficient buck converter, but with a limited voltage range [20], [21], [22], [23]. Maeng et al. [23] reported an IC-based buck converter for the input voltage up to 70 V with a power conversion efficiency of 84.7%.

Recently, Zhang et al. [24] proposed a discharge-based hysteresis switch for their high-voltage two-stage conditioning circuit, but the efficiency of the buck converter with this switch is merely 35%. Transformer is another option to step down the voltage [25], but it is usually unacceptably bulky and inefficient, which makes it unattractive in wearable applications. Therefore, development of small volume and efficient power management circuits is challenging especially for electret EHs.

Another major concern with electret EH is that the extractable power of electret EHs is severely limited by parasitic capacitance, by which the source current can be easily bypassed

Manuscript received 6 March 2023; revised 15 May 2023; accepted 10 July 2023. Date of publication 18 July 2023; date of current version 1 September 2023. This work was supported in part by JST CREST under Grant JPMJCR15Q3 and Grant JPMJCR19Q1, and in part by JSPS KAKENHI under Grant 22KK0054. Recommended for publication by Associate Editor K. Kim. *(Yiran Liu and Zehan Shi contributed equally to this work.) (Corresponding author: Yuji Suzuki.)*

Yiran Liu was with the Department of Mechanical Engineering, Graduate School of Engineering, The University of Tokyo, Tokyo 113-8656, Japan. He is now with the Mercedes-Benz R&D Japan, Kanagawa 212-0057, Japan (e-mail: yliu@mesl.t.u-tokyo.ac.jp).

Zehan Shi, Tomoya Miyoshi, and Yuji Suzuki are with the Department of Mechanical Engineering, Graduate School of Engineering, The University of Tokyo, Tokyo 113-8656, Japan (e-mail: zshi@mesl.t.u-tokyo.ac.jp; miyoshi@mesl.t.u-tokyo.ac.jp; ysuzuki@mesl.t.u-tokyo.ac.jp).

Adrien Badel is with the Laboratory SYMME, Université Savoie Mont Blanc, 74944 Annecy le Vieux, France (e-mail: adrien.badel@univ-smb.fr).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3296709.

Digital Object Identifier 10.1109/TPEL.2023.3296709

[17], [26]. The parasitic capacitance in electret EHs is mainly originated from the interdigitated electrodes and can also be introduced by the power management circuit and measurement setup. To tackle this issue, modified electrode designs, such as concave electrodes [27] and suspended electrodes [28], have been proposed to reduce the parasitic capacitance.

Synchronized switch harvesting on inductor (SSHI) [29], [30], [31] are widely studied for piezoelectric vibration EHs. In SSHI, the shunt effect caused by the parasitic capacitance can be removed by switching, so that SSHI should also be beneficial for electret EHs. We previously proposed an SSHI circuit tuned for electret EHs and obtained much higher output power for rotational electret EH [32]. However, SSHI also magnifies the output voltage by several times, which poses a significant challenge to the design of the dc/dc converter.

After these considerations, we focus on synchronized electric charge extraction (SECE) [33], [34], [35], [36], [37] for enhancing the output power of electret EHs. Compared with SSHI, SECE exhibits three advantages as follows.

1) Load independence: Using an inductor as the energy mediator, the generator and load are decoupled.
2) Free from bipolar power supply: The switch in SSHI is located on the ac side, where the voltage varies between the negative and positive rail voltages to deal with bidirectional currents. On the other hand, the synchronized switch in SECE is located on the dc side, so that its gate voltage varies between 0 V and the rail voltage.
3) Low rectified voltage: In SSHI, the maximum voltage is a function of the voltage-inversion ratio and is usually several times of the open-circuit voltage. On the other hand, the highest voltage present in the SECE circuit is twice the open-circuit voltage, and the load voltage at the SECE rectifier could be 5 V or below.

Most previous SECE designs are intended for low-voltage EHs and hence, cannot be directly adapted to electret EHs. A multishot SECE (MS-SECE) compatible with high voltage (>100 V) was reported in [25], using a transformer to step down the high voltage and an application-specific integrated circuit for switch control. Its application on electret EH shows a conversion efficiency of 60% [38]. However, such a transformer is too large for small-scale EH systems.

The following challenges exist for application of SECE to electret EHs: 1) control circuitry of SECE for high voltage; and 2) an efficient stepping-down method over 100 V to sub-5 V in a small scale. These issues will be addressed in this article.

II. Rotational Electret EH

Fig. 1 shows a schematic diagram of a rotational electret EH [16]. On the rotor substrate, fan-shaped interdigitated electrodes are formed as the base and guard electrodes, on which the polymer electret material such as CYTOP [39] is uniformly formed with a thickness of d. On the stator substrate, the same poles of interdigital electrodes are formed as the collector and ground electrodes. Bipolar charging [40] is utilized to enhance the output power of electret EH. The electret on the base and guard electrodes is charged with soft X-ray [41] to the surface

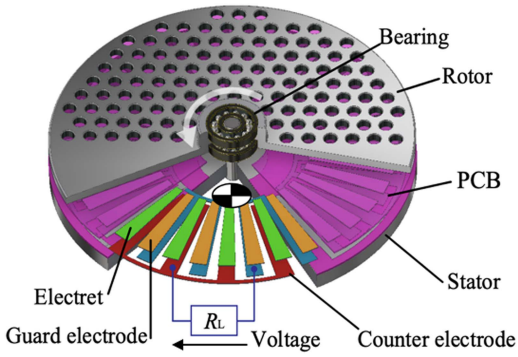

Fig. 1. In-plane rotational electret energy harvester [16].

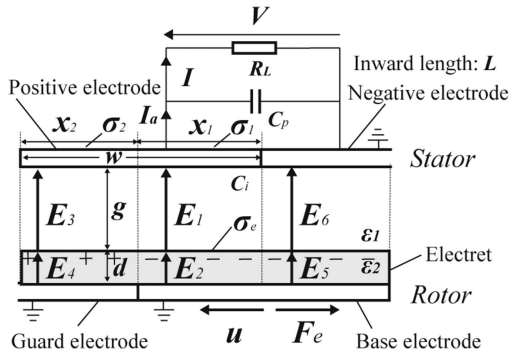

Fig. 2. 1-D model of in-plane electret energy harvester.

potential of $\pm V_{sb}$ corresponding to the equivalent surface potential $V_s = 2V_{sb}$. Note that a parasitic capacitance C_p exists between the collector and ground electrodes.

The air gap distance of g between the electret surface and the counter electrode is kept constant using a ball bearing unit integrated with the rotor and the stator. The charged electret induces charges on the charge-collecting electrode. When the rotor with eccentric mass is driven by external motion, the amount of induced charges on the collector electrode changes due to the overlapping area change by relative displacement u between the rotor and stator, resulting in an output current I in the external circuit as shown in Fig. 2. The electrical damping force F_e works against the rotor motion, thereby achieving mechanical-to-electrical energy conversion.

A generator model of the electret EH [32] is expressed as

$$\begin{cases} F_e = \alpha_e V, \\ I = \alpha_e \dot{u} - C_e \dot{V} \end{cases} \tag{1}$$

where $\alpha_e = \frac{n\varepsilon_2 L V_s}{d+\frac{\varepsilon_2}{\varepsilon_1}g}$ is the force factor; L is the radial length of electrode and $C_e = C_i + C_p$ is the shunt capacitance. C_e is the sum of internal capacitance $C_i = \frac{\varepsilon_2 A}{(d+\frac{\varepsilon_2}{\varepsilon_1}g)}$ and C_p, where $A = \frac{\pi}{2}(r_o^2 - r_i^2)$ is the total area of collector electrode, with r_o and r_i denoting the outer and inner radius of the fan-shaped electrodes. V is the output voltage. ε_2 and ε_1 are the permittivity of electret and air respectively. The electrical restoring force F_e is proportional to the output voltage V, and the output current

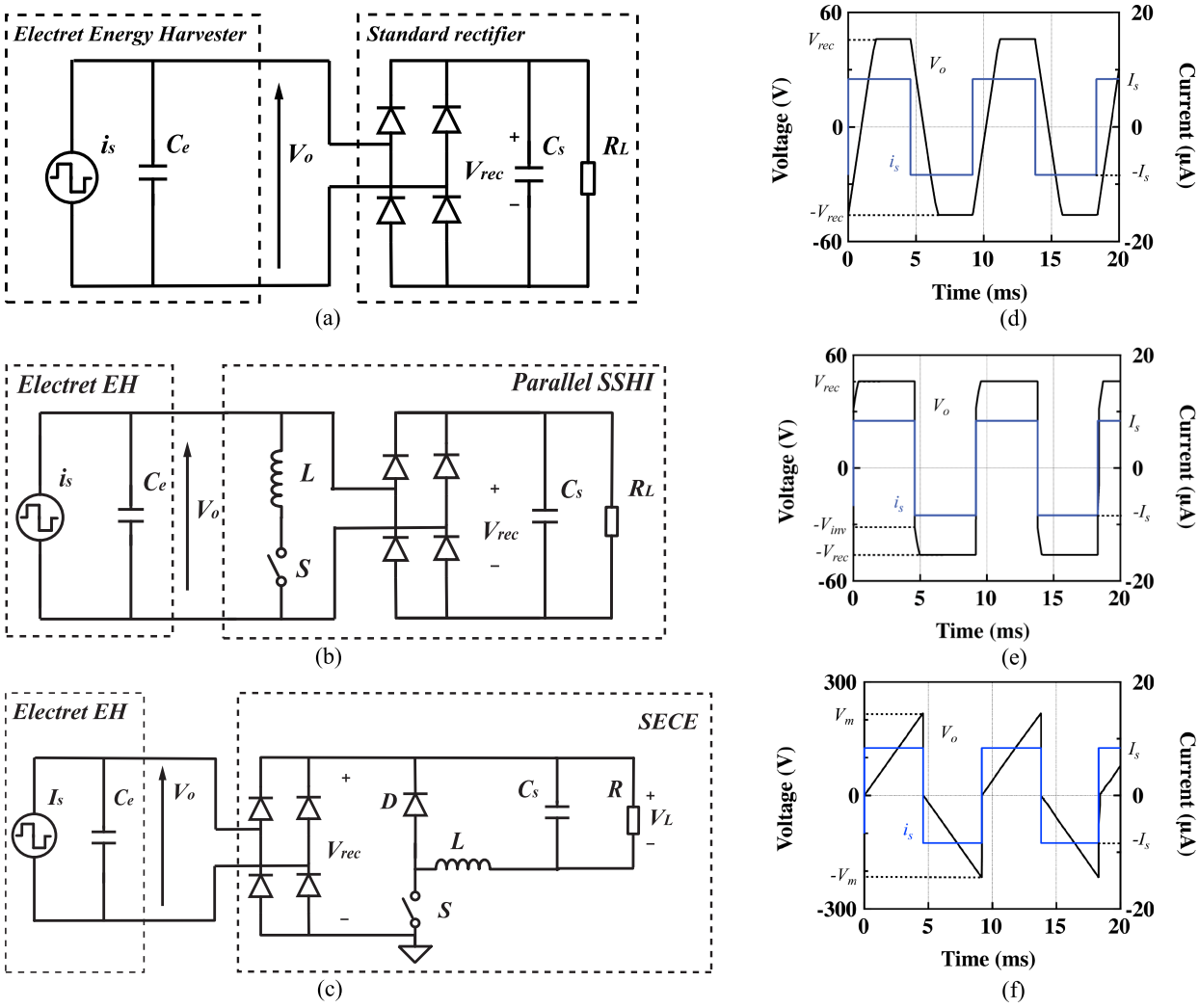

Fig. 3. Interface circuits for electret EH. Circuit diagrams for (a) Standard circuit, (b) Parallel SSHI circuit, (c) SECE circuit. (d), (e), and (f) Associated voltage and current waveforms.

I equals the induced current generated by $I_s = \alpha_e \dot{u}$ subtracted by the amount shunted by C_e.

A circuit model is derived as the generator part of Fig. 3. At a rotational frequency of f_r, the source current I_s is a squared wave with a period $T = \frac{1}{nf_r}$ (assuming $x_1 = 0$ at $t = 0$)

$$I_s = \begin{cases} 2C_i V_s n f_r, \ t \in \left[kT, \left(k+\frac{1}{2}\right)T\right) \\ -2C_i V_s n f_r, \ t \in \left[\left(k+\frac{1}{2}\right)T, (k+1)T\right) \end{cases} \quad k = 0, 1, 2 \ldots \tag{2}$$

III. Interface Circuits

A. Standard Rectifying Circuit

In the following sections, belief descriptions for standard rectifying and SSHI circuits are given for the continuity of our discussion. In the standard rectifying circuit shown in Fig. 3(a), the generator is connected to a storage capacitor C_s through a full-bridge rectifier. The extractable output power P_o is limited by the shunt capacitance C_e. Assuming the voltage across load resistor R_L is a dc constant voltage V_{rec} at the steady state, the charge conservation law in half a period gives

$$\frac{I_s T}{2} = 2C_e V_{rec} + \frac{V_{rec} T}{2R}. \tag{3}$$

The output power is then expressed as

$$P_o = \frac{V_{rec}^2}{R} = I_s V_{rec} - 4C_e f_s V_{rec}^2 \tag{4}$$

where the source current $I_s = 2C_i V_s n f_r$ and the source frequency $f_s = nf_r$. The output power is proportional to the number of poles n. Maximal power $P_{max} = \frac{C_i^2 V_s^2 f_s}{4C_e}$ is obtained at $V_{opt} = \frac{C_i V_s}{4C_e}$.

V_{opt} is typically several tens of volts for rotational electret EH [42], [43] due to high V_s, hence an additional buck converter is required to step-down the output voltage to sub-5 V. As aforementioned, the conversion efficiency of these converters for electret/electrostatic EH is much lower than those for piezoelectric EHs [44], [45] due to its high voltage. Therefore, the load

power P_L of electret EHs is also constrained by the efficiency of the buck converter η_{con}, i.e., $P_L = \eta_{con} P_o$.

B. SSHI Circuit

Parallel SSHI [Fig. 3(c)] is also shown here for comparison, where a switch is inserted in series with an inductor in parallel with the generator and a full-bridge rectifier. The switch action is synchronized with the polarity change of the current source to ensure that the output voltage and the source current always have the same sign, thereby achieving substantial power recuperation as shown in Fig. 3(d). Due to the loss in the *LC* resonant circuit, the voltage inversion is not perfect. The charge conservation law during half a period gives

$$\frac{I_s T}{2} = C_e \left(1-\gamma\right) V_{rec} + \frac{V_{rec} T}{2R} \tag{5}$$

where γ is the inversion ratio defined by $\gamma = \frac{V_{inv}}{V_{rec}}$. The output power in parallel SSHI is given by

$$P_o = \frac{V_{rec}^2}{R} = I_s \, V_{rec} - 2\left(1-\gamma\right) C_0 f_s V_{rec}^2. \tag{6}$$

The optimal voltage and maximal power are given as

$$V_{opt} = \frac{C_i V_s}{2\left(1-\gamma\right) C_e} , \tag{7}$$

$$P_{\max} = \frac{C_i^2 V_s^2 n f_r}{2\left(1-\gamma\right) C_e} . \tag{8}$$

By comparing the maximal power in the standard and SSHI circuits, it is found that the shunt capacitance C_e in parallel SSHI equivalently reduces by $\frac{(1-\gamma)}{2}$, corresponding to the power-enhancing ratio of $\frac{2}{1-\gamma}$.

The disadvantage of parallel SSHI is that the optimal voltage is also $\frac{2}{1-\gamma}$ times that of the standard circuit. Assuming an inversion ratio of $\gamma = 0.7$, the optimal voltage in SSHI is three times the open circuit voltage in the standard circuit. Typically, a converter with a maximal input voltage over 300 V is required, which is beyond the highest rating of available low-power buck converters. Instead, a fly-back transformer is often used in high-voltage applications, reporting 40%∼60% conversion efficiency [38]. However, the coupling coil can be bulky and suffers from low efficiency in the low-frequency range. Therefore, the load power in SSHI is constrained not only by the efficiency, but also by the input voltage rating of the converter.

C. SECE Circuit

In the SECE circuit shown in Fig. 3(c), a switch *S*, an inductor *L*, a diode *D*, and a full-bridge rectifier are inserted between the generator and the storage capacitor C_s. In each cycle, *S* is open for most of the time. Therefore, charges generated by I_s are accumulated across C_e from null. At the zero-crossing point of I_s, V_o reaches its maximum V_m. At this instant, *S* is closed for a very short period, discharging C_e to *L*. When V_{rec} decreases to 0, *S* is open again to disconnect the generator, initiating charge accumulation across C_e in the other direction. Meanwhile, energy stored in *L* is freewheeled to C_s through *D*. Note that the switch in Fig. 3 is implemented at the low side to reduce the control circuitry loss of the buck converter.

If the on-duration t_{on} of *S* is fixed as 1/4 of the *LC* resonance period, i.e., $t_{on} = 0.5\pi\sqrt{LC_e}$, V_o will ramp to V_L instead of zero. In other words, there will be a residual voltage V_L across C_e. This voltage is to be discharged in the next cycle by the source current. Unless V_o ramps to 0, the charge extraction from C_e is not complete, the source needs to discharge the residual voltage across C_e, thereby reducing the output power of generator in the next cycle. Therefore, it is favorable to discharge V_o to 0 with longer $t_{\rm on}$. In fact, to make sure V_o ramps to 0, the ON-duration of the switch should be [34]

$$t_{on} = \sqrt{LC_e} \cdot \cos^{-1} \frac{-1}{\frac{V_{SECE}}{V_L} - 1} \tag{9}$$

where $V_{SECE} = \frac{C_i V_s}{C_e}$ is the amplitude of the generator output voltage in the SECE circuit. In this case, the electrostatic energy stored in C_e before the turn-ON instant of *S* is expressed as

$$E_c = \frac{1}{2} C_e \, V_{SECE}^2 = \frac{1}{2} C_e \left(\frac{I_s T}{2C_e}\right)^2 = \frac{C_i^2 V_s^2}{2C_e} . \tag{10}$$

Since E_c is extracted every half period, the output power of generator is expressed as

$$P_o = \frac{E_c}{0.5T} = \frac{I_s^2 T}{4C_e} = \frac{C_i^2 V_s^2 f_s}{C_e} . \tag{11}$$

Comparing with the maximal power in the standard case, it is found that a power enhancing ratio of 4 is achieved with the proposed circuit, regardless of the load impedance. In other words, a higher power enhancing performance at low load voltage can be expected in the SECE circuit, which is especially favorable for electret EHs.

In practice, power loss occurs in transferring the generator output power to the load. Therefore, load power is expressed as

$$P_L = \eta_{SECE} P_o \tag{12}$$

where η_{SECE} denotes the conversion efficiency. Note that the difference between V_{SECE} and V_L can be hundreds of volts for electret EHs; hence, a large inductance is needed to reduce the current amplitude. As η_{SECE} is critical to achieve a superior overall performance, it will be analyzed in detail in the later section.

D. Generator Output Power

Fig. 4 depicts the dc output power of a rotational electret EH with the standard, SSHI, and SECE circuits. The parameters of the rotational electret EH are listed in Table I. Their theoretical values are based on (4), (6), and (11), respectively. The simulations are carried out using LTspice, where the synchronized switches in SSHI and SECE are based on a voltage-controlled switch model. In SSHI, the inversion ratio γ was tuned to 0.7 by setting the series resistance of the inductor to be 1.37 kΩ. In the simulation of SECE, the ON-state duration given by (9) cannot make V_o ramp to 0, which is probably influenced by the resistance in the circuit. Therefore, a longer ON-state duration $t_{on} = 2\pi\sqrt{LC_e}$ was set to ensure V_o ramp to 0. The simulated

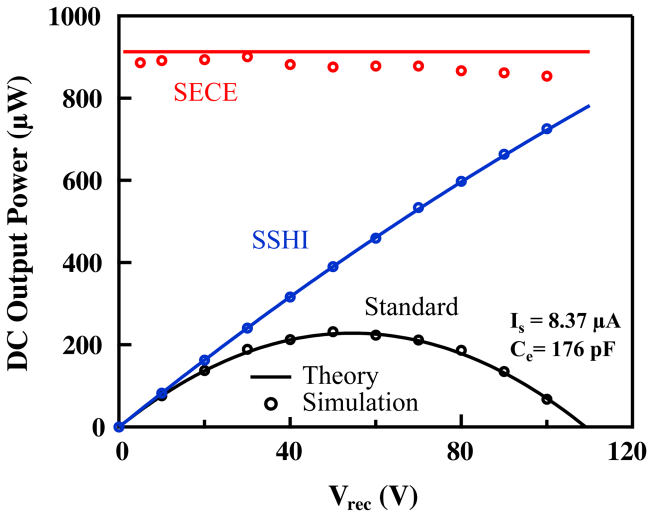

Fig. 4. Theoretical and simulated dc output power of a rotational electret EH with the Standard, SSHI, and SECE interface circuits.

TABLE I
PARAMETERS OF ROTATIONAL ELECTRET EH

f_r	Rotational frequency	1 Hz
n	Number of electrode pairs	109
A	Maximum overlapping area	5 cm^2
V_s	Surface potential of electret	800 V
ε_2	Permittivity of electret	1.86×10^{-11} F/m
ε_1	Permittivity of air	8.85×10^{-12} F/m
d	Thickness of electret	17 μm
C_p	Parasitic capacitance	128 pF

TABLE II
COMPARISON OF SSHI AND SECE

	Parallel SSHI	SECE
Generator output power[a]	4~10× ($\frac{2}{1-\gamma}$, γ=0.5~0.8)	4×
Generator output voltage	$\frac{2}{1-\gamma}V_{oc}$ [b]	$2V_{oc}$
Additional converter?	Yes	No
Requirements for converter	Dual-polarity, High input-voltage	/
Conversion efficiency	Low	Relatively High
Load power	Low	High

[a] Compared with maximal power in the standard circuit.
[b] V_{oc} is the open-circuit voltage in the standard circuit.

results agreed well with the theoretical results in the SSHI and standard cases. For SECE, the penalty here is the loss of some source charges, that are not accumulated in C_e due to the overlong ON-duration, resulting in a lower output power in the simulation than the theoretical results.

In the present study, SECE has been chosen based on the general comparison given in Table II. At low load voltage range, SECE exhibits superior power enhancing performance than SSHI. In other words, additional voltage conversion is not required in SECE, while an efficient dc/dc conversion for the ultrahigh voltage conversion ratio is required for SSHI.

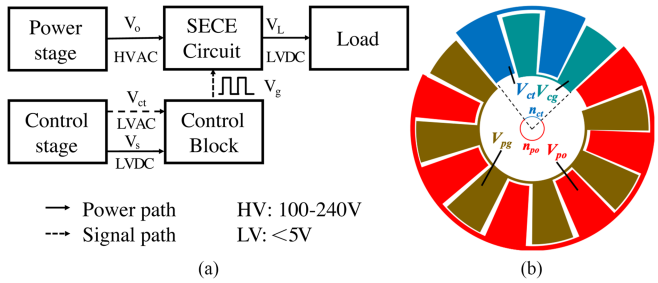

Fig. 5. (a) System design of dual-stage SECE. (b) Dual-stage electrode design with the power and control stages.

IV. SYSTEM IMPLEMENTATION

The challenges of implementing self-powered SECE on electret EHs include: 1) self-powering the control circuit with low consumed power; 2) switching the high output voltage with a low-voltage synchronous signal; and 3) an efficient switch control.

A. Dual-stage Electrode Design

Fig. 5(a) shows a block diagram of the present dual-stage SECE system design for rotational electret EHs. The charge-collecting electrodes of electret EH (see Fig. 2) are divided into two groups; a major area of electrodes is used for the power stage, while a minor area of electrodes is used for the control stage. The power stage is responsible for power generation with a high output voltage V_{po} to the SECE main circuit. The SECE main circuit is similar to a buck converter, but features a synchronized switch. The main circuit outputs sub-5 V dc voltage V_L for subsequent electronic loads. On the other hand, the control stage outputs low voltage V_{ct} to the control block, generating a trigger signal V_g to the synchronized switch in the SECE main circuit.

Fig. 5(b) shows a pole number-based dual-stage electrode design for SECE. In the following simulations, the numbers of poles for the control and power stages are 9 and 100, respectively.

B. SECE Main Circuit With a Low-Side Switch

In previous SECE circuits, a high-side switch [34] or a photo coupler-based switch [35] is employed for synchronous switching. In the high-side switch solution, a low-side NMOS is often necessary to indirectly trigger a high-side PMOS. When the NMOS is on, a conduction path is created from the generator output to the ground, which leads to substantial power loss when the generator output voltage is high. In addition, the highest voltage rating of commercialized small-signal PMOS is 250 V [45], constraining the application of this solution. In [35], a photocoupler was employed to drive the high-side switch, but it consumes mW-level power, which is unfavorable considering the μW-level power budget of our system.

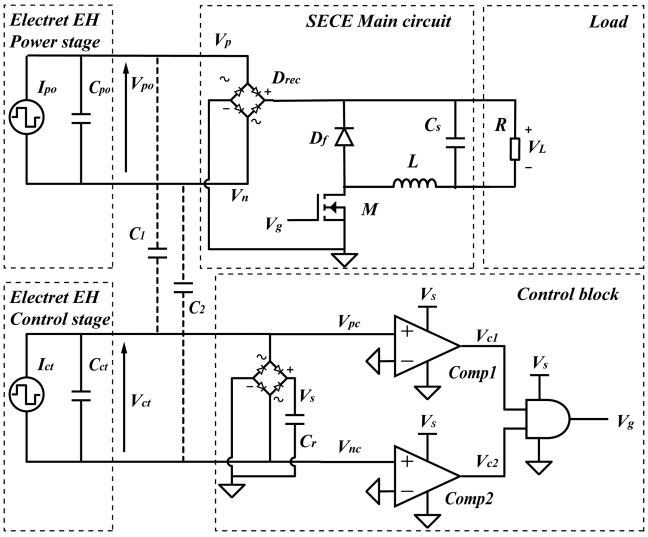

Fig. 6. Circuit design of dual-stage SECE.

Fig. 6 shows a detailed circuit design of the proposed circuit. In the present study, the main circuit features a low-side switch to enhance the circuit efficiency and the voltage rating. The power stage outputs high voltages V_p and V_n, while the control stage outputs low voltages V_{pc} and V_{nc}. Note that the ground in SECE is on the dc side, hence V_{pc} and V_{nc} could be negative values, which is necessary because the control block triggers switch actions by detecting the polarities of V_{pc} and V_{nc}. The currents generated by the power and control stages are defined as I_{po} and I_{ct}, respectively. Note that I_{po} and I_{ct} are inherently in phase, which makes it possible to employ V_{ct} to trigger the switch in the main circuit. The shunt capacitances of the power and control stages are C_{po} and C_{ct}, respectively. The source current and the shunt capacitance of each stage is proportional to its number of poles. The interterminal parasitic capacitances C_1 and C_2 (see Fig. 6) are useful for correctly determining the turn-OFF instant when discharging C_{po}, as will be explained in the switch control section.

The proposed low-side switch scheme eliminates high-side PMOS, thereby simplifying the switch drive and reducing the associated power loss. In the present study, considering that the measured open-circuit voltage of the electret EH is around 100 V [43], a high-voltage (rated at 240 V) small-signal N-type MOSFET BSP89 [46] is selected.

One issue is that since the load is floating, it is impossible to power the control circuit by V_L. Here, we propose to power the control circuit solely from the output power of the control stage, thereby achieving self-powering.

C. Switch Control

Table III shows a comparison of several control schemes in the implementation of SECE. A straightforward method is to use an external sensor, which tracks the motion of the EH, to trigger switch actions [34], [35]. It is easy to realize and adaptive to arbitrary internal shunt capacitance and external inductance. But it is not self-contained and sometimes bulky.

TABLE III
COMPARISON OF SWITCH CONTROL SCHEMES IN SECE

	Sensor [33], [35]	*RC* delay [47]	Dual-mode Comparator [44]	Polarity-based [This work]
Merits	-Adaptive -Easy to realize	-Reliable -Easy to realize	-Adaptive -Self-contained	-Adaptive -Easy to realize
Drawbacks	Bulky	Not adaptive	Hard to realize	--

Later, a self-contained method was proposed in [46]. It initiates the turn-ON of the switch by detecting the voltage extremums and turns OFF the switch after a fixed time duration realized by an *RC* delay unit. Therefore, it needs precise information on the internal shunt capacitance and external inductor in advance to tune the fixed duration. As a result, it does not adapt to the aging of the inductor or the generator. In addition, electret EHs have an internal shunt capacitance in the pF range, so that the total shunt capacitance is influenced by the external wiring, power management circuitry, and measurement setup. It is therefore hard to accurately estimate the total shunt capacitance. Recently, a self-contained adaptive method based on IC technology has been proposed [38]. A dual-mode comparator, which dynamically adjusts its threshold, is employed to trigger the turn-ON and turn-OFF timing of the switch. However, it is difficult to implement such a function using off-the-shelf discrete components. In this work, we propose a polarity-based method, that is self-contained, adaptive, and can be easily implemented using discrete components.

The proposed control block consists of a full-bridge rectifier, a storage capacitor C_r, two comparators *Comp1* and *Comp2*, and an AND gate (see Fig. 6). The input signals to the control block are the output voltages of the control stage (V_{pc} and V_{nc}).

The output of the control block is V_g to drive the NMOS switch. The control block turns on the switch by detecting the peaks of V_{po}, and turns OFF the switch when it detects the zero-crossings of V_{po}. The components of the control block are powered by the voltage V_s across the storage capacitor C_r.

Fig. 7 illustrates the associated waveforms in the control block. Assuming $I_s > 0$ and $V_{po} > 0$ since $t = 0^+$, we have $V_{pc} = V_s + V_D$ and $V_{nc} = -V_D$, where V_D is the forward voltage drop of the diodes in the rectifier. The condition for V_g = HIGH is $V_{pc} > 0$ and $V_{nc} > 0$ (thresholds of comparators neglected). Therefore, $V_g = 0$ since $t = 0^+$.

At $t = t_1$, I_{po} alters its direction to $-I_s$ and so does I_{ct}. Accordingly, V_{nc} starts to increase from $-V_D$ to 0; whilst V_{pc} stays positive but starts decreasing from $V_s + V_D$. At $t = t_2$, V_{nc} exceeds zero, satisfying the condition for V_g to output high, thereby the discharging of C_{po} is initialized. Here $\Delta t = t_2$-t_1 is the switch delay in this circuit. From $t = t_2$ to $t = t_3$, V_{po} quickly ramps to 0. Thanks to the inter-terminal capacitance C_1 between V_{po} and V_{pc}, V_{pc} also ramps to 0 accordingly. At $t = t_3$, V_{pc} drops below 0 while $V_{nc} > 0$, turning V_g from high to low, thus terminating the discharging phase. After $t = t_3$, another charging cycle is starting on the generator side. The stored energy in the inductor, on the other hand, freewheels

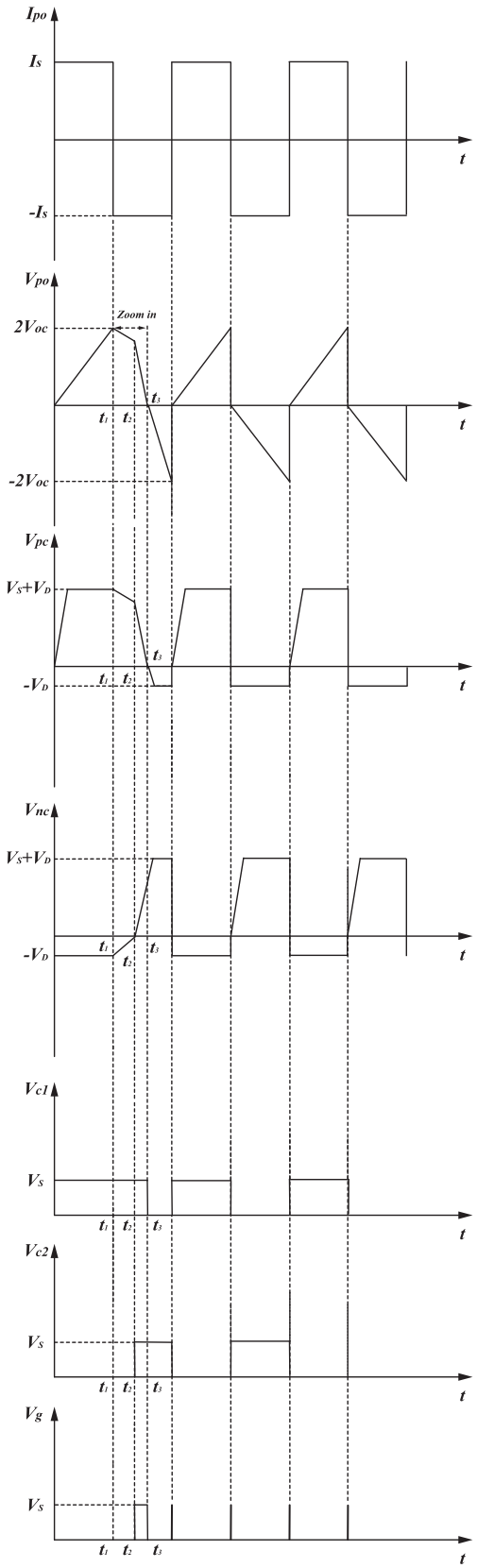

Fig. 7. Waveforms in the control block of SECE.

TABLE IV
PARAMETERS IN CIRCUIT SIMULATION

Definition	Value	Definition	Value
I_{po}	8.69 μA@109 Hz	M	BSP89 [46]
C_{po}	132 pF	C_s	0.1 μF
I_{ct}	0.78 μA@109 Hz	*Comp1*, *Comp2*	LTC1540
C_{ct}	12 pF	D_f	BAV21
L	1 mH	C_1	10 pF
R_{ser}	15.5 Ω	C_2	10 pF
R_{par}	130 kΩ	AND gate	SN74AHC1G08
C_{par}	6.33 pF	DC supply	3 V

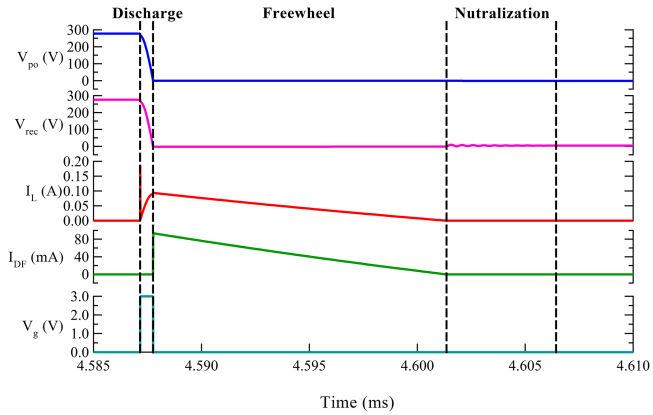

Fig. 8. Power transfer process in the SECE operation.

to the load. In this way, the control block governs the switch action, adapting to arbitrary internal capacitance and external inductor. Actually, the ON-duration of the switch is short ($<$10 μs) compared with the semi period ($\sim$5 ms) of the current source, hence the discharge phase appears instantaneous.

V. Circuit Simulation

To verify the effectiveness of the proposed design, the circuit illustrated in Fig. 6 is simulated using LTspice. The generator parameters and components are listed in Table IV, and were experimentally characterized as described in [42] and [43].

A. Power Transfer Process

Fig. 8 shows the simulated voltage and current to show the power transfer process. I_{DF} and I_L are the currents flowing through the freewheel diode and the inductor. There are four phases in the SECE operation: charging, discharging, freewheel, and neutralization. In the charging phase, the switch is turned OFF and the current source charges its shunt capacitance. The accumulated energy is

$$E_{SECE} = \frac{1}{2}\left(C_{po} + C_1\right) V_{SECE}^2. \tag{13}$$

Note that C_1 also serves as the parasitic capacitance to the generator. As aforementioned, there is a turning-ON delay of the switch beyond the actual peak point of V_{po}. Assume that

$C_0 = C_{po} + C_1$ and the voltage drop during the turning-ON delay is V_{dr}, the consequent power dissipation is

$$E_{d,on} = \frac{1}{2} C_0 V_{SECE}^2 - \frac{1}{2} C_0 (V_{SECE} - V_{dr})^2 = \frac{1}{2} C_0 (2V_{SECE} - V_{dr}) V_{dr}. \quad (14)$$

In addition, the input impedance of the rectifier, will also make V_{SECE} lower than the theoretical value, resulting in a reduction of the generator output power compared with the theoretical values.

The second phase consists of discharging the accumulated energy to the inductor. This phase starts when the switch is turned ON. In Fig. 8, it is worth noting that a current surge is observed through the inductor and the MOSFET before the *LC* resonance occurs. In this short process, the high-voltage stress shifts from the MOSFET to the freewheel diode and the inductor via the parasitic capacitance, as a result of the MOSFET being turned ON. Actually, substantial energy loss would result due to the high voltage of the generator. This is also known as dynamic loss in the MOSFET when it is turned ON. Afterwards, *LC* resonance takes place and the electrostatic energy in the shunt capacitance is transferred to the inductor as magnetic energy. Note that due to the ultrasmall value of the shunt capacitance, this process is much faster than those in piezoelectric cases, even with a 1 mH inductor. This phase ends when V_{rec} ramps to 0, stopped by the rectifier. When taking the series resistance R_{ser} of L into consideration, the transient expression of this process is given by [35]

$$V_{po} - V_L = (V_{SECE} - V_{L0})\, e^{-\frac{\omega_1 t}{2Q_I}} \times \left[\left(\frac{1}{2Q_I} \right) \sin(\omega_1 t) + \cos(\omega_1 t) \right],$$
$$I_L = (V_{SECE} - V_{L0})\, C_{s0} \omega_1 e^{-\frac{\omega_1 t}{2Q_I}} \sin(\omega_1 t), \quad \text{for } \frac{1}{Q_I^2} \approx 0 \quad (15)$$

where $C_{s0} = C_s\, C_0/(C_s + C_0)$ is the effective capacitance of C_s and C_0; $\omega_1 = 1/\sqrt{LC_{s0}}$ is the angular frequency of the *LC* resonance; $Q_I = \omega_1\, L/R_{ser}$ is the quality factor. With the parameters provided in Table IV, $Q_I = 171$. Note that this instant does not correspond to the peak current in the inductor, due to the existence of the load voltage. The dissipated power can be calculated by

$$E_{p,ds} = \int_{t_2}^{t_3} I_L(t)^2 R_{ser} dt = (V_{SECE} - V_{L0})^2\, C_{s0}^2 \omega_1^2 R_{ser} \int_0^{\frac{\pi}{2\omega_1}} e^{-\frac{\omega_1 t}{2Q_I}} \sin(\omega_1 t)\, dt. \quad (16)$$

There is also a turning-OFF delay of the switch *M*. The duration of the turning-OFF delay depends on the influence of inter-terminal capacitance C_1 and C_2 as well as the propagation delay of the comparators and the AND gate. On the other hand, because of the existence of V_L, the turning-OFF delay does not necessarily influence the harvested power. To forward the rectifier, I_{po} needs to charge C_{po} to V_L. This critical timeduration is $t_{cri} = C_{po}\ V_L/I_{po} = 77\ \mu$s at $V_L = 5$ V. During this period, even if *M* is ON, source charges are not delivered to C_s because the rectifier is reversed. In other words, the existence of load voltage V_L provides a margin that tolerates an overlong on-state duration no longer than t_{cri}.

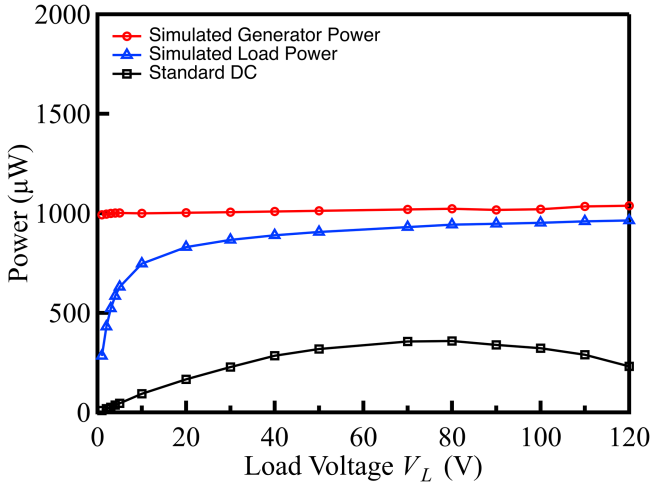

Fig. 9. Simulated power as a function of load voltage.

The third phase consists of freewheeling the energy in the inductor to the storage capacitor on the load side. After the *LC* resonance is terminated by the rectifier, the freewheel diode takes over the inductor current, and the storage capacitor is charged via *L*-D_f-C_s. This phase ends when the current in the inductor reaches 0. The power dissipation in this phase (mainly D_f and *L*) is given by [37]

$$E_{d,fw} = \frac{V_F}{V_L + V_F} E_{ind} \quad (17)$$

where V_F is the forward voltage drop of the freewheel diode and E_{ind} is the energy transferred to the inductor.

The last phase is the reverse recovery of diode D_f. At the end of this phase, V_{rec} equals to V_L and diode D_f is reversely biased. The power dissipation in this phase is negligible since V_{load} and the capacitance of D_f are low.

B. Generator Output Power

Fig. 9 shows the simulated power at generator output and dc load. The power enhancing ratio against the maximal output of the standard case is 3, which is 25% lower than the ideal case. As aforementioned, the following four factors could be responsible for this reduction:

1) input impedance of SECE main circuit;
2) interstage capacitance C_1 and C_2;
   nonideal switching timing (i.e.;
3) the switching-ON delay of *M*;
4) the switching-OFF delay of *M*).

To examine the weight of factor 1), a simulation without C_1 and C_2 is carried out. The gate of *M* is also connected to

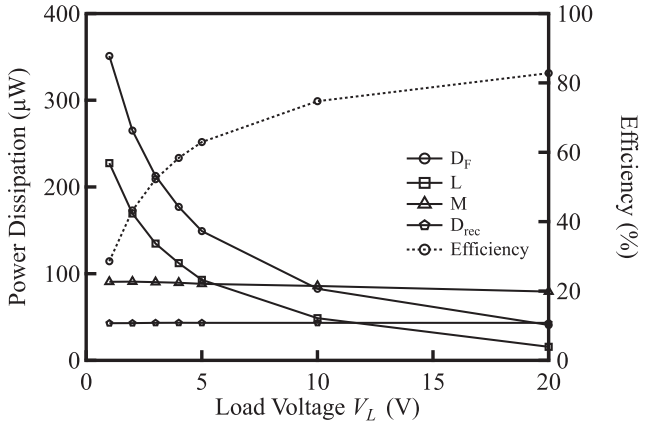

Fig. 10. Power dissipation of each component in SECE main circuit and circuit efficiency as a function of load voltage V_L.

a controllable voltage source, which is perfectly synchronized with I_{po} and its on-duration is tuned to ensure V_{rec} decrease to 0. In this way, factors 2), 3), and 4) are excluded so that the influence of factor 1) can be examined. Consequently, $V_{SECE} =$ 276 V (ideally, 302 V) is obtained with load voltage $V_L = 5$ V, corresponding to $P_{SECE} = 1096$ μW, which is the same as in Fig. 9. Therefore, it is found that the input impedance of the SECE main circuit is predominant for the output power deviation from the ideal case in the simulated range of load voltage.

C. Circuit Efficiency

Fig. 10 shows the power dissipation of each component in the SECE main circuit as a function of load voltage V_L. It is found that D_f consumes much power for V_L lower than 5 V, which agrees with (14). Therefore, reducing its forward voltage drop V_F is crucial to improve the circuit efficiency. Meanwhile, L causes the second largest loss in the sub-5 V range. It is worth noting that the power dissipations of D_f and L are sensitive to the variation of the load voltage and follow a similar trend, indicating that their power dissipations are mainly conduction losses during the freewheel phase.

On the other hand, the power dissipations in M and D_{rec} are relatively insensitive to the variation of the load voltage. For the rectification diodes D_{rec}, the power loss lies in their reversed leakage and forward voltage drop. Since V_{SECE} is independent of V_L, the loss in D_{rec} is therefore independent of V_L. The loss of M consists of three parts: dielectric loss during its OFF state, dynamic loss during its ON state, and conduction loss during the LC resonance. The dynamic loss mainly depends on V_{SECE} and hence, is not related to V_L, whilst the conduction loss depends on V_L since current amplitude in M is relevant to V_L. Since the RMS value of current decreases when V_L increases, the power dissipation of M slightly decreases with increasing V_L. Based on simulated values in Table V, it is found that the dynamic loss and the dielectric loss dominate the power loss of the MOSFET. Therefore, reducing the input capacitance and thus the width of the MOSFET is an effective way to reduce its power dissipation.

TABLE V
ENERGY DISSIPATION OF MOSFET IN A CYCLE

Type	Dielectric loss	Dynamic loss	Conduction loss in LC resonance
Energy loss (nJ)	191.95	189.64	15.93
Percentage	48.28%	47.70%	4.02%

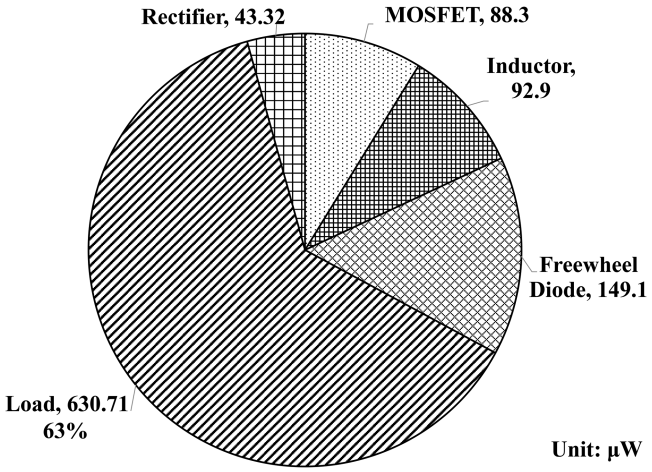

Fig. 11. Load power and power dissipations of components at a load voltage of 5 V.

Fig. 11 shows the consumed power of each component in the SECE main circuit at a load voltage of 5 V. A circuit efficiency of 63% is obtained. To improve the circuit efficiency, since the freewheel diode consumes the most power, it is beneficial to use low forward-voltage drop diode such as Schottky diodes, but high-voltage Schottky diodes usually have high leakage currents, which are not favorable in our case. In addition, to reduce the dynamic loss, the MOSFET should have a fast turning-ON rate and low input capacitance, whilst reducing the width of this MOSFET is also beneficial to reduce its leakage. The leakage of the rectification diodes should be as low as possible. The effect of the inductor is discussed in the next section.

D. Inductor Selection

The inductor not only influences the circuit efficiency, but also dominates the circuit volume. Fig. 12 shows the impacts of three parameters: 1) inductance; 2) series resistance, and 3) parasitic capacitance on load power. The range of the parameters is based on the range of commercially available components. As shown in Fig. 12(a), inductance is a major limitation on the load power if it is less than 0.5 mH. When the inductance exceeds 1 mH, the load power becomes saturated. This is because the increase of inductance reduces the current amplitude in the LC resonance, thereby reducing the conduction losses in the LC resonance and the freewheel phases. Since the inductor tends to be bulky when the inductance is high, a 1-mH inductor is chosen in the present study.

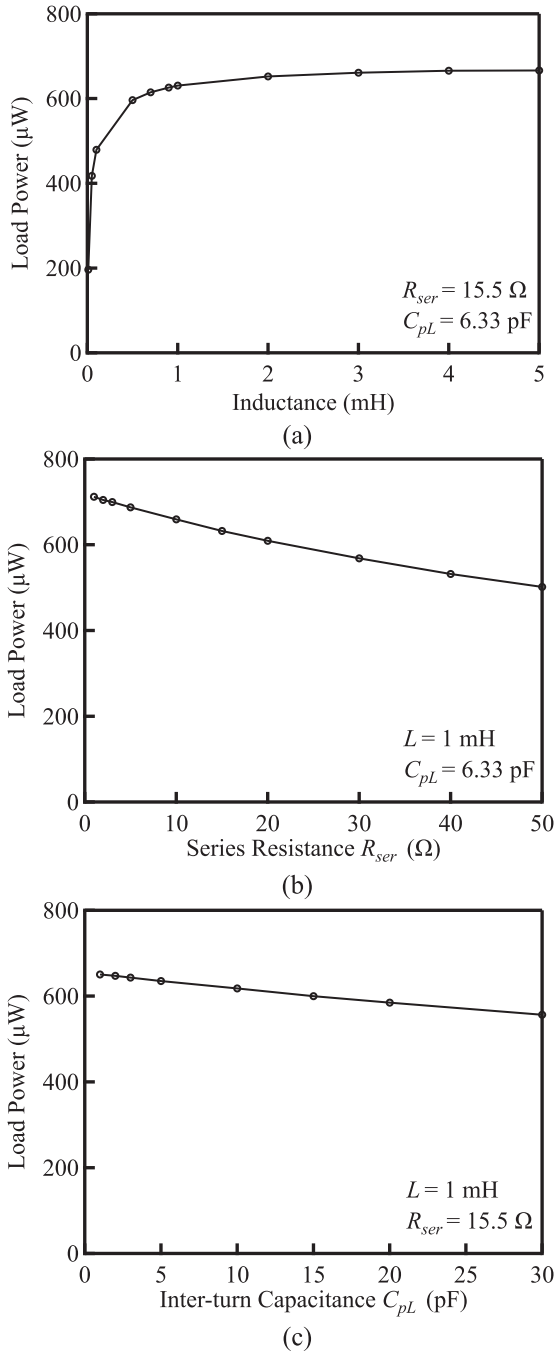

Fig. 12. Influence of (a) inductance, (b) series capacitance, and (c) interturn capacitance on load power.

Fig. 12(b) shows the impact of the series resistance of the inductor on load power. Series resistance consumes power in the *LC* resonance phase and the freewheel phase. Of course, there is a tradeoff between the inductance and the series resistance of the inductor. However, an increase of R_{ser} from 3 to 20 Ω results in only a 13% decrease in the load power. This reduction of load power is less if the inductance is higher.

Fig. 12(c) shows the impact of the parasitic capacitance of the inductor on the load power. It is found that in the range of commercially available components, the load power is not sensitive to the parasitic capacitance of the inductor, because in the present topology, *L* and *M* are in series, this parasitic capacitance is not a source of parasitic capacitance to the generator in the charging phase, thereby eliminating its negative impact on the generator power. Its limited influence on output power lies in its shunt effect during the turning-ON of *M*.

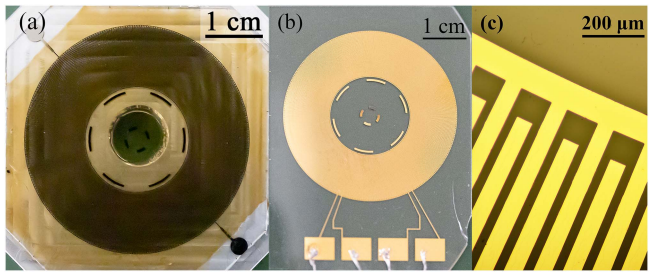

Fig. 13. Fabricated rotational electret EH. (a) Rotor, (b) stator with dual-stage design, and (c) magnified view of the stator.

In terms of the inductor selection, we obtained three findings; First, there is no need to strive for inductance higher than 1 mH, which favors inductor miniaturization. Second, the increase of the series resistance modestly reduces the load power, hence the pursuit of extremely low resistance is not as important as in the piezoelectric energy harvesters. It is possible to reduce the inductor volume by using thinner wires at the expense of higher R_{ser}. Third, the load power is not sensitive to the parasitic capacitance of the inductor due to the circuit topology, which allows for a more compact design of the inductor.

VI. Experimental Results

A. Rotational Electret Generator Fabrication

In the present study, the rotor and stator for the rotational electret generator are fabricated based on MEMS technologies. In the rotor part [Fig. 13(a)], a 360-nm thick Cr/Au/Cr layer is first sputtered on a Tempax (glass) wafer. A total of 300 poles are then patterned by standard photolithography. The horizontal gap between electrodes at the innermost edge is 30 μm. Then, 17-μm thick polymer electret material CYTOP EGG is spun on the patterned electrodes and cured at 280 °C. The electret on the base electrode and guard electrode is respectively charged with soft X-ray [41] to a surface potential of ±800 V. In the stator part [Fig. 13(b)], the same number of poles are formed without the electret film. The number of poles for control and power stages are 40 and 260, respectively. Fig. 13(c) shows a magnified view of the stator. Note that this Tempax wafer-based generator is intended to be used at our test bench to validate our theoretical analyses and numerical simulations. For practical applications, an integrated PCB-based rotational EH with ball bearings has been developed [16], [43], [47]. The measured parameters of the generator are listed in Table VI.

TABLE VI
SYSTEM PARAMETERS IN EXPERIMENTS

f_r	Rotational frequency	1 Hz
n_{po}	Number of electrode pairs in power stage	260
n_{ct}	Number of electrode pairs in control stage	40
V_s	Surface potential of electret	±800 V
d	Thickness of electret	17 μm
C_{po}	Parasitic capacitance of power stage	175 pF
C_{ct}	Parasitic capacitance of control stage	29 pF
I_{po}	Output current of power stage	15.85 μA@300 Hz
I_{ct}	Output current of control stage	2.44 μA@300 Hz

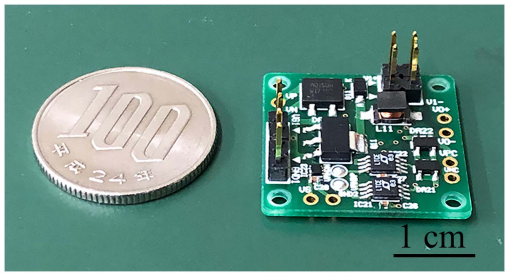

Fig. 14. SECE prototype.

B. SECE Circuit Prototype and Power Generation Experimental Setup

Fig. 14 shows a prototype of the SECE circuit on a double-side PCB using off-the-shelf discrete components. The total volume is 24 mm × 24 mm × 3.6 mm. The inductor (LQH43NH, Murata) is characterized using an impedance analyzer, and its inductance $L = 1$ mH, series resistance $R_{ser} = 15.5\ \Omega$, and parasitic capacitance $C_{pL} = 6.33$ pF are specified. The storage capacitors in the power block (GRM31CR60J227ME11, Murata) and control block (C3216C0G1H, TDK) are $C_s = 220\ \mu$F and $C_r = 200$ nF, respectively. See Table IV for details of the discrete devices. The spice models of the MOSFET BSP89 and the comparators LTC1540 for *Comp1* and *Comp2* are picked from the LTspice library. 250 V-tolerable diodes BAV21 are characterized using a multimeter (U1282A, Keysight), with forward voltage drop $V_F = 1$ V and measured reverse resistance $r_{rev} = 376\ \text{M}\Omega$.

Fig. 15 shows the experimental setup. The rotor is attached to a precision rotational stage (DDR100/M, Thorlabs) by thermal glue and is rotated at 1 rps. On the other hand, the stator is attached to the upper metal frame via a vacuum chuck, thereby creating a uniform air gap between the rotor and stator. The metal frame is connected to a five-axis stage that enables adjustment of the position and inclination of the stator. This allows alignment of the center and parallelism between the rotor and stator using a confocal laser displacement meter (LT-9500, Keyence). A stepping motor (DS102, Suruga Seiki) is then used to adjust the air gap distance accurately.

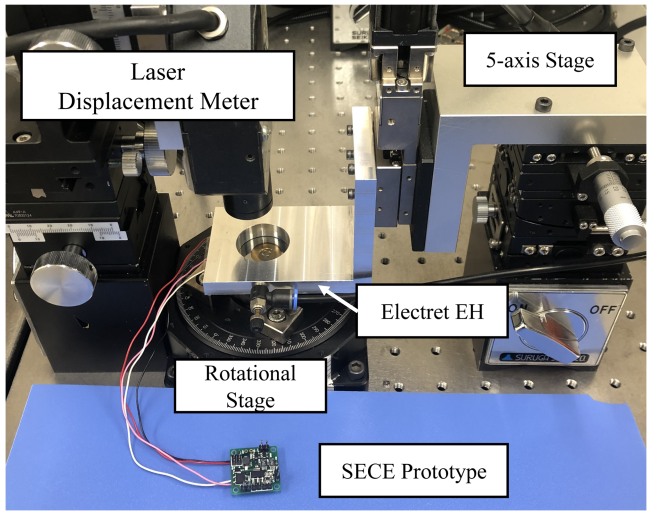

Fig. 15. Experimental setup.

C. Measured Results

Since the electret EH exhibits ultrahigh impedance, a high-input-impedance (1 GΩ, 5 pF) voltage probe (HV-P60A) was used with an oscilloscope (DSO6014A, Agilent) to measure voltages in the main circuit, and it is detached when measuring power. The output power is calculated by measuring the current through the load resistor with a current amplifier (CA5350, NF Corporation).

Fig. 16(a) shows the measured voltages V_{rec} and V_{g}. The typical voltage SECE waveform is obtained at the power stage output. The measured voltage amplitude is 200 V, which is lower than the theoretical value of 266 V considering that the measured open-circuit voltage was 133 V. It could be caused by the finite input impedance of the measurement probe. In addition, an overlong on-state duration of around 210 μs was observed. Therefore, some charges are directly delivered to the load without being stored in the shunt capacitance. In this sense, the overlong duration is also responsible for reduced voltage amplitude. Fig. 16(b) shows the characteristic signals in a half period. The comparators exhibit a propagation delay of approximately 60 μs, while the AND gate demonstrates an extremely weak impact on the total delay. Note that there is no significant difference in the propagation delay of the comparators between the rising and falling edges. Therefore, the contribution to the overlong ON-state duration mainly comes from the influence of parasitic capacitance of the control stage and inter-terminal capacitance between the power stage and control stage.

Fig. 17 shows the output power at the load versus the load voltage. In the standard circuit, a buck converter with full-bridge rectifier (EHPM-50-AB, OWL Solution) is employed to step down the output voltage of the generator to a low dc voltage. The input voltage of the buck converter is rated at 50 V for maximal power transfer (as the measured open-circuit voltage is 133 V). In the SECE circuit, 2.33 mW has been harvested at the load voltage of 4.6 V, which is 2.15 times higher than that in the standard circuit with the buck converter.

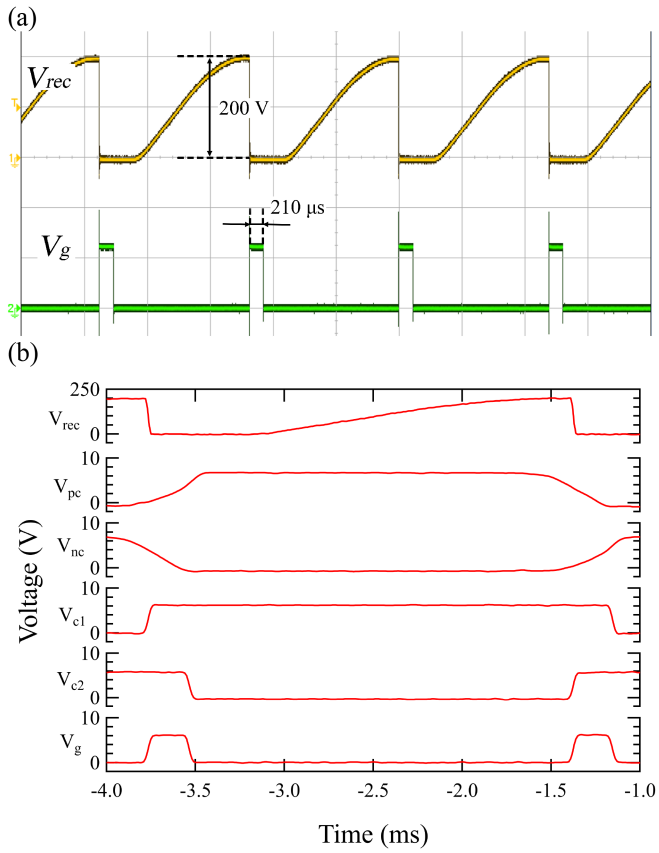

Fig. 16. Measured voltage waveforms in SECE.

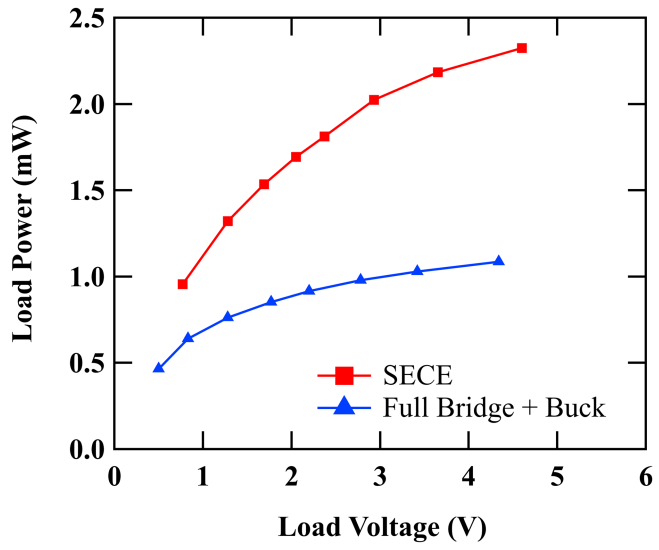

Fig. 17. Load power versus load voltage for the present SECE and for the standard bridge circuit with a buck converter.

To emulate the open-circuit condition, the generator outputs of both power and control stages are connected to the high-input-impedance voltage probe. There is an approximately 6% deviation between the measured output-circuit voltage and the theoretical value derived from Table VI. This could be due to the parasitic capacitance introduced by the probe.

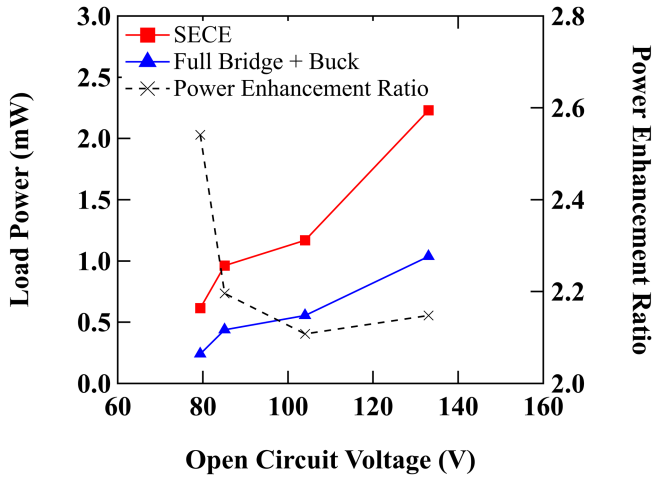

Fig. 18. Harvested power at the load voltage of 5 V with different open-circuit voltages.

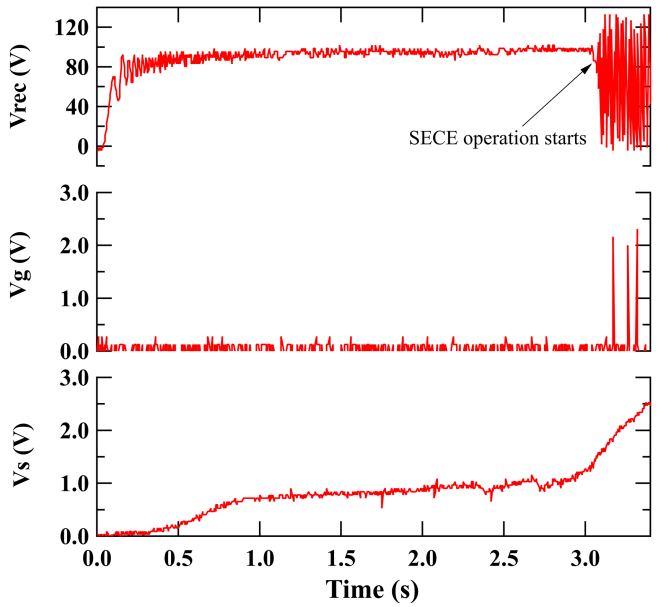

Fig. 19. Cold start of self-powered SECE.

Fig. 18 shows the harvested power at the load voltage of 5 V with the open-circuit voltage V_{oc} varying from 80 to 134 V by changing the air gap between the rotor and stator. The load power increases with higher V_{rec} caused by the increase of V_{oc}.

The power enhancement ratio between SECE and buck converter is at least 2.1 (at $V_{oc} = 104$ V) in the tested range.

Fig. 19 illustrates the measured voltage waveforms during the cold-start process of the self-powered SECE. The driving signal of synchronous switch V_g and typical waveform V_{rec} of SECE is observed when the voltage across the storage capacitor reached 2 V. At the 1 rps rotational speed, V_s is monotonically increased with time, and reaches 1 V after 2.5 s. The SECE operation has successfully started after 3 s. It is noted that the V_g pulses are

TABLE VII
COMPARISON WITH REPORTED TRANSFORMER-FREE SECE CIRCUITS

Work	Source type	Input voltage	Generator capacitance	Harvested power	Power enhancement ratio	Circuit efficiency	Self-powered	Cold start	Technology	Control modules
[34]	Piezo	< 20V	19.5 nF	59 μW	1.23	Up to 85%	Yes	Yes	Integrated	PD, ZCD
[37]	Piezo	< 50V	35.09 nF	2.2 mW	2.6	N/A	No	No	Discrete	ZCD, MCU
[45]	Piezo	< 5V	47.4 nF	< 60 μW	N/A	85.3 %	Yes	Yes	Integrated	PD, ZCD
This work	Electret	100–240 V	175 pF	2.33 mW	> 2.10	63 %	Yes	Yes	Discrete	ZCD

PD: peak detector; ZCD: zero-crossing detector; MCU: microcontroller unit.

not well captured in this measurement due to the limited time resolution.

A comparison with SECE circuits without a transformer is summarized in Table VII. In the previous SECE circuits for piezoelectric EH, the input voltage is lower than 50 V. Considering the ultrahigh voltage of electret energy harvester (100–240 V), the dual-stage design proposed in this work eliminates the usage of an additional power-consuming stage which converts high voltage to low-voltage (<5 V) for the control block [32], thereby improving the circuit efficiency. In addition, the concise yet effective control scheme shows very low (<5 μW) power overhead even with discrete components, which results in self-powering performance. Moreover, the start of the control block does not rely on the residual energy on the load side, instead it directly exploits the energy harvested from the initial motion of electret energy harvester, resulting in a cold-start feature which is important for practical application.

VII. CONCLUSION

In this work, the development of SECE for rotational electret EH is presented for the first time. Considering the ultrahigh output voltage of the electret EH, a novel dual-stage design has been proposed to provide a low-voltage yet synchronous signal for the control circuit. The proposed topology of the SECE main circuit with a low-side switch is able to enhance the voltage rating, reduce the power losses in the driving switch and provide a margin for switching timing. The proposed control scheme is adaptive to internal capacitance and external inductance, and can be easily implemented using off-the-shelf components with a very low power dissipation (1∼2 μW). Using a rotational electret generator prototype, 2.33 mW has been obtained on a 4.6 V load, which is 2.15 times of that obtained by a conventional buck converter with a standard bridge rectifier.

Based on the circuit simulation, the proposed circuit shows a circuit efficiency of 63% when the load voltage is 5 V. The major loss is in the freewheel diode, followed by the conduction loss in the inductor and the MOSFET. Therefore, reducing the forward voltage drop of the freewheel diode could be an effective way to improve the efficiency. An inductor with an inductance of about 1 mH is preferred. However, unlike in the piezoelectric energy harvester, the load power is somewhat insensitive to the series resistance. Therefore, a more compact inductor at the expense of its series resistance can be used for further miniaturization of the present circuit.

In our future work, an integrated circuit will be designed with a high-voltage technology to realize a more compact SECE circuit compatible with electret EHs for wearable devices.

ACKNOWLEDGMENT

The Photo-mask was made using the University of Tokyo VLSI Design and Education Center (VDEC)'s 8-inch EB writer F5512+VD01 donated by ADVANTEST. The microfabrication process was partially supported by "Advanced Research Infrastructure for Materials and Nanotechnology in Japan (ARIM)" of the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Proposal Number JPMXP1222UT1009.

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Yiran Liu received the graduation degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2013, and the Dr. Eng. degree in mechanical engineering from the University of Tokyo, Tokyo, Japan, for his work on nonlinear interface circuit design for electret energy harvester in 2020.

He is currently an Engineer with Mercedes-Benz R&D Japan, Kanagawa, Japan.

Zehan Shi received the B.Eng. degree in ocean enginnering and technology from Zhejiang University, Hangzhou, China, in 2019, and the M.Eng. degree in mechanical engineering in 2022 from the University of Tokyo, Tokyo, Japan, where he is currently working toward the Ph.D. degree in mechanical engineering with the Graduate School of Engineering, the University of Tokyo, Tokyo, Japan.

His current research interests include kinetic energy harvesting and nonlinear interface circuit design.

Adrien Badel received the M.S. degree in electrical engineering from the National Institute of Applied Sciences of Lyon and the Ph.D. degree in vibration control and energy harvesting from the Electrical Engineering and Ferroelectricity Laboratory, INSA Lyon, Villeurbanne, France, in 2002 and 2005, respectively.

From 2005 to 2007, he was a Japanese Society for the Promotion of Science (JSPS) Postdoctoral Fellow with the Institute of Fluid Science, Tohoku University, Sendai, Japan. He is currently a Full Professor with the Laboratory of Systems and Materials for Mechatronics, University of Savoie Mont Blanc, Annecy, France. His current research interests include energy harvesting, vibration damping, and piezoelectric actuators modeling and control.

Tomoya Miyoshi (Member, IEEE) received the M.Eng. degree in mechatronics from the Tokyo Institute of Technology, Tokyo, Japan, in 2014, and the Dr.Eng. degree in microelectro-mechanical systems from the Department of Mechano-Micro Engineering, Tokyo Institute of Technology, Tokyo, Japan, in 2017.

He was a Postdoctoral Fellow with the Department of Mechanical Engineering, the University of Tokyo, Tokyo, Japan, in 2017. He was a Visiting Researcher with the Advanced Materials and Liquid Crystal Institute, the Kent State University, Kent, OH, USA, in 2019. He is currently a Project Assistant Professor with the Department of Mechanical Engineering, the University of Tokyo, Tokyo, Japan. His current research interests include energy harvesting, electret, liquid crystal application, and energy autonomy of wearable device.

Yuji Suzuki (Fellow, IEEE) received the Dr.Eng. degree in mechanical engineering from The University of Tokyo, Tokyo, Japan, in 1993.

He is currently a Professor with the Department of Mechanical Engineering, the University of Tokyo. His current research interests include energy harvesting using electrets, microscale combustion, and optimal design and active control of microthermo-fluids systems.

Dr. Suzuki serves as Steering Committee Member of PowerMEMS Conference, International Scientific Advisory Committee Member of IEEE International Symposium on Electret, and Senior Editor for *IEEE Sensor Letters*. He also served as Chair of Micro-Nano Science and Technology Division, JSME (2015), a general co-chair of IEEE MEMS 2010, and a general chair of PowerMEMS 2017.