Reducing the Input Capacitance to Minimize the Right-Half-Plane Zero Effect for Buck Converters in Wireless Power Receiver Systems

Shuai Dong, Jie Liu, Baichuan Zhang, Chen Lin, and Chunbo Zhu

***Abstract*—Buck converters are widely used in wireless power receiver systems for voltage conversion, impedance matching, and power regulation. However, when the receiver's resonant network has a current-source nature, it introduces a right-half-plane zero in the control-to-output transfer function, which adversely affects the system's transient performance. This article presents a proposed solution by reducing the dc-link capacitance, which coincides with the input capacitance of the buck converter. The critical value of the input capacitance is examined through theoretical analysis and mathematical derivation. The experimental results demonstrate that reducing the input capacitance effectively mitigates output overshoot and reduces the adjustment time, thereby confirming the accuracy of the critical capacitance value.**

***Index Terms*—Buck converter, capacitor, overshoot, right-half-plane (RHP) zero, wireless power transfer (WPT).**

I. Introduction

WIRELESS power transfer (WPT) technology enables contact-free power connection between the power supply and the load, offering improved security, convenience, and intelligence compared with the traditional wired power supply methods. The potential applications of WPT are of great significance in fields, such as industrial automation, electric vehicles, and aerospace [1], [2], [3], [4], [5].

The classical buck converter is widely employed in WPT systems as an essential component on the receiver side to lower voltage levels. It is commonly understood that when operating in continuous conduction mode (CCM) with a voltage-source input, the control-to-output transfer function of a buck converter does not contain a right-half-plane (RHP) zero [6], [7]. However, a recent observation has reported an interesting phenomenon in which the adoption of current-source nature compensation networks, such as series–series (S–S), *LCC–LCC*, and *LCL–LCL*, in WPT systems introduces the presence of an RHP zero [8], thereby transforming the buck converter into a non-minimum-phase system. Consequently, the buck converter exhibits a different frequency characteristic compared with the conventional voltage-source step-down converters.

The existence of the RHP zero in the control-to-output transfer function of the current-source buck converter in WPT leads to negative overshoot voltage and slow response [9]. Traditionally, when designing the closed loop for a non-minimum-phase system, the voltage loop bandwidth is set to be sufficiently low to eliminate the impact of the RHP zero, ensuring that stability requirements are met. However, this approach is unsuitable for applications requiring fast dynamics [10], [11], [12].

Efforts have been made to address the RHP zeros and their effects on the dynamic performance of wireless power receivers through the proposal of new control schemes or circuit topologies. One control strategy developed to eliminate the RHP zero involves adding a feedforward path for the dc-link voltage in the wireless power receiver controller [13], [14], [15]. By increasing damping, this approach achieves overshoot damping and dynamic improvement, enabling significant control gains. Another proposed solution involves a double closed-loop power controller (comprising a current inner loop and a power outer loop) for the buck converter in WPT systems with dual *LCC* compensation topology, resulting in improved transient performance of the system [16].

Another effective method for mitigating the RHP zero in the control-to-output transfer function of a wireless power receiver is to adopt a novel topology. A modified receiver with an active rectifier for the WPT current-source dc–dc converter has been proposed in previous studies [17], [18]. This modified receiver exhibits minimum-phase characteristics and offers greater control flexibility. Additionally, a separate study introduces an electrolytic capacitorless wireless WPT system that eliminates the need for a dc/dc converter [19].

This article investigates a novel alternative approach to address the RHP zero issue through parameter optimization. The influence of passive components, including the inductor, input capacitor, and output capacitor, on the RHP zero is analyzed based on the small-signal model of the current-source buck converter. One obvious solution to eliminate the RHP zero effect is by reducing the input capacitance of the buck converter. This method also presents the advantage of employing a thin

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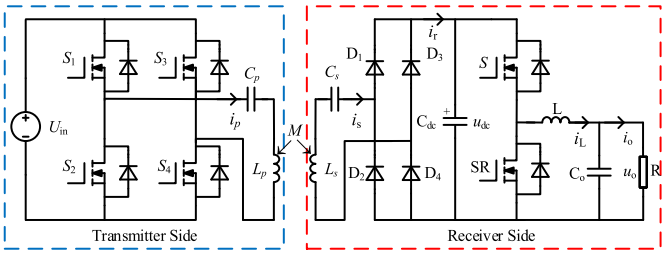

Fig. 1. Schematic diagram of a WPT system with S–S compensation circuit and buck-converter receiver.

film capacitor with enhanced resistance against high-frequency noise and a longer lifespan; the reliability of the system could be improved when utilizing smaller capacitances. Furthermore, determining the minimum value holds guiding significance for capacitance design in intrinsically safe systems. The experimental results were used to validate the effectiveness of the proposed critical capacitance approach.

II. Impact Analysis of the Buck Input Capacitance for RHP Zero

A. RHP Zero of the Buck Converter

The circuit topology of the WPT system utilizing an S–S compensation circuit and a buck-converter receiver is depicted in Fig. 1. The transmitter side comprises a full-bridge inverter (with switches $S1$–$S4$) and a primary coil L_p connected in series with a resonant capacitor C_p. On the receiver side, there is a secondary coil L_s with a series resonate capacitor C_s, a high-frequency uncontrolled rectifier (consisting of diodes $D1$–$D4$ and a dc-link capacitor $C_{\rm dc}$), a synchronous buck converter (including switches S, synchronous rectification (SR) MOSFET, inductor L, and capacitor C_o), and a load resistor R. The full-bridge inverter operates at the switching frequency f_s, which is equal to the resonant frequency (i.e., $1/\sqrt{L_pC_p} = 1/\sqrt{L_sC_s} = 2\pi f_s$) of the system. It is important to note that specific relationships between the buck-converter switching frequency f_b and the resonant frequency f_s must be satisfied. It has been demonstrated that the interaction between the switching frequency of the buck converter and the resonant frequency of the wireless system can lead to beat frequency oscillation [20]. To mitigate the adverse effects of beat frequency oscillation, the following parameters should be considered: $f_b > 10f_s$, $f_b = 2f_s$, or $f_b < 0.4f_s$. However, a high switching frequency can result in increased losses, while a low switching frequency may not be conducive to reducing the capacitance value. Therefore, in this study, the switching frequency of the buck converter (f_b) was set to twice the resonant frequency (f_s).

Due to the presence of the S–S resonate circuit, the secondary coil L_s generates an independent sinusoidal current $i_s(t)$, which acts as a current source for the receiver input side. When the buck converter operates in CCM, two distinct equivalent WPT receiver-side topologies can be observed, as depicted in Fig. 2(a) and (b).

In Mode 1 [see Fig. 2(a)], the S switch is turned ON, allowing energy transfer from the current source to the load, while the SR switch remains OFF. Conversely, in Mode 2 [see Fig. 2(b)], the S switch is turned OFF, interrupting the energy transfer between the receiver input current source and the load, while the SR switch is turned ON.

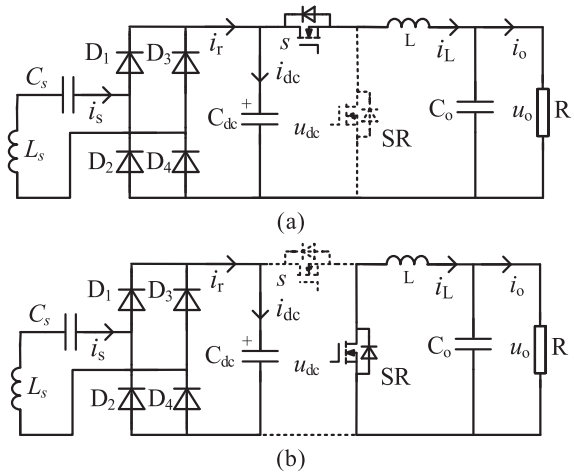

Fig. 2. Equivalent operation modes of the WPT receiver. (a) Mode 1. (b) Mode 2.

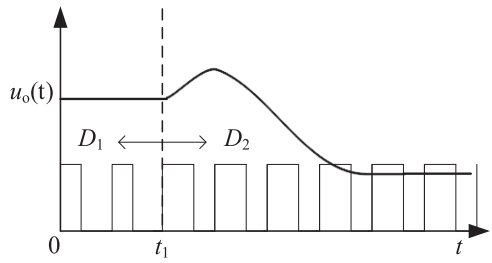

Fig. 3. Waveforms of the buck converter showing step response in the duty cycle.

By deriving the equation of state for the aforementioned two modes and utilizing per-switching-cycle state-space averaging, the steady-state dc values and small-signal model can be obtained [8]. The equations are given as follows:

$$\begin{cases} U_{\rm dc} = \frac{2RI_s}{\pi D^2} \\ I_L = \frac{2I_s}{\pi D} \\ U_o = \frac{2RI_s}{\pi D} \end{cases} \tag{1}$$

$$G_{uo}(s) = \frac{2RI_s\left(C_{\rm dc}Rs - D^2\right)}{\pi D^2\left[C_oC_{\rm dc}LRs^3 + C_{\rm dc}Ls^2 + \left(C_oRD^2 + C_{\rm dc}R\right)s + D^2\right]}. \tag{2}$$

Here, the capital letters U and I represent the instantaneous voltage and current values, respectively.

B. Physical Origins of RHP Zero in the Current-Source Buck Converters

Based on (2), the control-to-output transfer function of the buck converter exhibits an RHP zero represented by RHP zero $= D^2/(C_{\rm dc}R)$. Fig. 3 illustrates the typical waveforms of the transient response for a step change in the duty cycle. In this

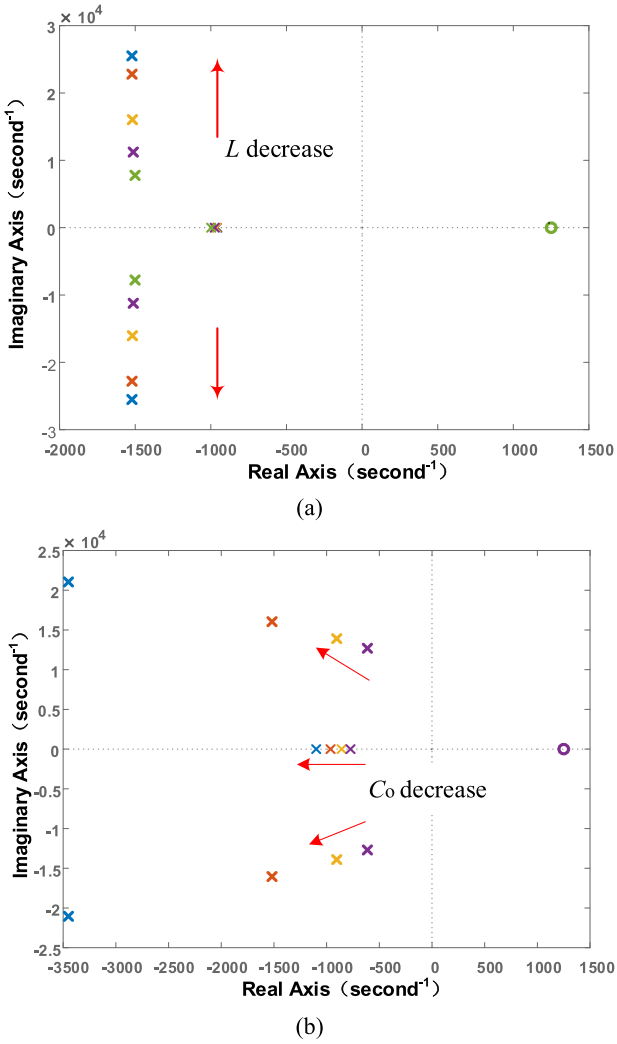

Fig. 4. Pole–zero map of G_{uo} (s) with varying values of buck converter (a) inductance and (b) output capacitance.

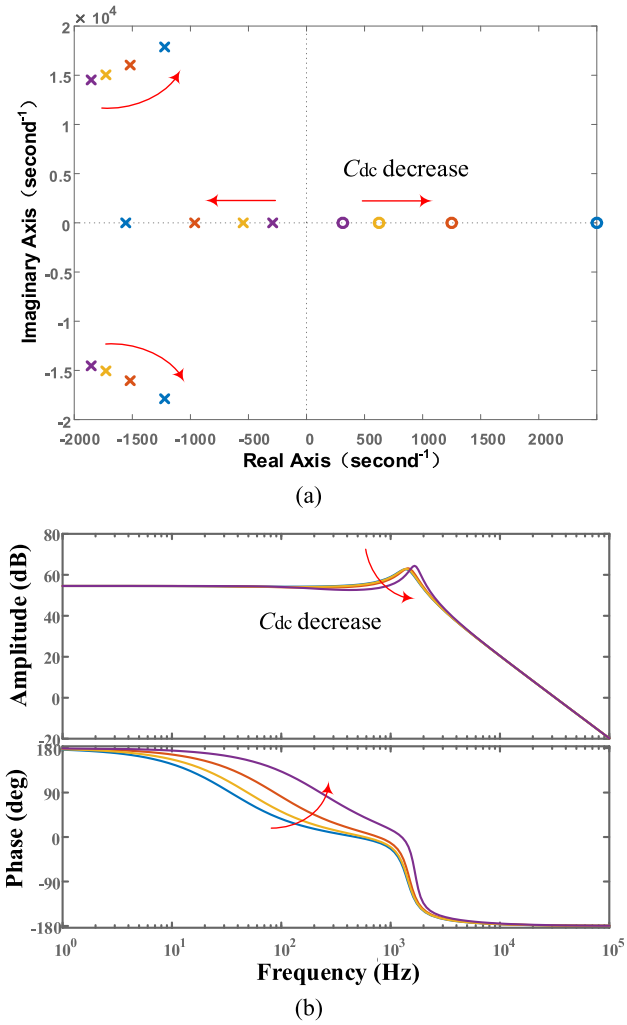

Fig. 5. (a) Pole–zero map and (b) bode plots of G_{uo} (s) with varying buck-converter input capacitances.

example, the buck converter initially operates in equilibrium with a duty cycle of D_1. Considering the balance of inductor charge, the average inductor voltage is zero, and the average output voltage $<u_o>_{\mathrm{T}}$ is given by

$$\langle u_o \rangle_T = D \times \langle u_{\mathrm{dc}} \rangle_T \tag{3}$$

where $<u_{\mathrm{dc}}>T$ represents the average input capacitor voltage over one switching cycle.

At time $t = t_1$, the duty cycle increases to D_2 (where $D_2 > D_1$). As a result, the average output voltage magnitude, as indicated by (3), initially increases. The extended duty cycle leads to a gradual decrease in the input capacitor voltage u_{dc}, as shown in Fig. 3. Consequently, the average output voltage will eventually decrease, reaching a new equilibrium value corresponding to D_2.

C. Inductor and Capacitor Parameters Impact Analysis of the Zero

Fig. 4 presents the pole–zero maps of the control-to-output transfer function with a parametric sweep of the inductor L and output capacitor C_o while maintaining a fixed duty ratio. The analysis reveals that variations in inductance or output capacitance have minimal impact on the RHP zeros.

Moving on to Fig. 5(a), the pole–zero map of $G_{uo}(s)$ is displayed. It demonstrates that reducing the value of C_{dc} generally causes the zeros to shift from the origin toward the RHP along the real axis, while allowing the conjugate poles to approach the imaginary axis. It is well-known that a tradeoff exists between the position of open-loop zeros and the output responses of the closed-loop system. Hence, designing the input capacitance to be as small as possible helps move the zeros farther away from the origin, mitigating this tradeoff. Otherwise, the angle between the conjugate pole and the negative real axis gradually increases, and it adversely affects the relative stability of the system. The comprehensive performance of the system can be obtained by analyzing the bode plots.

Fig. 5(b) illustrates the bode plots of $G_{uo}(s)$. It is evident that, as C_{dc} decreases, the low-frequency gain remains relatively unchanged, while the low-frequency phase improves. This improvement proves advantageous for the design of lag closed-loop controllers, such as the proportional-integral (PI) controller.

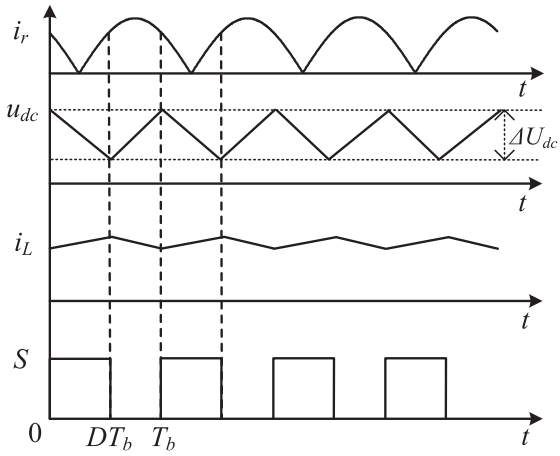

Fig. 6. Theoretical waveforms of the buck converter.

III. Critical Buck Input Capacitance

Based on the aforementioned analysis, it is evident that reducing the input capacitance $C_{\rm dc}$ results in greater deviation of the RHP zero from the imaginary axis, thereby improving the system performance. However, it is important to note that $C_{\rm dc}$ cannot be excessively small, and a critical minimum value needs to be determined using the following equations.

Assume that the expression of the sinusoidal current $i_s(t)$ at the input side of the receiver is

$$i_s(t) = I_s \sin(\omega t) \tag{4}$$

where ω represents the angle frequency, $\omega = 2\pi f$.

As a result of the rectification action of the diodes, the rectified current $i_r(t)$ can be expressed as follows:

$$i_r(t) = I_s \left|\sin(\omega t)\right|. \tag{5}$$

During the period 0 to DT_b, when the switch S is turned ON, the rectified current $i_r(t)$ and the input capacitor $C_{\rm dc}$ charge the inductor together. As shown in Figs. 2(a) and 6, the $C_{\rm dc}$ voltage continuously decreases, while the inductor current increases. The average discharge current $I_{\rm dc1}$ of $C_{\rm dc}$ during this stage is given by

$$\begin{aligned} I_{\rm dc1} &= I_L - \frac{1}{DT_{\rm b}} \int_0^{DT_b} i_r d(t) \\ &= \frac{U_o}{R} - \frac{1}{DT_{\rm b}} \int_0^{DT_b} I_s \left|\sin \omega t\right| d(t) \end{aligned} \tag{6}$$

where T_b represents the switching duty of the buck converter, $T_b = 1/f_b$. The circuit operates in CCM, and the inductance L is sufficiently large such that the inductor current can be considered constant during this period, $I_L = I_o = U/R$.

When $I_r(t)$ is within the minimum range, the average discharge current of $C_{\rm dc}$ reaches its maximum value, satisfying the following equation:

$$I_{\rm dc1\,max} = \frac{Uo}{R} - \frac{T_s}{2\pi DT_b} \int_{\pi - \frac{DT_b\pi}{T_s}}^{\pi + \frac{DT_b\pi}{T_s}} I_s \left|\sin \omega t\right| d(\omega t). \tag{7}$$

According to the capacitor charge equation $Q = C{*}\Delta U = i{*}T$. To determine the minimum capacitance $C_{\rm dc\text{-}min1}$, which corresponds to this condition, the following requirement needs to be met:

$$C_{\rm dc-min\,1} = \frac{I_{\rm dc1\,max} \times DT_b}{\Delta U_{\rm dc}}. \tag{8}$$

To simplify the analysis, the waveform of $u_{\rm dc}$ is approximated as a triangular wave. For the critical mode, the following relation is established:

$$\Delta U_{\rm dc} = 2U_{\rm dc} = \frac{4RI_s}{\pi D^2}. \tag{9}$$

By combining (6)–(9), the following equation can be obtained:

$$C_{\rm dc-min\,1} = \frac{D^2}{4Rf_b} - \frac{D^2}{4Rf_s} \cos\left[\frac{f_s(1-D)\pi}{f_b}\right]. \tag{10}$$

During the period DT_b to T_b, when the switch S is turned OFF, the rectified current i_r(t) charges the input capacitor $C_{\rm dc}$. The $C_{\rm dc}$ voltage gradually increases while the inductor current continues to flow through diode D, as depicted in Figs. 2(b) and 6, and the inductor current continues to flow along diode D, as shown in Figs. 2(b) and 6. The average charging current $I_{\rm dc2}$ of $C_{\rm dc}$ at this stage can be expressed as follows:

$$\begin{aligned} I_{\rm dc2} &= \frac{1}{(1-D)\,T_b} \int_{DT_b}^{T_b} i_r d(t) \\ &= \frac{1}{(1-D)\,T_b} \int_{DT_b}^{T_b} I_s \left|\sin \omega t\right| d(t). \end{aligned} \tag{11}$$

When $I_r(t)$ is within the maximum range, the $C_{\rm dc}$ charging average current reaches its maximum, satisfying the following equation:

$$I_{\rm dc2\,max} = \frac{T_s}{2\pi\,(1-D)\,T_b} \int_{\frac{\pi}{2} - \frac{(1-D)T_b\pi}{T_s}}^{\frac{\pi}{2} + \frac{(1-D)T_b\pi}{T_s}} I_s \left|\sin \omega t\right| d(\omega t). \tag{12}$$

The minimum capacitance $C_{\rm dc\text{-}min2}$ at this stage should meet the following requirement:

$$C_{\rm dc-min\,2} = \frac{I_{\rm dc2max} \times (1-D)\,T_b}{\Delta U_{\rm dc}}. \tag{13}$$

By combining (12) and (13), the following equation can be obtained:

$$C_{\rm dc-min\,2} = \frac{D^2}{4Rf_s} \sin\left[\frac{f_s(1-D)\pi}{f_b}\right]. \tag{14}$$

Based on (10) and (14), the critical value of $C_{\rm dc}$, denoted as $C_{\rm dc\text{-}min}$, can be calculated as follows:

$$C_{\rm dc-min} = \max\left(C_{\rm dc-min\,1},\ C_{\rm dc-min\,2}\right). \tag{15}$$

According to (15), when the ratio f_b/f_s is fixed, the relationship curves of the critical capacity $C_{\rm dc\text{-}min}$, duty cycle D of the buck circuit, and resonant frequency f_s can be obtained, as shown in Fig. 7.

Fig. 7 also illustrates that the critical capacitance $C_{\rm dc\text{-}min}$ increases with an increase in D and decreases with an increasing resonant frequency.

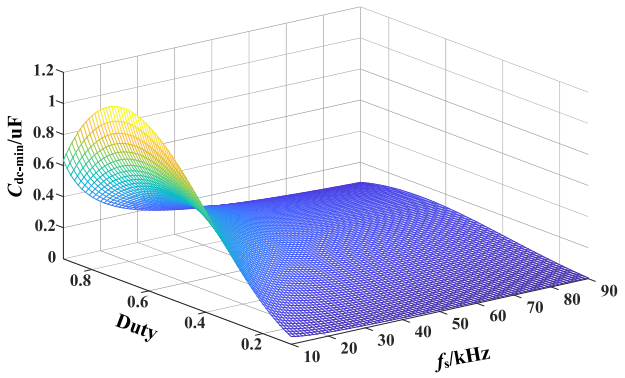

Fig. 7. $C_{\text{dc-min}}$ with different resonant frequencies at different duty ratios.

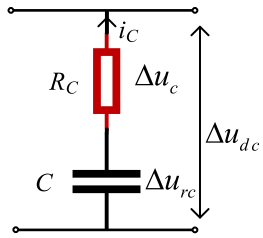

Fig. 8. Capacitor model considering ESR.

IV. Discussion

A. Voltage Ripples in U_{dc}

Reducing C_{dc} to mitigate the negative effects of the RHP zero and enhance system performance also results in an increase in the dc-link voltage ripple.

The charging and discharging of capacitors are balanced within a switching cycle. During the switch-ON period ($0 < t < DT_b$), the state equation of C_{dc} is

$$C_{\text{dc}}\frac{du_c}{dt} = i_r - i_L \tag{16}$$

and the voltage ripple on the capacitor Δu_{dc} can be expressed as follows:

$$\Delta u_{\text{dc}} = \int_0^{DT_b} \frac{(i_r - i_L)}{C_{\text{dc}}} dt. \tag{17}$$

By substituting the steady-state operating point of the system into (17), the following equation can be obtained:

$$\Delta U_{\text{dc}} = \frac{2(1-D)I_s}{\pi C_{\text{dc}} f_b}. \tag{18}$$

It is worth noting that the voltage ripple in (18) is based on an ideal capacitor; however, commonly used electrolytic capacitors have a large equivalent series resistance (ESR), which increases the output ripple voltage of the capacitor. As depicted in Fig. 8, C represents an ideal capacitor, R_c represents the ESR, and the output voltage ripple Δu_{dc} consists of the capacitive voltage ripple Δu_c and the ESR voltage ripple Δu_{rc}.

Taking the ESR into account, the total voltage ripple during the switch-ON period is given as follows:

$$\Delta u_{\text{dc-on}}(t) = \Delta u_c(0) + \frac{1}{C_{\text{dc}}}\int_0^t i_r(t) - i_L(t)dt + [i_r(t) - i_L(t)]\,R_C. \tag{19}$$

The total voltage ripple during the switch-ON period is given as follows:

$$\Delta u_{\text{dc-off}}(t) = \Delta u_c(DT_b) + \frac{1}{C_{\text{dc}}}\int_0^t i_r(t)dt + i_r(t)R_C \tag{20}$$

where $\Delta u_c(0)$ is the initial voltage across the capacitor at $t = 0$, and $\Delta u_c(DT_b)$ is the initial voltage across the capacitor at $t = DT_b$. In the steady state, $\Delta u_c(DT_b) = \Delta u_c(0)$.

If the minimum value of $u_{\text{dc-on}}$ appears at time t_1 and the maximum value of $u_{\text{dc-off}}$ occurs at t_2, the following equation can be derived:

$$\Delta u_{\text{dc}} = \Delta u_{\text{dc-off}}(t_2) - \Delta u_{\text{dc-on}}(t_1). \tag{21}$$

In this article, reducing the C_{dc} to the critical value increases the voltage ripple. Additionally, a smaller capacitance has a larger ESR, which theoretically further increases the voltage ripple. However, when the C_{dc} is small enough, a film capacitor can be used instead of an electrolytic capacitor. Furthermore, the ESR of a film capacitor is very small, usually not more than 1 mΩ, rendering the voltage ripple caused by the ESR negligible.

B. Loss of ESR of C_{dc}

The power loss generated on the ESR of C_{dc} can be expressed as follows:

$$P_{\text{ESR}} = \left[\frac{\frac{2}{\pi}I_r(1-D)T_b + (I_L - \frac{2}{\pi}I_r)DT_b}{T_b}\right]^2 R_C. \tag{22}$$

By simplifying (22), the following equation can be obtained:

$$P_{\text{ESR}} = \left[\frac{4(1-D)I_r}{\pi}\right]^2 R_C. \tag{23}$$

From (23), we can observe that using a thin film capacitor with a small ESR will result in minimal loss caused by C_{dc} and has the potential to improve the system's efficiency. The actual impact on system efficiency will be discussed in Section V.

C. Influence of Large Voltage Ripple

When the input capacitance C_{dc} reaches its critical value, the voltage ripple will be at its maximum. By substituting the expression of the critical capacitance into (18) and assuming $f_b = 2f_s$, the maximum voltage ripple can be obtained as follows:

$$\Delta u_{\text{dc-max}} = \frac{4\,(1-D)\,RI_s}{\pi D^2 \sin\left(\frac{(1-D)}{2}\pi\right)}. \tag{24}$$

The condition for the buck converter to operate in CCM is given as follows:

$$I_o > \frac{\overline{U_{\text{dc}}}T_b}{2L}D\,(1-D) \tag{25}$$

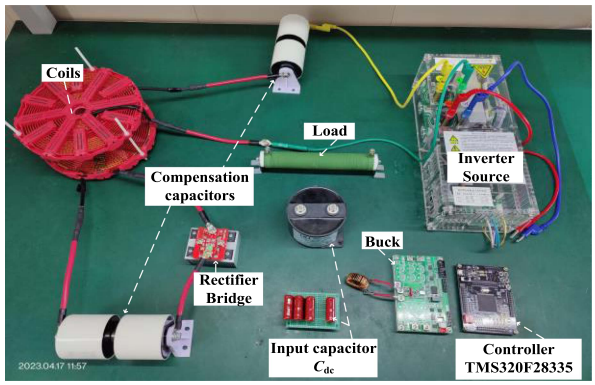

Fig. 9. Schematic diagram of the experimental platform.

where I_o is the output current and $\overline{U_{\rm dc}}$ is the average input voltage during the switch-ON period. Due to the critical input capacitance at this time, the following equation can be obtained:

$$\overline{U_{\rm dc}} = \frac{1}{2}\Delta u_{\rm dc-max}. \tag{26}$$

By combining (24), (25), and (26), the condition necessary for the buck converter to operate in CCM can be obtained as follows:

$$I_o > \frac{(1-D)^2 R I_s}{\pi D L f_b \sin\left(\frac{(1-D)}{2}\pi\right)}. \tag{27}$$

If the system parameters are appropriate, the impact of the input capacitance on the inductor ripple is not significant and generally does not cause the buck converter to operate in DCM. Additionally, the output voltage ripple is filtered out by the output capacitor C_o. Therefore, a larger input voltage ripple will not cause abnormal operation of the subsequent circuits.

It is noteworthy that this work focuses on the lower limit of capacitance and provides guidance for parameter design. However, having an excessively small bus capacitor may lead to issues, such as larger voltage ripple, increased device stress, and lower efficiency, which may not be acceptable in certain systems. Therefore, in practical applications, the capacitance does not necessarily have to be at its minimum value, and it should be selected in consideration of the actual circumstances.

V. Experimental Verification

An experimental platform was constructed to validate the effectiveness of buck converters in mitigating the impact of the RHP zero by reducing the input capacitance, as illustrated in Fig. 9. The transmitter side consisted of a dc power supply, a full-bridge inverter, and a coupling mechanism with a series resonant capacitor. On the receiver side, there was a coupling mechanism with a series resonant capacitor, a buck converter, and a load. The experimental parameters of the prototype are presented in Table I. In this system, a TMS320F28335 microcontroller was employed as the controller to facilitate tasks, such as output voltage sampling,PI closed-loop control, pulsewidth modulation output, and frequency synchronization.

TABLE I
System Experimental Parameters

Parameters	Values
inverter switching frequency f_s	85 kHz
Buck switching frequency f_b	170 kHz
primary self-inductor L_p	140.8 μH
primary capacitor C_p	24.9 nF
secondary self-inductor L_s	140.5 μH
secondary capacitor C_s	24.9 nF
mutual inductor M	41.1 μH
load R	5Ω
Buck converter inductor L	220 μH
output C_o	220 μF

A. Impact of C_{dc} on System Performance

When the output voltage was operating in an open-loop configuration, modifications were made to the buck input capacitance, $C_{\rm dc}$, in order to observe the impact on the phenomenon of RHP zero.

Fig. 10 illustrates the time-domain experimental response waveform of the output voltage U_o for different values of $C_{\rm dc}$: 220 μF, 100 μF, and 50 μF. The U_o decreased from 7 to 3.4 V when $C_{\rm dc}$ was set to 220 μF, 4.1 V when $C_{\rm dc}$ was 100 μF, and 4.84 V when $C_{\rm dc}$ was 50 μF. Subsequently, the voltage entered a new steady-state value of 11.8 V. Consequently, the U_o overshoot values were 51.4%, 41.4%, and 30%, respectively.

As the value of the input capacitance decreased, the adjustment time gradually decreased as well. Specifically, it took 25 ms for adjustment with $C_{\rm dc}$ at 220 μF, 20 ms with $C_{\rm dc}$ at 100 μF, and 14 ms with $C_{\rm dc}$ at 50 μF.

Fig. 12 depicts the experimental waveform of the system operating under closed-loop feedback control (K_p = 1/80 and $K_i = 5$), as illustrated in Fig. 11. The values of $C_{\rm dc}$ used in the experiment were 220 μF and 50 μF, respectively.

Fig. 12 further demonstrates that when $C_{\rm dc}$ was set to 220 μF, both U_o and $U_{\rm dc}$ exhibited periodic fluctuations, indicating an unstable system. However, with $C_{\rm dc}$ reduced to 50 μF, the frequent variations in U_o and $U_{\rm dc}$ disappeared, resulting in system stability. The reduction in input capacitance $C_{\rm dc}$ improved the steady-state performance of the closed-loop system, aligning with the findings of prior theoretical analysis. To restore stability with $C_{\rm dc}$ at 220 μF, the integration coefficient K_i needed to be correspondingly reduced (K_p = 1/80 and $K_i = 2$).

B. Verification of Critical C_{dc}

Based on Table I and (15), the critical capacitance $C_{\rm dc\text{-}min}$ was calculated to be 76 nF.

Fig. 13(a) illustrates the experimental results for the rectified current I_r, dc-link voltage $U_{\rm dc}$, load voltage U_o, and load current I_o, with the following parameters: transmitter-side dc voltage $U_{\rm in} = 30$ V, $f_b = 170$ kHz, output voltage $U_o = 9$ V, and $C_{\rm dc} = 220$ nF ($> C_{\rm dc\text{-}min}$). As shown in Fig. 12(a), the system remained stable with $U_{\rm dc} = 12$ V and a voltage difference of $\Delta U = 9.4$ V. The actual test results demonstrated an output voltage $U_o = 9.13$ V and output power $P_o = 16.7$ W, which closely matched the theoretical values.

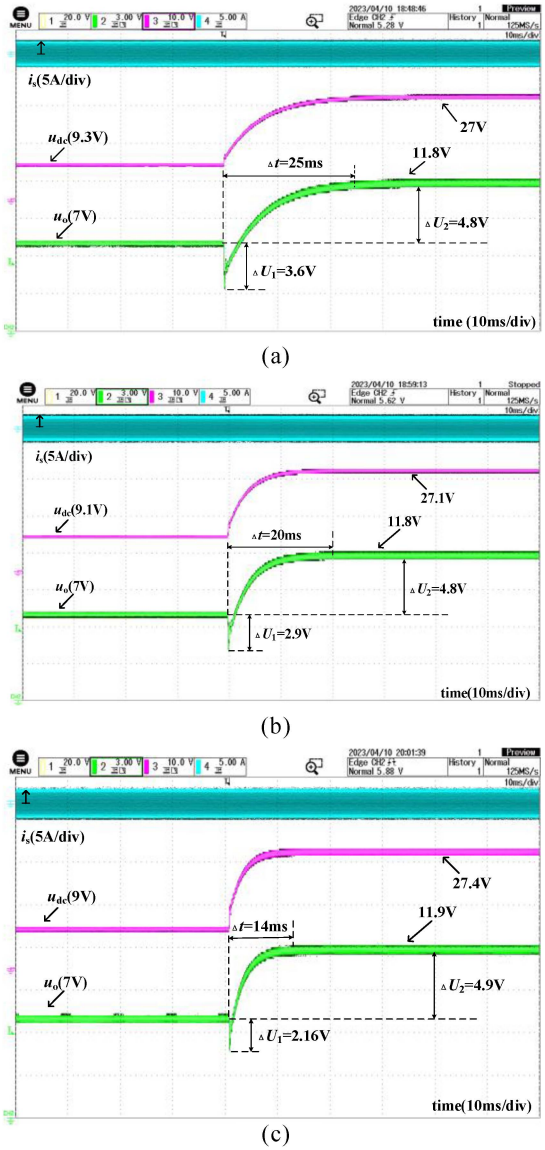

Fig. 10. Step response for different input capacitance values. (a) $C_{\rm dc}$ = 220 μF. (b) $C_{\rm dc}$ = 100 μF. (c) $C_{\rm dc}$ = 50 μF.

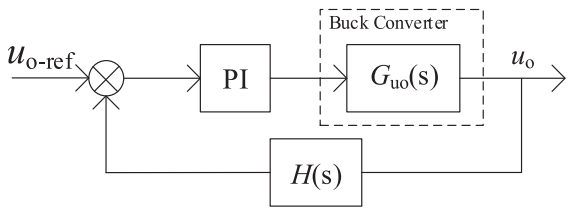

Fig. 11. Block diagram of the closed-loop control of u_o.

Fig. 13(b) illustrates the critical state operation of the buck converter when $C_{\rm dc}$ was set to 76 nF (equal to $C_{\rm dc\text{-}min}$). The system maintained stability with $U_{\rm dc}$ = 11.4 V, a voltage difference of ΔU = 22 V, and $\Delta U_{\rm dc}$ approximately equal to $2U_{\rm dc}$. The actual test results yielded an output voltage U_o = 9.07 V and output power P_o = 16.5 W.

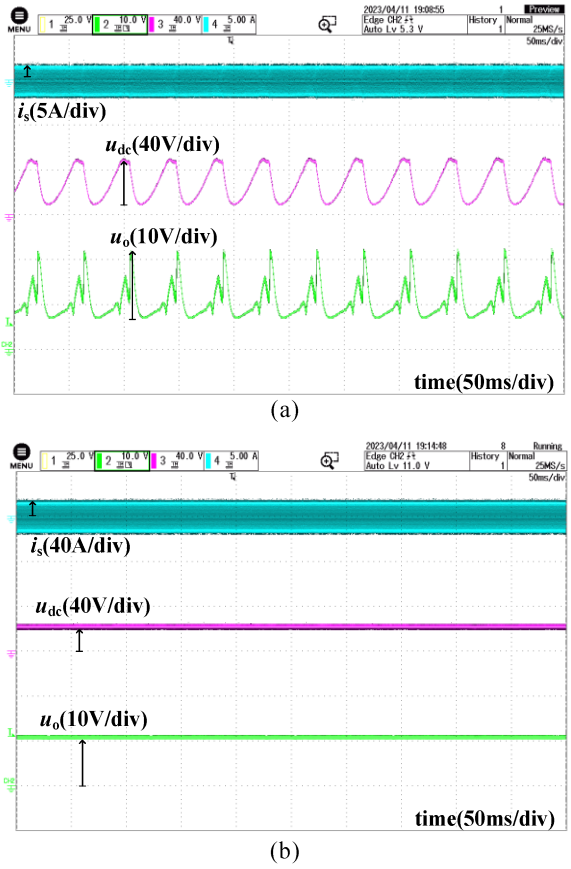

Fig. 12. Stability demonstration at different input capacitance values. (a) $C_{\rm dc}$ = 220 μF. (b) $C_{\rm dc}$ = 50 μF.

Furthermore, Fig. 13(c) demonstrates the case of $C_{\rm dc}$ = 33 nF ($< C_{\rm dc\text{-}min}$, where $C_{\rm dc\text{-}min1} < C_{\rm dc} < C_{\rm dc\text{-}min2}$). To mitigate the risk of device damage resulting from the abnormal operation of the buck converter, the specified output voltage U_o was adjusted to 7 V. Fig. 13(c) also reveals that when the switch S was turned ON, $C_{\rm dc}$ was unable to fully absorb the energy transmitted by I_r, leading to a high amplitude of I_r. The remaining energy was transferred to the load when the switch S was turned OFF, resulting in a high output voltage U_o = 8.5 V. Consequently, the buck converter entered an abnormal operating state. During this time, $U_{\rm dc}$ = 11.2 V and $\Delta U_{\rm dc}$ = 23.8 V.

Fig. 14 illustrates the transient performance of two different cases: $C_{\rm dc} > C_{\rm dc\text{-}min}$ (220 μF) and $C_{\rm dc} = C_{\rm dc\text{-}min}$ (76 nF). During the experiment, the specified output voltage was changed from 9 to 11 V. With $C_{\rm dc} > C_{\rm dc\text{-}min}$ (220 μF), a negative overshoot voltage of 0.54 V and an adjustment time of 40 ms were observed. However, when $C_{\rm dc}$ decreased to the critical value of $C_{\rm dc\text{-}min}$ (76 nF), the negative overshoot phenomenon vanished, and the adjustment time was reduced to 8 ms.

C. *Efficiency and Output Characteristics*

When using a small dc capacitor, voltage ripples tend to be high, and the conduction loss on the ESR of an aluminum

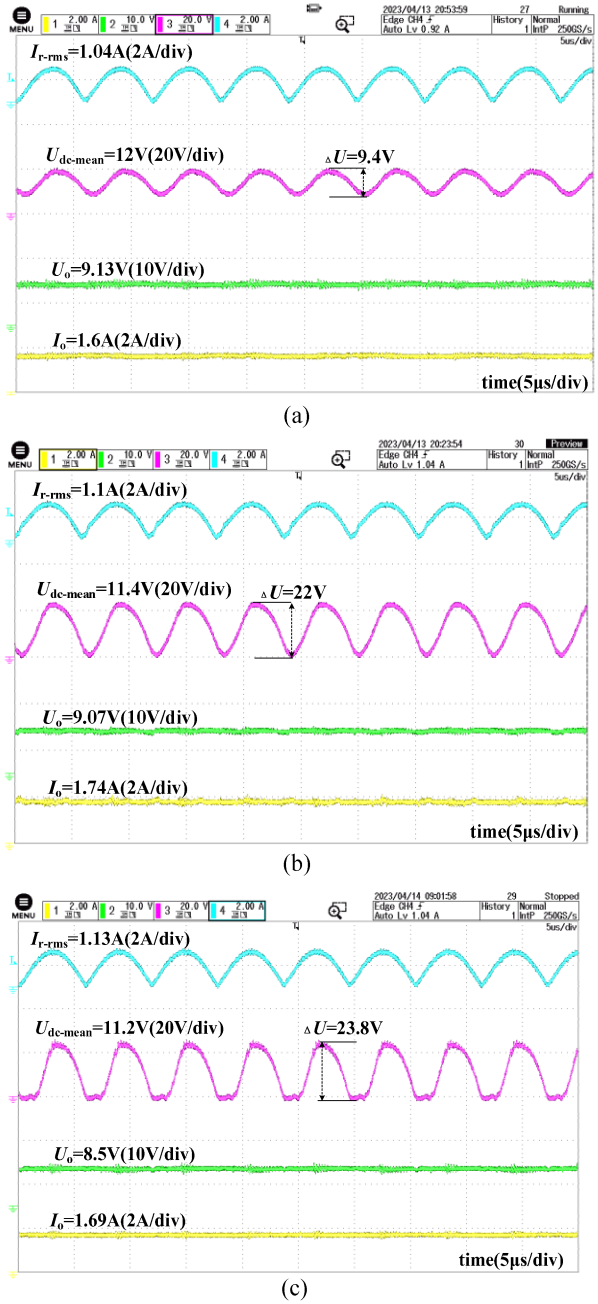

Fig. 13. Circuit operating states at different input capacitance values. (a) $C_{\rm dc}$ = 220 nF. (b) $C_{\rm dc}$ = 76 nF. (c) $C_{\rm dc}$ = 33 nF.

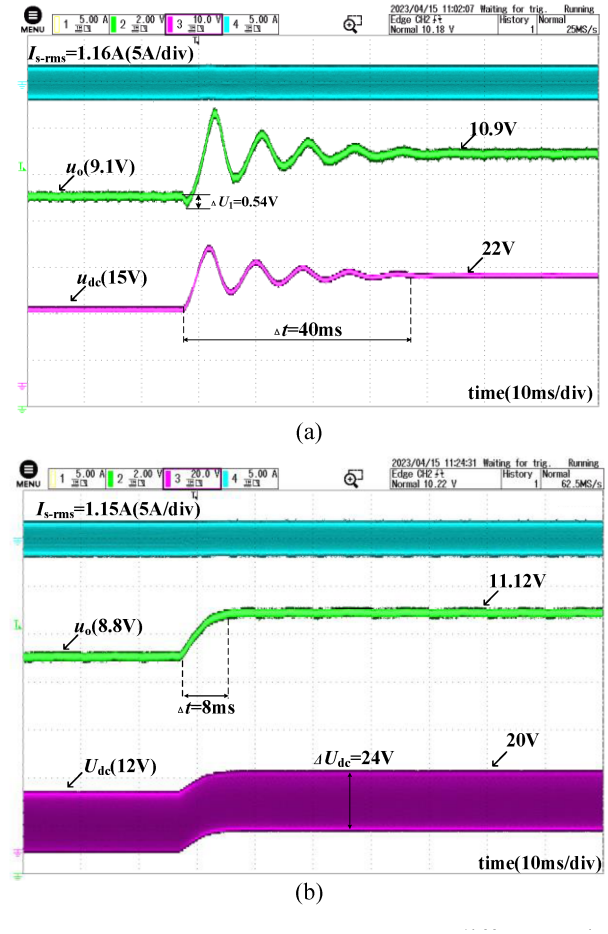

Fig. 14. Transient performance at different input capacitance values. (a) $C_{\rm dc}$ = 220 μF. (b) $C_{\rm dc}$ = 76 nF.

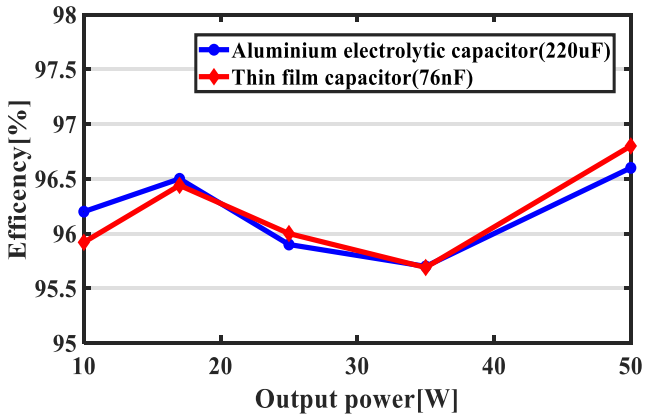

Fig. 15. Efficiency of the buck converter with different input capacitors.

electrolytic capacitor increases. However, for critical capacitance values, low ESR thin film capacitors can be utilized. To evaluate the efficiency of the buck converter under different power levels, two input capacitors were compared: a 220 μF aluminum electrolytic capacitor and a 76 nF thin film capacitor.

Fig. 15 displays the efficiency of the buck converter as the output power ranges from 10 to 50 W. The converter achieves an efficiency of approximately 96%. Notably, replacing the larger aluminum electrolytic capacitor with a critical thin film capacitor causes a change in efficiency of no more than 0.5%. In fact, at certain power points, the efficiency of the thin film capacitor surpasses that of the aluminum electrolytic capacitor.

Fig. 16 illustrates the impact of the input capacitance $C_{\rm dc}$ on the output power and output voltage ripple at U_o = 14 V. It is evident that even with a decrease in $C_{\rm dc}$, the output power and output voltage ripple of the system remain largely unaffected.

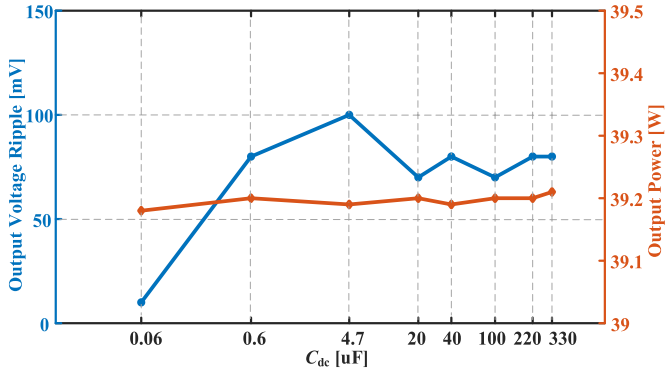

Fig. 16. Output voltage ripple and output power at different input capacitance values.

VI. Conclusion

In this work, the control-to-output transfer function of the buck converter was established under the condition that the resonant network of the receiver exhibited current-source characteristics. Furthermore, the formation and influence mechanism of RHP zero were analyzed. It was observed that the value of the input capacitor $C_{\rm dc}$ had a significant impact on the system's transient performance and stability. To mitigate the RHP zero phenomenon, a practical and convenient approach was proposed, reducing the input capacitor $C_{\rm dc}$. Additionally, by employing a thin film capacitor with enhanced resistance against high-frequency noise and a longer lifespan, the reliability of the system could be improved when utilizing smaller capacitances. A minimum critical capacitance value was derived. Experimental results demonstrated that reducing the input capacitance $C_{\rm dc}$ effectively minimized system overdrive and response time while enhancing system stability.

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