Non-Isolated PFC SEPIC Rectifier in IPOP Connection With Current Self-Sharing Capability

Jessika Melo de Andrade, William de Jesus Kremes, Carlos Henrique Illa Font, *Member, IEEE*, and Telles Brunelli Lazzarin, *Senior Member, IEEE*

***Abstract*—This article proposes a method for increasing the nonisolated rectifiers' power capability by adding more modules in parallel without the drawback of increasing current control complexity. The article applies the method to conceive a SEPIC rectifier from input- and output-parallel connection (IPOP) of modular nonisolated conventional SEPIC rectifiers in discontinuous conduction mode (DCM) operating. The main attribute of the proposed structure is to provide a current self-sharing capability in IPOP connection, with no extra current control. The current-balancing mechanism approaches herein for the SEPIC topology are applicable to all nonisolated rectifiers. The static and dynamic analyses are presented in the article, as well as the output characteristic analysis to show the self-sharing capability when the rectifier operates in DCM. A single voltage-control system is proposed for the modular connection, and there is no need for output-current control per module to guarantee a balanced power and input-current control to guarantee a high-power factor. A 1500 W prototype with three modules is designed, built, and tested in the laboratory to verify the theoretical analysis. The peak of efficiency was 93%, and the input current harmonic distortion was 2.85%, leading to a power factor of 0.999.**

***Index Terms*—Current self-sharing, IPOP connection, PFC rectifier, SEPIC rectifier.**

I. Introduction

SUSTAINABLE solutions and new methods of generating and processing energy have been motivating high demand for new solutions in power electronics [1], [2], [3], [4]. One of the demands is the increase in the current and voltage efforts of the converters, which has required new semiconductor solutions, topologies, and configurations.

The three main ways to overcome these challenges can be highlighted: development of new semiconductor technologies, which generally implies a higher cost and more significant switching losses [5]; series- and parallel-connection of semiconductors aiming to increase the capability of conventional topologies [6], this possibility requires strategies to guarantee the equalization of the voltage or current among switches during the blocking step and special care is also required during switching, as delays in command signals and parametric differences among the switches can cause unbalanced voltage or current spikes, which are harmful to the converter operation [6]; and development of new structures/topologies using conventional semiconductors [5], [6], [7], [8], [9], [10], [11], [12].

Among the new topologies that use conventional semiconductors, it should be highlighted the modular converters. This technique connects the input and output ports of two or more modules that are part of the power stage of the converter. Each module is composed of a converter and either voltage or current stress in the components divides proportionally to the number of modules [13]. The four types of modular converter connections well knowing in the literature are defined as follows: input series—output series [14], input series—output parallel (ISOP) [15], input parallel—output series (IPOS) [16] and input parallel—output parallel (IPOP) [13], [17]. These connection types are often used for dc–dc converters [17].

The advantages of the modular systems are [10], [18]: possibility of redundancy (in the event of a failure in one of the modules, there is the possibility of sharing the processed power among the other modules); design simplicity; expandable to n modules; the association of the same power modules allows standardizing components (reducing time and cost of production of the converter); and allows achieving optimal levels of efficiency.

Despite the advantages, modularity also brings some challenges for proper operation [10]. The main challenge is ensuring a balanced power division among the modules. In series connections, balance is ensured by the proper distribution of voltage among the modules. In parallel connections, the power balance is performed ensuring the sharing current among the converters.

In the literature, several methodologies are presented to carry out power sharing among modules; however, existing studies are applied only to isolated or dc–dc converters [14], [19], [20], [21]. When it comes to rectifiers, the literature approaches just a few solutions based on modular rectifiers, and, all of them, are isolated topologies [22], [23], [24].

In addition, such methodologies bring some complexity and increase the cost of the system. An alternative is the self-sharing inherent in some topologies, depending on the operating mode. With the self-sharing mechanism, the system can find a

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stable operating point even with parametric variations among the modules. In this way, it is possible to send a single common command signal to all the switches. This characteristic makes the strategy more attractive than the use of multiple control loops. However, this automatic distribution is not seen in all topologies and may also depend on the system's operation mode. Therefore, auto-sharing needs to be carefully evaluated to be used as a load-sharing strategy among modules [25], [26], [27].

It is essential to highlight that, usually, rectifiers are not designed in a modular way and as the power increases, it is necessary to search for the best topology, and often the entire converter design changes.

In this scenario, the article proposes a modular and simple solution operating in discontinuous conduction mode (DCM), which can increase the power of single-phase rectifiers, when necessary, connecting more modules in parallel and using a standard project. Thus, one module can be designed and replicated n times to increase the power of the rectifier by n without worrying about current control (self-sharing of the current). There is no maximum number of modules, since each module will process power that is not very high and the increase in power will be due to the number of modules used. The proposed topology is the unique solution in the literature to nonisolated rectifiers and the unique one that presents the characteristic of self-balance of the currents.

SEPIC rectifier operating in DCM presents advantages that make it attractive for several applications, such as it is less bulky compared to converters in continuous conduction mode (CCM), it operates as an input voltage follower, it does not need a control loop to guarantee the high-power factor, the SEPIC input current does not contain a third harmonic component, the topology allows easy isolation between input and output and it operates as a step-down or step-up converter [28]. As a drawback, it presents level power limitations due to losses in DCM and it is a nonisolated topology (but there are isolated versions). To take advantage of operating in DCM and overcome this disadvantage, it was proposed to use converters in parallel, making a module operate in the region of maximum efficiency and adding modules in IPOP connection, increasing the power of the system, and maintaining high efficiency for higher power levels. This solution can be advantageous in scalable systems such as UPSs, switched-mode power supplies, and standard voltages like 24 or 48 V.

In this article, is proposed a SEPIC rectifier, however, the technique is generic for any single-phase nonisolated and isolated rectifier operating in DCM, for example bridgeless [29] and high gain (hybrid) [30] SEPIC rectifiers. The converters are used in modular structures, maintaining their inner characteristics, such as dividing or multiplying a voltage without increasing the voltage stress across the semiconductors.

The rest of this article is organized as follows. The static analysis of the SEPIC rectifier operating in DCM, as well as the mechanism for self-sharing currents are presented in Section II. Posteriorly, in Section III, the dynamic model of the rectifier is exhibited. The comparison analysis is presented in Section IV. In Section V, the results to validate the theoretical analyzes. Finally, Section VI concludes the article.

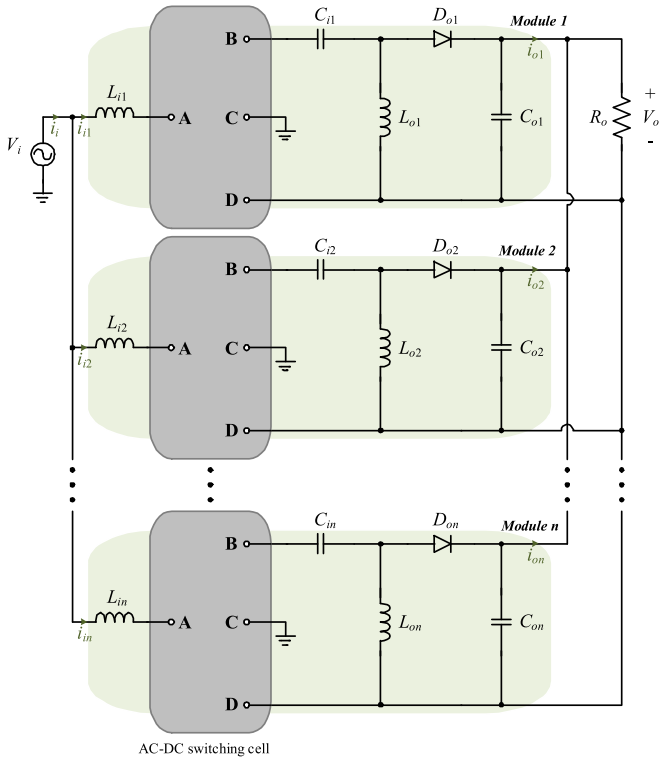

Fig. 1. SEPIC rectifier with IPOP modular connection.

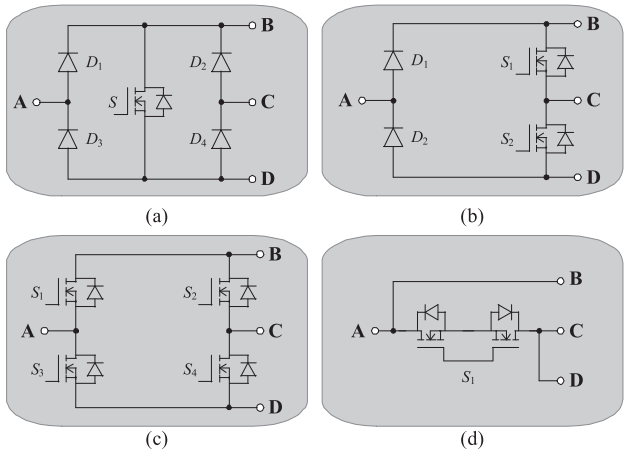

Fig. 2. Switching cells. (a) One controlled switch. (b) Two controlled switches. (c) Four controlled switches. (d) One bidirectional controlled switch.

II. SEPIC Rectifier With IPOP Modular Connection

This section approaches the SEPIC rectifier with IPOP modular connection (see Fig. 1). A generic ac–dc switching cell is illustrated in Fig. 1, which can be implemented using one of the cells shown in Fig. 2. On choosing the switching cell with a smaller number of controlled switches, the resulted topology is depicted in Fig. 3.

Due to the self-sharing current mechanism herein proposed (detailed in item *C*), it is possible to send the same command signal to all switches.

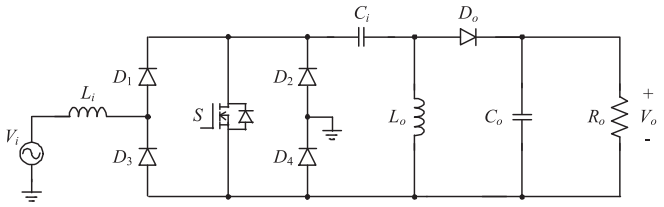

Fig. 3. SEPIC rectifier with one controlled switch.

A. Input and Output Currents

The root mean square (rms) value of the input currents of each module, in relation of peak value of input voltage (V_p), duty cycle of each module (D_1, D_2, and D_n), switching frequency (f_s), is given by [30] and [31]

$$\begin{aligned} I_{i\_\mathrm{rms}_1} &= \frac{D_1 V_p}{24 V_o L_{i_1} L_{o_1} f_s}\sqrt{6D_1\begin{bmatrix}12V_o^2 L_{i_1} D_1 (L_{i_1}+2L_{o_1})\\ +L_{o_1}^2\left(16V_o^2-9V_p^2 D_1^2\right)\end{bmatrix}}\\ I_{i\_\mathrm{rms}_2} &= \frac{D_2 V_p}{24 V_o L_{i_2} L_{o_2} f_s}\sqrt{6D_2\begin{bmatrix}12V_o^2 L_{i_2} D_2 (L_{i_2}+2L_{o_2})\\ +L_{o_2}^2\left(16V_o^2-9V_p^2 D_2^2\right)\end{bmatrix}}\\ &\vdots\\ I_{i\_\mathrm{rms}_n} &= \frac{D_n V_p}{24 V_o L_{i_n} L_{o_n} f_s}\sqrt{6D_n\begin{bmatrix}12V_o^2 L_{i_n} D_n (L_{i_n}+2L_{o_n})\\ +L_{o_n}^2\left(16V_o^2-9V_p^2 D_n^2\right)\end{bmatrix}} \end{aligned} \quad (1)$$

The output current average values of each module are defined by

$$\begin{aligned} I_{o_1} &= \frac{D_1^2 V_p^2}{4V_o L_{\mathrm{eq}_1} f_s}\\ I_{o_2} &= \frac{D_2^2 V_p^2}{4V_o L_{\mathrm{eq}_2} f_s},\\ &\vdots\\ I_{o_n} &= \frac{D_n^2 V_p^2}{4V_o L_{\mathrm{eq}_n} f_s} \end{aligned} \quad (2)$$

where

$$\begin{aligned} L_{\mathrm{eq}_1} &= \frac{L_{i_1} L_{o_1}}{L_{i_1}+L_{o_1}}\\ L_{\mathrm{eq}_2} &= \frac{L_{i_2} L_{o_2}}{L_{i_2}+L_{o_2}}\\ &\vdots\\ L_{\mathrm{eq}_n} &= \frac{L_{i_n} L_{o_n}}{L_{i_n}+L_{o_n}} \end{aligned} \quad (3)$$

B. Static Gain

From the analysis of expression (2), the static gain of each module is given by

$$\begin{aligned} G_{\mathrm{DCM}_1} &= \frac{V_o}{V_p} = \frac{D_1^2 V_p}{4I_{o_1} L_{\mathrm{eq}_1} f_s}\\ G_{\mathrm{DCM}_2} &= \frac{V_o}{V_p} = \frac{D_2^2 V_p}{4I_{o_2} L_{\mathrm{eq}_2} f_s}\\ &\vdots\\ G_{\mathrm{DCM}_n} &= \frac{V_o}{V_p} = \frac{D_n^2 V_p}{4I_{o_n} L_{\mathrm{eq}_n} f_s} \end{aligned} \quad (4)$$

The equations in (4) can be rewritten as

$$\begin{aligned} G_{\mathrm{DCM}_1} &= D_1\sqrt{\frac{R_1}{4L_{\mathrm{eq}_1} f_s}}\\ G_{\mathrm{DCM}_2} &= D_2\sqrt{\frac{R_2}{4L_{\mathrm{eq}_2} f_s}}\\ &\vdots\\ G_{\mathrm{DCM}_n} &= D_n\sqrt{\frac{R_n}{4L_{\mathrm{eq}_n} f_s}} \end{aligned} \quad (5)$$

Rearranging the expressions in (5)

$$\begin{aligned} \frac{1}{R_1} &= \frac{D_1^2}{4G_{\mathrm{MCD}_1}^2 L_{\mathrm{eq}_1} f_s}\\ \frac{1}{R_2} &= \frac{D_2^2}{4G_{\mathrm{MCD}_2}^2 L_{\mathrm{eq}_2} f_s}\\ &\vdots\\ \frac{1}{R_n} &= \frac{D_n^2}{4G_{\mathrm{MCD}_n}^2 L_{\mathrm{eq}_n} f_s} \end{aligned} \quad (6)$$

The outputs of all modules are in parallel in the IPOP configuration and, therefore, the load resistance is the result of the parallel association of the "virtual resistances" of each module, as shown in

$$\frac{1}{R_o} = \frac{1}{R_1}+\frac{1}{R_2}+\cdots+\frac{1}{R_n}. \quad (7)$$

Substituting (6) into (7), considering the gain of all modules is equal, and, all modules work on the same switching frequency, it is obtained

$$\frac{1}{R_o} = \frac{1}{4G_{\mathrm{DCM}}^2 f_s}\left(\frac{D_1^2}{L_{\mathrm{eq}_1}}+\frac{D_2^2}{L_{\mathrm{eq}_2}}+\cdots+\frac{D_n^2}{L_{\mathrm{eq}_n}}\right). \quad (8)$$

The equation that describes the SEPIC rectifier static gain in DCM is achieved by the isolation of the G_{DCM} variable in (8). Thus, the static gain is given by

$$G_{\mathrm{DCM}} = \frac{1}{2}\sqrt{\frac{R_o}{f_s}\left(\frac{D_1^2}{L_{\mathrm{eq}_1}}+\frac{D_2^2}{L_{\mathrm{eq}_2}}+\cdots+\frac{D_n^2}{L_{\mathrm{eq}_n}}\right)}. \quad (9)$$

C. Output Characteristic and Mechanism for Self-Sharing Currents in IPOP Connection

Rewriting the static gain in DCM given by (9), as a function of the output current of each parameterized module, as shown in (10), it is defined the parameterized output currents described by (11)

$$\begin{aligned} G_{\mathrm{MCD}_1} &= \frac{D_1^2}{4\overline{I_{o_1}}}\\ G_{\mathrm{MCD}_2} &= \frac{D_2^2}{4\overline{I_{o_2}}}\\ &\vdots\\ G_{\mathrm{MCD}_n} &= \frac{D_n^2}{4\overline{I_{o_n}}}\\ \overline{I_{o_1}} &= \frac{L_{\mathrm{eq}_1} f_s}{V_i} I_{o_1}\\ \overline{I_{o_2}} &= \frac{L_{\mathrm{eq}_2} f_s}{V_i} I_{o_2} \end{aligned} \quad (10)$$

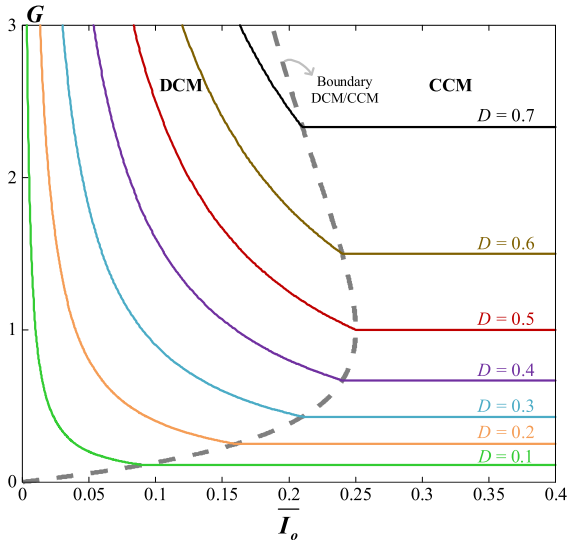

Fig. 4. Output characteristic of SEPIC rectifiers.

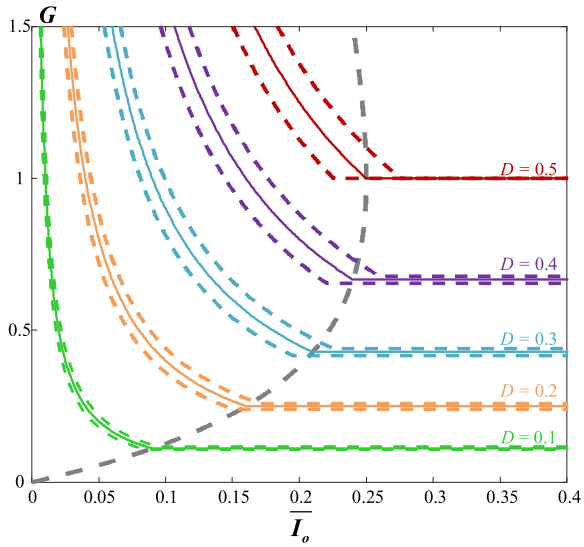

Fig. 5. Output characteristic of SEPIC rectifiers with ±5% of duty cycle variation.

$$\vdots$$

$$\overline{I_{o_n}} = \frac{L_{\mathrm{eq}_n} f_s}{V_i} I_{o_n}. \tag{11}$$

The static gain of the SEPIC topologies in the CCM is given as

$$G_{\mathrm{CCM}} = \frac{D}{1-D}. \tag{12}$$

From expressions (11) and (12), it is drawn the dc-voltage ratio (output characteristic) of the SEPIC rectifiers, as shown in Fig. 4. In the DCM region, the static gain decreases when the load output current increases. On the other hand, in CCM operation the static gain is linear regardless of the value of the output current (see Fig. 4). It should be highlighted that the gain droop behavior regarding the output current in the DCM region can be used to provide sharing of either current or voltage in parallel or series connections.

In an IPOP connection, all modules present the same input and output voltages, that is, the same static gain. Thus, (10) can be rearranged, and the equations in (13) are obtained

$$\begin{aligned} \overline{I_{o_2}} &= \left(\tfrac{D_2}{D_1}\right)^2 \overline{I_{o_1}} \\ \overline{I_{o_3}} &= \left(\tfrac{D_3}{D_1}\right)^2 \overline{I_{o_1}} \\ &\vdots \\ \overline{I_{o_n}} &= \left(\tfrac{D_n}{D_1}\right)^2 \overline{I_{o_1}} \end{aligned}. \tag{13}$$

Consideration the same duty cycle applied in all modules [in all equations in (13)], the parameterized output currents is given by

$$\begin{aligned} \overline{I_{o_2}} &= \overline{I_{o_1}} \\ \overline{I_{o_3}} &= \overline{I_{o_1}} \\ &\vdots \\ \overline{I_{o_n}} &= \overline{I_{o_1}} \end{aligned}. \tag{14}$$

Equation (14) demonstrates that all output currents will be equal, which means the IPOP connection is guaranteed for the SEPIC rectifier in DCM. Even considering small parametric variations, the self-balancing of output currents keeps the connections stable and provides an adequate current sharing. This happens due to the static gain depending on the output current. Considering parametric variations, the converter changes the output current in a small value to respect that all converters have the same voltage gain (IPOP), which keeps the system stable and ensures the self-balancing of output currents. Exemplifying this characteristic, Fig. 5 considers a duty cycle variation of ±5% in all curves from Fig. 4 and it should be highlighted that in DCM is possible to provide the same voltage gain in IPOP considering a small variation in output currents. The curve for $D = 0.3$ is detailed in Fig. 6 considering three converters in IPOP operating at $D = 0.3$, $D = 0.3 + 5\%$, and $D = 0.3$–5%. Two operation point is highlighted in Fig. 6, one of them in DCM ($G = 0.5$) and another in CCM ($G = 0.4285$).

It should be observed that, in the DCM, with the variation of D ($\Delta_D = \pm 5\%$), the same static gain is maintained ($G = 0.5$ for the three points A, A_1, and A_2) and the output current varies around 10%, due to the quadratic relation (13).

On the other hand, in the CCM, considering G = 0.4285 and $\Delta_D = \pm 5\%$, there is no common static gain to guarantee the operation in IPOP configuration and the parametric variation is enough to unbalance the output currents and to make unstable the system ($G \neq G_1 \neq G_2$, see Fig. 6).

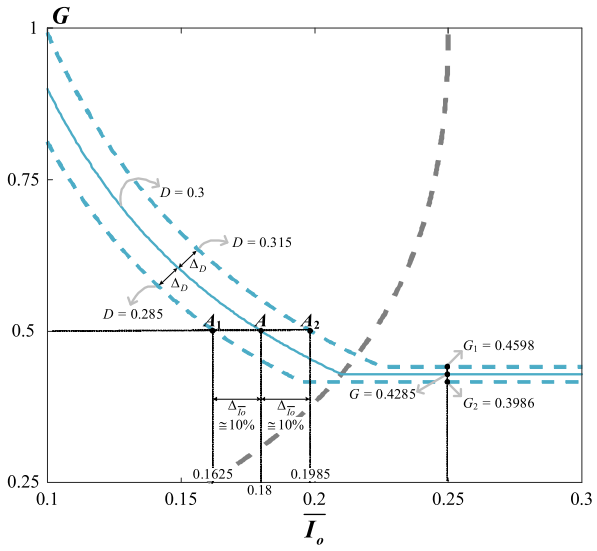

Fig. 6. Example of output characteristic of SEPIC rectifiers for $D = 0.3 \pm 5\%$.

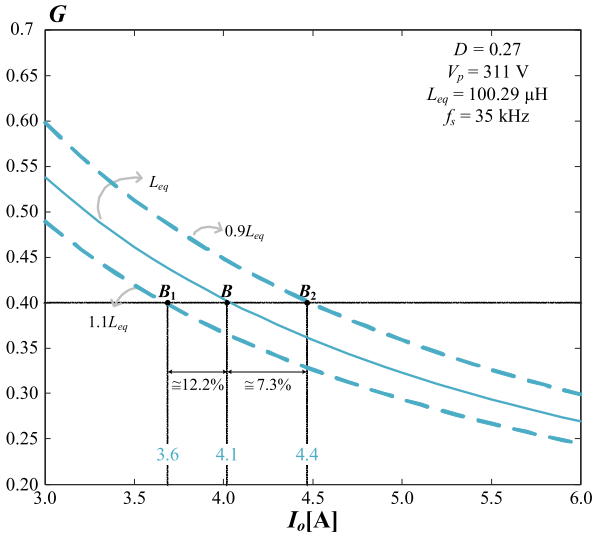

Fig. 7. Example of the inductors influency in the SEPIC static gain.

Fig. 7 shows the influency of the inductors in the static gain. It should be note that a change in inductance ($\pm 10\%$) values results in a proportional change in output current (see B_1, B, B_2 points in Fig. 7). Simulation results exhibited in Fig. 8(a) and (b) corroborate with the theory addressed in this section. The figure shows the input currents, output voltage, and the output-currents under duty cycles [see Fig. 8(a)] and inductances variation [see Fig. 8(b)]. It should be highlighted in Fig. 8(a) and (b) that the output voltage remains unchanged in both cases, and parametric variations cause a difference in the input- and output currents. In other words, parametric variations can cause unbalance in the power supplied by each module (for instance, 10% of difference among the inductance causes around 10% of unbalanced in processed power). However, the system is stable in the face of these variations and finds an operating point with a

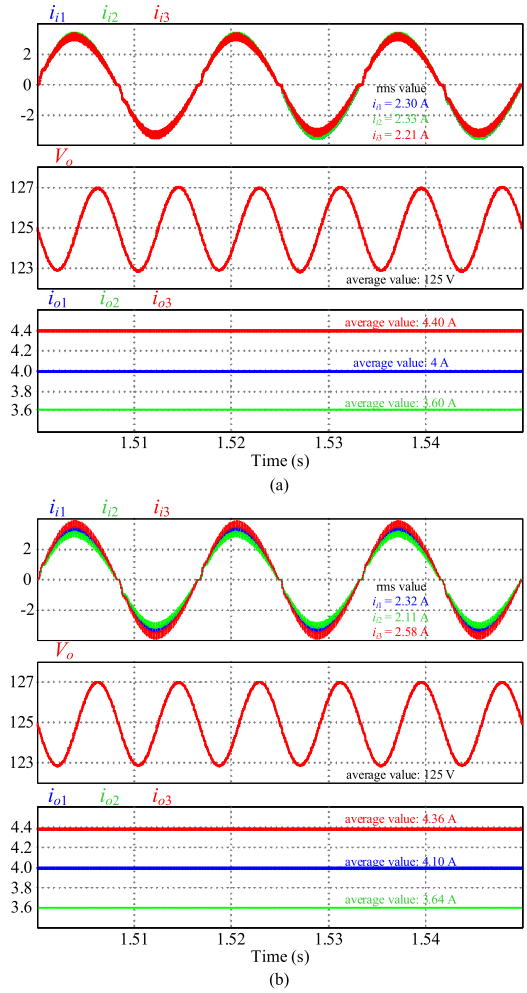

Fig. 8. Simulation results of three SEPIC rectifiers in DCM operation and IPOP connection. (a) $D_1 = D$, $D_2 = 1.1D$, $D_3 = 0.9D$ and $L_{eq1} = L_{eq2} = L_{eq3}$. (b) $D = D_1 = D_2 = D_3$ and $L_{eq1} = L_{eq}$, $L_{eq2} = 1.1L_{eq}$ and $L_{eq3} = 0.9L_{eq}$. Parameters used in the simulation are in Table II.

current balance proportional to the parametric variations (a self-balance mechanism). Thus, the system has to support variations of currents (and power) close to parametric variation accepted in its components.

It should be also highlighted that rectifiers in DCM operation work on a constant duty cycle, then the theory herein discussed can be applied to rectifiers. Based on that characteristic and (13), the nonisolated rectifiers in DCM have the capability to operate in parallel (IPOP) guaranteeing a self-balancing of output currents. In this article, this principle is verified in the SEPIC rectifier. However, theoretical analysis shows that it is valid for other nonisolated rectifiers such as buck, boost, cuk, and zeta types.

D. Components Design

Considering all the components of each module equal, the input inductors are given by

$$L_i = \frac{V_p D}{\Delta i_{Li} f_s} \tag{15}$$

where Δi_{Li} is the input inductors current ripple.

From (2), the output inductors are determined by

$$L_o = \frac{nL_iR_oV_p^2D^2}{4L_iV_o^2f_s - nR_oV_p^2D^2}. \tag{16}$$

Input and output capacitors are described by

$$C_i = \frac{D^2V_p[V_pL_oD + V_oL_i(2-D)]^2}{8V_o^2L_i^2L_o\Delta V_{Ci}f_s^2} \tag{17}$$

$$C_o = \frac{[V_p(L_i+L_o)R_oD - V_oL_iL_of_s]}{2V_oL_iL_o(L_i+L_o)R_o\Delta V_{Co}f_s^2} \tag{18}$$

where ΔV_{Ci} and ΔV_{Co} are the input- and output-capacitors voltage ripple, respectively.

The voltage and current stresses of each module components are equal to a conventional SEPIC converter, whose equations are well-established in the literature.

E. Losses and Efficiency Analysis

The losses and efficiency analysis approached in this article considered the diode, switches, and magnetic losses.

The diodes losses can be calculated by (19), where V_F is the diodes forward voltages, r_D is the parasitic resistance, I_{avg} is the average current and I_{rms} is the rms current

$$P_{\text{diodes}} = V_FI_{\text{avg}} + r_DI_{\text{rms}}^2. \tag{19}$$

The losses in the power switches can be estimated by (20), where r_S is the conduction resistance, t_f is the fall time, t_r is the rise time, I_{pk} is the peak current and V_{pk} is the peak voltage

$$P_{\text{switches}} = r_SI_{\text{rms}}^2 + \frac{f_s}{2}(t_f+t_r)I_{pk}V_{pk}. \tag{20}$$

The magnetic losses can be calculated by (21) and (22). Equation (21) is the copper losses, where N_L is the turn numbers, l_t is the average length of a turn, ρ is the conductor resistivity and $T_{\max}$ is the maximum temperature. Equation (22) is the core losses, where V_n is the core volume and Δ_B is the variation of the flux density

$$P_{Lcu} = N_Ll_t\rho I_{\text{rms}}^2[1 + 0.00393(T_{\max} - 20)] \tag{21}$$

$$P_{L\text{core}} = 16.9V_nf_s^{1.25}\left(\frac{\Delta_B}{2}\right)^{2.35}. \tag{22}$$

The theoretical total losses is given by

$$P_{\text{total}} = P_{\text{diodes}} + P_{\text{swtiches}} + P_{Lcu} + P_{L\text{core}} \tag{23}$$

and the theoretical efficiency is described by

$$n\% = \frac{P_o}{P_o + P_{\text{total}}}100\%. \tag{24}$$

III. Dynamic Modeling and Control

The self-sharing current mechanism of the SEPIC rectifier in IPOP connection and operating in DCM allows a single control system for the modular connection without needing individualized output current control per module. Due to operating as an input voltage follower, an extra input current control loop is not necessary to guarantee the power factor correction. Thus, a simple control system is proposed only for the output voltage, as depicted in Fig. 9.

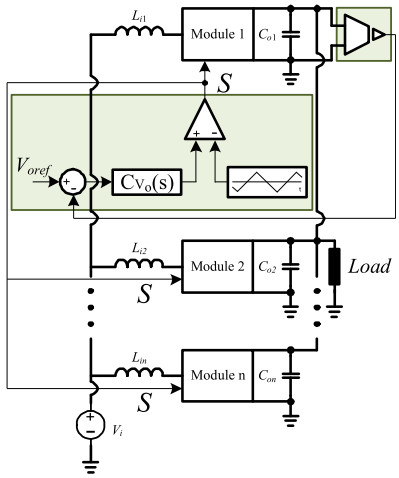

Fig. 9. System control diagram.

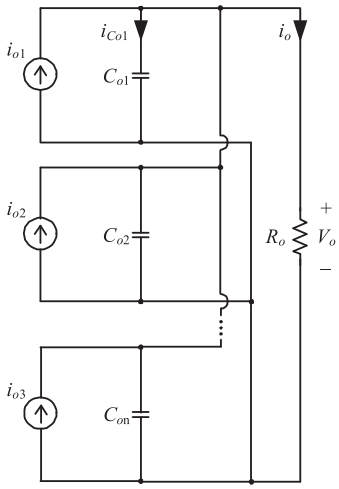

Fig. 10. Simplified model for obtaining the output voltage transfer function.

The transfer function of the output voltage per duty cycle is defined considering the simplified model (seen in Fig. 10), which uses identical parameters to all modules.

By the analysis of Fig. 10, the module 1 output current is given by

$$i_{o_1}(d, v_o) = i_{Co_1} + \frac{i_o}{n} = C_o\frac{dv_o}{dt} + \frac{v_o}{nR_o} \tag{25}$$

where n is the number of modules and C_o is the capacitance of one of the converters.

Applying the small perturbations predicted by the small-signal model in (25), it is obtained

$$\left(I_{o_1} + \hat{i}_{o_1}\right)\left(D + \hat{d}, V_o + \hat{v}_o\right) = C_o\frac{d(V_o + \hat{v}_o)}{dt} + \frac{(V_o + \hat{v}_o)}{nR_o}. \tag{26}$$

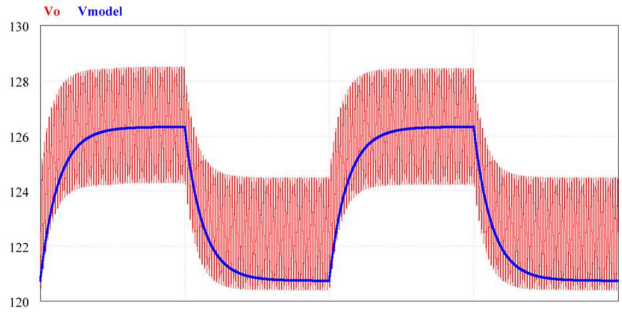

Fig. 11. Validation of the transfer function for the SEPIC rectifier with three modules in parallel.

Linearizing the expression (26), the results is given by

$$\hat{i}_{o_1}\left(\hat{d},\hat{v}_o\right) = C_o\frac{d\hat{v}_o}{dt} + \frac{\hat{v}_o}{nR_o}. \tag{27}$$

By analyzing (2), it can be seen that the output current depends on the duty cycle value and the output voltage. Therefore, the current variation for a given disturbance in the duty cycle is given in partial functions as

$$\hat{i}_{o_1}\left(\hat{d},\hat{v}_o\right) = \frac{\partial i_o}{\partial t}\hat{d} + \frac{\partial i_o}{\partial v_o}\hat{v}_o. \tag{28}$$

On substituting (2) into (28) and making the necessary operations, it is defined

$$\hat{i}_{o_1}\left(\hat{d},\hat{v}_o\right) = \frac{DV_p^2}{V_oL_{\text{eq}}f_s}\hat{d} - \frac{D^2V_p^2}{2V_o^2L_{\text{eq}}f_s}\hat{v}_o \tag{29}$$

where L_{eq} is the equivalent inductance of one of a single converter.

Equating (27) to (29) and applying the Laplace transform results in

$$\frac{DV_p^2}{V_oL_{\text{eq}}f_s}d\left(s\right) - \frac{D^2V_p^2}{2V_o^2L_{\text{eq}}f_s}v_o\left(s\right) = sC_ov_o\left(s\right) + \frac{1}{nR_o}v_o\left(s\right). \tag{30}$$

Reorganized (30), the voltage transfer function by the duty cycle of the proposed rectifier is given by

$$\frac{v_o\left(s\right)}{d\left(s\right)} = \frac{\frac{DV_p^2}{V_oL_{\text{eq}}f_s}}{C_os + \frac{D^2V_p^2}{2V_o^2L_{\text{eq}}f_s} + \frac{1}{nR_o}}. \tag{31}$$

To validate the obtained dynamical model defined in (31), a simulation was carried out in the software *PSIM*, considering the specifications of Table II. For this purpose, a small perturbation of 3% was applied on the duty cycle, to verify the output voltage behavior. The result is shown in Fig. 11, which compares the dynamic responses of the circuit (V_o) and the small signal average model (Vmodel). It should be noted that the average model satisfactorily represents the switched rectifier.

A. Control

The output voltage is regulated through a proportional-integral controller designed to comply with a phase margin (M_ϕ) of 90° and crossover frequency (f_c) of 4 Hz, described by

$$C\left(s\right) = \frac{K_C\left(s+\omega_z\right)}{s} \tag{32}$$

where K_c is the gain of the controller (equal to 0.391) and ω_z is the frequency of the zero of the controller (equal to 15.833 rad/s).

The controller was implemented in analogic and digital way, both of them shown similar and satisfactory results. In the digital way was used the digital signal processor TMS320F28027 of Texas Instruments.

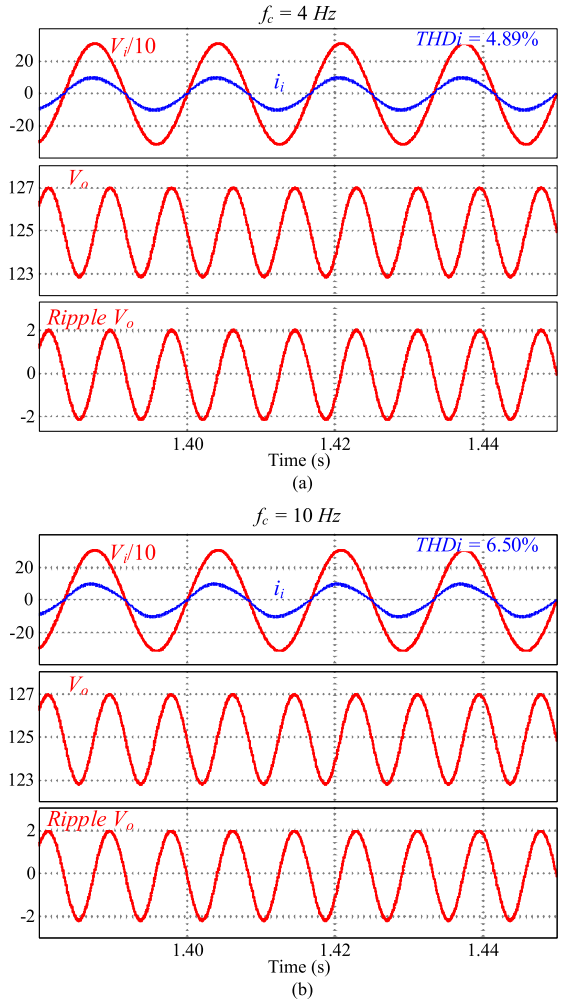

Fig. 12. Simulation results—input voltage (V_i), input current (i_i), output voltage (V_o), and output voltage ripple considering. (a) f_c = 4 Hz. (b) f_c = 10 Hz.

B. Control Influence on Output Voltage and Input Current

Fig. 12 presents the waveforms of the input voltage, input current, output voltage and output voltage ripple, obtained via simulation, considering the values given in Table II. The crossover frequency (f_c) of the controller was changed to show its influence on these variables. Fig. 12(a) is for f_c = 4 Hz and Fig. 12(b) for f_c = 10 Hz.

TABLE I
COMPARISON ANALYSIS

Converters	Isolated or nonisolated	Modulation	Modular connection type	Techniques to balance the modules
Proposed	Nonisolated	PWM[1]	IPOP	Self-balance
Chaudhary et al. [22]	Isolated	Control based	ISOP	Control techniques
Fang et al. [23]	Isolated	CBM[2]	IPOP/IPOS	Transformer
Kasper et al. [24]	Isolated	PSM[3]	ISOP	Control techniques

[1]Pulsewidth Modulation
[2]Carrier-based Modulation
[3]Phase-shifted Modulation

Observe that, the output voltage has a 120 Hz oscillation (twice the frequency of the input voltage) typical of single-phase systems. The control does not influence the output voltage ripple (f_c is less than the output voltage ripple frequency). The method to decrease it is increasing the output capacitor. Regarding the input current, a faster voltage controller increases the total harmonic distortion (THD_i) due to the third harmonic caused by the component of output voltage ripple present in the voltage loop.

IV. COMPARISON ANALYSIS

The proposed rectifier is compared to other topologies in the literature, as given in Table I. The first issue to be highlighted when the literature is checked is that the literature approaches just a few solutions based on modular rectifiers, and all of them are isolated and use control techniques to balance the currents in the modules. The proposed rectifier in this article is the unique solution in the literature to nonisolated rectifiers and the unique one that presents the characteristic of self-balance of the currents.

In [22], ISOP configuration is presented for single-phase front-end buck rectifiers. The solution is isolated, and the parallelism is based on a control technique. The work in [23] is approached modulation strategies for modular isolated rectifiers in IPOP and IPOS connections. The work in [24] is proposed multicell rectifiers for telecom using isolated dc–dc converter modules and parallelism control. The three solutions highlight how vital is the IPOP configuration for rectifiers. On the other hand, they are different solutions in relation to the proposed in this article, which shows that the proposed technique for nonisolated rectifiers is novel. Thus, some advantages and contributions of the proposed rectifier are as follows.

1) Nonisolated topology.
2) Self-balance of the currents, without extra control techniques.
3) Simpler implementation.
4) Proposal based on conventional converters.

V. EXPERIMENTAL RESULTS

The proof-of-concept prototype shown in Fig. 13 was built and tested to verify the experimental performance of the proposed rectifier with three modules in the IPOP connection. The

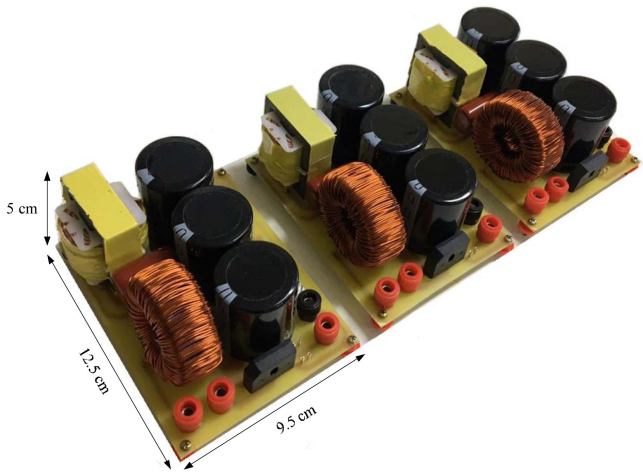

Fig. 13. Developed prototypes.

TABLE II
DESIGN SPECIFICATIONS

Parameters	Values
Duty cycles (D)	0.27
Input voltage (V_i)—rms value	220 V
AC input frequency	60 Hz
Output voltage (V_o)	125 V
Switching frequency (f_s)	35 kHz
Input inductors current ripple (Δi_{Li})	25%
Input capacitors voltage ripple (ΔV_{Ci})	10%
Output capacitors voltage ripple (ΔV_{Co})	2%
Output power (P_o)	1500 W
Number of modules (n)	3

TABLE III
PROTOTYPE COMPONENTS

Components	Specifications
Inductors L_i	6 mH Turns: 46 Wire: 21 AWG Core: APH46P60
Inductors L_o	102.25 μH Turns: 38 Wire: 32 × 32 AWG Core: EE 42/15 3C90
Capacitors C_i	EPCOS—2.2 μF / 450 V
Capacitors C_o	3 x 1500 μF / 250 V
Switches S	SCT3120AL—650 V / 21 A
Diodes D_o	R1560PF2—600 V / 15 A

specifications and components are presented in Tables II and III.

Input voltage (v_i) and input current (i_i) are shown in Fig. 14. The input current is in phase with the input voltage, characterizing the high-power factor. The harmonic distortion of the input current is 2.85% and the power factor is about 0.999.

Fig. 15 exhibits the total input current (i_i) and the input current of each module (i_{i1}, i_{i2}, i_{i3}). The total input current corresponds to the sum of the currents i_{i1}, i_{i2}, and i_{i3}.

In Fig. 15(a) the currents i_{i1}, i_{i2}, i_{i3} are overlapping and present rms value of 2.59, 2.50, and 2.57 A, which corroborate

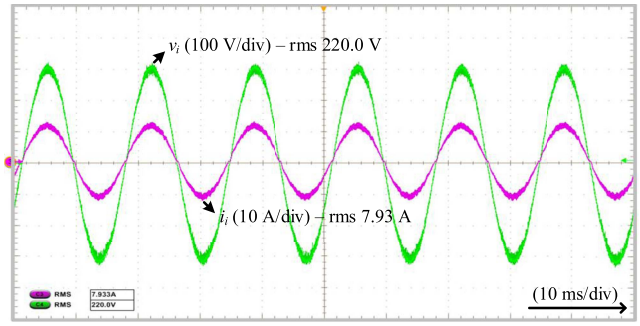

Fig. 14. Experimental results: input voltage (v_i) and input current (i_i).

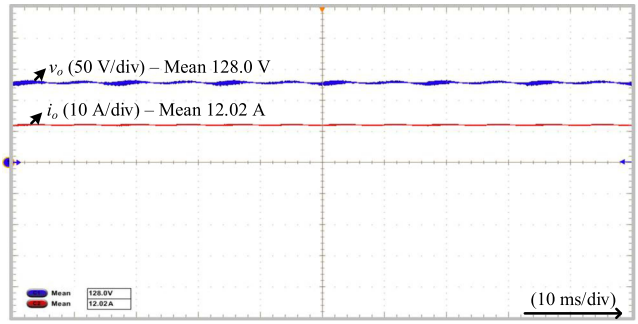

Fig. 16. Experimental results: output voltage (v_o) and output current (i_o).

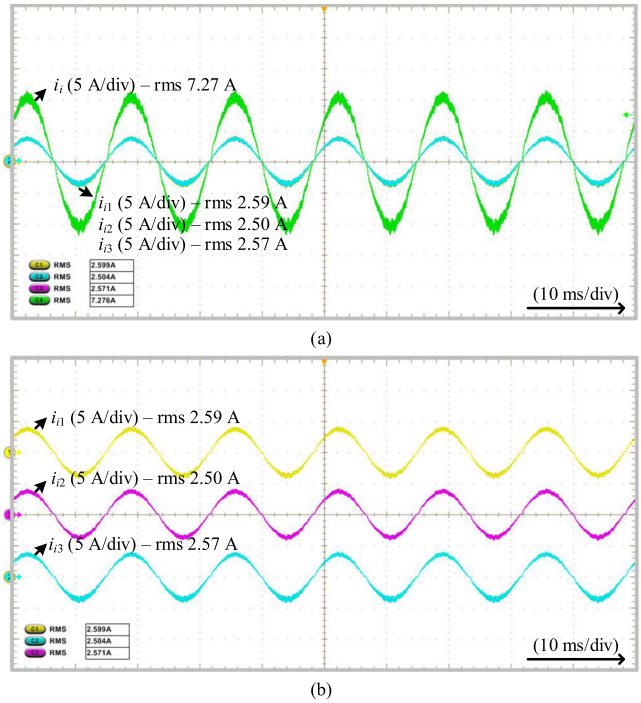

Fig. 15. Experimental results. (a) Input current (i_i) and input current of each module (i_{i1}, i_{i2}, i_{i3}). (b) Input current of each module (i_{i1}, i_{i2}, i_{i3}).

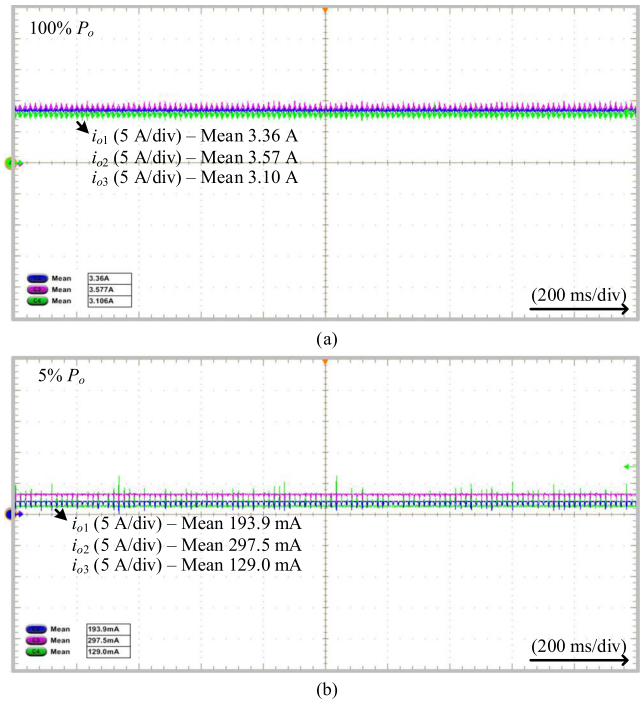

Fig. 17. Experimental results – output current of each module (i_{o1}, i_{o2}, i_{o3}): (a) in rated power and (b) in 5% of rated power.

with the self-sharing analysis since it presents a minimal unbalance in the power distribution among the modules. In Fig. 15(b), the input currents of each module are presented on different axes in order to enable the visualization of the sinusoidal and phased format of all of them.

Output voltage (v_o) and output current (i_o) are shown in Fig. 16. The average values are 125 V and 12 A, resulting in 1500 W as designed. The output ripple seen in Fig. 15 is due to the 120 Hz (twice the ac input frequency) oscillating power, which is typical of every single-phase system.

Outut currents (i_o) at rated power (1500 W) and at 5% of rated power (75 W) are depicted in Fig. 17(a) and (b), respectively. These results verify the self-sharing in all range of the system operation, and all modules deliver similar power to the load. The difference between currents at low load may be related to equipment measurement/calibration errors, since their values are very low.

Power imbalance at low load is not a problem for the converters in terms of overload, as it would not damage the converter since the power is well below at the rated power. The important thing is for the system to remain statically stable. In an evolution of the prototype, one of the modules, in situations of low load, could be disconnected, seeking a better operating point for the converters (similar as seen in Fig. 19). As long as the converters operate in DCM, the currents will naturally self-sharing.

In Fig. 18(a) and (b) are show the output voltage (v_o) and the input current (i_i) during a load step from 50% to 100% of P_o and vice versa. Overshoot (MP) and settling time are highlighted in the figures. In both cases, after the load step, the output voltage follows the voltage reference and these results validated the output voltage control strategy.

A test with turn OFF of one of the modules was performed and the result is shown in Fig. 19(a). Initially, the three modules

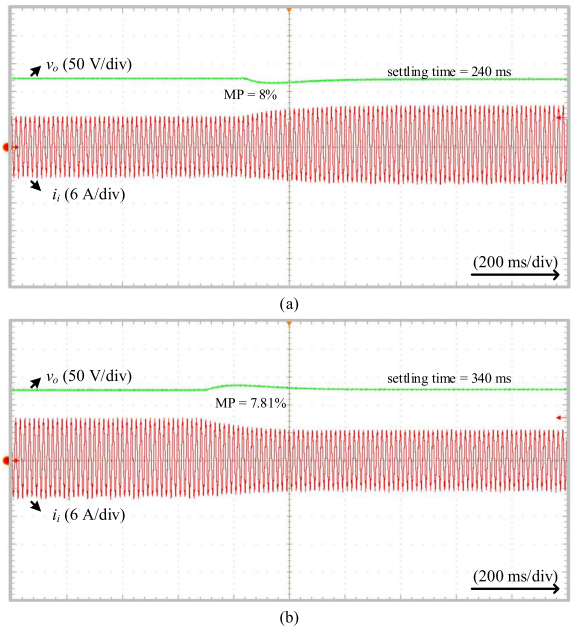

Fig. 18. Experimental results—output voltage (v_o) and input current (i_i) during a load step: (a) 50% P_o to 100% P_o and (b) 100% P_o to 50% P_o.

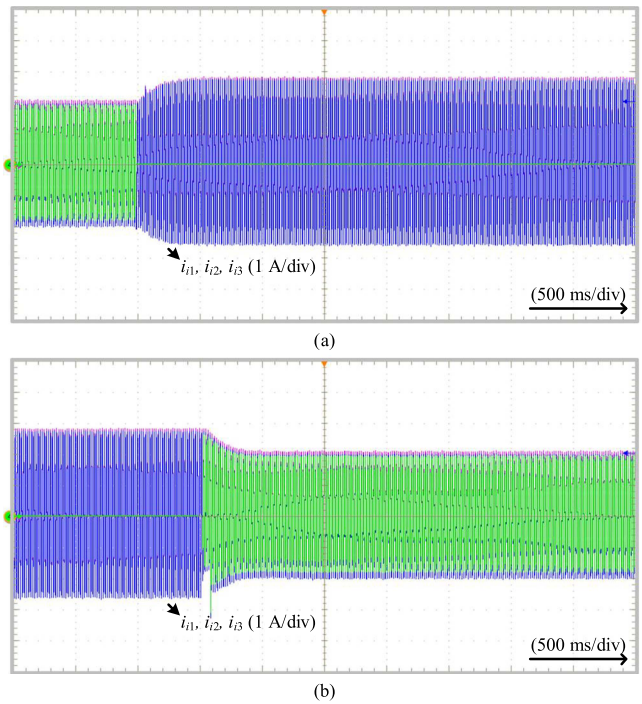

Fig. 19. Experimental results—input current of each module (i_{i1}, i_{i2}, i_{i3}) with. (a) Turn OFF of one module. (b) Turn ON of one module.

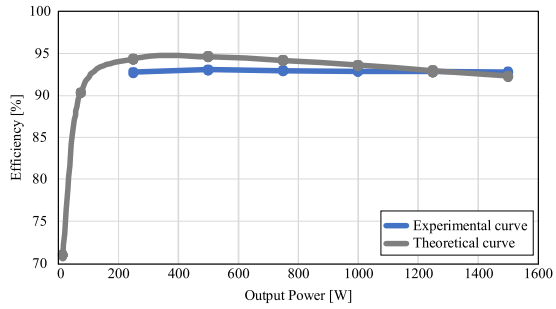

Fig. 20. Experimental and theoretical efficiency curve for all range os power.

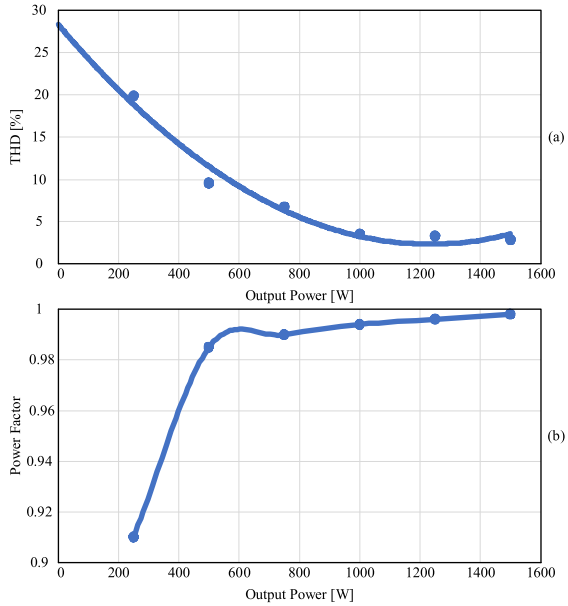

Fig. 21. Experimental points and trend curve. (a) THD e. (b) Power factor.

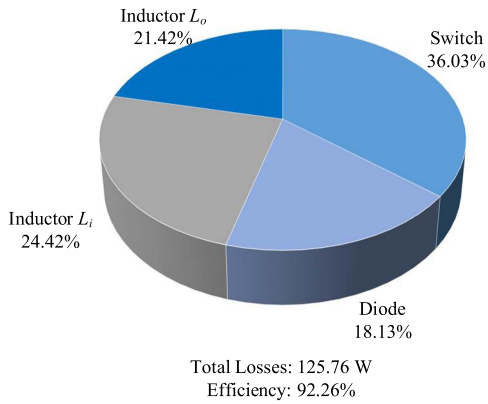

Fig. 22. Theoretical distribution of losses at rated power per component.

are operating, each one with 2/3 of rated power (total system processes 1000 W).

After a period of time, one of the modules is turned OFF and, at this moment, the other two modules remain in operation, looking for a new stable operating point. From that moment, the two active modules start to process 100% of the rated power. Thus, the system keeps processing 1000 W, as at the beginning of the operation. The results show the system self-sharing, in order to find a new stable operating point.

After a period of time, one of the modules is turned OFF and, at this moment, the other two modules remain in operation, looking for a new stable operating point. From that moment, the two active modules start to process 100% of the rated power. Thus, the system keeps processing 1000 W, as at the beginning of the

operation. The results show the system self-sharing, in order to find a new stable operating point.

A second test was performed by turning ON the third module when two are initially operating at rated conditions, as exhibited in Fig. 19(b). By turning ON the third module, the system looks for a new stable operating point again, with the three modules sharing the rated power.

The experimental and theoretical efficiency curves in the function of the output power are shown in Fig. 20. The theoretical curve was obtained by equations presented in Section II. The experimental points were measumented by WT3000 Precision Power Analyzer of Yokogawa. The efficiency obtained was close to 93% for the entire operating range, with a maximum value of 93%, close to 1/3 of the rated power.

The experimental points and trend curve in the function of the output power are shown in Fig. 21(a) for THD and in Fig. 21(b) for the power factor. At rated power, the THD was 2.85%, and the power factor was 0.998.

Fig. 22 exhibits the theoretical distribution of losses at rated power per component, calculated by equations presented in Section II. It should be highlighted that the largest parcel of losses is in the inductors (45.84%).

VI. Conclusion

This article analyzed and verified the principle of self-sharing in the SEPIC rectifier with IPOP connection when operating in DCM. Rectifiers in DCM operation work on a constant duty cycle, then, based on that characteristic and (13), they operate in parallel (IPOP), even nonisolated structures, and it is guaranteed a self-balancing of output currents. In this article, this principle is verified in the SEPIC rectifier. However, it is valid for all nonisolated rectifiers.

The article brings up the possibility of increasing the power range of the nonisolated rectifiers using IPOP configuration since DCM operation is used. The solution does not harm the efficiency, uses commercial components and, mainly, and employs a simple control (only one loop to control the output voltage) regardless of number of modulers.

It should be highlighted that the DCM condition has to be guaranteed. If one of the converters fails, either a redundant structure is designed to avoid overload in each module, or the duty cycle should be saturated in a value close to the limit between DCM and CCM and thus the output voltage will decrease (the system works with saturated control, similar to open loop operation, without control of the output voltage). If there is still an overload, the system must be turned OFF.

The theoretical analysis was verified by experimental results through the 1500 W prototype composed of three modules, which corroborated the current self-balance and, consequently, the sharing power among the modules, without the need for additional control loops. In addition, the results show that the system can find a new stable operating point during unbalances (as load step, turned-OFF, and turned-ON of news modules), even with parametric variations among modules. The proposed solution is very useful in scalable systems, such as UPSs, switched-mode power supplies, and standard voltages like 24 or 48 V.

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