Low-Order Harmonic Current Suppression Method Based on Adaptive Fractional-Order Capacitor Considering Parameters Error

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***Abstract*—In a microgrid system, the current in the dc bus may contain undesired low-order harmonics when multiple converters are employed. The integer negative order capacitor has been verified to be an effective method. However, the performance of harmonic suppression may deteriorate because of the parameter error. To address the issue, this article proposes an adaptive fractional-order capacitor (FOC) based method, in which the order of the capacitor can be modulated, depending on the impedance needed to be compensated. The terminal voltage of adaptive FOC is determined by the external circuit while the current can be adjusted freely, thus, different port impedance characteristics can be performed. The method uses a capacitor as its power storage instead of a dc supply and has nondissipative components to bring no additional loss. To stabilize the internal energy of the adaptive FOC circuit and make the port current accurate, a parallel double closed-loop control is employed. And the parameter error can be calculated from the harmonic content of the bus current. The simulation and experimental results are presented to validate the feasibility of the proposed method. The proposed method opens up an avenue for expanding the application of asymmetric parameter systems.**

***Index Terms*—Active power filter (APF), fractional-order capacitor (FOC), harmonic current, parameter error.**

I. Introduction

When multiple loads are employed on the dc voltage bus, several undesirable low-order harmonic currents occur, such as second-order harmonic from single-phase inverters. Such low-order harmonic current may affect the realization of maximum power point tracking in photovoltaic applications, reduce the soft-switching range of dc–dc converter, induce loss, and so on [1], [2], [3].

To reduce the damage of such harmonics to electrical equipment, the methods of suppressing harmonics come into being. The harmonic suppression methods can be grouped into two types. The first type does not change the original circuit structure, only changes the control strategy. For example, impedance editing [4], [5], the resonant regulator [6], [7], and model predictive control [8], [9] can be utilized in the control loop of front-end converters in cascading systems. But the harmonic current transferred to the bus capacitor, causing a voltage ripple on the dc bus. The second type, as shown in Fig. 1, adds or modifies part of the circuit structure so that the system can suppress harmonic. For example, the two terminal active capacitor converter [10], [11], buck-boost branch [12], [13], symmetrical half-bridge circuit [14], [15], [16], [17], and negative-order capacitor [18], [19]. In [14], [15], [16], [17], [18], and [19], the structures, as shown in Fig. 2(a), can suppress harmonics and replace the bulk dc bus capacitor, which greatly improves the power density. The voltages of the two capacitors, u_{c1} and u_{c2}, vary symmetrically while the sum of voltages remains constant, keeping the bus voltage stable. When the parameters of the two capacitors are the same, the total power fluctuates equally to absorb the pulsating

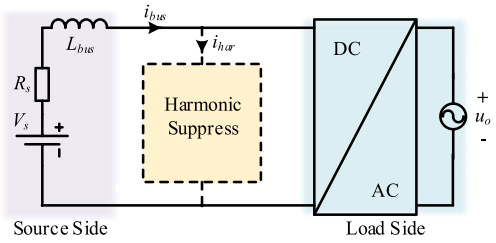

Fig. 1. Sketch view of a single-phase PWM inverter with a harmonic suppression circuit.

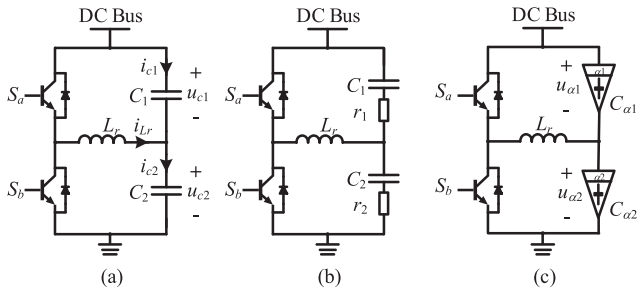

Fig. 2. Symmetric half-bridge circuit for harmonic suppression. (a) Integer-order circuit. (b) Paractical circuit with discrete element representation. (c) Paractical circuit with fractional order representation (Cx and r_x are the capacitance and ESR of $C_{\alpha x}$, respectively, x=1,2). $0<\alpha_x<1$.

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power generated by the load. However, the parameter error of the device must be controlled very precisely. And the abovementioned literature [10], [11], [12], [13], [14], [15], [16], [17], [18], [19] are all discussed under the integer order theory. But in nature, the fractional modeling of the capacitor is more practical [20], [21]. There always are equivalent series resistance (ESR) in capacitors, as shown in Fig. 2(b). Correspondingly, the phase difference between the voltage and current of the capacitor is not exactly 90°. The relationship between voltage and current is not an integer-order derivative. The fractional order of the capacitor in Fig. 2(b) is determined by its capacitance and ESR, which is uncontrollable.

The parameter error would make the performance of harmonic suppression worse. Moreover, the parameters of passive devices will offset over time due to aging. Ignoring the error in component parameters may lead to the degradation of suppression performance. While blindly selecting high-precision components greatly increases the cost. There are cases of parameter modification in various fields, such as interleaved boost converters [22], electromagnetic interference filters [23], modular multilevel converters [24], [25], [26], [27], and so on. Although these methods provide references, they cannot be directly employed to low-order harmonic suppression. Fortunately, a variable capacitor [28], [29], [30] is proposed for parametric errors. But it can only change the equivalent reactance. To obtain a larger equivalent capacitance, the capacitor voltage should be raised, which increases the voltage stress. In [16] and [17], adjusting the midpoint voltage level has also been shown to eliminate the capacitance asymmetry. But it will reduce the maximum suppressible harmonic power. Moreover, it cannot solve the asymmetries caused by ESR. So the fractional order circuit has been proposed to adjust the impedance of the port [20], [21], and [31], [32], [33], [34], like adaptive fractional order capacitors (FOC). With fractional order changing, the equivalent impedance of FOC changes. In half-bridge structures, if the capacitance and fractional order of the two capacitors are controlled to be consistent with each other, as shown in Fig. 2(c), the perfect harmonic suppression performance can be achieved. When an additional isolated power supply is employed [31], [32], the equivalent impedance can even be negative resistance. But the isolated power makes the system cumbersome. In some fractional-order circuits, capacitors are used instead of power supplies [33], [34]. However, more passive devices and sensors employed are required [34]. And the precision of the control method is still affected by the circuit parameters. Even if the sensor is error-free, the error of the equivalent impedance cannot be eliminated.

In general, the methods to compensate for parameter error have several technical issues.

1) The capacitance or resistance can only be adjusted separately.
2) The equivalent capacitance is smaller than the actual capacitors employed.
3) The error compensation of device parameters cannot avoid the sacrifice of maximum harmonic suppression capability.

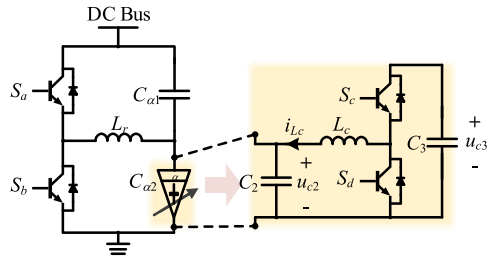

Fig. 3. Proposed adaptive fractional order circuit.

To address the abovementioned issues, this article proposes an adaptive variable parameter capacitor. Its main contribution lies in addressing the demanding requirements for device parameters in various scenarios, such as power decoupling-based harmonic suppression and multilevel converters. The circuit of the method is shown in Fig. 3. The yellow part is the place where the adaptive FOC is employed. The proposed FOC consists of two switches, a capacitor and an inductor. The fractional order can be modulated according to the capacitance and resistance needed to be compensated. It does not require an additional power supply and has nondissipative components to bring no additional loss. The proposed method does not need to measure the parameters of the two capacitors separately. The asymmetry can be calculated from the harmonic content of the bus current. To stabilize the internal energy of the fractional circuit and make the port current accurate, a parallel double closed-loop control is proposed. Its terminal voltage is determined by the external circuit, but its terminal current can be adjusted freely, thus showing different port impedance characteristics.

The rest of this article is organized as follows. Section II introduces the principle of the proposed FOC. Section III presents the simulation and experimental results of the proposed method. Finally, Section IV concludes this article.

II. Suppression Principle and FOC Operation Analysis

A. Concept of the FOC Circuit

The current-voltage relationship of a conventional integer-order model capacitor is described by first-order calculus, as

$$i_c(t) = C\frac{du_c(t)}{dt}. \tag{1}$$

While in contrast to the integer-order capacitor, the capacitor in the fractional-order model is

$$i_c(t) = C_\alpha \frac{d^\alpha}{dt^\alpha} u_c(t) \tag{2}$$

where α is the fractional order, d^α/dt^α is termed the fractional order derivative operator, and C_α is the equivalent pure capacitance value. The impedance of a fractional-order capacitor is described as

$$Z = \frac{1}{\omega^\alpha C_\alpha}\cos(0.5\pi\alpha) - j\frac{1}{\omega^\alpha C_\alpha}\sin(0.5\pi\alpha) \tag{3}$$

where ω is the operating angular frequency. When ω or α changes, the capacitance and resistance of a fractional order capacitor both change. With an additional free variable α, fractional order devices can be more flexible to adapt to different occasions.

When the order α belongs to (1), (2), there is negative resistance to generate power. When the order belongs to (0, 1), there will be positive resistance to consuming power. In the positive half plane, the fractional order capacitor presents variable capacitance with positive or negative resistance.

In the theory of integer order, the structure in Fig. 2(a) has the best harmonic suppression effect when the capacitance values are equal. However, there always are parasitical parameters in capacitors. And no capacitors can be the same. To achieve higher robustness and better harmonic suppression performance, an adaptive FOC circuit is employed. As shown in Fig. 2(c), both capacitors can be replaced by adaptive FOCs. By controlling the capacitance and fractional order α to be consistent, the parameters of $C_{\alpha 1}$ and $C_{\alpha 2}$ can be completely equal. In practice, this can be replaced with only one adaptive FOC and the other is still a regular capacitor (fractional but not controllable), as shown in Fig. 3.

In traditional fractional circuits, to show negative resistance, the circuit needs to contain an independent power supply. But the negative-order capacitor branch in Fig. 3 is special: the ac voltages on both capacitors are superimposed with dc bias and are positive at all times. Therefore, the fractional capacitor proposed in this article does not need an additional power supply to reflect the negative resistance of the ac. And only one bridge arm is required to meet the voltage modulation range. C_2 can also be directly used as the output filter capacitor of the fractional circuit. To control the output current, a fractional circuit must have an inductor at its output. To store energy, the circuit must contain an energy storage element. The power density of the capacitor is higher than that of the inductor, so the capacitor is chosen. Finally, the fractional capacitor circuit proposed in the article is shown in Fig. 3.

By controlling the capacitance and order α_2 of $C_{\alpha 2}$ to be consistent with $C_{\alpha 1}$, a stable and excellent harmonic suppression effect can be achieved.

B. Secondary Pulsating Power Decoupling Principles under Parameters Error

Taking the single-phase inverter output voltage u_o and current i_o as

$$\begin{cases} u_o = U_o \sin \omega t \\ i_o = I_o \sin(\omega t + \theta). \end{cases} \tag{4}$$

Then, the output power p_o yields

$$p_o = u_o i_o = \frac{U_o I_o}{2} \left[\cos\theta - \cos\left(2\omega t + \theta\right)\right]. \tag{5}$$

Such pulsating power contains a 2ω ac component. Considering the constant voltage characteristics of the power supply, the output current of the power supply will contain a double frequency component $i_{\text{in-2nd}}$ with a magnitude of

$$i_{\text{in-2nd}} = -\frac{U_o I_o}{2U_{\text{bus}}} \cos(2\omega t + \theta). \tag{6}$$

To suppress the pulsating power, an equivalent negative-order capacitor branch is proposed in [18] and [19], as shown in Fig. 2. Through switches S_a, S_b and inductor L_r, the fractional order of the two capacitors are modulated that one is positive and the other is negative. Assuming the order of $C_{\alpha 1}$ is positive and the voltages in circuits can be written as

$$\begin{cases} u_{\alpha 1} = 0.5U_{\text{bus}} + u_h \\ u_{\alpha 2} = 0.5U_{\text{bus}} - u_h \\ u_h = U_h \sin(\omega t + \beta) \end{cases} \tag{7}$$

where u_h is the modulation voltage, and U_h and β denotes amplitude and the phase of u_h, respectively.

When the fractional order $\alpha_1 = -\alpha_2 = 1$, it means there is no ESR in capacitors. The power of all the energy storage elements, p_{all}, in the branch is

$$p_{\text{all}} = u_{\alpha 1} \cdot C_{\alpha 1} \frac{du_{c1}}{dt} + u_{\alpha 2} \cdot C_{\alpha 2} \frac{du_{c2}}{dt} + i_{Lr} \cdot L_r \frac{di_{Lr}}{dt}. \tag{8}$$

Assuming $C_{\alpha 1} = C_{\alpha 2} = C$ and L_r is small enough, then p_{all} can be simplified as

$$p_{\text{all}} = 2Cu_h \frac{du_h}{dt} = \omega C U_h^2 \sin(2\omega t + 2\beta). \tag{9}$$

The SHC can be absorbed completely when p_{all} equals the secondary pulsating power in magnitude while opposite in phase, so

$$\begin{cases} \omega C U_h^2 = \frac{U_o I_o}{2} \\ \sin(2\omega t + 2\beta) = \cos(2\omega t + \theta). \end{cases} \tag{10}$$

So U_h and β should satisfy the following conditions:

$$\begin{cases} U_h = \sqrt{\frac{U_o I_o}{2\omega C}} \\ \beta = \frac{\pi}{4} + \frac{\theta}{2}. \end{cases} \tag{11}$$

The second harmonic current in the dc bus can be absorbed completely. However, (8)–(11) are based on the integer-order ($\alpha_1 = -\alpha_2 = 1$) and ideal occasion ($C_1 = C_2$). The integer order is only a special ideal case in the fractional order model. And two capacitors cannot be exactly equal in fact.

When parameters of $C_{\alpha 1}$ and $C_{\alpha 2}$ are different ($\alpha_1 \neq -\alpha_2 \neq 1$), there come errors in capacitance and ESR as (12) (take $C_{\alpha 1}$ for example)

$$\begin{cases} \tan\frac{\pi}{2}\alpha_1 = \frac{1}{\omega C_{\alpha 1} r_1} \\ r_1 = \frac{1}{\omega C_{\alpha 1}} \cos\frac{\pi}{2}\alpha_1 \\ \frac{1}{j\omega C_1} = \frac{1}{j\omega C_{\alpha 1}} \sin\frac{\pi}{2}\alpha_1 \end{cases} \tag{12}$$

where r_1 is the ESR of $C_{\alpha 1}$, C_1 is the pure capacitance of $C_{\alpha 1}$. And so are r_2 and C_2 to $C_{\alpha 2}$. The energy on C_1 and C_2 can suppress harmonic while the energy on r_1 and r_2 is killed.

Through (2), the voltage u_{c1} of pure capacitance C_1, the voltage u_{c2} of pure capacitance C_2, the current i_{c1} across $C_{\alpha 1}$,

and the current i_{c1} across $C_{\alpha 2}$ are expressed, respectively, as

$$u_{c1} = \frac{U_{\text{bus}}}{2} + \frac{U_h \sin(\omega t + \phi_1)}{\omega^2 C_1^2 r_1^2 + 1}, \text{where } \phi_1 = \frac{\pi}{2}(1-\alpha_1) + \theta \tag{13}$$

$$u_{c2} = \frac{U_{\text{bus}}}{2} + \frac{U_h \sin(\omega t + \phi_2)}{\omega^2 C_2^2 r_2^2 + 1}, \text{where } \phi_2 = \frac{\pi}{2}(1-\alpha_2) + \theta \tag{14}$$

$$i_{c1} = \lambda_1 \cos(\omega t + \phi_1), \lambda_1 = \frac{\omega C_1 U_h}{\omega^2 C_1^2 r_1^2 + 1} \tag{15}$$

$$i_{c2} = \lambda_2 \cos(\omega t + \phi_2), \lambda_2 = \frac{-\omega C_2 U_h}{\omega^2 C_2^2 r_2^2 + 1}. \tag{16}$$

According to Kirhhoff's current law, i_{Lr} is expressed as

$$\begin{aligned} i_{Lr} &= -\lambda_1 \cos(\omega t + \phi_1) - \lambda_2 \cos(\omega t + \phi_2) \\ &= -\lambda_3 \cos(\omega t + \phi_3) \end{aligned} \tag{17}$$

where λ_3 and ϕ_3 are the amplitude and phase of i_{Lr}, respectively, and their expressions are

$$\begin{cases} \lambda_3 = \sqrt{\lambda_1^2 + \lambda_2^2 + 2\lambda_1\lambda_2 \cos(\phi_1 - \phi_2)} \\ \phi_3 = \tan^{-1}\left(\frac{\lambda_1 \sin\phi_1 + \lambda_2 \sin\phi_2}{\lambda_1 \cos\phi_1 + \lambda_2 \cos\phi_2}\right). \end{cases} \tag{18}$$

Then, the voltage of L_r, u_{Lr}, is

$$u_{Lr} = L_r \frac{\mathrm{d}i_{Lr}}{\mathrm{d}t} = \omega L_r \lambda_3 \sin(\omega t + \phi_3). \tag{19}$$

Now the instantaneous power p_{all} of the suppression circuit is

$$\begin{cases} p_{all} = p_{c1} + p_{c2} + p_{Lr} \\ p_{c1} = u_{c1} \cdot i_{c1} + r_1 \cdot i_{c1}^2 \\ p_{c2} = u_{c2} \cdot i_{c2} + r_2 \cdot i_{c2}^2 \\ p_{Lr} = i_{Lr} \cdot u_{Lr} + i_{Lr}^2 \cdot r_{Lr}. \end{cases} \tag{20}$$

As seen from (20), p_{all} includes 3 parts: instantaneous power of $C_{\alpha 1}$, $C_{\alpha 2}$, and L_r, namely p_{c1}, p_{c2}, and p_{Lr}. p_{c1} includes two parts: 1) voltage multiplied by the current across C_1, containing components with angular frequencies ω and 2ω; 2) the consumption on ESR r_1, containing components with angular frequencies 0 (dc component) and 2ω.

Such ω component causes first-order harmonic in the bus current and the 2ω one deteriorates the performance of second-order harmonic suppression. The dc component will dissipate directly and has no further impact on the harmonic suppression effect. Then, the same goes for p_{c2} and p_{Lr}.

The abovementioned consumption of the dc component cannot be compensated without additional active power injection while the 2ω one can partially self-correct in the second-order harmonic suppression close-loop [16], [17], [19]. Therefore, the ω component which causes the first-order harmonic should be dealt with emphatically. From (15) to (20), we can get the ω component power $p_{1\text{-}\omega}$ is

$$p_{1-\omega} = \frac{V_{\text{dc}}}{2}\left[\lambda_1 \cos(\omega t + \phi_1) + \lambda_2 \cos(\omega t + \phi_2)\right]. \tag{21}$$

When this power is transmitted on the bus, the harmonic current generated by parameters error is shown in (22), which

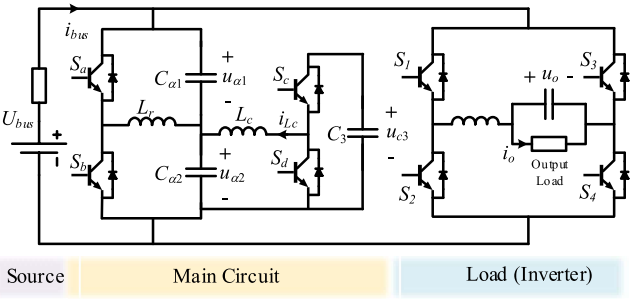

Fig. 4. Adaptive FOC-based harmonic suppression circuit.

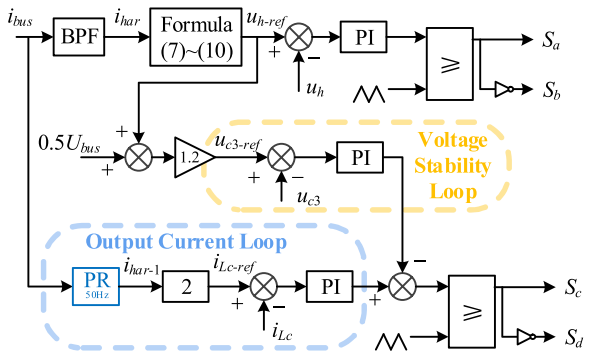

Fig. 5. Control block diagram of adaptive FOC-based method. (BPF means bandpass filter).

is exactly half the difference between i_{c1} and i_{c2}

$$\begin{aligned} I_{har-1} = \frac{p_{1-\omega}}{V_{\text{dc}}} &= \frac{1}{2}\left[\lambda_1 \cos(\omega t + \phi_1) + \lambda_2 \cos(\omega t + \phi_2)\right] \\ &= \frac{1}{2}(i_{c1} - i_{c2}). \end{aligned} \tag{22}$$

When controlling the capacitance and order α of $C_{\alpha 2}$ to be consistent with $C_{\alpha 1}$, i_{c1}, and i_{c2} should be the same (As the ac component of their voltages, u_{c1} and u_{c2}, are opposite). At this point, i_{c2} is needed to be compensated by the adaptive FOC port current i_{lc}, to control the port impedance, as shown in Fig. 4. In this way, the reference value of i_{lc} is obtained by the first-order harmonic current $I_{har\text{-}1}$ in the dc bus.

C. Control Strategy of the FOC Circuit

As the usage time increases, the parameter offset gradually occurs. There may be no reserved current sensor in the branch. And it is impractical to take down the capacitors for measurement. To address the issue, this article proposes an adaptive FOC based method, as shown in Fig. 4.

According to (22), the injection current i_{Lc} can be obtained from the first-order harmonic of the bus current. In this way, the cumbersome impedance measurement can be bypassed. And the FOC output port current i_{Lc} can be directly controlled to achieve the fractional characteristics.

To stabilize the internal energy of the fractional circuit and make the port current accurate, a parallel double closed-loop control is proposed in Fig. 5.

The output current loop is used to control the output current. Its reference value is obtained from the first-order harmonic of the dc bus current. A proportional resonator is used here to obtain the first-order harmonic.

The voltage stability loop is used to maintain the internal energy stability of the fractional circuit during a working cycle, namely, to maintain the voltage of energy storage capacitor C_3. The higher its voltage, the more energy it stores, but the voltage stress will become greater. According to the circuit structure, the voltage of C_3 must be higher than that of C_2. And it does not have to have a high value, because there may suffer a huge voltage stress. Here, the reference voltage $u_{c3\text{-}ref}$ is set to the sum of 0.6 times $U_{\rm bus}$ and 1.2 times U_h, which will be explained in Section III-A with details.

D. Parameter Design

According to (10), the rated capacitance of C_1 and C_2 are related to the harmonic power of the load p_{ohar}. So their minimum value $C_{1,2\min}$ is

$$C_{1,2\,\min} = \frac{4p_{ohar}}{\omega U_{\rm bus}^2}. \tag{23}$$

In general, the capacitance accuracy requirement for brand-new capacitors on the market is within 5% error, while 20% is the standard for aging and scrapping. So to present the error case, the capacitance deviation is set to be 20% ($C_2 = 0.8C_1$). And the undesired pulsating power caused by parameters error is essentially absorbed or released by C_3. For higher efficiency and system power density, minimum capacitance, and voltage pressure of C_3 are needed to be designed.

Through (13), (14), and (22), which capacitance is more different from the design value can be calculated. Compensating the capacitor with more errors can make the overall circuit performance closer to the design goal. Assuming the parameters of $C_{\alpha 1}$ are standard, the instantaneous change of charge Δq_1 and voltage Δu_{c1} of $C_{\alpha 1}$ can be written as

$$\Delta q_1 = \int i_{c1}{\rm d}t \tag{24}$$

$$\Delta u_{c1} = \frac{\Delta q_1}{C_1}. \tag{25}$$

Since the harmonics are suppressed, the bus voltage will not fluctuate and is a constant value, so

$$\Delta u_{c1} = -\Delta u_{c2} = U_h. \tag{26}$$

As seen in Fig. 3, the proposed FOC circuit is a kind of buck–boost converter. So the voltages of its two ports have the relationship as

$$\frac{\Delta u_{c2}}{\Delta u_{c3}} = d. \tag{27}$$

In the same way, the current of the two ports of the adaptive FOC circuit yields

$$\frac{i_{Lc}}{i_{c3}} = \frac{1}{d}. \tag{28}$$

So the change of charge Δq_3 on C_3 can be obtained as

$$\Delta q_3 = \int i_{c3}{\rm d}t = d(\Delta q_1 - \Delta q_2). \tag{29}$$

Combining (26), (27), and (29), it can be derived as

$$\Delta u_{c3} = -\frac{1}{d}\cdot\frac{\Delta q_1 - \Delta q_2}{C_1 - C_2}. \tag{30}$$

Normally, before entering the stable state, the voltage of C_3 should be raised to a certain extent value, as shown in (23). Assuming $Q_{3,init}$ is the initial charge on C_3 at the beginning. Thus, the instantaneous charge on C_3 can be written as

$$q_3 = Q_{3,init} + \Delta q_3. \tag{31}$$

Then, a quadratic equation with one variable for the duty d is obtained through $q_3 = C_3 u_{c3}$

$$d^2\cdot(\Delta q_1 - \Delta q_2) + d\cdot Q_{3,init} + C_3\frac{\Delta q_1 - \Delta q_2}{C_1 - C_2} = 0. \tag{32}$$

For the equation to be physical meaning in practice, two conditions must be satisfied: 1) the discriminant of the root is no less than 0; 2) the duty ratio d ranges from 0 to 1. Through these two conditions, two formulas can be obtained to calculate the relationship between the voltage stress, the capacitance of C_3 and the compensable range of $C_{\alpha 2}$

$$\frac{-Q_{3,init} + \sqrt{Q_{3,init}^2 - 4(\Delta q_1 - \Delta q_2)\frac{C_3}{C_1 - C_2}}}{2(\Delta q_1 - \Delta q_2)} < 1 \tag{33}$$

$$Q_{3,init}^2 - 4\Delta q_1^2\frac{C_3}{C_1} \geq 0. \tag{34}$$

Substituting (26), $Q_{3,init} = C_3 U_{3,init}$ ($U_{3,init}$ is the initial voltage on C_3 at the beginning) and $C_1 = C_2 + \Delta C$ (Assuming the parameter error of C_2 is ΔC), (33) and (34) can be written as

$$\frac{C_3}{\Delta C + C_3}U_{c3,init} \geq \Delta u_{c2} \tag{35}$$

$$\sqrt{\frac{C_3}{\Delta C}}U_{c3,init} \geq 2\Delta u_{c2}. \tag{36}$$

III. Simulation and Experimental Results

A. Simulation Results of the Adaptive FOC Circuit

To verify the feasibility of the proposed method, simulation is first performed in *Saber* software. The circuit diagram utilized in the simulation is shown in Fig. 4. The parameters are shown in Table I.

In general, the capacitance accuracy requirement for brand-new capacitors on the market is within 5% error, while 20% is the standard for aging and scrapping. So the capacitance deviation ΔC is $20\%C_1 = 30$ uF. To present the error case, let's design $C_1 = 150$ uF while $C_2 = 120$ uF. The ESRs of C_1 and C_2 are both about 0.3 Ω from 10 Hz to 100 Hz in the datasheet. To simulate the increase of ESR during capacitor aging, C_2 is in series with a 0.5 Ω resistor. Assuming initial voltage $U_{3,init}$ on C_3 at the beginning, as same as $u_{c3\text{-}ref}$ is

$$u_{c3-ref} = 120\%\,(0.5V_{\rm dc} + U_h). \tag{37}$$

TABLE I
PARAMETERS OF THE PROTOTYPE AND SPECIFICATIONS OF THE UTILIZED COMPONENT IN THE ASYMMETRIC CASE

Parameter	Value	Parameter	Value
Bus Voltage U_{bus}	350 V	Capacitor C_1	150 uF
Output Power P_o	600 W	ESR of C_1, r_1	0.3 Ω
Switching Frequency f_s	25 kHz	Order α_1	0.986
Inductor L_r	150 uH	Capacitor C_2	120 uF
Inductor L_c	400 uH	ESR of C_2, r_2	0.8 Ω
Capacitor C_3	20 uF	Order α_2	−0.967

(The ESR of the capacitor is obtained from the datasheet. To create the difference in parasitic resistance, C_2 is connected in series with a 0.5 Ω resistor.)

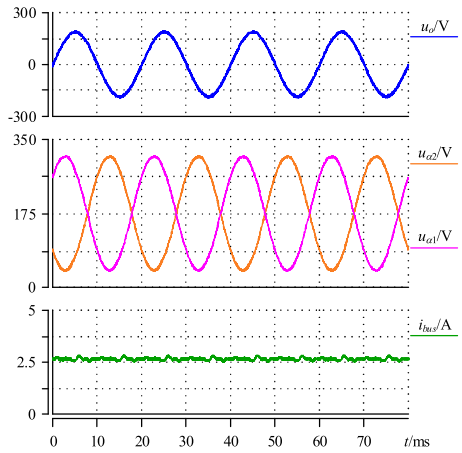

Fig. 6. Simulation results when $C_{\alpha 1}$ and $C_{\alpha 2}$ have the same parameters (C_1=C_2=150 uF, α_1=−α_2=1).

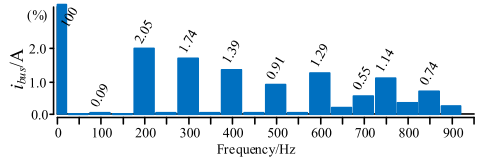

Fig. 7. Fourier analysis of $i_{\rm bus}$ when harmonic current is suppressed in simulation (C_1=C_2=150 uF, α_1=−α_2=1).

Since duty cycle cannot reach 100%, U_h must be less than half of $U_{\rm bus}$. A duty cycle range is set from 0.05 to 0.95 for the safety. So the maximum U_h and Δu_{c2} are both 0.45 $V_{\rm dc}$. According to (35) and (36), C_3 is set to 20 uF.

First, when $C_{\alpha 1}$ and $C_{\alpha 2}$ have the ideal parameters in the integer-order model ($C_1 = C_2 = 150$ uF, $\alpha_1 = -\alpha_2 = 1$), the output voltage u_o, capacitor voltage u_{c1}, u_{c2} and bus current $i_{\rm bus}$ is shown in Fig. 6. Because the parameters of the capacitor are symmetry, SHC is well suppressed and first-order harmonic current does not appear in the $i_{\rm bus}$. According to the theoretical analysis in Section II-B, the amplitude of SHC may be the same as that of the dc component. Compared with the Fourier analysis of $i_{\rm bus}$, as shown in Fig. 7, SHC only accounts for 0.09% of the dc component.

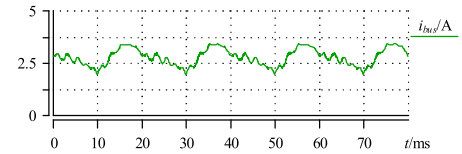

Fig. 8. Simulation results when the parameters of $C_{\alpha 1}$ and $C_{\alpha 2}$ are not the same (C_1=150 uF, α_1=0.986; C_2=120 uF, α_2=−0.967).

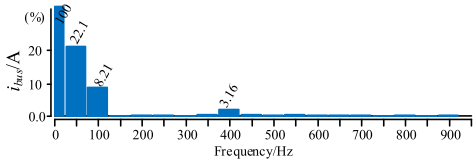

Fig. 9. Fourier analysis of $i_{\rm bus}$ when harmonic current is suppressed in simulation (C_1=150 uF, α_1=0.986; C_2=120 uF, α_2=−0.967).

Second, in the fractional order model, when the parameters of $C_{\alpha 1}$ and $C_{\alpha 2}$ are not the same ($C_1 = 150$ uF, $\alpha_1 = 0.986$; $C_2 = 120$ uF, $\alpha_2 = -0.967$), the output voltage u_o, capacitor voltage u_{c1}, u_{c2} and bus current $i_{\rm bus}$ is shown in Fig. 8. Because of the parameter asymmetry, the additional first-order harmonic current appears in the bus current. The Fourier analysis is shown in Fig. 9. The SHC is increased to 8.21% of the dc component and the first-order harmonic is increased to 22.1%. The parameter error does harm harmonic suppression performance. Meanwhile, these harmonic currents cause additional line loss. Without considering the skin effect, the line resistance $R_{\rm line}$ is a fixed value. When there is no harmonic current, the line loss P_{ldc} is

$$P_{ldc} = I_{\rm dc}^2 R_{\rm line}. \tag{38}$$

And when there is harmonic current, the line loss P_{lhar} is

$$P_{lhar} = I_{\rm dc}^2 R_{\rm line} \left(1 + {\rm THD}^2\right). \tag{39}$$

Where the THD means total harmonic distortion. According to (38) and (39), line loss due to parameter error is increased by 5.6%.

Third, when $C_{\alpha 1}$ is inconsistent with $C_{\alpha 2}$ and the proposed FOC is activated to compensate for the influence caused by parameter errors. In Fig. 10, the high-frequency ring of u_{c2} is slightly increased due to the effect of the adaptive FOC being in parallel with C_2. i_{Lclp} is the waveform of i_{Lc} filtered by the low-pass filter. It can be seen that FOC periodically extracts or injects energy into the external circuit to correct parameter errors. Fourier analysis of $i_{\rm bus}$ is shown in Fig. 11. All low-frequency harmonics in the current are suppressed to less than 4%. At this point, the low-order harmonics in the bus current are effectively suppressed.

B. Experiment Results of the Adaptive FOC Circuit

The abovementioned simulation results have verified the feasibility of the proposed method, and the experiment is implemented for further verification. The experimental parameters

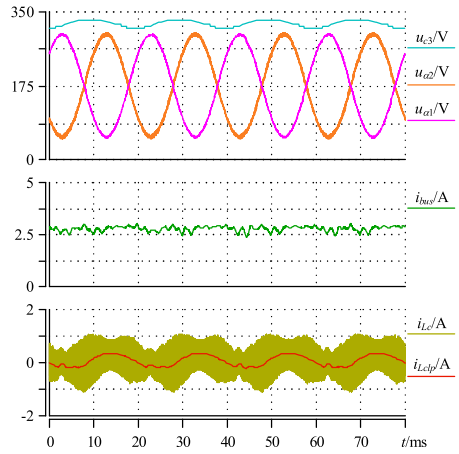

Fig. 10. Simulation results when $C_{\alpha 1}$ and $C_{\alpha 2}$ are asymmetric and the proposed FOC is activated.

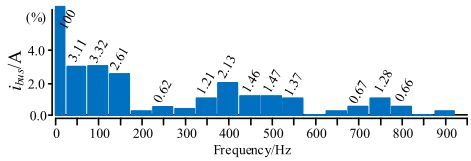

Fig. 11. Fourier analysis of i_{bus} when the proposed FOC is activated in simulation.

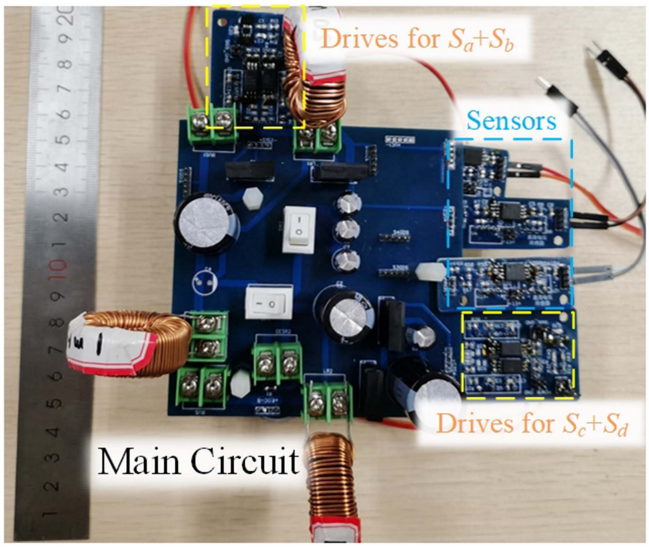

Fig. 12. Prototype of main circuit. (The proposed FOC circuit and harmonic current suppression circuit).

and circuit are shown in Table I and Fig. 4, respectively. And the prototype is shown in Fig. 12, which is the Main Circuit part in Fig. 4. And its components are all on a 10 × 10 cm^2 board.

When the inverter is employed, the output voltage u_o and bus current i_{bus} are shown in Fig. 13. The output power fluctuates at twice the line frequency and the bus current i_{bus} contains a 1.74 A secondary harmonic, as shown in Fig. 14. The amplitude of SHC slightly less than that of dc because the circuit is equivalent to

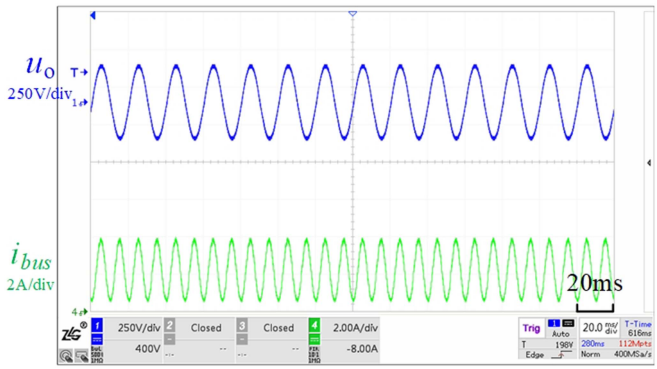

Fig. 13. Voltage u_o and bus current i_{bus} when harmonic suppression circuit is not employed.

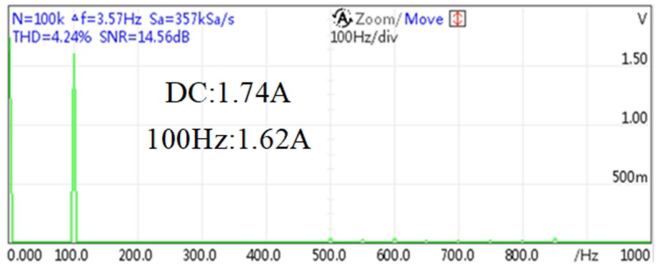

Fig. 14. Fourier analysis of i_{bus} when harmonic suppression circuit is not employed.

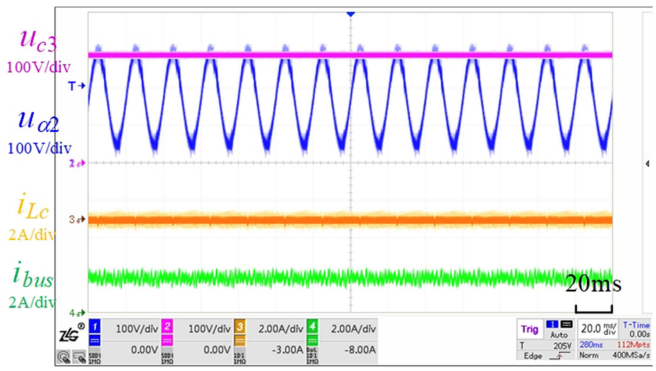

Fig. 15. Voltage u_{c2} and bus current i_{bus} when harmonic suppression circuit is employed. (C_1=C_2=150 uF, α_1=−α_2=1).

an ordinary small capacitor in the inactive state and has a weak harmonic suppression ability.

Then, the harmonic suppression circuit is activated. At this time, $C_{\alpha 1}$ and $C_{\alpha 2}$ have the same parameters ($C_1 = C_2 =$ 150 uF, $\alpha_1 = -\alpha_2 = 1$). The voltage u_{c2} of capacitor C_2 and bus current i_{bus} is shown in Fig. 15. The Fourier analysis of i_{bus} is shown in Fig. 16. SHC is reduced to 1.73% of the dc component (DC:1.81 A; SHC:31.3 mA). And the components of other low-order harmonic currents increase slightly. As C_1 and C_2 cannot guarantee perfect consistency under ideal conditions, there is still a small amount of first-order harmonic current in the bus current (37.2 mA, 2.01% of dc component). Among the first 20th-order harmonics, the 950 Hz component has the

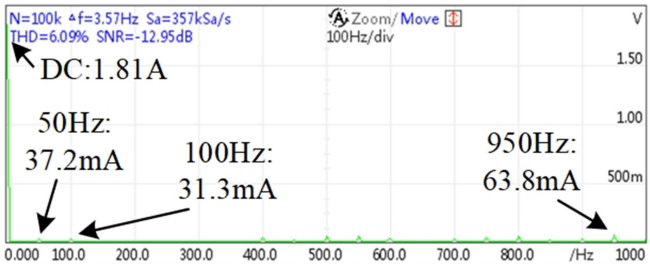

Fig. 16. Fourier analysis of $i_{\rm bus}$ when harmonic current is suppressed (C_1=C_2=150 uF, α_1=$-\alpha_2$=1).

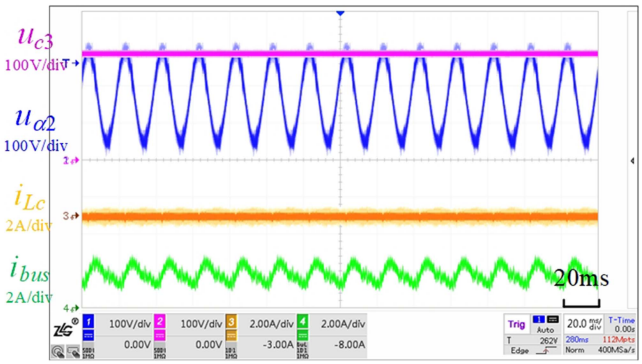

Fig. 17. Voltage u_{c2} and bus current $i_{\rm bus}$ when harmonic suppression circuit is employed. (C_1=150 uF, α_1=0.986; C_2=120 uF, α_2=$-$0.967).

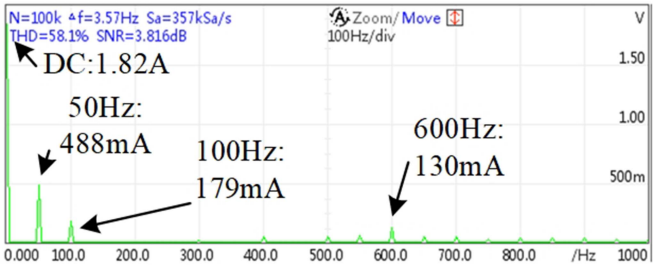

Fig. 18. Fourier analysis of $i_{\rm bus}$ when harmonic current is suppressed (C_1=150 uF, α_1=0.986; C_2=120 uF, α_2=$-$0.967).

largest amplitude of 63.8 mA, accounting for 3.5% of the dc component. The proposed FOC circuit is inactivated at that time, so the energy storage capacitor is in passive rectification and the output current i_{Lc} of the circuit is around zero at a steady state.

Next, it comes to serious parameter errors occurred in parameters of $C_{\alpha 1}$ and $C_{\alpha 2}$ (C_1 = 150 uF, α_1 = 0.986; C_2 = 120 uF, α_2 = $-$0.967). According to (9) in Section II-B, the residual amount of SHC is going to be (C_1-C_2)/(C_1+C_2) = 10%. In the experiment, the voltage u_{c2} and bus current $i_{\rm bus}$ are shown in Fig. 17. Due to the asymmetry parameter, not only SHC cannot be suppressed completely, but also the additional first-order harmonic current appears in the bus current. Although the waveform of $u_{\alpha 2}$ is still sinusoidal, $i_{\rm bus}$ contains a large number of harmonics. The Fourier analysis of $i_{\rm bus}$ is shown in Fig. 18. SHC is increased to 9.83% of the dc component and the first-order harmonic is increased to 26.8% (DC: 1.82 A; First-order: 488 mA; SHC: 179 mA), which is consistent with theoretical analysis. In addition to the abovementioned, among the first 20th-order harmonics, the 600 Hz component has the largest amplitude of 130 mA, accounting for 7.14% of the dc component.

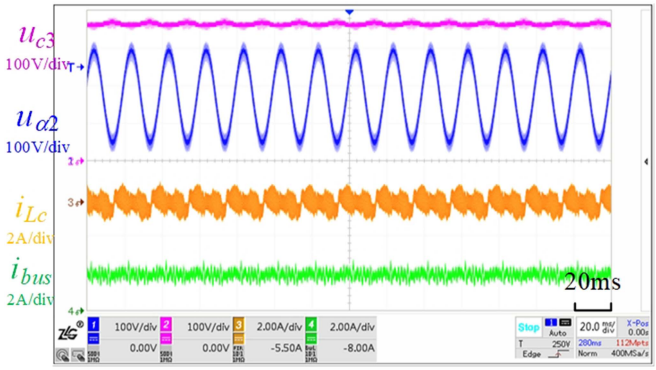

Fig. 19. Key waveforms when the proposed fractional order capacitor is employed to compensate parameter asymmetry (i_{Lc} is not filtered).

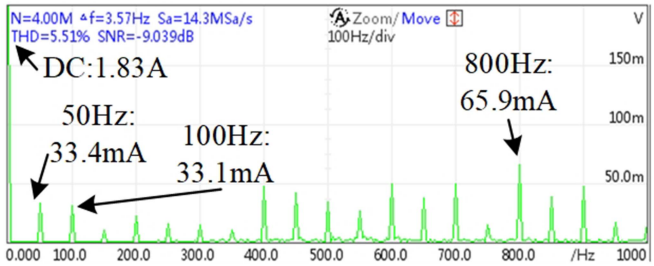

Fig. 20. Fourier analysis of $i_{\rm bus}$ when FOC is employed to compensate the negative effects of parameter asymmetry.

Finally, to compensate for the negative effects of parameter asymmetry, the proposed FOC is employed. The key waveforms are shown in Fig. 19. Harmonics in the dc bus are successfully suppressed again. The voltage u_{c3} of energy capacitor C_3 oscillates around the reference value. The abovementioned small oscillation cannot be eliminated, because at every moment the FOC exchanges energy with the external circuit, either in or out. Therefore, u_{c3} only needs to maintain a relatively stable voltage in one working cycle. The first and second harmonics in $i_{\rm bus}$ are both suppressed to less than 4% as Fourier analysis in Fig. 20 shows. SHC is reduced to 1.81% and the first-order harmonic is reduced to 1.83% (DC: 1.83A; SHC: 33.1 mA; first-order harmonic: 33.4 mA). Among the first 20th-order harmonics, the 800 Hz component has the largest amplitude of 65.9 mA, accounting for 3.6% of the dc component.

The FOC output current i_{Lc} contains a switching frequency harmonic because the front and back ends of the inductor L_c are both MOSFETs. By filtering and extracting low-frequency signals, as shown in Fig. 21, it can be seen that the low-frequency components (50 Hz) in i_{Lc} are consistent with the theory.

To further verify the proposed method adaptation for suppressing the harmonic current under various types of loads, experiments are also performed under resistive-inductive load.

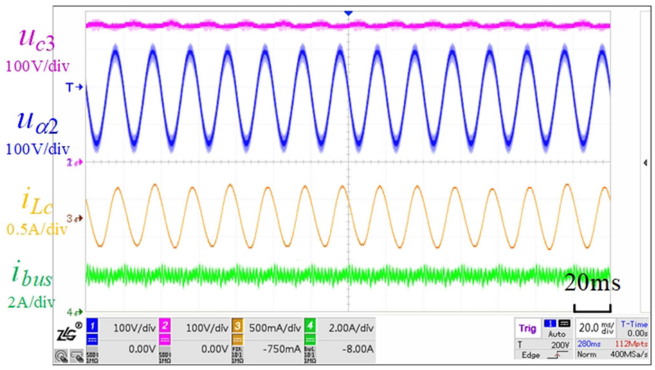

Fig. 21. Key waveforms when the proposed FOC is employed to compensate parameter asymmetry (i_{Lc} is filtered).

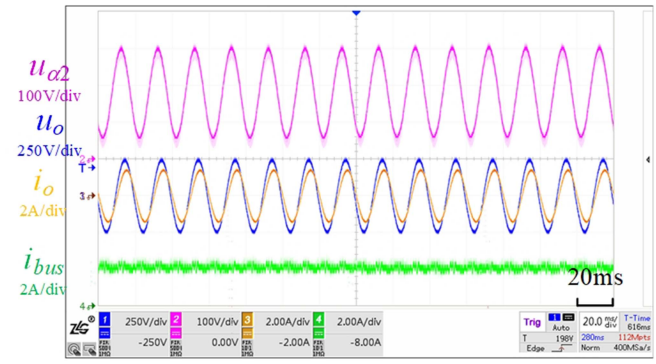

Fig. 22. Experimental waveforms when inverter powers RL loads.

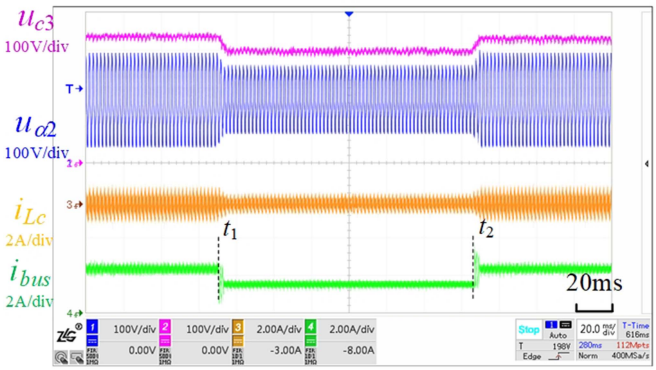

Fig. 23. Harmonic suppression performance of the proposed FOC when output power jumps.

The results are shown in Fig. 22. The SHC is reduced to 41.5 mA, which is only 2.16% of the dc component (1.92 A). It verifies that the proposed method can absorb the secondary harmonic current well even when the inverter powers a nonpure resistive linear load, by adjusting the voltage phase β in (11).

The dynamic response is shown in Fig. 23. Initially, the system is at 100% power output. At time t_1, the output power jumps down to 50%. As can be seen from the figure, $i_{\rm bus}$ can reach a new steady state after a short time of oscillation. Then, at time t_2, the output power jumps back to 100%, $i_{\rm bus}$ can also return to

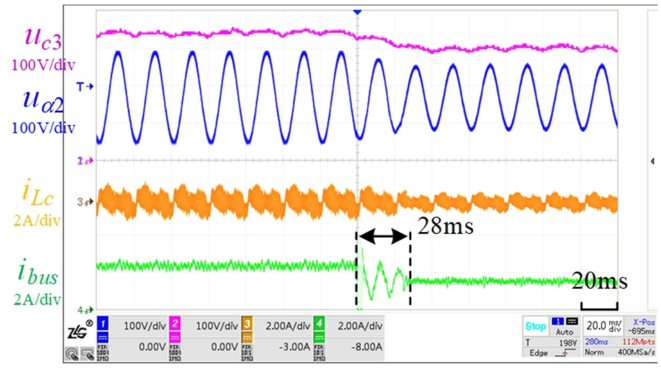

Fig. 24. Harmonic suppression performance of the proposed FOC when output power jumps down.

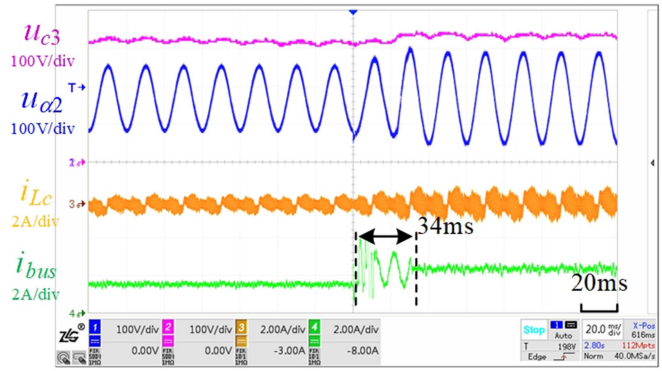

Fig. 25. Harmonic suppression performance of the proposed FOC when output power jumps up.

the state as before. The low-order harmonic components of $i_{\rm bus}$ still can be well suppressed in the case of load jumps.

The key waveforms at t_1 are particularly shown in Fig. 24. After the power jumps down, the low-order harmonics will appear again. The ac component on u_{c2} starts to decrease, so as the amplitude of u_{c3} and i_{Lc}. After about 28 ms, the low-order harmonic components of $i_{\rm bus}$ are suppressed. The key waveforms at t_2 is particularly shown in Fig. 25. When the power jumps up, lower-order harmonics appear. The ac component on u_{c2} starts to increase, and so as the amplitude of u_{c3} and i_{Lc}. After about 34 ms (a little longer than power jumps down), the low-order harmonic components of $i_{\rm bus}$ are suppressed again.

The experiment results show that the proposed method can well compensate for the parameter asymmetry in those types of harmonic suppression circuits. Under ideal conditions, the harmonic suppression circuit with symmetric parameters can suppress the SHC down to below 2%. However, once the device is aged, the parameters will change. For example, a 20% capacitance value deviation and an additional 0.5 Ω ESR in the experiment will cause a great negative impact on the harmonic suppression performance (SHC is increased to 9.83% and first-order harmonic is increased to 26.8%). When the proposed FOC circuit is applied, the first- and second-order harmonics can be suppressed again down to below 2%. And none of the first 20th-order harmonics exceeds 4% of the dc component.

TABLE II
PERFORMANCE COMPARISON OF HARMONIC CURRENT SUPPRESSION

Paper	Power level/ dc voltage	Cap. robust	ESR robust	Capacitor (uF)	Inductor (uH)	Switches number	Switching frequency	First har. reduction	Second har. reduction
[14]	1 kW/380 V	×	×	90, 90	2000	2	/	/	/
[16]	1 kW/450 V	√	×	108, 90	1800	2	10 kHz	/	7%
[17]	568 W/250 V	√	×	450, 300	500	2	/	12%	1%
[34]	800 W/200 V	√	√	330, 220, 187	330, 120	6	10 kHz	19.8%	6.8%
Proposed	600 W/350 V	√	√	150, 120, 20	400, 150	4	25 kHz	25.0%	8.0%

*"First ,second har. reduction" represents first-, second-order harmonic current suppression ability. They indicate the suppression ratio of additional harmonics generated by and parameter error. For example, because of the parameters error, the first-order harmonic current is 26.8% of dc component when FOC is inactivated, while that current is reduced to 1.83% when FOC is activated, so the "frist har. reduction." is 26.8%-1.83%=24.97%.

Table II shows the performance comparison of parameter deviation between the proposed method and other power decoupling methods. Generally speaking, in terms of cost, it is challenging to make precise comparisons due to the different manufacturing methods employed. However, Table II lists the number of passive components and switches, which can provide a rough estimate of the cost involved. For reliability, the reduction level of each harmonic component listed in Table II can be compared relatively accurately. Regarding invasiveness, both [16] and [17] can be optimized at the control level, making them easy to upgrade in the original system. However, they cannot provide complete upper power harmonic suppression ability for the original system. On the other hand, both [34] and this manuscript involve additional structures in parallel, which makes upgrading the original circuit easier. In comparison to [34], this manuscript does not require extra measurements of the current of two decoupling capacitors. Instead, the shared bus current information is sufficient for its operation.

IV. CONCLUSION

This article proposes a method based on adaptive FOC to compensate for the parameter error in low-order harmonic suppression.

1) The order of FOC can be adjusted, making the port equivalent impedance cover the entire impedance plane in theory.
2) The proposed method can compensate for the worsen harmonic suppression caused by parameter deviations while maintaining the harmonic suppression ability of the original circuit.
3) The proposed FOC-based method does not contain an additional independent power supply and the asymmetry can be calculated from the harmonic content of the bus current.
4) Since the FOC is completely composed of nondissipative components, in theory, no additional power loss will be incurred.

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