Load-Independent Push–Pull Class-Φ_2 Inverter With Single Compact Three-Winding Inductor

Xiaosheng Huang, *Member, IEEE*, Yongshu Lin, Yi Dou, *Member, IEEE*, Shuyi Lin, and Jing Huang

***Abstract*—This article proposes a push–pull class-Φ_2 inverter with a single three-winding integrated inductor. A design methodology is presented to achieve load-independent operation of the proposed class Φ_2 inverter, ensuring consistent soft-switching operation and constant voltage gain under varying load conditions. A compact magnetic structure is proposed to implement the three-winding integrated inductor, which distinctly reduces the number and size of magnetic components compared with conventional class Φ_2 inverters. By flux cancellation and core sharing, the magnetic integration not only reduces the inductor's overall volume and losses but also maintains the inverter's high efficiency. A 6.78-MHz *LCC*-S resonant wireless power transfer prototype is built to validate the proposed methodology and the magnetic structure. Furthermore, an active push–pull class-Φ_2 rectifier is implemented and demonstrates the load-independent resistive input. The experimental results indicate that the prototype performs robust soft switching over the entire load range, from no load to 320 W output. The voltage gain remains nearly constant, varying within +1%/-3.5%. Moreover, the measured dc–dc peak efficiency of the system reaches 91% at 170 W output, whereas the estimated peak efficiency of the class-Φ_2 inverter attains 96.6%. The proposed magnetic structure offers compact dimensions and low loss characteristics for the megahertz inverter.**

***Index Terms*—Active rectifier, class-Φ_2, class-EF, inverter, load-independent, magnetic integration, wireless power transfer (WPT).**

I. Introduction

WIRELESS power transfer (WPT) based on magnetic coupling has gained significant traction in diverse power-conversion applications, including portable devices, drones, industrial automatic guided vehicles, and electric vehicles [1], [2], [3], [4], [5]. The prominent factors determining the overall size and weight of WPT systems are typically around the coupling coils. Increasing the operating frequency to multimegahertz (MHz) shows promise in reducing the weight of the coupling coils and improving the quality factors. The high-frequency inverter plays a pivotal role in the WPT systems by effectively energizing compensated coupling coils and establishing inductive links to ensure high-efficiency transfer under receivers' misalignment and varying loads. The inverter must exhibit wide-load-range soft switching and estimable voltage/current gain. However, when the operation reaches multiMHz range, determining the most suitable inverter topology to achieve optimal efficiency becomes less apparent.

The active bridge-based inverters have been widely used in WPT systems operating at several hundred kilohertz [6], [7], [8]. These inverters require fewer magnetic components compared with other topologies and can maintain soft switching with proper driven load matching and dead-time regulation. Consequently, they are attractive for achieving high-power density and reducing circuit complexity. Nevertheless, designing the high-side drives up to multiMHz remains challenging. In addition, MOSFET devices, which have relatively large parasitic capacitance, face difficulties in attaining stable zero-voltage switching (ZVS). Recent advancements in wide-band-gap power devices (GaN, SiC) have made it easier to increase the operating frequency of active bridges to several megahertz. However, the switching voltage of high slew rate (dV/dt) causes more harmonic contents, thereby compromising the electromagnetic interference (EMI) performance. Furthermore, precise dead-time control achieving ZVS up to multiMHz is tricky.

The class-E inverter is widely used in low- to medium-power WPT systems operating at several MHz [9], [10], [11], [12]. The conventional single-end class-E inverter uses a low-side driven switch, which simplifies the driving circuit. The participation of the semiconductor's parasitic capacitance in the load network facilitates reliable soft switching at several MHz operations [13]. Moreover, the class-E inverter achieves ZVS and zero-current switching (ZCS) at a particular optimal load, reducing switching loss and EMI noise. However, due to the load network's strong dependency on output current, the original class-E topology with large dc-feed inductance fails to maintain ZVS at light loads. To address the limitation, finite dc-feed inductance can be implemented to inject the necessary resonant current and achieve ZVS across the entire load range. Moreover, the inverter can achieve load-independent ZVS and constant voltage

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Xiaosheng Huang, Yongshu Lin, and Jing Huang are with the Fujian Provincial University Engineering Research Center for Industrial Automation, School of Electronic, Electrical Engineering and Physics, Fujian University of Technology, Fuzhou 350118, China (e-mail: hxs@fjut.edu.cn; linyongshu1998@qq.com; huangj@fjut.edu.cn).

Yi Dou is with the Resonant Link Inc., Zurich 8002, Switzerland (e-mail: ydou@resonant-link.com).

Shuyi Lin is with the Development Center for Industrial Automation Technology of Fujian Province, School of Electronic, Electrical Engineering and Physics, Fujian University of Technology, Fuzhou 350118, China (e-mail: linshuyi1985@qq.com).

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gain by parameter optimization [14]. Nevertheless, this solution introduces another issue: the high-amplitude harmonic currents drawn from dc side cause high-frequency losses of the input inductor. It also results in large filter capacitance to suppress the input voltage ripples. The push–pull class-E topology, which comprises two interleaved switches operating with 180° phase shift, can double the output power and suppress the input current ripples simultaneously [15]. However, class-E inverters exhibit inherent high-peak switch voltage, which can exceed four times dc input and significantly limits the available semiconductors and power level [16].

The class-EF$_2$ (with large dc-feed inductance) and class-Φ_2 (with finite dc-feed inductance) inverters are specific instances within the class-EF topology family [17], [18]. They can also be considered variations derived from class-E inverters with additional resonant branches. These modifications significantly reduce the switching peak voltage or enhance the power delivery capability, while maintaining the same devices' voltage/current stress [19], [20], [21]. Consequently, they adhere to a similar design concept where the resonant parameters are designed to shape the switch voltage and realize soft switching [22]. Introducing the finite dc-feed inductance can inject harmonic currents to effectively shape the switch voltage waveform and achieve wide-load-range soft switching [23], [24]. Likewise, the load-independent ZVS and constant voltage (or current) gain can be achieved through optimized parameters [14], [24]. Furthermore, the push–pull class-EF$_2$/Φ_2 inverters using two interleaved switches leads to reduced current ripples on the dc side [25]. Moreover, T networks can be implemented to share the inductors injecting even and odd harmonic currents [26], [27], [28]. The T-network-based push–pull topology retains large dc-feed inductance, thus providing both low-input current ripples and wide-load-range ZVS.

Typically, the push–pull class-EF$_2$/Φ_2 inverters require four individual inductors (two for the input and two for tuning the second-order harmonic) in addition to the load branch to form the resonant network that shapes the switch voltage. As a result, the number of magnetic components in these topologies is generally twice that of class-E inverters, regardless of whether T networks are utilized. Thus, a major drawback of the class-EF$_2$/Φ_2 topologies is their increased requirement for magnetic components. Furthermore, the resonant branches of the topologies need to handle large-amplitude harmonic currents, resulting in significantly increased circuit size and high-frequency losses. Therefore, reducing the number and size of the magnetic components becomes an attractive prospect for overcoming the current limitations of class-EF$_2$/Φ_2 inverters.

This article proposes a push–pull class-Φ_2 inverter with a single three-winding integrated inductor, offering significant reductions in both the number and overall volume of magnetic components compared with the conventional inverters. The rest of this article is organized as follows. In Section II, a simplified derivation is presented to parametrize the design, enabling load-independent operation with ZVS and constant voltage gain, regardless of load variations. In Section III, a magnetic structure is proposed to implement the three-winding integrated inductor, which offers a more compact solution compared with conventional class-Φ_2 inverters. Section IV describes an example design and implementation of a 6.78-MHz WPT prototype, which incorporates the class-Φ_2 inverter, *LCC*-S compensated coupling coils, and an active class-Φ_2 rectifier. Section V presents and discusses the experimental results obtained from the prototype. The performance of the system is analyzed and evaluated based on these results. Finally, Section VI concludes this article.

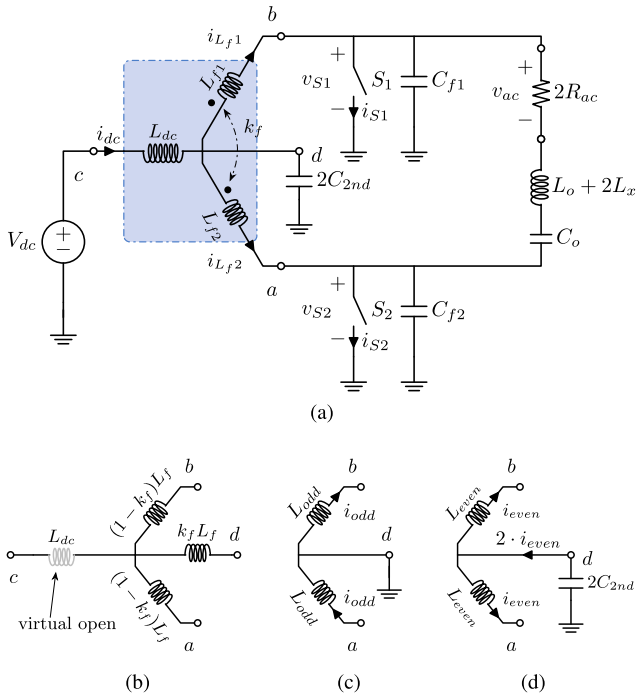


Fig. 1. Proposed push–pull class-Φ_2 inverter with a single three-winding inductor. (a) Inverter topology. (b) Decoupled three-winding inductor. (c) Equivalent T network for odd harmonics. (d) Equivalent T network for even harmonics. Assuming $L_{dc} \gg L_f$, terminal c is virtually opened for high-frequency harmonics. The resonant winding L_{f1} and L_{f2} are coupled with a coupling coefficient of $k_f < 0$, and have identical self-inductance of L_f. Thus, $L_{odd} = (1 - k_f)L_f$ and $L_{even} = (1 + k_f)L_f$.

II. Modeling of Load-Independent Operation for Three-Winding Push–Pull Class-Φ_2 Inverters

Fig. 1(a) shows the proposed push–pull class-Φ_2 inverter with a three-winding integrated inductor. Due to the introduced three-winding inductor with coupled windings, the circuit model differs from conventional class-EF$_2$/Φ_2 inverters [17], [24], [26]. This section investigates the modeling and parametric design of the proposed inverter, achieving load-independent ZVS and constant output voltage.

A. Circuit Analysis

The introduced coupling resonant windings and output reactance L_x inherently change the resonant network. Thus, the proposed topology differs from the conventional T-network-based class-Φ_2 inverters [26]. To simplify the analysis, assumptions are made as follows.

1) The inductance of the dc-feed winding L_{dc} is large enough to eliminate current ripples of i_{dc}, of which dc component is $2I_{\text{dc}}$.
2) The switches have zero ON-resistance and infinite OFF-resistance. The passive components are lossless.
3) The interleaved S_1 and S_2 have an identical duty cycle D with 180° phase shift. i.e., S_1 is ON during $0 < \omega t \leq 2D\pi$ and OFF during $2D\pi < \omega t \leq 2\pi$, where ω is the angular velocity. While S_2 is ON during $\pi < \omega t \leq (2D+1)\pi$ and OFF during the rest interval. Therefore, the switch voltages of S_1 and S_2 can be defined as $v_S(\omega t) = v_{S1}(\omega t) = v_{S2}(\omega t + \pi)$.
4) The characteristic impedance $\sqrt{L_o/C_o}$ of the filter is high enough to form a sinusoidal output voltage v_{ac} of $2 \cdot V_{\text{ac}}$ is the amplitude. Thus, the output current i_{ac} can be expressed by

$$i_{\text{ac}}(\omega t) = I_{\text{ac}} \cdot \sin(\omega t + \varphi) \tag{1}$$

where I_{ac} and ϕ are the current amplitude and phase shift, respectively.

As in Fig. 1(b), the three-winding inductor can be decoupled to a four-winding network with a common point, where terminal c is virtually opened as L_{dc} is large enough to block high-frequency harmonics. This network presents different impedance for odd and even harmonics. Since the switching phases of S_1 and S_2 are interleaved, operating in differential mode, the odd harmonic currents flow from terminal a to b in differential mode. Therefore, the three-winding magnetic structure prevents the odd harmonic currents from passing terminal c and d. As in Fig. 1(c), the common point is equivalently grounded for odd harmonic currents, since there is no difference in voltage between the common point and ground. On the other hand, since the dc-feed inductance L_{dc} is large enough, terminal c is equivalently open for high-frequency harmonics. Therefore, the coupled L_{f1} and L_{f2} can be decoupled to a T network, as in Fig. 1(d). The even harmonic currents passing the mutual inductance branch are $2 \cdot i_{\text{even}}$. Thus, the branch inductance is twice the mutual inductance $(2 \cdot k_f L_f)$ for i_{even}. Eventually, the equivalent inductance for odd and even harmonics are $L_{\text{odd}} = (1 - k_f)L_f$ and $L_{\text{even}} = (1 + k_f)L_f$, respectively.

The capacitor $C_{2\text{nd}}$ and L_{even} form a resonant branch to short the second-order harmonic and shape the switch voltage. Using a lower L_{even} reduces the second-order harmonic voltage across the dc-feed winding L_{dc}, leading to lower current ripples and losses. Therefore, the introduced coupling provides a flexible way to optimize the integrated inductor, which differs from the conventional class-Φ_2 inverters. Assuming that the higher order even harmonics are negligible, the current through $C_{2\text{nd}}$ can be expressed by

$$i_{nC_{2\text{nd}}}(\omega t) = \frac{i_{C_{2\text{nd}}}(\omega t)}{I_{\text{dc}}} = a_2 \sin(2\omega t) + b_2 \cos(2\omega t). \tag{2}$$

Since the two switches are interleaved, the phase shift of the resonant winding currents is 180°. Thus, the winding currents can be defined as $i_{L_f}(\omega t) = i_{L_f1}(\omega t) = i_{L_f2}(\omega t + \pi)$, of which expression during $0 < \omega t \leq 2D\pi$ is

$$\begin{aligned} i_{nL_{f\_\text{ON}}}(\omega t) &= \frac{i_{L_{f\_\text{ON}}}(\omega t)}{I_{\text{dc}}} \\ &= \frac{p_{\text{ac}}^2 q^2}{2p_r} \cdot \omega t + p_{\text{in0}} + i_{nC_{2\text{nd}}}(\omega t) \end{aligned} \tag{3}$$

where $p_{\text{ac}} = \frac{I_{\text{ac}}}{I_{\text{dc}}}$, $q = \frac{1}{\omega\sqrt{L_{\text{odd}}C_f}}$, $p_r = \frac{1}{\omega C_f R_{\text{ac}}}$, and $p_{\text{in0}} = \frac{i_{L_{f\_\text{ON}}}(0)}{I_{\text{dc}}}$ is the normalized initial current value at $\omega t = 0$. The resonant winding current can be decomposed into dc bias, odd harmonics, and second-order harmonic. In this equation, $i_{nC_{2\text{nd}}}$ indicates the second-order harmonic, while the rest indicates the superposed dc bias and odd harmonics. Similarly, the expression of i_{L_f} during $2D\pi < \omega t \leq 2\pi$ is given by

$$\begin{aligned} i_{L_{f\_\text{OFF}}}(\omega t) = \frac{1}{\omega L_{\text{odd}}} \int_{2D\pi}^{\omega t} &(v_{C_{2\text{nd}}}(\omega t_1) \\ &- v_{S\_\text{OFF}}(\omega t_1))d\omega t_1 + i_{L_{f\_\text{ON}}}(2D\pi) \end{aligned} \tag{4}$$

where $v_{C_{2\text{nd}}}(\omega t)$ is the voltage across $C_{2\text{nd}}$ given by

$$v_{C_{2\text{nd}}}(\omega t) = V_{\text{dc}} + \frac{1}{\omega C_{2\text{nd}}} \int_0^{\omega t} i_{C_{2\text{nd}}}(\omega t_1) d\omega t_1. \tag{5}$$

The OFF-state switch voltage is formed by charging the parallel capacitor C_{f1} and C_{f2}. The switch voltages of S_1 of S_2 can be defined as $v_{S_1}(\omega t) = v_{S_2}(\omega t) = v_S(\omega t + \pi)$. Let $C_{f1} = C_{f2} = C_f$, then v_S during $2D\pi < \omega t \leq 2\pi$ is

$$v_{S\_\text{OFF}}(\omega t) = \frac{1}{\omega C_f} \int_{2D\pi}^{\omega t} \left(i_{L_{f\_\text{OFF}}}(\omega t_1) + i_{\text{ac}}(\omega t_1)\right) d\omega t_1. \tag{6}$$

Substituting (5) and (6) into (4) gives

$$\frac{d^2 i_{L_{f\_\text{OFF}}}(\omega t)}{d\omega t^2} = 4i_{C_{2\text{nd}}}(\omega t) - q^2(i_{L_{f\_\text{OFF}}}(\omega t) + i_{\text{ac}}(\omega t)) \tag{7}$$

which gives the general solution of $i_{L_{f\_\text{OFF}}}$ as

$$\begin{aligned} \frac{i_{L_{f\_\text{OFF}}}(\omega t)}{I_{\text{dc}}} &= a_f \cos(q \cdot \omega t) + b_f \sin(q \cdot \omega t) \\ &\quad - \frac{p_{\text{ac}} q^2}{q^2 - 1} \sin(\omega t + \varphi) - \frac{4}{q^2 - 4} i_{nC_{2\text{nd}}}(\omega t) \end{aligned} \tag{8}$$

where a_f and b_f are current amplitudes excited by the resonance of L_{odd} and C_f.

When the design parameters q, D, and p_r are determined, the following constraints can be used to solve the seven state variables (i.e., a_f, b_f, a_2, b_2, p_{in0}, p_{ac}, and φ) and detail the operating waveforms of the inverter.

1) The voltage-second balance of L_f gives

$$\frac{1}{2\pi} \int_{2D\pi}^{2\pi} v_{S\_\text{OFF}}(\omega t) d\omega t = V_{\text{dc}}. \tag{9}$$

2) The average switch current meets

$$\frac{1}{2\pi} \int_0^{2D\pi} (i_{L_{f\_\text{ON}}}(\omega t) + i_{\text{ac}}(\omega t)) d\omega t = I_{\text{dc}}. \tag{10}$$

TABLE I
PARAMETER SETS ACHIEVING LOAD-INDEPENDENT OPERATION

Duty cycle	D	0.3	0.33	0.35	0.4	0.45
Normalized parameters	ϕ	0.628	0.534	0.471	0.314	0.157
	q	1.124	1.185	1.239	1.441	1.769
	$p_{r\,\mathrm{optm}}$	1.233	1.883	2.508	5.203	10.947
	p_{ac}	1.696	1.665	1.645	1.598	1.554
	p_x	0.17	0.11	0.082	0.038	0.017
Voltage gain	G_v	1.179	1.201	1.216	1.252	1.287
Switch (rated load)	V_p/V_{dc}	2.091	2.121	2.157	2.319	2.792
	$I_{\mathrm{rms}}/I_{\mathrm{dc}}$	1.98	1.885	1.831	1.723	1.642
L_{f1},L_{f2} (rated load)	$I_{\mathrm{pp}}/I_{\mathrm{dc}}$	5.145	4.15	3.654	2.778	2.208
	$I_{\mathrm{rms\,total}}/I_{\mathrm{dc}}$	1.851	1.586	1.470	1.293	1.198
	$I_{\mathrm{rms\,2nd}}/I_{\mathrm{dc}}$	0.921	0.844	0.794	0.678	0.576

[a] Note that the input current i_{dc} has an amplitude of $2I_{\mathrm{dc}}$.
[b] G_v is calculated according to Fourier series of the switch voltage, thus the push–pull Class-Φ_2 inverter has an overall voltage gain of $2G_v$.

3) The second-order harmonic voltage is shorted by the resonant branch formed by $C_{2\mathrm{nd}}$ and L_{even}. Therefore,

$$\begin{cases} \frac{1}{2\pi}\int_{2D\pi}^{2\pi} v_{S\_\mathrm{OFF}}(\omega t)\cdot\sin(2\omega t)d\omega t = 0 \\ \frac{1}{2\pi}\int_{2D\pi}^{2\pi} v_{S\_\mathrm{OFF}}(\omega t)\cdot\cos(2\omega t)d\omega t = 0. \end{cases} \tag{11}$$

4) The current continuity of L_f gives

$$\begin{cases} i_{L_f\_\mathrm{OFF}}(2\pi) = i_{L_f\_\mathrm{ON}}(0) \\ i_{L_f\_\mathrm{OFF}}(2D\pi) = i_{L_f\_\mathrm{ON}}(2D\pi). \end{cases} \tag{12}$$

5) The ZVS turn-ON condition gives

$$v_{S\_\mathrm{OFF}}(2\pi) = 0. \tag{13}$$

Since it is difficult to derive the equations analytically, we solve the variables numerically. Then, explicit expressions can be obtained to analyze the circuit operation.

B. Parameter Sets Achieving Load-Independent Operation

Similar to the load-independent class-EF inverters with large dc-feed inductance, there are particular sets of design parameters for the proposed class-Φ_2 inverters to achieve ZVS and constant voltage gain regardless of load variation [24].

The circuit parameters of the inverter are calculated using the solved state variables and the predefined design parameters. According to the definition, the load factor p_r corresponds to load resistance R_{ac}. The phase shift ϕ can be regarded as a design parameter [24]. If the expected ϕ, which satisfies ZVS condition, is constant as p_r varies, the desired circuit parameters are also invariant. In this case, the inverter achieves load-independent operation. Therefore, the load-independent ZVS constraint can be expressed by

$$\frac{d\phi}{dp_r} = 0. \tag{14}$$

As this equation is not explicit, the expected ϕ is not solved directly. To find out the solutions, we sweep p_r with a given D, then solve the constraint equations to get the load-independent ϕ along with a corresponding q.

The parameter sets are listed in Table I, where V_p is the peak value of switch voltage. I_{rms} is the rms value of the switch current. I_{pp} and $I_{\mathrm{rms_{total}}}$ are the winding current's peak-to-peak and rms values, respectively. The normalized parameters can be used to design practical class-Φ_2 inverters based on required specifications.

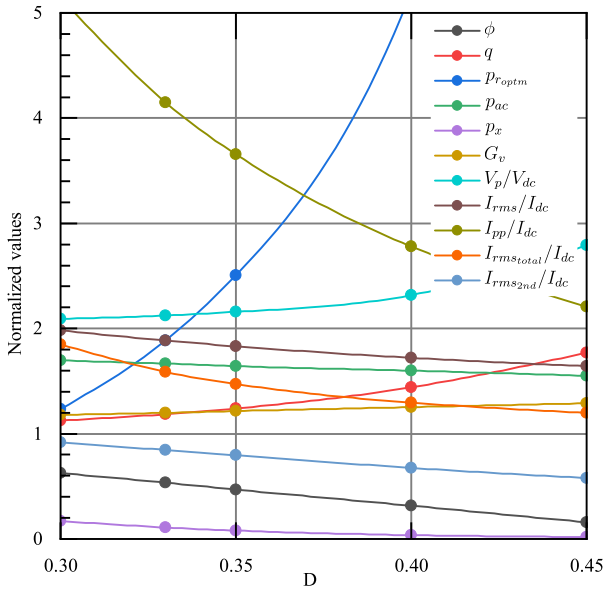


Fig. 2. Normalized parameters versus duty cycle D.

Although it is difficult to derive ϕ analytically, a fitting expression can be found according to the numerical solutions. The desired ϕ can be calculated by

$$\phi = \left(\frac{1}{2} - D\right)\cdot\pi. \tag{15}$$

The voltage gain G_v is given by

$$G_v = \frac{V_{\mathrm{ac}}}{V_{\mathrm{dc}}} = \frac{1}{V_{\mathrm{dc}}}\left|\int_{2D\pi}^{2\pi} v_{S\_\mathrm{OFF}}(\omega t)\cdot\sin(\omega t+\phi)d\omega t\right| \tag{16}$$

which is constant regardless of load variation. Note that the output voltage has an amplitude of $2V_{\mathrm{ac}}$ thus the actual voltage gain for push–pull inverters is $2G_v$. An additional parameter $p_x = \omega^2 L_x C_f$ is added for calculating L_x.

Generally, the optimal load factor $p_{r_{\mathrm{optm}}}$, which achieves both ZVS and ZCS turn-ON, is used to calculate the circuit parameters with the nominal load. The load factor p_r achieving ZCS turn-ON is solved by

$$\left.\frac{dv_{S\mathrm{del_{OFF}OFF_{off}}}}{d\omega t}\right|_{\omega t=2\pi} = 0. \tag{17}$$

This design criterion also results in larger L_f than using other values of p_r. The winding current reduces as L_f increases.

To visualize the normalized parameters and get the variation trend, Table I is illustrated in Fig. 2. It can be seen that using a higher duty cycle will increase the voltage stress and decrease the current stress. Therefore, a proper duty cycle D should be selected according to the voltage/current stresses. The decomposed second-order harmonic current (i.e., $I_{\mathrm{rms_{2nd}}}$) also shows a similar trend. A duty cycle from 0.3 to 0.4 is usually preferred to trade-off component stresses and efficiency.

Eventually, the inverter's circuit parameters can be designed based on the rated power $2P_r$ and input dc voltage $V_{\rm dc}$, i.e.,

$$R_{{\rm dc}_r} = \frac{V_{\rm dc}^2}{P_r} \tag{18}$$

$$R_{{\rm ac}_r} = \frac{2R_{{\rm dc}_r}}{p_{\rm ac}^2} \tag{19}$$

$$C_f = \frac{1}{\omega p_{r_{\rm optm}} R_{{\rm ac}_r}} \tag{20}$$

$$L_{\rm odd} = \frac{1}{\omega^2 q^2 C_f} \tag{21}$$

$$C_{\rm 2nd} = \frac{2}{(2\omega)^2 L_{\rm even}} \tag{22}$$

$$L_x = \frac{p_x}{\omega^2 C_f} \tag{23}$$

where $R_{{\rm dc}_r}/2$ and $2R_{{\rm ac}_r}$ are the inverter's rated input and load resistance, respectively. The values of $L_{\rm odd}$ and $L_{\rm even}$ are determined by L_f and k_f, which are designed according to the implemented magnetic structure of the three-winding inductor. Thus, the normalized parameter sets provide a concise guideline to design the load-independent push–pull class-Φ_2 inverter with the three-winding inductor.

C. Key Waveforms and Design Consideration

Fig. 3 shows the switch voltages at various duty cycles and loads, i.e., D and $R_{\rm ac}$. The practical inverters operate at constant duty cycles. The voltages present similar trends as analyzed previously, i.e., the peak values increase as the duty cycle increases or the load resistance decreases. Meanwhile, using a lower duty cycle will reduce the variation of peak voltages. The switches maintain ZVS across various loads and achieve zero-voltage-derivative-switching turn-ON at the rated load, which indicates the achievement of ZCS. It is worth noting that the proposed load-independent model achieves strict ZVS turn-ON over the entire load range with the additional output reactance L_x, which differs from the existing literature.

The inverter features near-constant output voltage amplitude like a voltage source. Thus, the unloaded operation corresponds to $R_{\rm ac} = +\infty$. The $V_{\rm ds}$ has the lowest peak value at the unloaded condition. In comparison, when the inverters are overloaded (i.e., $R_{\rm ac} < R_{{\rm ac}_r}$), there is a particular interval that the switches' voltage reverses to negative before the turning-ON transient. The peak $V_{\rm ds}$ increases as $R_{\rm ac}$ decreases. In this case, the practical inverter's switches usually conduct reversely, since most semiconductor switches cannot withstand reverse voltage. Considering the nonlinear parasitic capacitance of the switch devices, the actual switches' voltage waveforms will be different from the theoretical results in Fig. 3. However, the load-independent features can still be obtained by adjusting the external part of C_f.

Fig. 4 shows a noticeable difference in the amplitude and rms value of the switch current at various loads. Since the average switch current equals the dc input, a lower duty cycle leads to a higher peak current. Meanwhile, the peak-to-peak

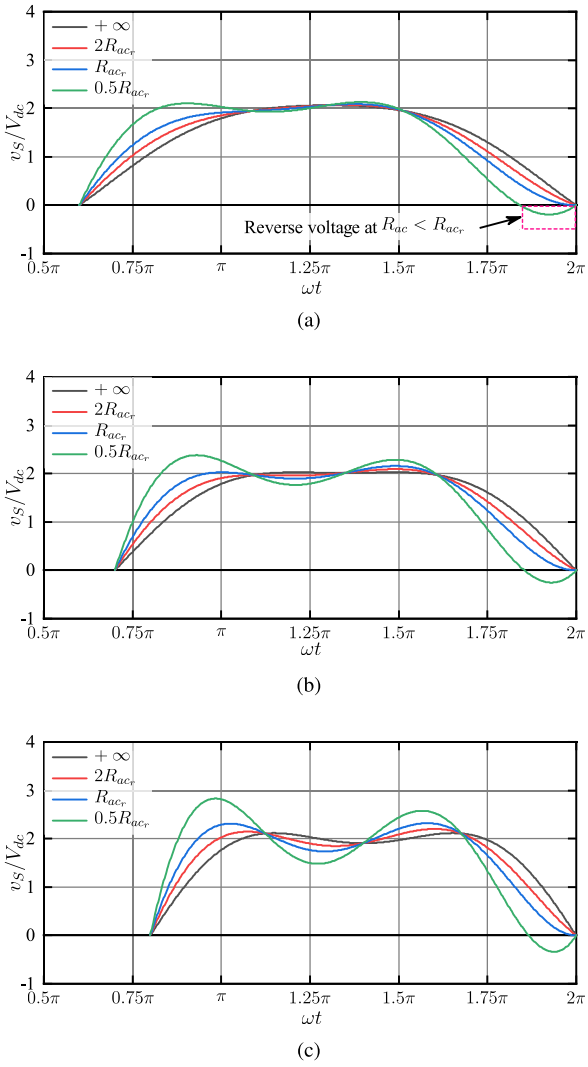


Fig. 3. Normalized switch voltage versus load resistance $R_{\rm ac}$. (a) $D = 0.3$. (b) $D = 0.35$. (c) $D = 0.4$. The nominal $R_{\rm acr}$ corresponds to the optimal load achieving both ZVS and ZCS. The ideal switches perform strict ZVS turn-ON regardless of load variation.

value increases as load resistance decreases. When the designed rated load resistance is higher than $R_{{\rm ac}_r}$, the switch realizes the subnormal condition achieving only ZVS at the rated power. Since the current will be negative at the beginning of the ON-state interval, the peak-to-peak and rms values of the current will increase. Thus, configuring the rated load at $R_{{\rm ac}_r}$, which achieves both ZVS and ZCS, benefits lowering conduction losses.

Fig. 5 shows the resonant winding currents at various duty cycles and loads. Likewise, the current amplitudes keep relatively large at various loads. In comparison, the rms values of the currents are distinctly reduced as $R_{\rm ac}$ increases. Thus, the inductor's loss is expected to be lower at light loads. According to Table I, the resonant winding currents' peak-to-peak and rms values decrease as the duty cycle increases. Nevertheless, a higher duty cycle leads to higher required inductance of the resonant windings. Parametric design requires a tradeoff between the current and the inductance of the resonant winding. Since

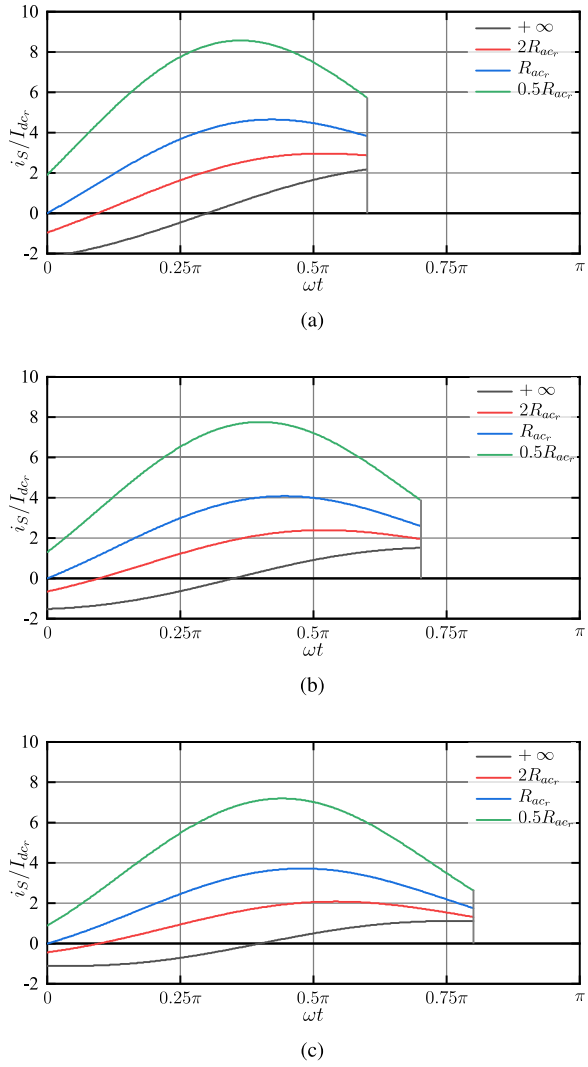


Fig. 4. Normalized switch current versus load resistance R_{ac}. (a) $D = 0.3$. (b) $D = 0.35$. (c) $D = 0.4$.

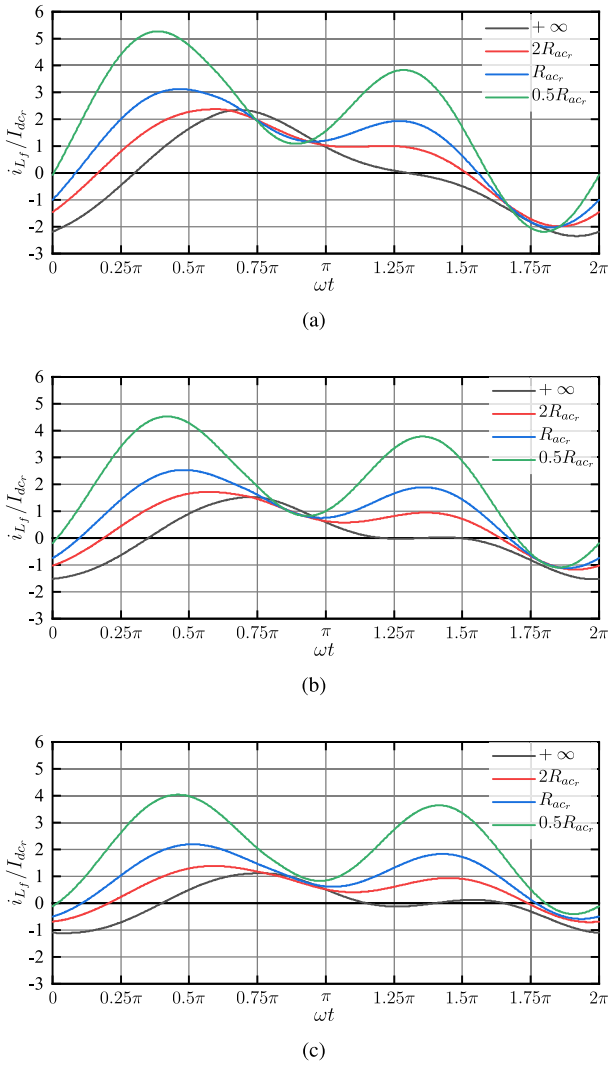


Fig. 5. Normalized resonant winding current versus load resistance R_{ac}. (a) $D = 0.3$. (b) $D = 0.35$. (c) $D = 0.4$. The current amplitudes of i_{L_f} are dominated by the second-order harmonic and dc bias.

high-frequency winding loss is a substantial part of the total loss, choosing a proper duty cycle is crucial for improving efficiency.

III. Magnetic Structure of Three-Winding Integrated Inductor

This section proposes a magnetic structure to implement the three-winding inductor of the push–pull class-Φ_2 inverter. Generally, the existing push–pull class-Φ_2 or EF_2 inverters require four inductors in addition to the load branch. The added magnetic components increase overall size and losses of the inverters. As aforementioned, the proposed push–pull class-Φ_2 inverter has a single three-winding integrated inductor, significantly reducing the number and volume of magnetic components. Moreover, the odd and even harmonics are adjustable by coupling the two resonant windings.

As shown in Fig. 6, the three windings are arranged in two back-to-back EI-type cores. The flux generated by winding currents can be decomposed into dc, odd, and even components. The flux is bilateral symmetric since the superimposed flux is identical when even components reverse. However, the flux density is not uniform on the legs. Specifically, the outer columns' magnetic flux density is higher than the inner columns. This feature results in heat generation differences. It benefits the magnetic component's heat dissipation since the heat convection on the outer surface is stronger than on the inner surface. In the proposed topology, the resonant winding L_{f1} and L_{f2} share one dc input winding L_{dc}, which is different from the conventional T-network-based push–pull inverters [26].

Generally, the core losses are dominated by high-frequency fluxes. Since the common point is equivalently shorted as in Fig. 1(c), the dc input inductor withstands no differential-mode switch voltages, mainly comprising fundamental and third-order harmonics. In contrast, the second-order harmonic voltage of C_{2nd} is applied on the dc-feed winding. With a proper k_f, the induced second-order flux in the dc-feed winding has a much lower amplitude than the odd flux in conventional separated dc-feed inductors. Thus, sharing one dc-feed winding helps to reduce core losses. By sharing the cores, all three windings have

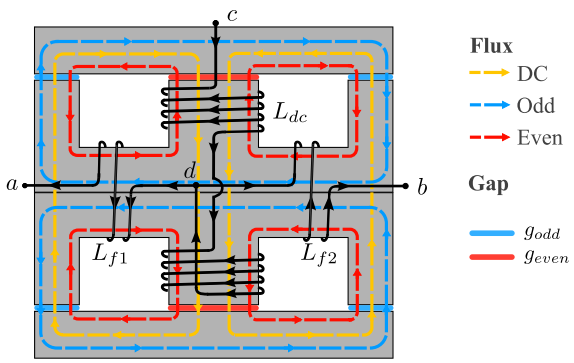


Fig. 6. Proposed three-winding magnetic structure with back-to-back EI cores. The L_{f1} and L_{f2} have a coupling coefficient of $k_f < 0$. The I-type cores can be optionally removed without changing the basic concept of this structure.

a larger, effective cross-sectional area (A_e) than the conventional discrete inductors. Besides, the dc flux in the shared part of the EI cores is partially canceled where the flux bias generated by L_{dc} is opposite to that of L_{f1} and L_{f2}. The even and odd fluxes are also partially canceled on the inner legs. Therefore, the magnetic integration approach can reduce the overall volume and losses of the cores.

Normally, the winding inductance can be estimated according to basic magnetic circuits. As in Fig. 6, assuming the magnetic structure has side-leg gaps g_{odd} and center-leg gaps g_{even}, and the E cores have identical A_e on the center legs and half of that on side legs. Hence, the coupling coefficient $k_f \approx -g_{\text{even}}/(g_{\text{even}} + 2g_{\text{odd}})$. The actual coupling is affected by the shape and permeability of the cores.

To implement the inverter, a particular L_{odd}, which is calculated by q and p_r, is required to meet the parameter sets in Table I. Considering $L_{\text{odd}} = (1 - k_f)L_f$, using a negative k_f can lower the required L_f and reduce the winding loss. The L_f can be roughly estimated by

$$L_f = \frac{L_{\text{odd}}}{1 - k_f} \approx N^2 \mu_0 \frac{A_e}{2} \left(\frac{1}{g_{\text{odd}}} + \frac{1}{g_{\text{odd}} + g_{\text{even}}} \right). \quad (24)$$

Considering the magnetic cores working at multiMHz usually have very low permeability, using (24) can result in larger values than the actual inductance of L_f. Hence, (24) can only be used for initial design. According to finite element method (FEM) simulations, the actual coupling is significantly affected by the shape and permeability of the cores. Moreover, when the I-type cores are removed, (24) is no longer applicable. Therefore, FEM simulation is preferred to estimate the inductance with higher accuracy. The value of L_{even} can be rewritten as

$$L_{\text{even}} = \frac{1 + k_f}{1 - k_f} \cdot L_{\text{odd}}. \quad (25)$$

The inductance L_{even} is compensated by C_{2nd} to short the second-order harmonic voltage. Thus, the value of L_{even} is not restrictive as it is compensated and the required second-order current is injected. Generally, using a smaller L_{even} will lower the second-order harmonic voltage across all the three windings, and reduces core losses. Hence, coupling the two L_f windings not only reduces the number and volume of the magnetic components, but also lowers the losses. Therefore, the proposed three-winding inverter provides a new feature that the introduced coupling k_f is able to adjust the harmonic voltages on the windings.

TABLE II
PARAMETERS OF CLASS-Φ_2 INVERTER AND ACTIVE RECTIFIER

L_{odd}	373 nH
L_x	43 nH
C_f	962 pF
Operation frequency	6.78 MHz
Duty cycle	0.35
Input voltage	48 V
Rated power	350 W

Ideally, L_{dc} should be sufficient to eliminate the input current ripples. Nevertheless, the actual input current contains second-order harmonic induced by $v_{C_{\text{2nd}}}$ due to the limited inductance of L_{dc}. To involve this effect in an actual design, (22) can be modified to a more accurate form given by

$$C_{\text{2nd}} = \frac{1}{(2\omega)^2} \cdot \frac{2L_{\text{dc}} + L_{\text{even}}}{2L_{\text{dc}}L_{\text{even}}} \quad (26)$$

where L_{dc} is in parallel with L_{even}. As analyzed previously, the proposed magnetic structure prevents the odd harmonic currents from passing the dc-feed winding, as shown in Fig. 1(c), where the common point is equivalently grounded. Therefore, the actual dc-feed winding current comprises additional second-order harmonic, while it has no odd-order components.

IV. EXAMPLE DESIGN AND IMPLEMENTATION OF CLASS-Φ_2 INVERTER AND ACTIVE RECTIFIER FOR MHZ-WPT

This section implements a 6.78-MHz WPT prototype to validate the proposed push–pull class-Φ_2 topology. As in Fig. 7, the system comprises the inverter and active rectifier, which are connected by a resistive-input resonant tank formed by *LCC*-S compensated coupling coils. The *LCC*-S resonant tank and the active rectifier's switching phase detector are based on the previous work in [15].

A. Three-Winding Push–Pull Class-Φ_2 Inverter

Fig. 8 shows the design flow of the proposed class-Φ_2 inverter. The inverter's circuit parameters are calculated according to (18)–(23) with specified input voltage and output power. The values of L_{odd} and L_{even} are determined by L_f and k_f. Load-independent operation can still be affected by the unrestricted L_{even} if the characteristic impedance $\sqrt{L_{\text{even}}/C_{\text{2nd}}}$ is too small and causes additional higher order harmonic currents. According to circuit simulations, the $|k_f|$ value should not be higher than 0.5.

As in Table II, the class-Φ_2 inverter is designed to process 350 W with 48 V on the dc side. To simplify the design, the active rectifier uses identical parameters. Considering the switch voltage stress as in Table I, the 150 V MOSFETs (BSC160N15NS5) are implemented for the inverter and active rectifier operating at a fixed duty cycle of 0.35. The peak switch voltage is about 2.157 times the dc input.

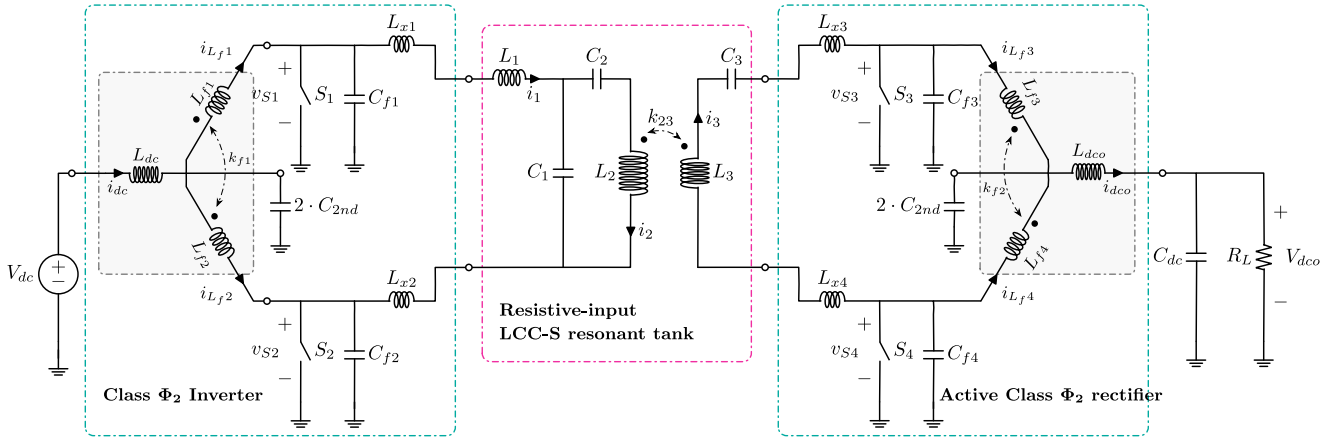


Fig. 7. *LCC*-S resonant MHz-WPT topology combined with the proposed three-winding class-Φ_2 inverter, along with the resistive-input resonant tank and active class-Φ_2 rectifier. The additional inductance L_x is merged with the resonant tank by using two toroids T9.5/4.8/3.2 of Fair-Rite 67 material.

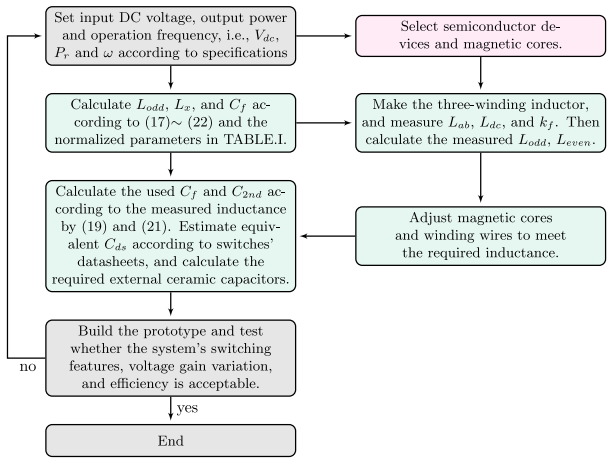


Fig. 8. Design flowchart of the proposed push–pull class-Φ_2 inverter.

The implemented three-winding inductor comprises two E-type cores, while the I-type cores in Fig. 6 are removed to simplify the magnetic structure and get the required inductance. As analyzed previously, the design principle of the implemented inductor is identical to the proposed magnetic structure in Fig. 6. As the operating frequency reaches 6.78 MHz, using Litz wires will no longer reduce the winding losses compared with solid wires. Thus, the windings are made of solid wires. Considering the proximity effect between winding turns, the wire diameter should be adjusted to reduce the high-frequency eddy current losses. The windings also left a small distance from each other to lower the proximity effect. Eventually, the $L_{\rm dc}$ is made by eight turns (four for each E core) solid wire of 0.9-mm diameter, whereas L_{f1} and L_{f2} are made by two turns wire of 1.2-mm diameter, as in Fig. 9.

The actual $L_{\rm odd}$ is obtained by measuring the inductance between terminal a and b, i.e., $L_{ab} = 2L_{\rm odd}$. Thus, the k_f can be calculated according to (24). Then, $L_{\rm even}$ and $C_{\rm 2nd}$ are given by (25) and (26). The measured $L_{ab} = 735$ nH, $L_{ad} = L_{bd} = 275$ nH, $L_{\rm dc} = 1.08\,\mu$H, and $k_f \approx 0.34$. According to the decoupling circuits, the measured L_f, $L_{\rm odd}$, and $L_{\rm even}$ are 275, 368, and

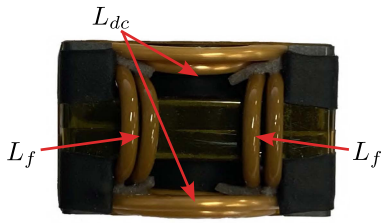


Fig. 9. Implemented three-winding integrated inductor using two EQ20/14/6.4 magnetic cores of Fair-Rite 67 material.

183 nH, respectively. The estimated $C_{\rm 2nd} \approx 750$ pF is implemented by two ceramic capacitors of 470 and 270 pF.

Due to the nonlinear parasitic capacitance of the MOSFETs, an equivalent drain-source capacitor $C_{\rm ds}$ should be estimated and combined with the used ceramic capacitors to construct C_f. According to SPICE-based simulation, $C_{\rm ds}$ can be approximately calculated by

$$C_{\rm ds} \approx \frac{2 \cdot \int_0^{V_{\rm ds,peak}} v \cdot C_{\rm oss}(v) dv}{V_{ds,\rm peak}^2} \tag{27}$$

where output capacitance $C_{\rm oss}$ is extracted from the datasheet. $V_{\rm ds,peak}$ is the peak $V_{\rm ds}$[29]. Thus, the estimated $C_{\rm ds}$ is about 550 pF, and the external capacitance is about 400 pF for each switch device.

Fig. 10 shows the implemented printed circuit board (PCB) for both the inverter and the active rectifier. The driving pulses of 0.35 duty cycle are generated by retriggerable monostable multivibrators, which are driven by the digital oscillator of the inverter or the synchronous switching signal of the active rectifier. The driving pulse circuit and gate drivers (1EDN7512) are powered by an external dc source. The overall driving loss is about 1.92 W for each PCB.

B. Resistive-Input Active Class-Φ_2 Rectifier and LCC-S Resonant Tank

As previously analyzed, the inverter maintains a constant phase shift ϕ during load-independent operation. When the

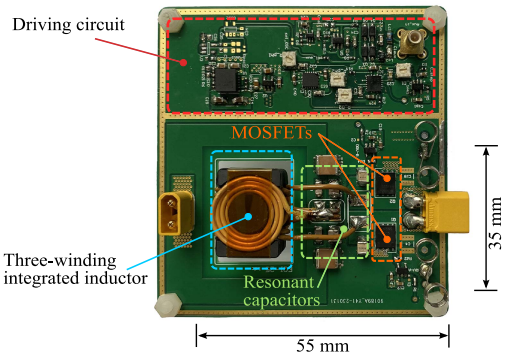


Fig. 10. PCB for the class-Φ_2 inverter and active rectifier.

inverter works as an active rectifier, the switching phase remains unchanged. The synchronous switches' driving pulses can be generated using a phase detector with a constant phase shift from the rectifier's alternating input current. Meanwhile, the rectifier maintains resistive input irreverent to load variation.

The *LCC*-S compensated coupling coils are used to link the inverter and active rectifier. Compared with the simple series–series compensation, the *LCC*-S network offers a load-independent resistive input for the proposed inverter. The transmitter still works normally when the receiver is removed. Typically, coupling coils with series–series compensation cannot function at the unloaded condition because the removal of the receiver results in a reduction in the inverter's output.

In the experiment setup, the *LCC*-S resonant tank and the phase detector are based on our previous work [15], which includes the detailed design process. Thus, only simplified results are described here. The phase detector generates the driving pulses with a constant phase shift from the alternating input current, where the switching phase is synchronized by an auxiliary coil integrated into the receiving coil.

As in Fig. 7, the parameters of the rectifier are identical to the inverter, as in Table II. The rectifier has a resistive input impedance given by $2G_v^2 R_L$. The *LCC*-S compensated network has three resonant loops constructed by $L_{1\text{–}3}$ and $C_{1\text{–}3}$. By resonating at 6.78 MHz, the *LCC*-S tank realizes a constant voltage gain given by $G_{LCC\text{-S}} = \frac{k_{23}\sqrt{L_2 L_3}}{L_1}$. Thus, the inverter's load can be calculated by

$$R_{\text{ac}} = \frac{2G_v^2 L_1^2}{M_{23}^2} \cdot R_L \tag{28}$$

where $M_{23} = k_{23}\sqrt{L_2 L_3}$ is the mutual inductance of the coupling coils. The inverter maintains a resistive load at different loads. Furthermore, the *LCC*-S tank functions as a filter by minimizing harmonic contents and offering a preferred load resistance for the load-independent class-Φ_2 inverter.

V. Experimental Measurement and Analysis

Fig. 11 shows the experiment setup of the MHz-WPT prototype, comprising the inverter, the active rectifier, and the *LCC*-S resonant tank. All experimental results are measured under open-loop operation, since feedback control is unnecessary for load-independent operation. The coupling coils are adjusted to a fixed coupling coefficient to realize a conversion ratio of about 48 to 48 V. The switches operate at 6.78 MHz with a duty cycle of 0.35. When the output power varies, the output voltage is fixed at 48 V by slightly adjusting the input voltage.

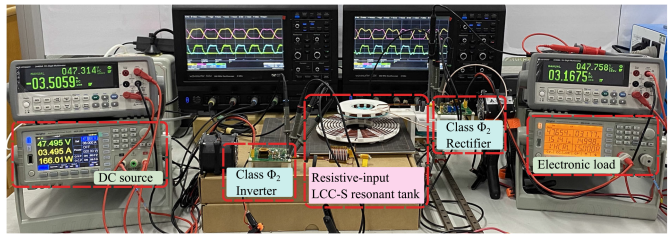


Fig. 11. Experiment setup.

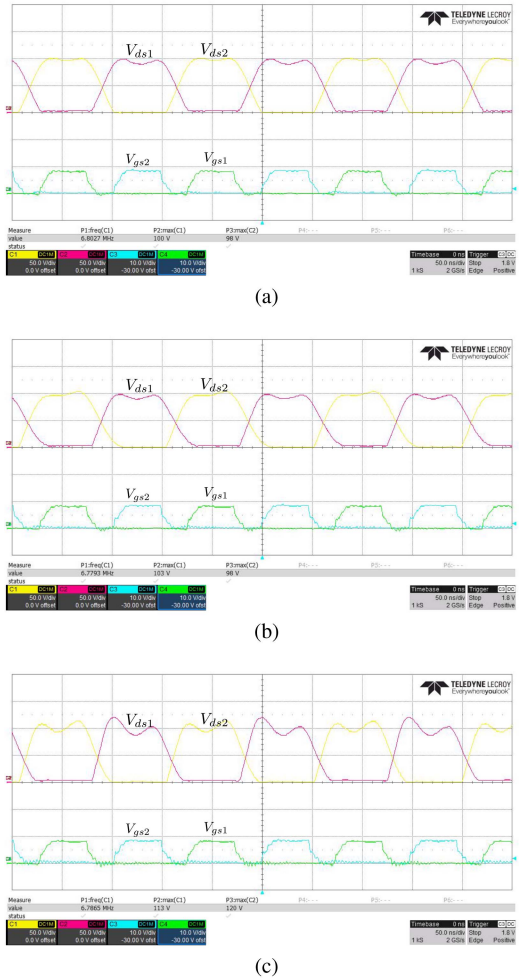
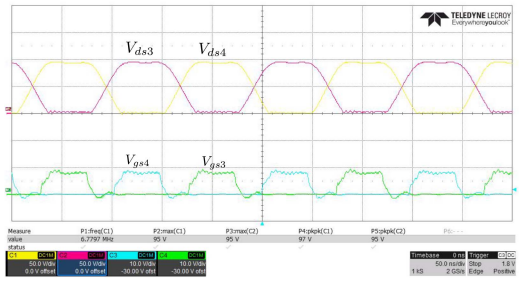
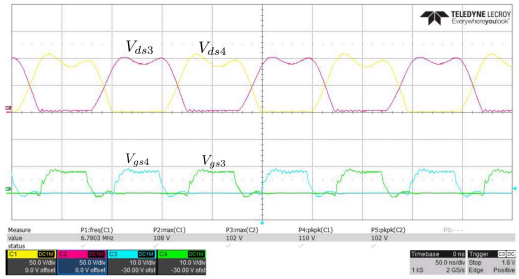


Fig. 12. Measured V_{ds} and V_{gs} of the inverter varies with output power P_{out}. (a) $P_{\text{out}} = 0$ W. (b) $P_{\text{out}} = 150$ W. (c) $P_{\text{out}} = 320$ W. The switches perform robust ZVS turn-ON over the entire load range.

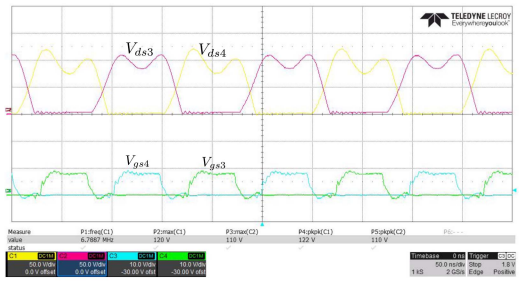
Fig. 12 shows the measured V_{ds} and V_{gs} of the class-Φ_2 inverter at various loads. The switching speed of Si MOSFETs is relatively slow at 6.78 MHz, a clear interval exists between the Miller plateau and the fully ON-state of the switches. This phenomenon is also observed under no-load conditions. The measured V_{gs} and V_{ds} indicate that the switches maintain ZVS over the entire load range. When the output power reaches 320



(a)

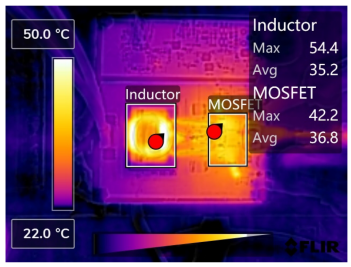


(b)

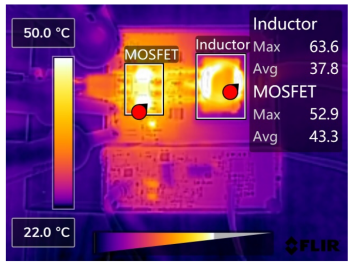


(c)

Fig. 13. Measured $V_{\rm ds}$ and $V_{\rm gs}$ of the active push–pull class-Φ_2 rectifier. (a) $P_{\rm out} = 0$ W. (b) $P_{\rm out} = 150$ W. (c)$P_{\rm out} = 320$ W. The switches maintain ZVS over the entire load range.



(a)



(b)

Fig. 14. Steady thermal images at 360 W input to 320 W output. (a) Inverter. (b) Active rectifier. The total losses are dominated by the switches and the inductors.

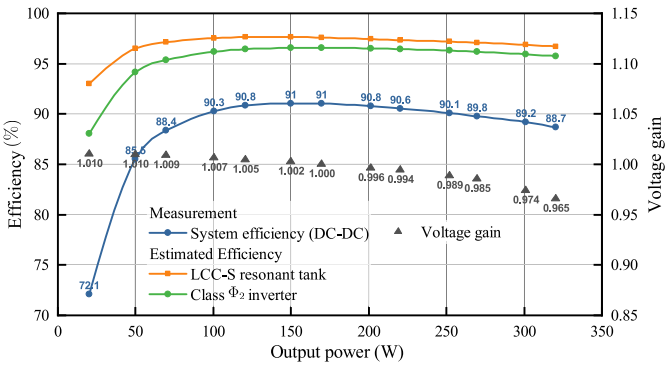


Fig. 15. Efficiencies and voltage gain.

W, corresponding to an input power of about 360 W, the ZVS turn-ON is not distinctly lost. Thus, the inverter performs robust soft switching. In addition, higher output power results in an increase in peak switch voltage. This trend is consistent with the theoretical results in Fig. 3. The $V_{\rm ds}$ is below 120 V over the entire load range and is close to the calculated peak voltage of 107 V. Due to the nonlinear parasitic capacitance, the measured switch voltage differs slightly from the theoretical calculation. As in Fig. 13, the active rectifier's $V_{\rm ds}$ is nearly symmetric to that of the inverter. Meanwhile, the synchronous switches maintain ZVS turn-ON over entire output power range from no load to 320 W.

Fig. 14 shows the steady-state thermal images at 360 W input and 320 W output, respectively. Air-cooling fans are implemented to limit the prototype's temperature rise. There is no heat sink on the MOSFETs. The overall temperature rise is mainly influenced by the power dissipation of the switches and the inductor. The inverter's MOSFETs show a maximum temperature of 42.2 °C, while the inductor has a higher value of 54.4 °C. For the active rectifier, the maximum temperatures are 52.9 °C and 63.6 °C. The average switch temperature exhibited a difference of about 6.5 °C between the inverter and the rectifier, whereas the difference in temperature between the inductors was relatively small. The difference in loss of the MOSFETs is the primary cause of the temperature difference. Although the design of the inverter and rectifier is identical, their switching behavior differs in terms of turn-ON current and driving phase shift. A SPICE-based simulation is implemented to validate this qualitative analysis. The SPICE models of MOSFETs (BSC160N15NS5) and driver IC (1EDN7512) are provided by the manufacturer. The inverter's input voltage and power are set to 49.6 V and 360 W to replicate the measured operating conditions. The output power and voltage of the rectifier are 320 W and 48 V. Each MOSFETin the inverter has a simulated loss of 1.205 W. The loss of each synchronous switch for the rectifier is 1.642 W, which is about 1.4 times that of the inverter. The significant difference in loss can be attributed to the difference in switching phase and current, as validated by the circuit simulation.

Fig. 15 shows the prototype's efficiencies and dc–dc voltage gain. The output voltage is fixed at 48 V by slightly adjusting

TABLE III
PERFORMANCE COMPARISON OF RECENT RESEARCH ON HIGH-FREQUENCY INVERTERS

Reference	Topology	Frequency	Output power	Efficiency	Input voltage	Voltage stress	Voltage gain	Number of inductors
2015 [23]	Single-end class-Φ_2	27.12 MHz	25 W	≈ 90%	30 V	≈65 V	–	2
2018 [14]	Single-end class-EF	13.56 MHz	150 W	94%	96 V	≈220 V	–	2
2020 [26]	Series-stacked PPT class-Φ_2	6.78 MHz	312 W	96%	100 V	≈105 V	≈1	4
2022 [15]	Push–pull class-E	6.78 MHz	320 W	95.6%	48 V	≈ 200 V	3.1	1
2022 [25]	Push–pull class-Φ_2	6.78 MHz	277 W	87%	50 V	≈100 V	–	4
2022 [27]	PPT class-Φ_2	12.56-18.06 MHz	300 W	93%	50 V	≈105 V	≈2	4
This work	Push–pull class-Φ_2	6.78 MHz	320 W	96.6%	48 V	≈110 V	2.4	1

[a] Note that the output filter inductors are excluded from inductor count since they are usually implemented by the coupling coils in WPT applications.

the input voltage. The maximum system efficiency of 91% is achieved across 150–170 W output. The efficiency calculation excludes the measured driving loss of 1.93 W per PCB. The measured dc–dc voltage gain, i.e., $V_{\rm dco}/V_{\rm dc}$, is near constant, varying within +1%/-3.5% over the entire load range. The prototype exhibits the predicted load-independent operation, achieving a stable voltage gain and robust ZVS, regardless of load variation.

In order to evaluate the inverter's performance, estimated efficiencies are also given in Fig. 15. The transfer efficiency of the *LCC*-S resonant tank can be calculated according to the measured inductance and the equivalent series resistance (ESR) at 6.78 MHz. The resonant tank is constructed by air-core coupling coils and high-quality ceramic capacitors. Since the used capacitors (ATC100B) have significantly higher quality factors than the coupling coils, the effect of nonlinear dielectric loss on link efficiency is negligible. The air-core coils' losses can be affected by temperature rise. Nonetheless, the temperature rise of the coupling coils is below 10°C because of the ample cooling surfaces. Given that the temperature coefficient of copper resistance is approximately 0.0039/°C, the ESRs of the coupling coils remain nearly constant. Therefore, the small signal measurement is valid for efficiency estimation.

The diameters of the transmitting and receiving coils are 16 and 10 cm, respectively. The measured quality factors of $L_{1\text{–}3}$ are 300, 371, and 446 at 6.78 MHz, respectively. The coupling coefficient k_{23} is fixed at about 0.26 to achieve the expected dc–dc conversion ratio. The link efficiency is calculated according to the *LCC*-S tank's quality factors, coupling coefficient, and load resistance [15]. The peak efficiency of the prototype is 91%, which corresponds to the maximum link efficiency of 97.6%.

As mentioned previously, although the inverter and the active rectifier have identical parameters, the inverter's efficiency is higher than that of the rectifier according to thermal measurement. Thus, the achievable efficiency of the inverter can be estimated by assuming the inverter and rectifier have the same efficiency. The estimated value is convincing since the inverter's efficiency is expected to be higher. The assumption cannot be applied to evaluate the rectifier due to its lower efficiency compared with the inverter. The estimated drain efficiency of the proposed class-Φ_2 inverter reaches 96.6% at 170 W output, and it stays above 95% over the power range of 70 to 320 W.

Table III compares this work and recent research on high-frequency inverters. The proposed push–pull class-Φ_2 inverter is characterized by the magnetic integration of the inductors. The number of inductors is even less than that of the single-end class-EF inverter. Meanwhile, the proposed inverter retains the advantages of the conventional class-Φ_2/EF$_2$ inverters, i.e., low-voltage stress and high efficiency.

VI. CONCLUSION

The proposed three-winding push–pull class-Φ_2 inverter offers a reduced number of magnetic components compared with the conventional class-EF$_2$ and class-Φ_2 inverters, enabling robust soft switching across various loads. The analytical model presented in this study provides a concise and straightforward approach for designing the proposed class-Φ_2 inverter, ensuring load-independent operation characterized by wide-load-range soft switching and constant voltage gain. A magnetic structure is introduced to implement the three-winding integrated inductor, which effectively reduces the size of magnetic components compared with the conventional approaches. In order to validate the performance of the proposed class-Φ_2 inverter and the magnetic structure, a 6.78-MHz *LCC*-S resonant WPT prototype is constructed. The experimental results demonstrate that the prototype achieves robust soft switching across the entire load range, from no load to 320 W output. Moreover, the voltage gain remains nearly constant with a variation within +1%/-3.5%. The measured dc–dc peak efficiency reaches 91% at 170 W output. The estimated peak efficiency of the class-Φ_2 inverter reaches 96.6% at 170 W output and remains above 95% over a wide power range spanning from 70 to 320 W.

REFERENCES

[1] H. Zhang, Y. Shao, N. Kang, H. Qin, C. Ma, and M. Liu, "A vertically modularized reconfigurable wireless power transfer system: Architecture, modeling, and design," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 2730–2742, Feb. 2023.

[2] J. Li, R. Qin, J. Sun, and D. Costinett, "Systematic design of a 100-W 6.78-MHz wireless charging station covering multiple devices and a large charging area," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4877–4889, Apr. 2022.

[3] R. Qin, J. Li, and D. Costinett, "A 6.6-kW high-frequency wireless power transfer system for electric vehicle charging using multilayer nonuniform self-resonant coil at MHz," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4842–4856, Apr. 2022.

[4] C. R. Teeneti, T. T. Truscott, D. N. Beal, and Z. Pantic, "Review of wireless charging systems for autonomous underwater vehicles," *IEEE J. Ocean. Eng.*, vol. 46, no. 1, pp. 68–87, Jan. 2021.

[5] S. Wu, C. Cai, L. Jiang, J. Li, and S. Yang, "Unmanned aerial vehicle wireless charging system with orthogonal magnetic structure and position correction aid device," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7564–7575, Jul. 2021.

[6] Y. Zhang et al., "Integration of onboard charger and wireless charging system for electric vehicles with shared coupler, compensation, and rectifier," *IEEE Trans. Ind. Electron.*, vol. 70, no. 7, pp. 7511–7514, Jul. 2023.

[7] L. Gu, G. Zulauf, A. Stein, P. A. Kyaw, T. Chen, and J. M. R. Davila, "6.78-MHz wireless power transfer with self-resonant coils at 95% DC–DC efficiency," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2456–2460, Mar. 2021.

[8] B. Regensburger, S. Sinha, A. Kumar, S. Maji, and K. K. Afridi, "High-performance multi-MHz capacitive wireless power transfer system for EV charging utilizing interleaved-foil coupled inductors," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 1, pp. 35–51, Feb. 2022.

[9] H. Oh et al., "6.78 MHz wireless power transmitter based on a reconfigurable class–E power amplifier for multiple device charging," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5907–5917, Jun. 2020.

[10] M. Liu and M. Chen, "Dual-band wireless power transfer with reactance steering network and reconfigurable receivers," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 496–507, Jan. 2020.

[11] M. Fu, H. Yin, M. Liu, Y. Wang, and C. Ma, "A 6.78 MHz multiple-receiver wireless power transfer system with constant output voltage and optimum efficiency," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5330–5340, Jun. 2018.

[12] A. Ayachit, F. Corti, A. Reatti, and M. K. Kazimierczuk, "Zero-voltage switching operation of transformer class-E inverter at any coupling coefficient," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1809–1819, Mar. 2019.

[13] A. Lotfi et al., "Subnominal operation of class-E nonlinear shunt capacitance power amplifier at any duty ratio and grading coefficient," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 7878–7887, Oct. 2018.

[14] S. Aldhaher, D. C. Yates, and P. D. Mitcheson, "Load-independent class E/EF inverters and rectifiers for MHz-switching applications," *IEEE Trans. Power Electron.*, vol. 33, no. 10, 8270–8287, Oct. 2018.

[15] X. Huang, Z. Yu, Y. Dou, S. Lin, Z. Ouyang, and M. A. E. Andersen, "Load-independent push–pull class E^2 topology with coupled inductors for MHz-WPT applications," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8726–8737, Jul. 2022.

[16] M. Hayati, S. Roshani, M. K. Kazimierczuk, and H. Sekiya, "A class-E power amplifier design considering MOSFET nonlinear drain-to-source and nonlinear gate-to-drain capacitances at any grading coefficient," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7770–7779, Nov. 2016.

[17] S. Aldhaher, D. C. Yates, and P. D. Mitcheson, "Modeling and analysis of class EF and class E/F inverters with series-tuned resonant networks," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3415–3430, May 2016.

[18] J. W. Phinney, D. J. Perreault, and J. H. Lang, "Radio-frequency inverters with transmission-line input networks," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1154–1161, Jul. 2007.

[19] J. M. Rivas, Y. Han, O. Leitermann, A. D. Sagneri, and D. J. Perreault, "A high-frequency resonant inverter topology with low-voltage stress," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1759–1771, Jul. 2008.

[20] Z. Kaczmarczyk, "High-efficiency class E., EF_2, and E/F_3 inverters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1584–1593, Oct. 2006.

[21] S. D. Kee, I. Aoki, A. Hajimiri, and D. Rutledge, "The class-E/F family of ZVS switching amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 6, pp. 1677–1690, Jun. 2003.

[22] I. Nikiforidis, J. M. Arteaga, C. H. Kwan, N. Pucci, D. C. Yates, and P. D. Mitcheson, "Generalized multistage modeling and tuning algorithm for class EF and class Φ inverters to eliminate iterative retuning," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12877–12900, Oct. 2022.

[23] L. Roslaniec, A. S. Jurkov, A. A. Bastami, and D. J. Perreault, "Design of single-switch inverters for variable resistance/load modulation operation," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3200–3214, Jun. 2015.

[24] S. Aldhaher, P. D. Mitcheson, and D. C. Yates, "Load-independent class EF inverters for inductive wireless power transfer," in *Proc. IEEE Wirel. Power Transfer Conf.*, 2016, pp. 1–4.

[25] M. Kim and J. Choi, "Design of robust capacitive power transfer systems using high-frequency resonant inverters," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 3, no. 3, pp. 465–473, Jul. 2022.

[26] L. Gu, G. Zulauf, Z. Zhang, S. Chakraborty, and J. Rivas-Davila, "Push–Pull class Φ_2 RF power amplifier," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10515–10531, Oct. 2020.

[27] Z. Tong, L. Gu, and J. Rivas-Davila, "Wideband PPT class Φ_2 inverter using phase-switched impedance modulation and reactance compensation," *IEEE Trans. Ind. Electron.*, vol. 69, no. 6, pp. 5724–5734, Jun. 2022.

[28] J. S. Glaser and J. M. Rivas, "A 500 W. push-pull dc-dc power converter with a 30 MHz switching frequency," in *Proc. IEEE Appl. Power Electron. Conf.Expo.*, 2010, pp. 654–661.

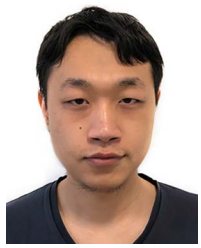
[29] Y. Dou, X. Huang, Z. Ouyang, and M. A. Andersen, "Modelling and compensation design of class-E rectifier for near-resistive impedance in high-frequency power conversion," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8812–8823, Aug. 2021.

Xiaosheng Huang (Member, IEEE) received the B.E. and Ph.D. degrees in electrical engineering from Fuzhou University, Fuzhou, China, in 2009 and 2015, respectively.

He is currently an Associate Professor with the School of Electronic, Electrical Engineering and Physics, Fujian University of Technology, Fuzhou. He is a Member of the Magnetic Component Specialty Committee of the China Power Supply Society. His research interests include power conversion, high-frequency magnetics, wireless power transfer, and electromagnetic field analysis and applications.

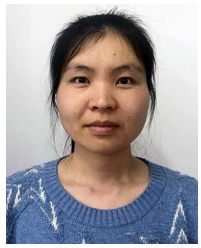
Yongshu Lin received the B.E. degree in electrical engineering from the Taizhou Institute of Science and Technology, Jiangsu, China, in 2020. He is currently working toward the M.E. degree with the School of Electronic, Electrical Engineering and Physics, Fujian University of Technology, Fuzhou, China.

His research interests include wireless power transfer and optimization of high-frequency magnetics.



Yi Dou (Member, IEEE) received the M.Sc. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2018 and 2022, respectively.

He is currently a Senior Engineer in power electronics with Resonant Link Inc., focusing on research and development in wireless power transfer systems for implanted medical devices. His research interests include the design of high frequency dc–dc converters, modeling and design of magnetic components, and modeling and optimization of MHz-range wireless power transfer systems.



Shuyi Lin received the B.E. and Ph.D. degrees in electrical engineering from Fuzhou University, Fuzhou, China, in 2008 and 2014, respectively.

She is currently an Associate Professor with the School of Electronic, Electrical Engineering and Physics, Fujian University of Technology, Fuzhou. Her research interests include power conversion, high-frequency magnetics, and wireless power transfer.

Jing Huang received the B.E. and M.Sc. degrees in electrical engineering from Fuzhou University, Fuzhou, China, in 1996 and 2006, respectively.

He is currently a Professor with the School of Electronic, Electrical Engineering and Physics, Fujian University of Technology, Fuzhou, where he is also the Director with the Fujian Provincial University Engineering Research Center for Industrial Automation. His research interests include intelligent control technology and power electronics technology.