Hybrid Isolated Modular Multilevel Converter Based Solid-State Transformer Topology With Simplified Power Conversion Process and Uneven Voltage Ratio

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***Abstract*—This article proposes a novel triple-port solid-state transformer (SST) topology based on a hybrid isolated modular multilevel converter (MMC), which overcomes the limitation of voltage ratio $R_{(\mathrm{pu})}$ in the conventional MMC-based SST. By integrating a high-frequency link into the MMC structure and applying various types of isolated submodule (ISM), the proposed SST can function as a step-down rectifier, where $U_{\mathrm{MVDC}} < U_{\mathrm{MVAC(p\text{-}p)}}$. In this case, the power electronics converters used to connect downstream medium-voltage direct current (MVdc) link and distributed energy resources or battery storage require fewer active devices and may minimize the cost of protection equipment. In addition, the proposed SST retains the significant advantages of single-stage SSTs, such as single-stage power conversion, saving capacitor, and a simple control system. First, the topology and modulation strategy of two types of ISMs are discussed. In addition, this article provides a detailed analysis of operation principles, power flow, grid-tied control, and system reliability. Moreover, the proposed converter is compared with other SST topologies in terms of key performance indicators, such as peak efficiency, system volume, and number of active semiconductor devices. Finally, a 300-V/20-kW scaled-down prototype is developed, and the experimental results demonstrate the performance and verify the correctness of the proposed converter.**

***Index Terms*—Medium voltage direct current (MVdc), modular multilevel converter (MMC), single-stage power conversion, solid-state transformer (SST), uneven voltage ratio.**

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I. Introduction

A SOLID-STATE transformer (SST), also known as a power electronic transformer, is a power electronic interface between a medium-voltage (MV) and a low-voltage (LV) system, which utilizes a large number of active power devices in combination with high-frequency transformers (HFTs) [1], [2], [3]. It enables full-range control of terminal voltage and current and, thus, active and reactive power flows. Therefore, it has been considered for replacing line-frequency transformers (LFTs) in MV high-power applications, such as traction on-board applications, where volume and weight savings can be achieved, or in smart grids because of their controllability [4], [5].

Numerous SST systems generally adopt modular multilevel configurations based on input-series and output-parallel (ISOP), which address the MV application issues by sharing the voltage and power in series connections [6]. Until today, a large variety of SST topologies have been proposed by both industry and academia. Most of the existing literature dealing with various SST-related topologies for MV high-power applications can be broadly categorized into either single-stage SST [7], [8], [9] or two-stage SST solutions [10], [11], [12], [13], [14] (the LVac port is not discussed in this article). As shown in Fig. 1(a), the typical cascaded submodule (SM) topology of single-stage SST adopts a direct matrix ac–ac converter on the MV side. It avoids the need for an individual capacitor on the dc link, resulting in a reduced volume [7]. However, this topology needs a complex switching method to alleviate the voltage oscillations or current spikes during the commutation process caused by the use of bidirectional switches [15].

As shown in Fig. 1(b), the typical cascaded SM topology of two-stage SST topologies generally has two dc links that achieve power quality regulation and also facilitate the integration of renewable energy and energy storage systems (ESS) for smart grid applications [13]. Due to its advanced control function features, the two-stage SST topology obtains the most popularity in research compared to other SST topologies [10], [12]. The most common two-stage SST could be classified into two categories: the cascaded H-bridge (CHB) based SST and the modular multilevel converter (MMC) based SST. The MMC-based SST can be seen as an evolution of the CHB [11],

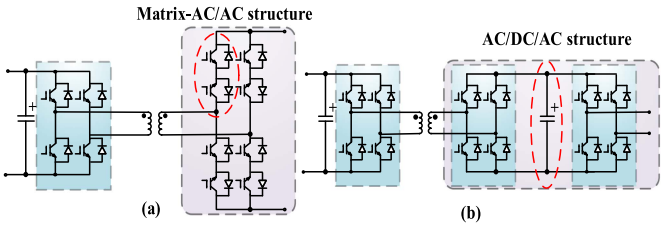

Fig. 1. Typical SM topology of SST. (a) Two-stage ac–dc–ac structure. (b) Single-stage direct matrix ac–ac structure.

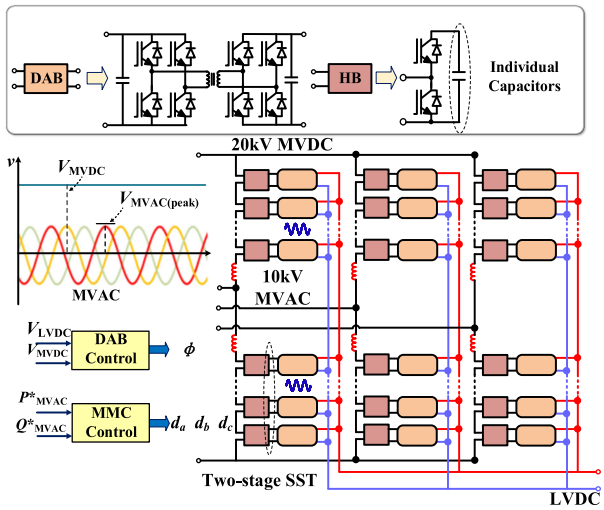

Fig. 2. Schematic of the conventional MMC-based SST.

and the major advantage is the MVdc link as a flexible point that connects the utility grid and new dc sources or loads, such as fast charging electric vehicle stations and distributed renewable energy. Consequently, it has emerged as an effective choice for establishing MVdc distribution systems. This article mainly focuses on MMC-based SST (without considering CHB-based SST) as the main topology research object.

For MVdc applications, the use of MVdc systems at the 5 kV to 35 kV level (or even higher depending on the power rating) covers a wide range of applications, including the well-known 3 kV railway networks, 6 kV power systems on ships, dc collection grids, and even MVdc transmission [3], [16], [17], [18], [19], [20]. In the conventional MMC-based SST, the limitation of the voltage ratio between MVdc and MVac is an easily overlooked issue. The schematic of conventional MMC-based SSTs interfacing MVdc and MVac is depicted in Fig. 2. In the design of conventional MMC [21], [22], the voltage ratio indicates the proportion of dc bus voltage used to create ac voltage. If triple harmonics of the phase voltage are not considered, this voltage ratio is identified as follows:

$$R_{(\mathrm{pu})} = \frac{2\left|V_{\mathrm{ac(peak)}}\right|}{V_{\mathrm{MVDC}}} \tag{1}$$

where V_{MVDC} is the voltage amplitude of the MVdc bus, $V_{\mathrm{ac(peak)}}$ is the peak value of the MVac utility grid, and $R_{(\mathrm{pu})}$ is the voltage ratio.

Generally, the $R_{(\mathrm{pu})}$ in the conventional MMC is less than one. The lower $R_{(\mathrm{pu})}$ indicates insufficient utilization of the SMs used to generate the MVac voltage. On the contrary, if $R_{(\mathrm{pu})}$ is close to one, it indicates that the SMs are being used more effectively [11]. Taking into account the voltage level of the utility grid and the safety margin, the value of $R_{(\mathrm{pu})}$ in the conventional MMC is 0.95. It indicates that the voltage amplitude of the MVdc bus must be at least twice that of the utility grid side, even if such a voltage level is not required. Therefore, a high-gain dc/dc transformer (DCT) and high-performance dc circuit breakers are required, which create design and cost issues for MVdc systems. In [23], a step-down LFT is used for the MMC port so as to obtain the desired voltage amplitude on the MVdc side. However, it will inevitably increase the system's volume and weight. In [24], it first analyzed the advantages of MMC based on a full-bridge structure operating as a step-down rectifier with uneven $R_{(\mathrm{pu})}$, where $U_{\mathrm{MVDC}}<U_{\mathrm{MVAC(p\text{-}p)}}$. It connects directly to the MV utility grid and achieves a higher $R_{(\mathrm{pu})}$, thereby reducing the cost of ultrafast charging stations. Therefore, breaking the $R_{(\mathrm{pu})}$ limitation of conventional MMC-based SST to realize the voltage level decoupling between MVac and MVdc ports may increase the degree of design freedom for certain system optimization applications.

On the other hand, the individual capacitor at the MV side is required to buffer the voltage fluctuation caused by inherent double-line frequency, which means that the bulky passive components account for a substantial portion of the size and limit the power density [25]. Recent research works [26], [27], [28], [29], [30], [31] have proposed single-stage SST topologies, which is an effective method for achieving compact design and increasing power density. In [26], [27], and [28], single-stage dc-ac converters give tough competition to SSTs and have proven to have high efficiency and power density. However, these converters are incapable of constructing MVdc links. In [29], the half-bridge (HB) SMs with mixed-frequency modulation are proposed to reduce the power conversion stage; however, more effective control strategies are required if the SM ripple is large. In order to avoid the complex voltage balance control of SM, the authors of [30] and [31] proposed the isolated submodule (ISM) based single-stage SST topology. The ISM's voltage can be effectively maintained at a stable value by the clamping effect of HFT. However, these ISM-based SST topologies still have the voltage ratio limitation and cannot be applied to some scenarios where voltage amplitudes do not match. The original contribution of this article is to achieve a higher voltage ratio while retaining the advantages of SSTs described in [30] and [31]. Therefore, this article proposes a novel triple-port single-stage SST with uneven $R_{(\mathrm{pu})}$, and the advantages are as follows.

1) The proposed SST can function as a step-down rectifier with uneven $R_{(\mathrm{pu})}$ to realize the decoupling design of MV ac/dc port voltage amplitude.
2) The individual capacitors of the SMs in the conventional MMC-based SST are totally eliminated.
3) The voltage balance of ISMs is realized naturally without any additional complex control strategy.

This article is organized as follows. Section II describes the system configuration and operation principles of the proposed

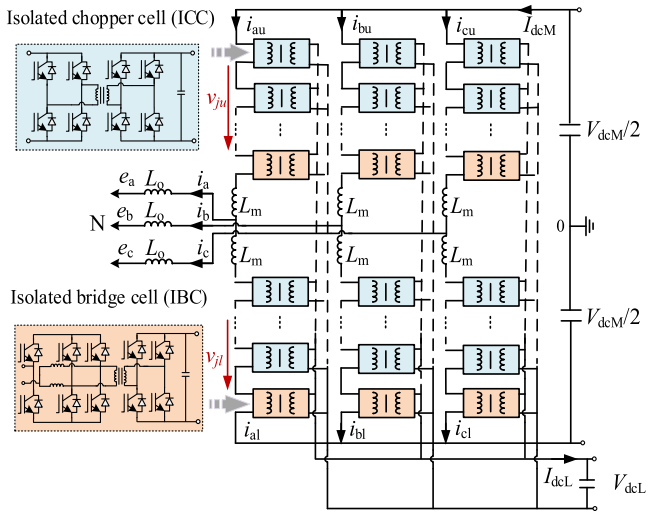

Fig. 3. Topology of the proposed three-phase HI-MMC system.

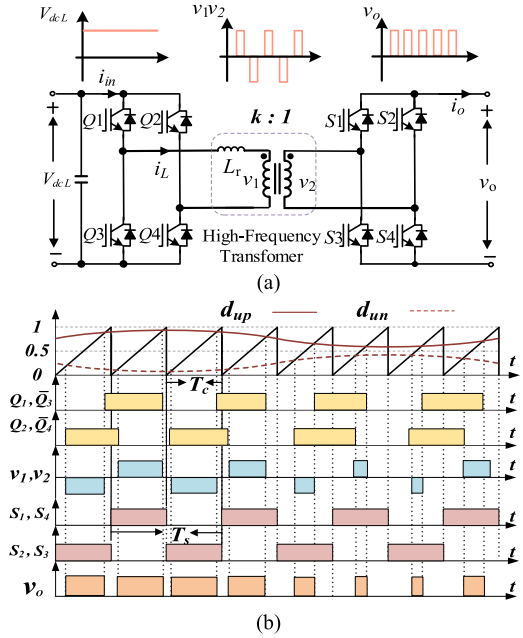

Fig. 4. (a) Topology structure of the ICC. (b) Modulation strategy of ICC in the upper arm.

hybrid isolated MMC (HI-MMC) based SST. The detailed analysis of power flow characteristics and steady-state operating boundaries is given in Section III. In Section IV, the detailed design methods of the control system, reliability analysis, and precharge circuit are illustrated. The full power simulation results are given in Section V. Finally, a 20-kW/300-V scaled-down experimental prototype and a comparison with respect to SST topologies are given in Section VI. The conclusion is given in Section VII.

II. System Structure and Operation Principle

As described in Fig. 3, all the ISMs are connected in parallel at the common LVdc side and in series at the MV side, respectively. To ensure HI-MMC has the ability to route energy, the proposed ISMs should have corresponding functions such as bidirectional free power flow and electrical isolation. Therefore, the design methods of ICC and IBC are introduced in this section, which include topology structure, modulation strategy, and equivalent average model.

A. Isolated Chopper Converter (ICC)

Compared with the resonant push–pull converter (RP^{2}C) in [30], the proposed HFL-SM in [31] totally eliminated the individual capacitors on the MV side. Therefore, HFL-SM is also adopted in the cascaded arm of the HI-MMC and is essentially a chopper converter working in buck or boost mode. Since the HFL-SM has the same output port characteristics as the HB, it is known as ICC. Fig. 4(a) depicts ICC's topology, which includes the primary full-bridge (Q_1–Q_4), the secondary full-bridge (S_1–S_4), and the HFT with the primary equivalent leakage inductor L_r. According to the direction of the current i_o, ICC can be divided into buck mode ($i_o>0$) and boost mode ($i_o<0$). No matter ICC works in which mode, a unified modulation strategy can be used, as shown in Fig. 4(b). It is worth noting that S_1–S_4 switches are always switched when the voltage v_o is zero, which avoids voltage spikes and oscillations in the commutation process. The specific working process of ICC will not be described in detail here [22]. The modulation signals of ICC in the upper arm and the lower arm can be expressed as follows:

$$\begin{cases} d_{up} = 0.5 + d_u = 0.5 + 0.5 \times (D + d_{a-C}) \\ d_{un} = 0.5 - d_u = 0.5 - 0.5 \times (D + d_{a-C}) \\ d_{lp} = 0.5 + d_l = 0.5 + 0.5 \times (D - d_{a-C}) \\ d_{ln} = 0.5 - d_l = 0.5 - 0.5 \times (D - d_{a-C}) \end{cases} \tag{2}$$

where $d_{up(n)}$ represents the leading-leg (lagging-leg) modulation signal for ICC in the upper arm, and $d_{lp(n)}$ represents the leading-leg (lagging-leg) modulation signal for ICC in the lower arm.

In addition, d_u and d_l should satisfy the following:

$$\begin{cases} d_u = D + d_{a-C} = 0.5 + d_{\text{am}}\sin(\omega t + \theta) \\ d_l = D - d_{a-C} = 0.5 - d_{\text{am}}\sin(\omega t + \theta) \end{cases} \quad (0 \le d_{u,l} \le 1). \tag{3}$$

For modeling simplicity, the following assumptions can be used: Switches are ideal, and there are no parasitic effects in switches; inductors and *LC* filters have low equivalent series resistance (ESR), which can be neglected; the load is a constant value, and an additional current source has been used to model the load change. If the dc modulation ratio D is generally set at 0.5, the amplitude of ac modulation ratio $d_{a\text{-}C}$ should satisfy $0 \le d_{\text{am}} \le 0.5$ to ensure a positive output voltage of the ICC. According to the above-mentioned equations, the output voltage of the ICC has dc and ac components at the same time. The secondary side can be regarded as a voltage source, whereas the primary side can be regarded as a current source. The average equivalent circuit models of ICC in the upper arm and lower arm are shown in Fig. 5.

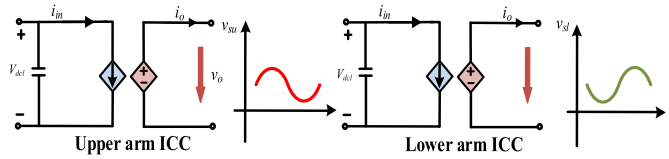

Fig. 5. Average equivalent model of ICC.

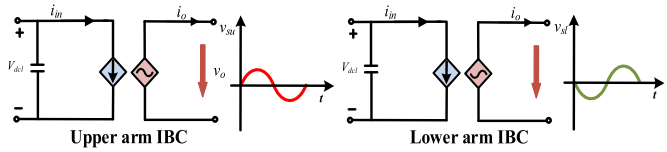

Fig. 7. Average equivalent model of IBC.

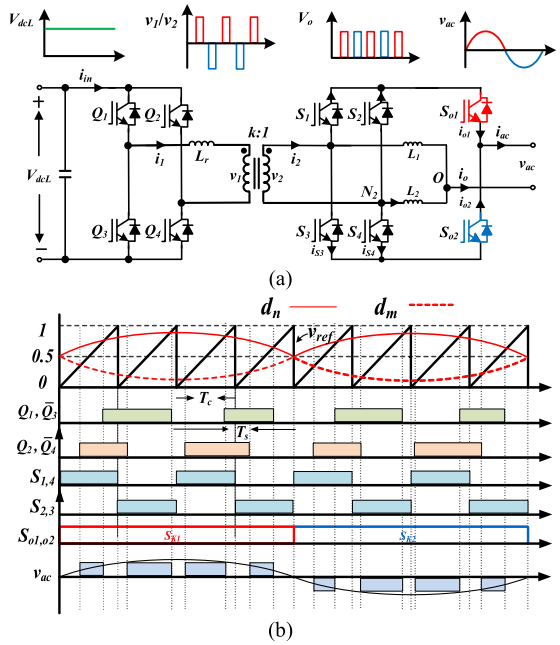

Fig. 6. (a) Topology structure of IBC. (b) Modulation strategy of IBC in the upper arm.

B. Isolated Bridge Converter (IBC)

The single-stage ac–dc topologies proposed in [26], [27], and [28] are not suitable for building hybrid cascaded arms with ICC in HI-MMC. Therefore, this article draws on the modulation ideas of single-stage ac/dc converters to construct an IBC topology, as shown in Fig. 6(a). A high-frequency isolated single-stage dc/ac converter known as an IBC is designed to obtain an uneven $R_{(\mathrm{pu})}$ and reduce the dc component of the output voltage on the cascaded arm. Similar to ICC, it consists of the primary full-bridge (Q_1–Q_4), the secondary full-bridge (S_1–S_4), and an HFT with the primary equivalent leakage inductor L_r. The turn ratio of the HFT is k, and two interleaved inductors (L_1, L_2) are connected to the secondary full-bridge middle point (N_1, N_2). An unfolder circuit (S_{o1}, S_{o2}) is adopted at last. Here, v_1 and v_2, i_1 and i_2, represent the voltage and current on the primary and secondary sides of the HFT, while v_ac and i_ac represent the voltage and current at the output. The dc-side voltage is $V_{\mathrm{dc}L}$.

The modulation strategy used in the proposed converter is shown in Fig. 6(b). Q_1–Q_4 and S_1–S_4 are driving signals of the corresponding insulated gate bipolar transistors (IGBTs); d_n and d_m are modulation waves of the leading and lagging bridge arms in the primary full bridge, respectively; v_ref represents the carrier signal. The switching cycle T_s is twice the carrier cycle T_c. As depicted, S_{o1} and S_{o2} are low-frequency (50 Hz) switches, which bring a low switching loss.

$$\begin{cases} d_n = 0.5 + 0.5 \times |d_{a-B}| \\ d_m = 0.5 - 0.5 \times |d_{a-B}| \quad (0 \le d_\mathrm{am} \le 1). \\ d_{a-B} = d_\mathrm{am} \sin(100\pi t) \end{cases} \tag{4}$$

The output voltage v_ac can be derived as follows:

$$v_\mathrm{ac} = \begin{cases} \frac{1}{2k} V_{\mathrm{dc}L} \times |d_{a-B}|, & S_{\mathrm{o}1} = 1 \\ \frac{-1}{2k} V_{\mathrm{dc}L} \times |d_{a-B}|, & S_{\mathrm{o}2} = 0 \end{cases}. \tag{5}$$

According to (5), the output voltage of the IBC consists of only ac components. The secondary side can be regarded as a voltage source, and the primary side can be regarded as a current source. The average equivalent model diagram of the IBC in upper arm and lower arm is shown in Fig. 7.

C. Operation Principle of HI-MMC

The conventional MMC-based SST can function properly without violating the voltage limit as the $R_{(\mathrm{pu})}$ value is less than one in the absence of additional devices. To achieve higher voltage ratios, the voltage amplitude of a cascaded arm requires more AC components. Based on the aforementioned designs of ICC and IBC, the relationship between the modulation ratio and the output voltage can be deduced without considering the leakage inductor as follows:

$$\begin{cases} V_{\mathrm{ICC}u} = \frac{V_{\mathrm{dc}L}}{k} \times (D + d_{a-C}) \\ V_{\mathrm{ICC}l} = \frac{V_{\mathrm{dc}L}}{k} \times (D - d_{a-C}) \end{cases} \quad \begin{cases} V_{\mathrm{IBC}u} = \frac{V_{\mathrm{dc}L}}{2k} \times d_{a-B} \\ V_{\mathrm{IBC}l} = -\frac{V_{\mathrm{dc}L}}{2k} \times d_{a-B} \end{cases}. \tag{6}$$

The proposed topology can achieve different $R_{(\mathrm{pu})}$ by adding different numbers of ISM in each cascaded leg. The following will demonstrate the operation principle of HI-MMC with different $R_{(\mathrm{pu})}$. The circuit model diagram of HI-MMC and the reference direction are noted in Fig. 8. According to the loop-voltage equations, if there are x ICCs and y IBCs in each cascaded leg, the output voltage of the MVdc and MVac ports can be calculated as follows:

$$\begin{aligned} V_\mathrm{MVDC} &= \sum_{i=1}^{n} (v_{ui} + v_{li}) = x \frac{V_{\mathrm{dc}L}}{k} \times D \\ v_\mathrm{MVAC} &= \sum_{i=1}^{n} v_{ui} - \frac{1}{2} V_\mathrm{MVDC} = \frac{-V_{\mathrm{dc}L}}{2k} (x d_{a-C} + y d_{a-B}). \end{aligned} \tag{7}$$

It can be seen from (7) that increasing the number of IBC can reduce the voltage amplitude at the MVdc port while maintaining

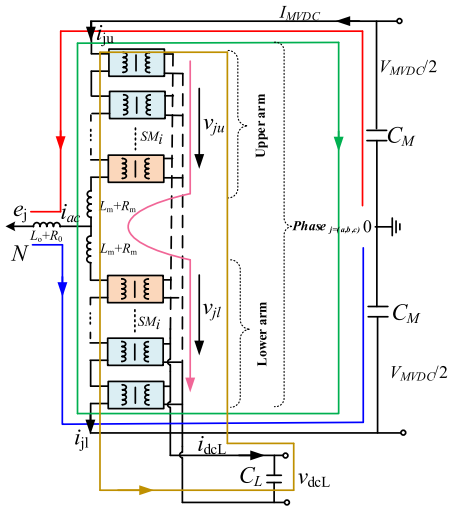

Fig. 8. Circuit diagram of HI-MMC.

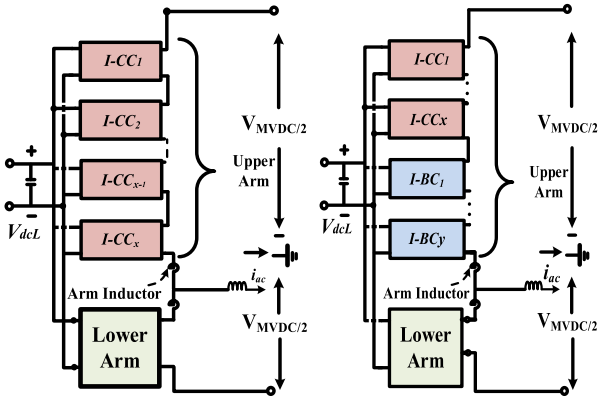

Fig. 9. Cascaded arm by adding different number of IBC.

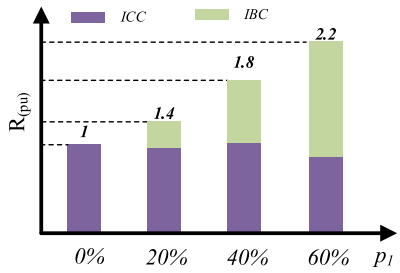

Fig. 10. $R_{(\mathrm{pu})}$ trend chart by adding different number of IBC.

the voltage level at the MVac port when the total number of ISM is fixed, as shown in Fig. 9.

In order to clearly see the growth trend of $R_{(\mathrm{pu})}$ with different numbers of ISM in the cascaded arm, the *y*/*x* is defined as p_1. Using the assumption that the modulation ratio amplitudes of D and d_{am} are set to 0.5, Fig. 10 depicts the relationships between $R_{(\mathrm{pu})}$ and p_1. If the cascaded arm contains only ICCs, $R_{(\mathrm{pu})}$ is close to one, and the output characteristics of triple-port HI-MMC are similar to the I-MCC-based SST proposed in [22]. As the number of IBCs increases, the $R_{(\mathrm{pu})}$ value will exhibit

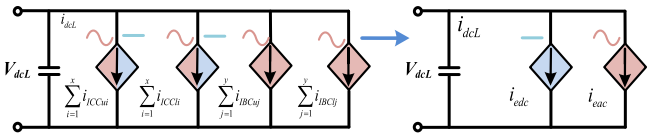

Fig. 11. Average equivalent model of LVdc side.

different trends, thereby expanding the $R_{(\mathrm{pu})}$ range. Therefore, HI-MMC is equipped with a function for decoupling MVdc and MVac voltage levels, which satisfies the grid-connected requirements of the MVac grid and the optimal selection of MVdc voltage levels.

III. Analysis of HI-MMC Power Flow

The proposed topology has three output ports, so it has different operation modes, such as power exchange from the MVac port to the MVdc port, power exchange from the MVac port to the LVdc port, and power exchange from the MVac port to the MVdc and LVdc ports. The following will give a characteristic analysis of average power flow (APF). The terminals of ISMs at the MV side are represented by the controlled voltage sources $V_{\mathrm{ICC}u(l)i}$ ($i = 1, \ldots, x$) or $V_{\mathrm{IBC}u(l)j}$ ($j = 1, \ldots, y$) while having the hybrid ac and dc modulation ratios found in (3). The arm currents $i_{\mathrm{ac}u}$ and $i_{\mathrm{ac}l}$ have relations with the MVdc I_{MVDC} and MVac currents i_{ac} as follows:

$$\begin{cases} i_{\mathrm{ac}u} = I_{\mathrm{MVDC}} + \frac{i_{\mathrm{ac}}}{2} \\ i_{\mathrm{ac}l} = -I_{\mathrm{MVDC}} + \frac{i_{\mathrm{ac}}}{2} \end{cases}. \tag{8}$$

According to (7) and (8), the instantaneous output power of the proposed two-type ISMs in the upper arm and the lower arm can be calculated as follows:

$$\begin{cases} p_{\mathrm{ICC}ui} = -\left(I_{\mathrm{MVDC}} + \frac{i_{\mathrm{ac}}}{2}\right) \times V_{\mathrm{ICC}ui} \\ p_{\mathrm{IBC}uj} = -\left(I_{\mathrm{MVDC}} + \frac{i_{\mathrm{ac}}}{2}\right) \times V_{\mathrm{IBC}uj} \\ p_{\mathrm{ICC}li} = \left(-I_{\mathrm{MVDC}} + \frac{i_{\mathrm{ac}}}{2}\right) \times V_{\mathrm{ICC}li} \\ p_{\mathrm{IBC}lj} = \left(-I_{\mathrm{MVDC}} + \frac{i_{\mathrm{ac}}}{2}\right) \times V_{\mathrm{IBC}lj} \end{cases}. \tag{9}$$

From (10) and (11), it can be seen that the APF of ICC consists of two parts: $P_{\mathrm{MVAC}u(l)i}$ and $P_{\mathrm{MVDC}u(l)i}$ ($i = 1, \ldots, x$) and the APF of IBC only consists $P_{\mathrm{MVAC}u(l)j}$ ($j = 1, \ldots, y$). They can be averaged over a line-frequency period

$$P_{\mathrm{ICC}u(l)i} = \frac{1}{T}\int_t^{t+T} p_{\mathrm{ICC}u(l)i}dt = -\frac{V_{\mathrm{dc}L}}{2kT}\int_t^{t+T} (i_{\mathrm{ac}}d_{a-C})\,dt - \frac{D}{k} I_{\mathrm{dc}L} V_{\mathrm{dc}L} \tag{10}$$

$$P_{\mathrm{IBC}u(l)j} = \frac{1}{T}\int_t^{t+T} p_{\mathrm{IBC}u(l)j}dt = -\frac{V_{\mathrm{dc}L}}{kT}\int_t^{t+T} i_{\mathrm{ac}}d_{a-B}dt \tag{11}$$

where T is the line-frequency period.

The average equivalent model on the common LVdc side of HI-MMC is depicted in Fig. 11, and the instantaneous current $i_{\mathrm{dc}L}$ is equal to the sum of all controlled current sources on the common LVdc side. According to the superposition theorem, the controlled current sources i_{edc} and i_{eac} can be represented

as follows:

$$i_{\mathrm{dc}L} = \sum_{i=1}^{x} i_{\mathrm{ICC}ui} + \sum_{i=1}^{x} i_{\mathrm{ICC}li} + \sum_{j=1}^{y} i_{\mathrm{IBC}uj} + \sum_{j=1}^{y} i_{\mathrm{IBC}lj}$$
$$= -\frac{1}{k}\left(\underbrace{2xI_{\mathrm{MVDC}}D}_{i_{\mathrm{edc}}} + \underbrace{xi_{\mathrm{ac}}d_{a-C} + yi_{\mathrm{ac}}d_{a-B}}_{i_{\mathrm{eac}}}\right). \quad (12)$$

It has two equivalent parts: dc active power P_{MVDC} from the MVdc port and ac active power P_{MVAC} from the MVac port. Thus, based on the above analysis of P_{MVAC}, P_{MVDC}, and P_{LVDC}, a detailed analysis of different operation modes can be easily derived. Especially in three-phase HI-MMC systems, the DLP of each phase can be collected into the common LVdc bus via the HFT of the SMs, thereby eliminating the need for this capacitor and resulting in a more compact topology.

According to the relationship between the output voltage and the modulation ratio, the following power transmission constraints can be obtained. Due to the unipolarity of the ICC port voltage, the amplitude of the modulation ratio is the primary factor limiting the transmission power of HI-MMC. First, the input voltage on the common LVdc side is set to 1 kV, and the dc modulation ratio D is set at 0.5 to improve the dc utilization ratio. The IBC can adopt the ac modulation ratio with the same amplitude as the ICC within the scaling range $|d_{a\text{-}C}| = 0.5|d_{a\text{-}b}|$. In addition, assume that the output voltage and current at MVac side are described as follows:

$$\begin{cases} v_{\mathrm{ac}m} = V_m \sin(\omega t + \theta_m) \\ i_{\mathrm{ac}m} = I_m \sin(\omega t + \theta_m - \varphi) \end{cases} \quad (13)$$

where $V_m(m = u,v,w)$ is the peak output voltage, I_m is the peak output current, ω is the output frequency, φ is the output power factor angle, and $\theta_m = \theta$, $\theta - 2\pi/3, \theta + 2\pi/3$. The amplitude of the modulation ratio d_{am} can be derived as follows:

$$d_{\mathrm{am}} = \frac{\sqrt{a^2 + b^2}\sin(\omega t + \theta_m + \varphi_a)}{(x + y)\frac{V_{\mathrm{dc}L}}{k}} \quad (14)$$

where $a = -V_m - I_m\omega(L_f + L_m/2)\sin\varphi$, $b = -I_m\omega(L_f + L_m/2)\cos\varphi$, and $\varphi_a = \arctan(b/a)$.

The grid current $i_{\mathrm{ac}m}$ can be divided into the active component $i_{\mathrm{ac}d}$ and the reactive component $i_{\mathrm{ac}q}$ based on the $v_{\mathrm{ac}m}$. If the total active power of LVdc port P_o is 1 MW, $V_{\mathrm{MVAC}} = 10$ kV, and $k = 1$, then the operation boundary diagram of HI-MMC is shown in Fig. 12. When the output power of the converter exceeds the boundary conditions, the proposed SST will become unstable and the power flow between ports is given by the following expression:

$$P_{\mathrm{dc}L} = P_{\mathrm{MVAC}} + P_{\mathrm{MVDC}} = \frac{3}{2}v_{\mathrm{ac}}i_{\mathrm{ac}d} + V_{\mathrm{MVDC}}I_{\mathrm{MVDC}}. \quad (15)$$

IV. Control Strategy and Optimal Design

In this article, the simulation of a 1 MW/10 kV HI-MMC-based SST is established by Matlab/Simulink software, and the detailed simulation parameters are listed in Table I. The system control strategy and the optimal design of HI-MMC are given. The overall control block diagram of HI-MMC is shown in Fig. 13.

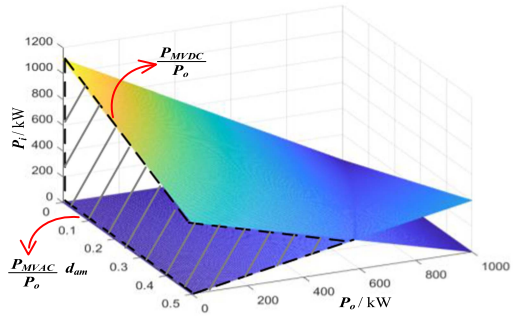

Fig. 12. Operation boundary diagram of HI-MMC.

TABLE I
Parameters of the Simulation System

Symbol	Parameter	Value
x	Number of ICCs in each arm	3
y	Number of IBCs in each arm	1
V_{dcL}	LVDC voltage	800 V
V_{dcM}	MVDC voltage	10 kV
V_{acM}	RMS of MVAC voltage	10 kV
f_c	Sawtooth carrier frequency	10 kHz
k	HFT turn ratio	800:4000
C_{LVDC}	Capacitor	5 mF
$R_{(pu)}$	Voltage ratio	1.63
L_{arm}	Arm inductor	4 mH
P_N	Rated power	1 MW

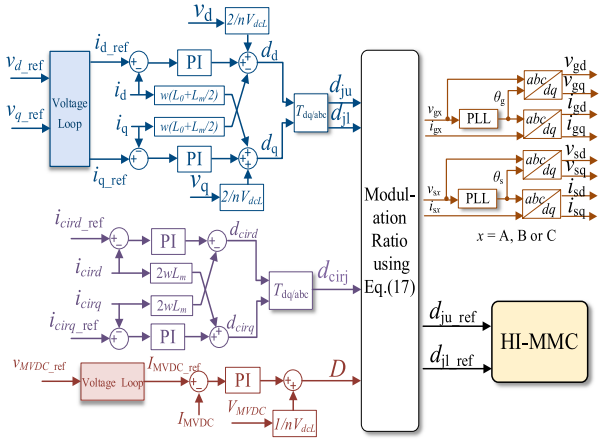

Fig. 13. Overall control diagram of HI-MMC.

A. Control Strategy Design

If the number of ISMs in each arm and the turn ratio of HFT k are determined, the modulation ratios d and D can control the output voltages of the MVdc and MVac ports, respectively. According to Kirchhoff's voltage law, a mathematical model of

the MVac port can be derived as follows:

$$\begin{cases} u_A = -(R_0 + \frac{R_m}{2})i_A - (L_0 + \frac{L_m}{2})\frac{di_A}{dt} + \frac{u_{Al} - u_{Au}}{2} - U_{NO} \\ u_B = -(R_0 + \frac{R_m}{2})i_B - (L_0 + \frac{L_m}{2})\frac{di_B}{dt} + \frac{u_{Bl} - u_{Bu}}{2} - U_{NO} \\ u_C = -(R_0 + \frac{R_m}{2})i_C - (L_0 + \frac{L_m}{2})\frac{di_C}{dt} + \frac{u_{Cl} - u_{Cu}}{2} - U_{NO} \end{cases}. \tag{16}$$

After the simplification and transformation, the relationship expressions between the three-phase voltage and current of the MVac port and the ac modulation ratio d can be obtained as follows:

$$\begin{cases} i_d = -\frac{(x+y)\times k\times U_{dcL}\times d_d}{2(sL+R)} - \frac{e_d}{sL+R} - \frac{\omega L i_q}{sL+R} \\ i_q = -\frac{(x+y)\times k\times U_{dcL}\times d_q}{2(sL+R)} - \frac{e_q}{sL+R} + \frac{\omega L i_d}{sL+R} \end{cases} \tag{17}$$

where subscripts d and q represent the corresponding variables on the d and q axes, respectively; $L = L_0 + (L_M/2)$, where L_0 is the filter inductor and L_M is the arm inductor; $R = R_0 + (R_M/2)$.

Since the three-phase bridge arms on the MVdc side are connected in parallel, the voltage loop equation on the MVdc side can be obtained for any phase. After the three-phase arm current is collected, the current equation on the MVdc side can be derived and the mathematical expressions are presented as follows:

$$s \cdot 2L_m \cdot \frac{i_{\mathrm{MVDC}}}{3} = nkDu_{\mathrm{dc}L} - u_{\mathrm{MVDC}} \tag{18}$$

$$s \cdot C_M \cdot u_{\mathrm{MVDC}} = i_{\mathrm{MVDC}} - \frac{u_{\mathrm{MVDC}}}{R_{\mathrm{MVDC}}} \tag{19}$$

where R_{MVDC} is the equivalent resistance of transmission power on the MVdc port.

The controller can be designed easily in accordance (16)–(19), and the MVac/dc ports can accomplish power decoupling. On the other hand, ISM does not require individual capacitors to buffer the double-frequency power fluctuation, so there is no need for a complex voltage balanced control strategy. The adoption of a three-phase parallel structure in HI-MMC results in the presence of a circulating current between each phase. Notably, it differs from the circulating current caused by the charging or discharging of individual capacitors in traditional MMC-based SST. The efficiency of HI-MMC may be compromised by minor manufacturing defects in the HFT turn ratio. First, the expression of circulating current $i_{\mathrm{cir}j}$ is defined as follows:

$$i_{\mathrm{cir}j} = \frac{i_{ju} + i_{jl}}{2} - \frac{I_{\mathrm{MVDC}}}{3}. \tag{20}$$

By controlling the unbalanced voltage $v_{\mathrm{cir}j}$, the circulating currents $i_{\mathrm{cir}j}$ can be regulated to their expected values. Therefore, the arm voltage references are given as follows:

$$\begin{cases} v_{ju\_\mathrm{ref}} = \frac{1}{2}[V_{\mathrm{MVDC}} + (v_{ju} - v_{jl})] - v_{\mathrm{cir}j} \\ v_{jl\_\mathrm{ref}} = \frac{1}{2}[V_{\mathrm{MVDC}} - (v_{ju} - v_{jl})] - v_{\mathrm{cir}j} \end{cases}. \tag{21}$$

By substituting the arm output voltage in (21), the modulation ratio of the circulating current can be obtained as

$$\begin{cases} d_{ju\_\mathrm{ref}} = \frac{D}{2} + \frac{d_{ju}}{4} + \frac{d_{jl}}{4} - d_{\mathrm{cir}j} \\ d_{jl\_\mathrm{ref}} = \frac{D}{2} - \frac{d_{ju}}{4} - \frac{d_{jl}}{4} - d_{\mathrm{cir}j} \end{cases}. \tag{22}$$

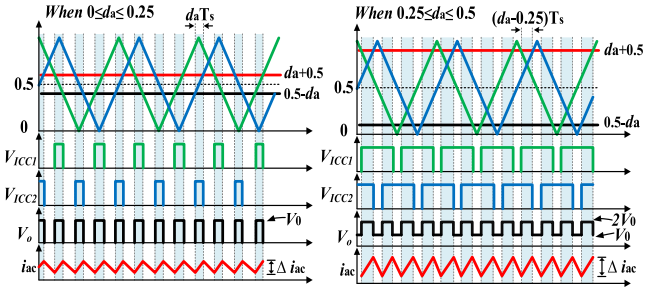

Fig. 14. CPS modulation strategy and current ripple.

The target reference values $i_{\mathrm{cir}\,d\mathrm{ref}}$ and $i_{\mathrm{cir}\,q\mathrm{ref}}$ can be obtained by transforming the three-phase circulating current into d-q frame. The target reference values $i_{\mathrm{cir}\,d\mathrm{ref}}$ and $i_{\mathrm{cir}\,q\mathrm{ref}}$ can be set at zero to eliminate the circulating current in the HI-MMC.

B. Carrier Phase-Shift (CPS) Pulsewidth Modulation (PWM) and Current Ripple Analysis

The modular topology of HI-MMC allows the CPS modulation strategy to be utilized. A higher equivalent switching frequency can reduce the volume of the passive components. Therefore, the proposed topology adopts CPS-PWM to improve the output voltage and current waveform quality. The current ripple analysis with CPS-PWM is analyzed in the following. Take ICC as an example the modulation signals can be equivalent to two-sine PWM modulation with the same triangle carrier frequency. The gate signals are phase-shifted by 180°/n, and the equivalent switching frequency f_e can theoretically double the switching frequency f_s. Fig. 14 shows the equivalent gate signals and current ripple waveforms of two cascaded ICCs. When considering x ICCs and y IBCs in the cascaded arm with CPS-PWM and the total number of ISM is n, the current ripple Δi_{ac} can be expressed as follows:

$$\begin{cases} \Delta i_{\mathrm{ac}} = \frac{\left(v_{\mathrm{dc}L} - n\frac{v_{\mathrm{dc}L}}{2k}d_{\mathrm{am}}\right)}{L} d_{\mathrm{am}} T_{\mathrm{s}}, 0 \le d_{\mathrm{am}} \le \frac{1}{2n} \\ \Delta i_{\mathrm{ac}} = \frac{\left(iv_{\mathrm{dc}L} - n\frac{v_{\mathrm{dc}L}}{2k}d_{\mathrm{am}}\right)}{L} \left(d_{\mathrm{am}} - \frac{i-1}{2n}\right) T_{\mathrm{s}}, \frac{i-1}{2n} \le d_{\mathrm{am}} \le \frac{i}{2n} \\ \Delta i_{\mathrm{ac}} = \frac{\left(nv_{\mathrm{dc}L} - n\frac{v_{\mathrm{dc}L}}{2k}d_{\mathrm{am}}\right)}{L} \left(d_{\mathrm{am}} - \frac{n-1}{2n}\right) T_{\mathrm{s}}, \frac{n-1}{2n} \le d_{\mathrm{am}} \le \frac{n}{2n} \end{cases}. \tag{23}$$

Therefore, assuming the value voltage of LVdc has been confirmed, the maximum value of current ripple can be calculated using (23), and the arm inductor and filter parameters can be designed and optimized.

C. Precharging Circuits Design

In contrast to the precharging circuits used in conventional MMC-based SST, which include an uncontrolled precharging period and controlled precharging [32], the proposed SST's ISM on the MV side does not require individual capacitor support, and the capacitors are primarily present on the LVdc side. As depicted in Fig. 15, a simple precharging circuit is designed for the HI-MMC converter. It charges the capacitors C_0 on the

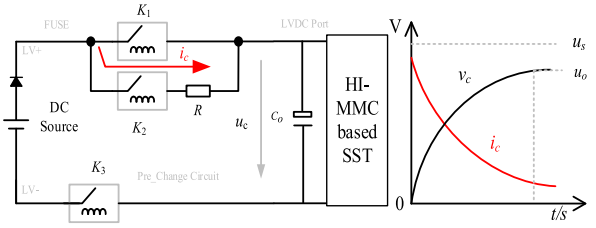

Fig. 15. Precharging circuits of HI-MMC.

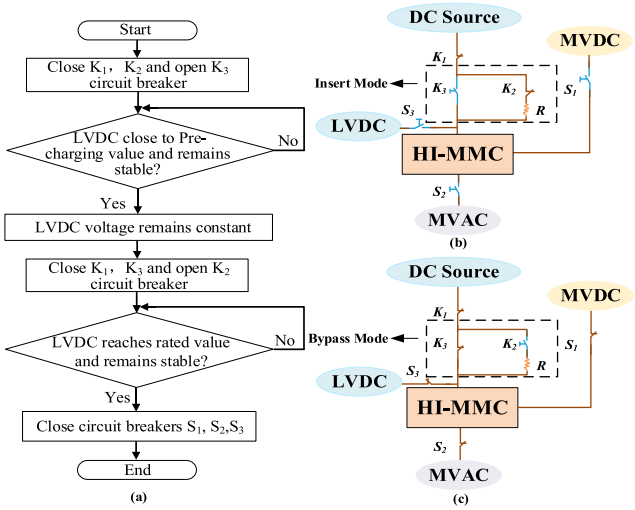

Fig. 16. Precharging circuits of HI-MMC. (a) Flowchart. (b) Insert mode. (c) Bypass mode.

common LVdc without generating a large surge current when the proposed converter begins in a zero-state condition.

The precharging circuits include a dc source, a precharge resistor R, and some circuit breakers. The precharge process is divided into two modes: insert mode (K_1 open and K_2 and K_3 close, RC series charging) and bypass mode (K_2 open, K_1, and K_3 close, C_o directly charging). Typically, the precharging process must be completed in 1.5 s. Therefore, the required precharge resistor R can be calculated as follows:

$$T_t = RC_o \ln\left[\frac{(U_s - U_o)}{(U_s - U_t)}\right]. \tag{24}$$

The operation flowchart of the precharging circuits is shown in Fig. 16(a). The entire process can be divided into two modes: insert mode and bypass mode. The designed precharging circuit is connected to the HI-MMC LVdc side port. First, close the circuit breakers K_1 and K_2 and open K_3, as shown in Fig. 16(b). At this time, the dc source, precharging resistance, and LVdc capacitor form a charging circuit. After the capacitor voltage has stabilized, close the circuit breakers K_1 and K_3 and open K_2, as shown in Fig. 16(c). At this time, the dc source is directly connected to the LVdc capacitor. The last step is closing circuit breakers S_1, S_2, and S_3.

D. Reliability Analysis

Reliable operation is important to the SST system, which improves its operating lifetime and avoids costly interruptions and maintenance [24]. A large number of active power devices result in a lower reliability for the SST system. However, the redundancy design of SMs in the overall system can improve system reliability [33]. Such reliability analyses of MMC systems under different SM topologies have been carried out [34]. Due to the fact that the proposed SST has different types and numbers of ISMs, it will present distinct reliability results.

Each type of ISM includes active (IGBTs) and passive (diodes) power devices, capacitors, inductors, and HFTs. This article mainly focuses on the influence of active power devices on system reliability. Since each power device suffers the same voltage and current stress, we can assume that all power devices have the same operation period and constant failure rate λ in the life curve [35]. The reliability can be expressed as a function of operation time t, meaning that the expected number of failures per one billion (10^9) hours of operation during their lifetime $-\lambda = 1/10^{-9}$. As the number of active power devices in IBC is greater than ICC, $\lambda_{\mathrm{IBC}} = 1.25{\cdot}\lambda_{\mathrm{ICC}}$. The reliability of a single ISM in each case is as follows:

$$R_{\mathrm{ICC/IBC}}(t) = e^{-\lambda_{\mathrm{ICC/IBC}}\cdot t}. \tag{25}$$

The mean time between failures (MTBF) is defined as the expectation of operating time between failures. If the failure rate of ISM is constant, the component level MTBF can be derived from the failure rate as

$$\mathrm{MTBF}_{\mathrm{ICC/IBC}} = \int_0^{\infty} R_{\mathrm{ICC/IBC}}(t)\mathrm{d}t = \frac{1}{\lambda_{\mathrm{ICC/IBC}}}. \tag{26}$$

According to the calculation method, the reliability analysis of cascaded ISMs can be easily obtained. If the number of ICC in each arm is x and the number of IBC is y, it can be obtained without redundancy

$$\begin{aligned} R_{\mathrm{ICC}x}(t) &= \sum_{i=0}^{x} C_x^i (-1)^i \left(1 - e^{-\lambda_{\mathrm{ICC}}\cdot t}\right)^i \\ R_{\mathrm{IBC}y}(t) &= \sum_{i=0}^{y} C_y^i (-1)^i \left(1 - e^{-\lambda_{\mathrm{IBC}}\cdot t}\right)^i. \end{aligned} \tag{27}$$

The correlation coefficient θ is correlation between ICC and IBC. Due to the three-phase symmetric structure of the HI-MMC-based SST system, the system reliability can be calculated using with Copula theory as follows:

$$\begin{aligned} R_{\mathrm{arm}}(t) &= \left[C\left(R_{\mathrm{ICC}x}, R_{\mathrm{IBC}y}\right)\right] \\ &= \exp\left[-\left((-\ln R_{Ex})^{1/\theta} + (-\ln R_{\mathrm{IBC}y})\right)^{1/\theta}\right]. \end{aligned} \tag{28}$$

Since the proposed SST is a modular system, higher reliability can be realized through redundancy design. The system reliability under the conditions of no redundancy, $\mathrm{A_{ISM}} = 2$ and $\mathrm{A_{ISM}} = 4$ redundancy is analyzed here, where at least two additional ISMs are inserted into each arm and n ISMs must be

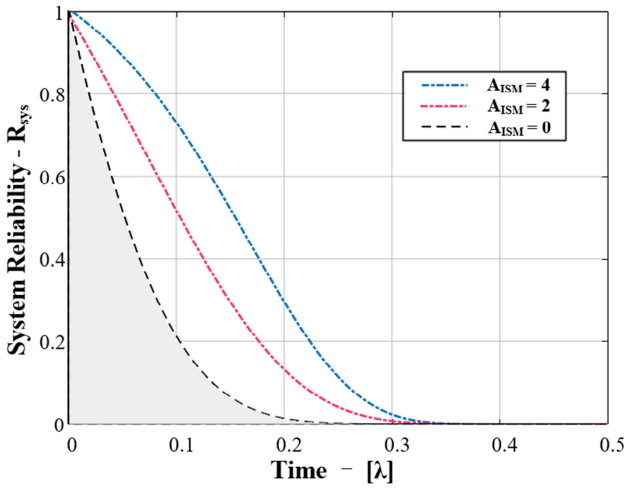

Fig. 17. System reliability curve of no redundancy, $A_{ISM} = 2$, and $A_{ISM} = 4$ redundancy.

in operation. The reliability curve of the HI-MMC system can be calculated as follows:

$$R_{\text{sys-A}}(t) = \left(\sum_{k=N}^{N+A} C_{N+A}^{k} R_{\text{arm}}^{k} (1 - R_{\text{arm}})^{N+A-k} \right)^{6}. \quad (29)$$

Fig. 17 depicts the system reliability curves of HI-MMC for each redundancy scheme. The gray area marked represents the expectation of the continuous system operation without failure. The red line and blue line represent the system reliability with n+2 and n+4, respectively. As the years of use increase, the system's reliability is rapidly reduced. From this point of view, a reasonable redundancy configuration for the HI-MMC system is very important.

V. Simulation Verification

In this article, the simulation of a 1 MW/10 kV HI-MMC-based SST is established by MATLAB/Simulink software. This section verifies the effectiveness of the proposed SST topology and control strategy. The simulation system parameters are listed in Table I, and the simulation results of the three-phase HI-MMC system are analyzed in this section.

The dynamic simulation results of a three-phase HI-MMC-based SST with $R_{(\text{pu})} = 1.63$ are shown in Fig. 18. In order to reduce the simulation calculation time, HFT with turn ratio of 800:4000 is utilized to reduce the number of cascaded ISMs. Due to the fact that the ISM number per arm is $n = 4$, the CPS modulation strategy is applicable, which employs a lower switching frequency to achieve a higher equivalent switching frequency of the output voltage waveform.

Till $t = 0.32$ s, the HI-MMC-based SST operated under steady conditions and transferred power from the LV to the MV side. The peak voltage values of MVdc port and MVac port are 10 kV and 8164 V, respectively. After FFT analysis, the amplitude and frequency are determined to be 36 A and 50 Hz, respectively. According to (17), the unit power factor can be regulated so that

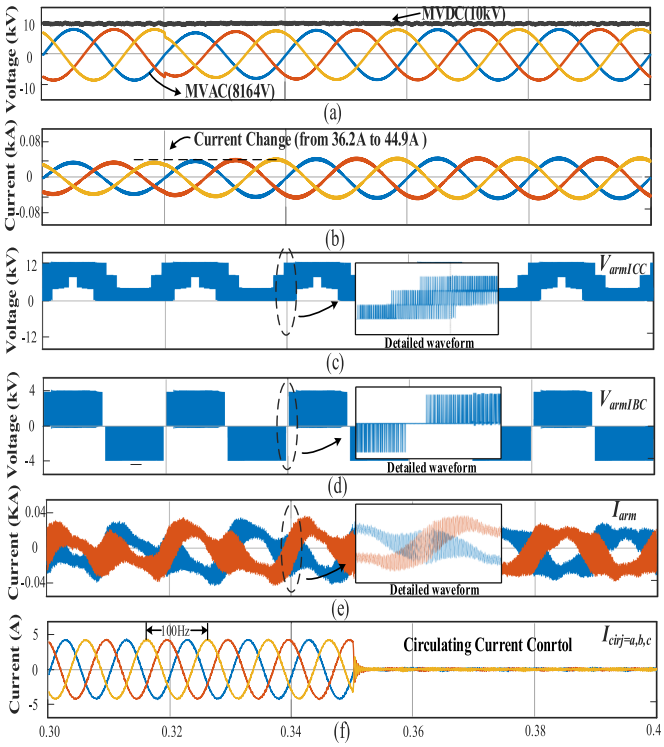

Fig. 18. Dynamic simulation results of three-phase HI-MMC. (a) Grid-side three-phase current. (b) Grid-side three-phase voltage. (c) ICC output voltage. (d) IBC output voltage. (e) Arm current. (f) Circulating current.

the grid current is in phase with the grid voltage by controlling $v_{q\text{ref}}$.

Fig. 18(a) and (b) shows the transient processes of voltage and current on the MVac side. At $t = 0.32$ s, the load on the MVac side suddenly increases by 100 kW. After a 5 ms transient process, the three-phase voltage waveforms of the MVac port recover to their rated values. It can be seen that the peak value of the three-phase current increases from 36.2 to 44.9 A.

Fig. 18(c) and (d) illustrates the output voltage waveforms of cascaded ICCs and IBCs on the A-phase upper arm, respectively. Due to the adoption of the CPS modulation strategy, the output voltage waveform of cascaded ICCs has three levels of 4, 8, and 12 kV. The output voltage waveform of IBC only contains an ac component. Notably, the output voltage of ICC is unipolar and contains both ac and dc components. The equivalent switching frequency of the ISMs is about 15 kHz. The effectiveness of the modulation strategy and operating principle has been verified.

At $t = 0.35$ s, the control strategy of circulating current restraint is initiated. As shown in Fig. 18(e), the peak value of the arm current is significantly reduced, which effectively reduces the SST system power losses. In Fig. 18(f), the amplitude of the circulating current with 100 Hz is controlled from 5 to nearly 0 A. The simulation waveforms verify the effectiveness of the proposed SST topology and modulation strategy. It is observed that the circulating current in the proposed SST differs from that of the SST based on MMC due to the charging or discharging of SMs. Therefore, under normal operating conditions, the amplitude of the circulating current in the three-phase HI-MMC system is very small.

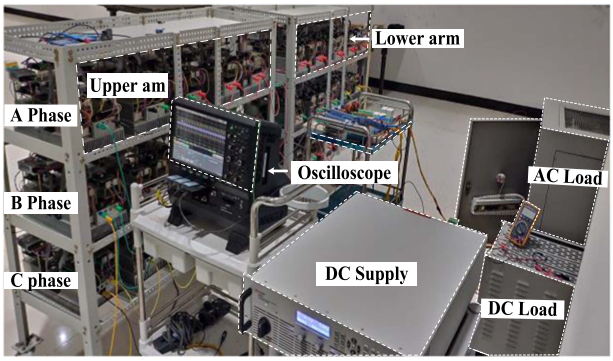

Fig. 19. Picture of the HI-MMC experimental hardware setup.

TABLE II
PARAMETERS OF THE EXPERIMENTAL SYSTEM

Symbol	Parameter	Value
V_{dcL}	LVDC voltage	100 V
C_{dcL}	LVDC capacitor	2 mF
L_r	HFT leakage inductor	3μF
f_s	Switching frequency	10 kHz
k	Transformer turns ratio	17:18
D	DC Modulation	0.45
d_a	AC Modulation	0.45
L_f, C_f	Output filter	0.5 mF,2 μF
C_{dcM}	MVDC capacitor	75 μF
P_N	Rated power	20 kW

VI. EXPERIMENTAL VERIFICATION

In order to verify the correctness of the operating principle and the theoretical analysis, a scaled-down three-phase HI-MMC prototype has been established. Fig. 19 shows the three-phase HI-MMC experimental hardware setup. The main controller is combined with the TMS320F28335 DSP from Texas Instruments and the EP4CE115F23I7 FPGA from Altera. The FPGA receives the modulation signals from the DSP and then generates the PWM. The main parameters of three-phase HI-MMC have been summarized in Table II.

A. Experimental Results

The details of the active switching transitions of Q_1 and Q_2 are shown in Fig. 20, which depict the transmission power under conditions of a light load (20% load rate). V_{Q1}, V_{Q2}, and V_{S1} denote voltages on the active power devices Q_1, Q_2, and S_1, respectively. S_{Q1}, S_{Q2}, and S_{S1} are driving signals belonging to Q_1, Q_2, and S_1, respectively. During the dead time, the primary current i_1 charges and discharges the parasitic capacitors of switching devices, resulting in the ZVS condition.

In each arm, there are three ICCs and two IBCs. The peak voltage values of MVdc and MVac under these conditions can be calculated using the voltage equation presented in the previous section. The source of input voltage for the LVdc is 100 V, $D = 0.45$, $d_{\rm am} = 0.45$, $x = 3$, $y = 2$, and $k = 17{:}18$, so the theoretical peak voltage values of the MVdc and MVac are 285 V and 238 V, respectively. The experimental values of MVdc and MVac are 283 V and 232 V, respectively, as shown in Fig. 20(a).

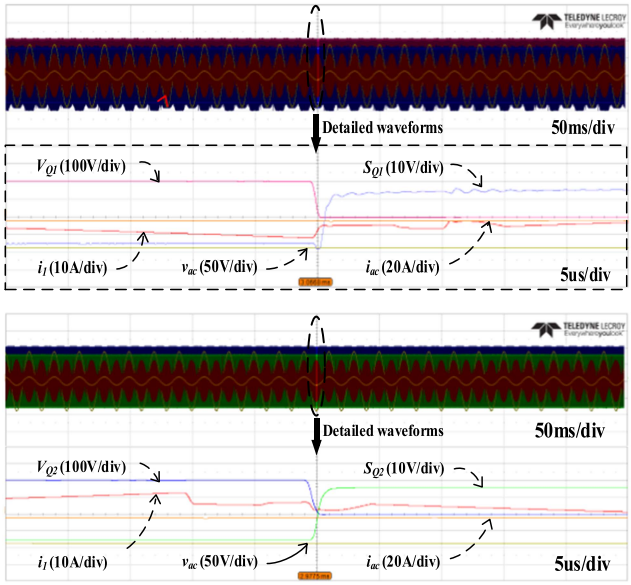

Fig. 20. Waveform diagram of the ZVS implementation process.

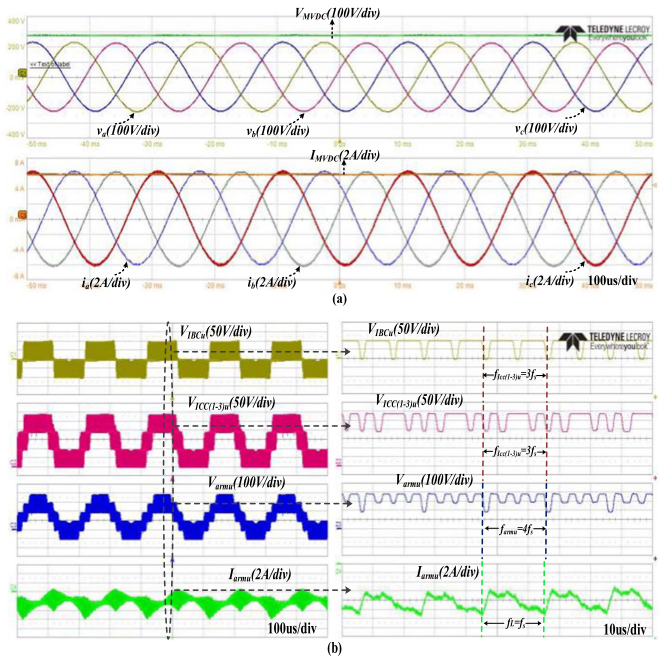

Fig. 21. Waveforms of steady state. (a) Waveforms of the output voltage and output current. (b) Waveforms of the upper arm current and the ISM's voltage in the upper arm.

The theoretical and experimental values agree, confirming the correctness of the voltage formulas. In this case, the value of $R_{(\rm pu)}$ equals 1.63.

Fig. 21 shows the waveforms of $V_{{\rm IBC}u}$ (output voltage of the IBC in the upper arm), $V_{{\rm ICC(1\text{-}3)}u}$ (total voltage of three ICCs in the upper arm), $V_{{\rm arm}u}$ (upper arm voltage), $I_{{\rm arm}u}$(the current in the upper arm). The equivalent frequency of the output voltage can be increased several times by CPS. This allows the switches

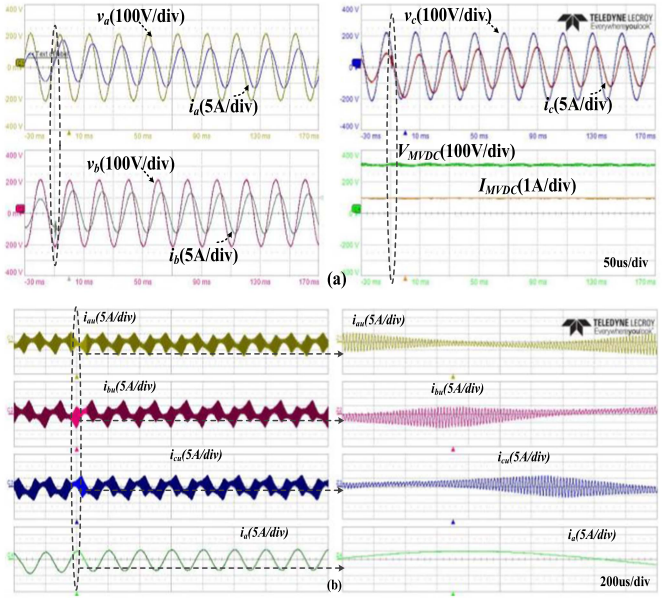

Fig. 22. Waveforms of transition process after adding inductance load $X = j48.4\ \Omega$. (a) Waveforms of output current and output voltage. (b) Waveforms of three-phase arm upper current i_{au}, i_{bu}, and i_{cu}.

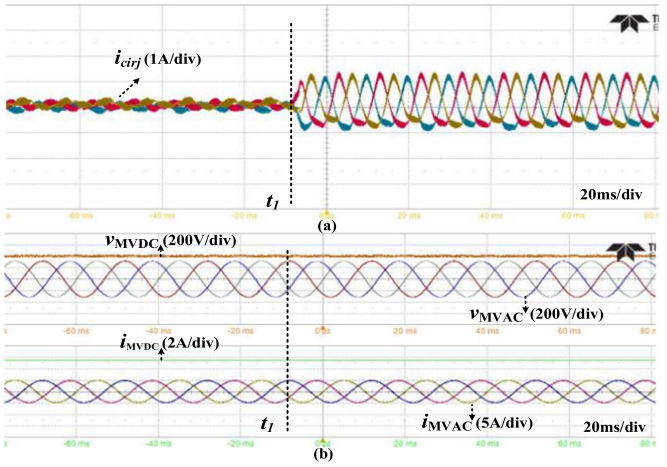

Fig. 23. Waveforms of circulating current control strategy.

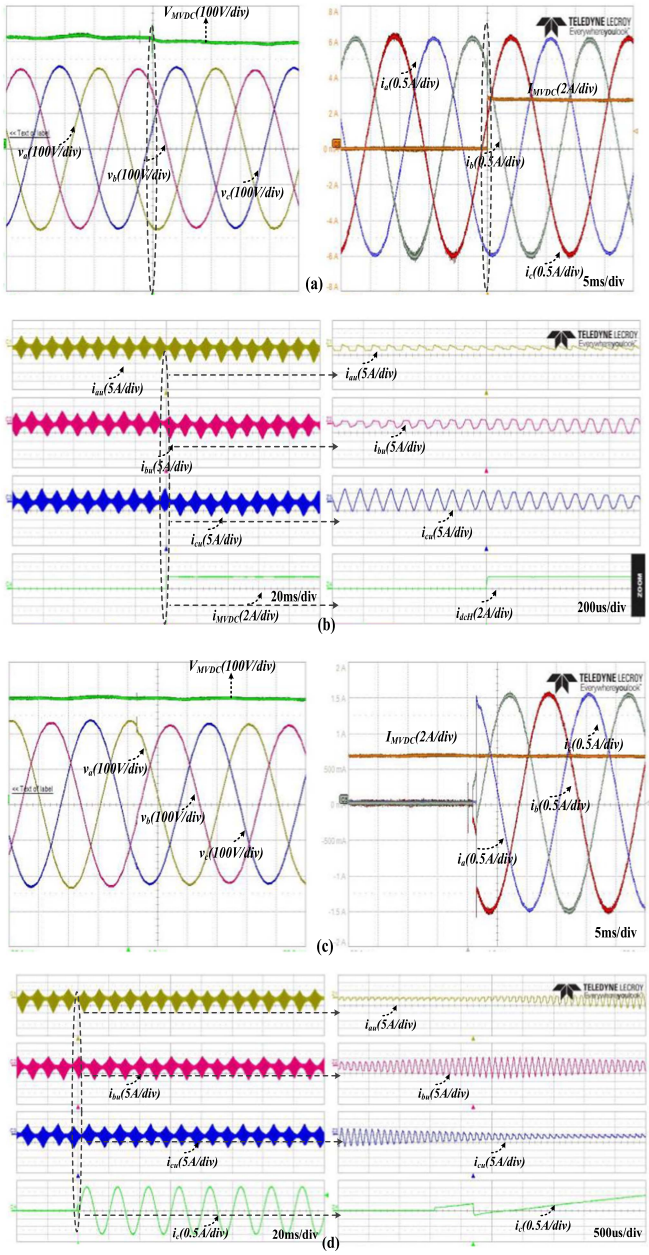

Fig. 24. Waveforms of the transition process. (a) DC load step condition from ∞ to 100 Ω. (b) Waveforms of three-phase arm current under the dc load step condition. (c) AC load step condition from ∞ to 160 Ω. (d) Waveforms of three-phase arm current i_{au}, i_{bu}, and i_{cu} under the ac load step condition.

to operate at a lower switching frequency while producing output voltage waveforms with fewer harmonics.

Fig. 22(a) demonstrates the transient process waveforms after adding MVdc load 320 Ω while maintaining MVac load 160 Ω and inductor load $X = j48.4$. According to the experimental waveforms, the three-phase voltage and current have high quality during this process. Active and reactive powers are freely transferred between LVdc, MVdc, and MVac ports. Fig. 22(b) shows the transient current waveform of the three-phase arm in this dynamic process.

As shown in Fig. 23(a), the reference value of circulating currents changes $i_{\mathrm{cir\cdot dref}}$ from nearly 0 A to a sinusoidal three-phase waveform with an amplitude of 1 A and a frequency of 100 Hz at t_1. In Fig. 23(b), the entire dynamic process of the circulating current reference value change has no effect on the MVdc and MVac ports of the HI-MMC converter, indicating that the circulating current is determined solely by the converter's internal characteristics.

When the MVdc load is changed from ∞ to 100 Ω and the MVac load maintains 160 Ω, the waveforms of the transition process under the dc load step condition are shown in Fig. 24(a). Fig. 24(c) shows the waveforms of the transition process under the ac load step condition when the MVac load is changed from ∞ to 160 Ω and the MVdc load keeps 100 Ω. Fig. 24(b) and (d) shows the three-phase current waveforms of the upper arms i_{au},

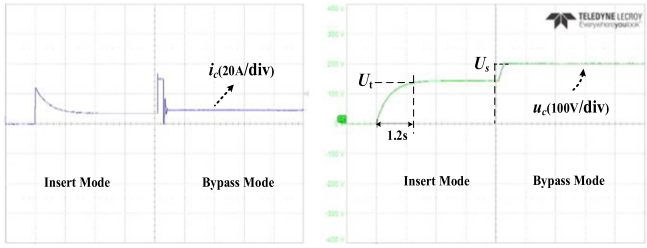

Fig. 25. Dynamic waveforms of the voltage and current during the precharging process.

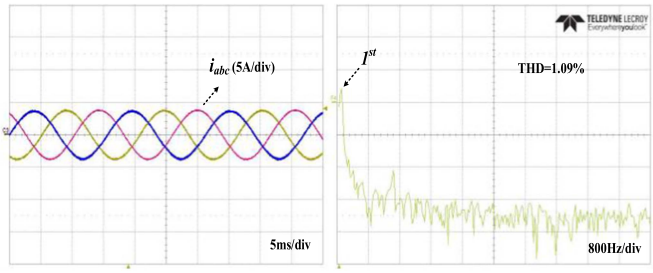

Fig. 26. Waveforms of the three-phase current and spectrum distribution.

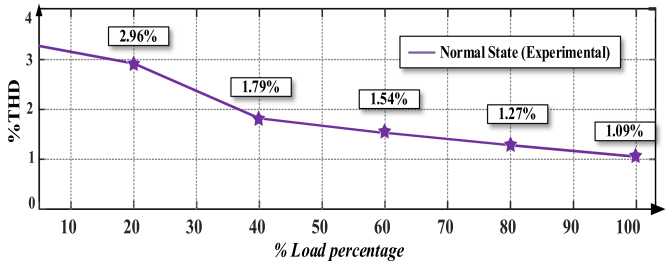

Fig. 27. Grid current's THD curve under 10%–100% load percentage.

i_{bu}, and i_{cu} when the MVac load or MVdc load are changed. In a transient process, the load step on one MV side has almost no effect on the other port, meaning that the power between the MVdc and MVac ports is decoupled.

During the precharging process, the dynamic waveforms of the capacitor voltage and current on the common LVdc side are shown in Fig. 25. The entire precharging process can be divided into insert mode and bypass mode. After 1.2 s, the capacitor voltage on the LVdc side rapidly rises from 0 to 140 V and reaches the expected value. During the whole precharging process, the surge current of the common capacitor does not exceed 40 A, which verifies the effectiveness of the proposed precharging circuit. At the same time, it can be seen that the proposed SST has a simpler precharging method than the conventional MMC-based SST.

As shown in Fig. 26, the value of the grid current's THD is 1.09% within a reasonable range. The grid current of HI-MMC is dominated by the 50 Hz fundamental wave component, and there are still relatively odd harmonic components such as the 5th, 7th, and 9th harmonics. The experimental prototype adopts a filter device with 1 kHz cut-off frequency. Therefore, the higher harmonics are effectively filtered out. In conclusion, HI-MMC has good waveform quality, and the THD values under different load conditions are given in Fig. 27.

B. Efficiency Analysis

In this section, an IBC (with more switches) has been selected as an example to evaluate the system's efficiency. The power losses of each component under the rated power 20 kW are analyzed. The calculation processes of theoretical efficiency are elaborated, which include four parts: active power devices, HFT, filter devices, and interleaved inductors.

First, the whole switching process of IGBT is nonlinear. Research on IGBT switching loss is mainly based on building IGBT physical model or calculating loss through formula derivation [36]. In this article, the loss calculation method given by Infineon's official website is carried out [37]. The loss of IGBT is mainly composed of switching loss $P_{\rm sw}$ and conduction loss $P_{\rm con}$.

The conduction loss of IGBTs can be expressed as

$$P_{{\rm con}T} = \frac{N}{T_S}\int_0^{|d|T_s} (u_{\rm CE} i_C(t) + r_C \cdot i_C^2(t))dt \tag{30}$$

where $u_{\rm CE}$ is the IGBT ON-state collector–emitter voltage; r_C represents a collector emitter ON-state resistance; i_C is the collector–emitter current; and N is the number of IGBTs.

The collector–emitter voltage can be found in the datasheet of the model FF300R06KE3 IGBT [38]. The same method can be used for the antiparallel diodes as follows:

$$P_{{\rm con}D} = \frac{N}{T_S}\int_0^{|1-d|T_s} (u_{D0} i_D(t) + r_D \cdot i_D^2(t))dt. \tag{31}$$

In addition, since the switching frequency of $S_{\rm o1}$ and $S_{\rm o2}$ is 50 Hz, the power losses of $S_{\rm o1}$ and $S_{\rm o2}$ are mainly conduction loss and the calculation method can also refer to (30) and (31). The switching loss of the IGBTs is caused by turn-ON loss and turn-OFF loss and the total switching energy can be expressed as

$$E_{\rm ts} = E_{\rm on} + E_{\rm off} \tag{32}$$

where $E_{\rm ts}$ is the total switching energy, and $E_{\rm on}$ and $E_{\rm off}$ represent turn-ON energy and turn-OFF energy, respectively.

In the proposed converter, the active power devices can achieve ZVS, so their turn-ON loss is approximately zero. According to the datasheet, the IGBT turn-OFF energy can be known as well. Therefore, the switching loss for IGBTs can be derived as follows:

$$P_{\rm SW} = \frac{N f_{\rm s}}{\pi}(E_{\rm on} + E_{\rm off}) \times \frac{I_S}{I_N} \times \frac{U_{\rm LVDC}}{U_N} \tag{33}$$

where f_s is 10 kHz; N is the number of IGBTs; I_S is the effective value of current (A) when the IGBT is in the ON-state; and I_N and $U_{\rm N}$ are the rated current and voltage, respectively.

The turn-OFF energy in the antiparallel diodes is normally neglected. The turn-ON energy in antiparallel diodes consists of mostly the reverse-recovery energy $E_{{\rm on}\,D}$ and it can be calculated

as follows:

$$E_{\mathrm{on}D} = \int_0^{t_{rf}} u_D(t) i_F(t) dt \approx \frac{1}{4} Q_{rr} \cdot U_{Drr} \tag{34}$$

where U_{Drr} and Q_{rr} are the maximum reverse recovery voltage and reverse recovery charge; t_{fr} is the forward recovery time.

The losses of the HFT and the inductors are usually composed of core loss P_{fe} and winding loss P_{cu}. The core loss can be calculated by the Steinmetz equation [39] using the following formula:

$$P_{\mathrm{fe}} = F_{w,c} C_m \times f^{\alpha} \times B_m^{\beta} \times 2 \times V_e \tag{35}$$

where $F_{w,c}$, C_m, α, and β are Steinmetz constants under square-wave excitation. V_{et} is the effective magnetic volume of the magnetic core (mm^3).

Different from the traditional Steinmetz equation [39], it is suitable for the condition of square-wave excitation by introducing a correction factor $F_{w,c}$. Meanwhile, the winding losses of the HFT and the inductors can be expressed as follows:

$$P_{\mathrm{cu-HFT}} = I_{\mathrm{pri.rms}}^2 \cdot R_{\mathrm{Cu.pri}} + I_{\mathrm{sec.rms}}^2 \cdot R_{\mathrm{Cu.sec}} \tag{36}$$

$$P_{\mathrm{cu-inductor}} = I_{L.\mathrm{rms}}^2 \cdot R_{\mathrm{Cu.inductor}} \tag{37}$$

where $R_{\mathrm{Cu.pri}}$, $R_{\mathrm{Cu.sec}}$, and $R_{\mathrm{Cu.inductor}}$ are the wire resistances of the HFT primary side, the HFT secondary side, and the interleaved inductors respectively.

The winding loss is modeled by considering a resistance in series with each winding, namely dc resistance (R_{cu}). It can be derived as follows:

$$R_{\mathrm{cu}} = \rho \frac{l_{\mathrm{wire}}}{A_{\mathrm{wire}}} = \rho \frac{l_{\mathrm{wire}}}{\pi \times \left(\frac{d_L}{2}\right)^2} \tag{38}$$

where ρ is the resistivity of copper material and $\rho = 1.724 \times 10^{-6}$ Ω/cm (25°C); l_{wire} is the total length of one winding wire.

The maximum effective value of the interleaved inductors can be calculated as follows:

$$I_{L-\mathrm{RMS}} = \sqrt{\frac{\int_0^{|d|T_s} i_L(t)^2 dt + \int_{0.5T_s}^{(|d|+0.5)T_s} i_L(t)^2 dt}{T_s}}. \tag{39}$$

In addition, high-frequency current produces alternating magnetic field, which will generate eddy currents in the windings. Eddy current effect causes an increase in winding loss, whose name is high-frequency winding ac loss. P_{AC} can be calculated with the help of winding ac resistance (R_{AC}). R_{AC} can be predicted by Dowell curve ($\varphi = h/u$) [40]. Subsequently, P_{AC} can be calculated by means of (13).

$$P_{\mathrm{AC}} = 2 \times \Delta I_{L-\mathrm{RMS}}^2 \times R_{\mathrm{AC}}. \tag{40}$$

According to [41], the loss of the output filter capacitor is primarily attributable to the ripple current flowing through the ESR. For the proposed converter, the filter capacitor model is MKP-C4BT, and its capacitance is 20 μF. From the datasheet, ESR $= 1.7 \times 10^{-3}$ Ω can be obtained. Thus, the loss of filter capacitor P_{FC} can be calculated as follows:

$$P_{\mathrm{FC}} = \left(\Delta I_{\mathrm{rip-max}}\right)^2 \times \mathrm{ESR}. \tag{41}$$

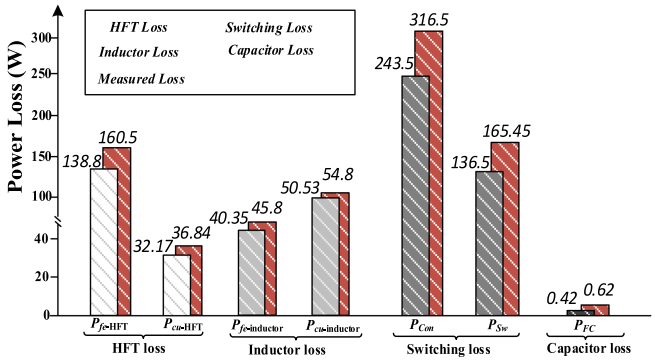

Fig. 28. Diagram of the power loss distribution.

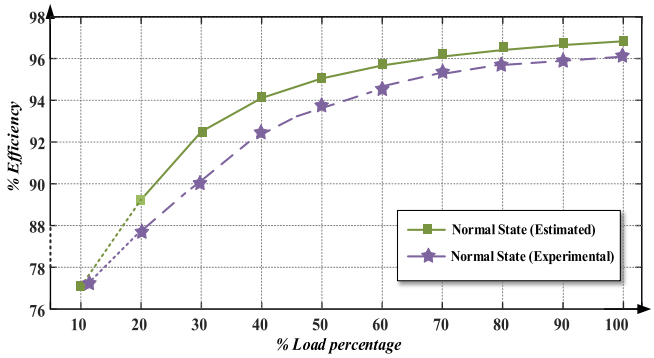

Fig. 29. Efficiency curve of the proposed converter under 10%∼100% load rate.

The theoretical value of η_{th} under various load percentages can be represented as follows:

$$\eta_{\mathrm{th}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} \times 100\% = \frac{P_{\mathrm{in}} - P_{\mathrm{loss}}}{P_{\mathrm{in}}} \times 100\% \tag{42}$$

where P_{in}, P_{out}, and P_{loss} are the rated power, output power, and overall power loss, respectively. P_{loss} can be represented as follows:

$$P_{\mathrm{loss}} = P_{\mathrm{loss-HFT}} + P_{\mathrm{loss-inductor}} + P_{\mathrm{sw}} + P_{\mathrm{con}} + P_{FC}. \tag{43}$$

In addition, the estimated losses and measured losses of each component under the rated power of 20 kW are summarized in Fig. 28. In addition, the efficiency curve under the conditions of 10%∼100% load rate is depicted in Fig. 29. During the testing of the experimental 20-kW prototype, the peak efficiency was determined to be 96.1%, with an estimated maximum efficiency of 96.8%.

C. Comparison With Other SSTs

A comparison of the proposed SST and other SST topologies is illustrated in Table II. For quantitative analysis, all SSTs are designed under conditions of 1 MW rated power and 10 kV grid voltage. The rated voltage of LVdc is set at 1 kV. The active power devices on the MV side and LV side are 3.3 kV/100 A IGBT and 1.7 kV/200 A IGBT, respectively. The voltage margin k_v and current margin k_i of power devices are 1.7 and

TABLE III
COMPARISON OF THE PROPOSED CONVERTER WITH OTHER SSTS

Parameters	*Industrial metrics* [43]	*W. Chen et al.* [30]	*Y. Kang et al.* [45]	*F.Briz et al.* [10]	*Z. Li et al.* [14]	*L.Camurca et al.* [25]	*X. Sun et al.* [31]	*C. Liu et al.* [32]	Presented work
SST type	CHB	MMC	MMC	HB-MMC	HB-MMC	FB-MMC	RP^{2}C-MMC	I-MMC	HI-MMC
Switching frequency	1.75 kHz	20 kHz	2 kHz	5 kHz	10 kHz	15 kHz	10 kHz	10 kHz	10 kHz
Conversion stages	2	1	1	2	2	2	1	1	1
Individual cap	×	4mF	1.2mF	2mF	0.65mF	1.4mF	120uF	0	0
SM's balance	Needed	Needed	Needed	Needed	Need	Needed	No need	No Need	No Need
Port number	2	3	2	3	3	2	3	3	3
SM's number (HB)	45 (one-phase)	242	165	360	200	280	240	240	≥240
$R_{(pu)}$	0.95	0.85	×	0.95	0.85	5	≤1	≤1	≥1
H/MFT number	9 (one-phase)	1	1	60	20	20	60(center-tapped)	60	60
THD	×	1%	5.5%	×	2.7%	×	2.4%	×	1.09%
Efficiency	⩾ 95%	97.1%	97.3%	×	95.8%	97.4%	96.9%	95.6%	96.8%
System weight	0.5 kVA/kg	++	++	++	+	+	—	—	—

*In this table, the symbols "+" indicates "high" while "–" means "low". The symbol "×" means no date. Industrial metrics refer to ABB's PETT white paper.

1.5, respectively. The comparison issues include the total SM numbers, the peak efficiency, the voltage ratio, and so on. In addition, some metrics of a suitable industrial SST system are added in Table III, referring to the parameters given in ABB's White Paper [42].

The CHB-based SST in [43] belongs to a two-stage topology and the power density of the whole system can be increased by a complex control strategy to suppress the ripple voltage on the SMs. It can effectively reduce the number of individual capacitors to 1.8 mF under the conditions of 10 kV MVac and 2 MVA rated power. However, that increases the complexity of the control system and does not have a MVdc port. The filter inductor of the experimental system is 4.5 mH and the actual measured value of THD is 1.68%.

The SSTs in [29] and [44] combine medium-frequency (MF) isolation technology with MMC structure. Applying the mixed-frequency modulation strategy to the SMs, the LF to MF conversion is realized directly. The main advantage of these SSTs is that there is no need for an extra DCT behind the MMC rectifier stage, which reduces the number of SMs. Especially under the conditions of 10 kV MVac and 1 MW rated power, the theoretical efficiency of the SST system exceeds 97%. However, a more effective control strategy is needed to suppress the SM's voltage fluctuation, and the use of an MF transformer results in a large system volume. The grid-side current has a large THD value of about 5.5% and the value of the arm inductor is 2 mH.

In [10], an MMC-based SST is proposed. Each phase contains 20 cascaded SMs, totaling 120 HB SMs and 20 HFTs. Due to the fact that the dc/dc converters are connected behind each SM in the MMC, this significantly increases the number of active power devices. Therefore, an ISOP dc–dc converter is connected behind the MMC rectifier stage in the SST [14], which greatly reduces the number of SMs and HFTs. However, the high-power HFT heat dissipation and the peak efficiency of the whole system are challenging. On the other hand, the two-stage SST contains a large number of capacitors, making the whole system volume difficult to further reduce. The peak efficiency and the grid current THD are measured at 95.8% and 2.7%, respectively. The parameter values of grid voltage, arm inductors, and load conditions are 10 kV, 6 mH, and 200 kW, respectively.

In [24], the MMC with FB-SMs is used as a direct connection to the MV utility grid, so as to get an uneven voltage ratio $R_{(\mathrm{pu})}$.

In this way, the MMC operates as a step-down rectifier, and the rated voltage of the MVdc link is decreased to 2 kV. The fewer active power devices in the second stage might minimize the amount or size of the protection equipment. The value of the arm inductor is 5 mH and the operated power is 400 kW.

In [30], a triple-port SST using an RP^{2}C is proposed. The number of individual capacitors is greatly decreased to 120 μF. The main advantage is that the SMs can realize automatic voltage balance. However, the push–pull converter and the center-tapped HFT are used on the secondary side, which causes large voltage stress on the active power devices and increases the difficulty of HFT design. The peak efficiency of the experimental prototype is 96.9% under the 2.4 kW load condition. The values of the gird current THD and arm inductor are 2.4% and 1.2 mH, respectively.

The qualitative comparison of the proposed converter with other SSTs seems to reveal the weaknesses of the proposed SST, and the main issues can be divided into two aspects: the number of the SMs and system efficiency. Since an important feature of the proposed HI-MMC-based SST is the impact on downstream converters connected to the MVdc link, the number of DCTs with a small or high number of connections is further elaborated. These issues are explained as follows.

1) SM's Number: Compared with other ISM-based SSTs [30] and [31], the proposed converter does require more active power devices when obtaining a higher voltage ratio $R_{(\mathrm{pu})}$. However, it can provide an MVdc link with a lower voltage amplitude, which means that the number of active power devices in the converters connected downstream will be reduced. Therefore, the total number of active power devices will have a different trend depending on the specific situation.

Let us assume that the DCT connection of either the proposed HI-MMC-based SST or other ISM-based SSTs has N_{DCT} DCTs for the MVdc to LVdc stages. The total number of active power devices in the whole MVdc system with different number of the DCTs is depicted in the Fig. 30. It can be seen that for a low number of DCTs, the approaches in [30] and [31] will require fewer active power devices to construct MVdc system. On the

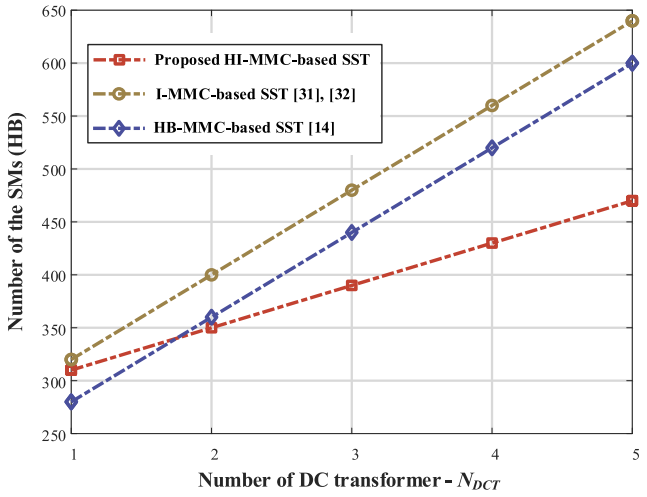

Fig. 30. Total number of active power devices in the whole MVdc system with different number of DCTs.

other hand, for a high N_{DCT}, the proposed HI-MMC-based SST always requires a fewer total number of active power devices in the MVdc system.

An example is given for quantitative analysis. Assuming that the MVdc system includes two DCTs connected to the photovoltaic and the ESS, the proposed HI-MMC-based SST can match a 10 kV MVac utility grid and a 10 kV MVdc system. Therefore, HI-MMC needs 270 HBs in the system, which include 5 ICCs and 5 IBCs in each arm. In addition, the two 10 kV DCTs need 20 isolated dc/dc converters. A total of 350 HBs are needed in the MVdc system. Under the same conditions of voltage levels, Sun et al. [30] and Liu et al. [31] require 240 HBs to build a three-port hybrid power conversion system and 40 isolated dc/dc converters used in two DCTs. A total of 400 HBs are needed in the MVdc system. From this perspective, the objective of the proposed SST would be to have a lower MVdc-link voltage for the next stage to reduce the number of converters connected downstream.

2) System Efficiency: Compared with the other SST topologies, the proposed HI-MMC, the I-MMC-based SST [30], and the RP^{2}C-MMC-based SST [31] do not have the highest system efficiency, even though these SSTs can realize single-stage power conversion. The main reason for limiting their further efficiency improvement is that the isolation stage adopts a sinusoidal power transfer strategy. It means that it is difficult to optimize the efficiency of the ISM over the entire operating range. However, the FB-MMC-based SST proposed in [24] uses a constant modulation ratio in the dc/dc isolation stage, and it suggests that it is possible to reach an efficiency bordering 99% ($\eta_{\mathrm{DC/DC}} \approx 98.8\%$). Even if the MMC stage ($\eta_{\mathrm{MMC}} \approx 99\%$) is considered, it still has a good efficiency of more than 97%. However, it should be noted that the proposed HI-MMC-based SST, the I-MMC-based SST [30], and the RP^{2}C-MMC-based SST [31] can effectively reduce the weight and volume of the overall system, which is an important characteristic of a single-stage SST. Therefore, it is more suitable for some MV multiport application scenarios with limited volume or weight.

VII. Conclusion

This article proposes a novel topology known as HI-MMC, which achieves a higher $R_{(\mathrm{pu})}$ to realize difference voltage level between MVdc and MVac. In previous sections, the operating principle, the efficiency analysis, and the design methods are illustrated. The simulation and experimental results of three-phase HI-MMC validate the correctness of the proposed SST. Compared with the conventional MMC-based SST topology, the HI-MMC topology has the following advantages.

1) Compared with the conventional MMC-based SST, the proposed topology has a higher $R_{(\mathrm{pu})}$, which can realize the decoupling design of MVac and MVdc voltage amplitudes.
2) Due to the concept of high-frequency link introduced in the SMs, it totally eliminates the individual capacitors, which avoids complex voltage-balancing control and has a simple precharging process.
3) The output voltage of the IBC includes positive and negative levels, which have dc fault recovery potential. It will further be discussed in future work.

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