Fault Current Limitation With Energy Recovery Based on Power Electronics in Hybrid AC–DC Active Distribution Networks

Bin-Long Zhang, *Graduate Student Member, IEEE*, Mou-Fa Guo, *Member, IEEE*, Ze-Yin Zheng, *Member, IEEE*, and Qiteng Hong, *Senior Member, IEEE*

***Abstract*—The active distribution networks have a tendency to develop toward hybrid ac–dc systems constructed by power electronics, the magnitude and direction of power may change randomly at any time, making the usual protection potentially insensitive, raising the negative impacts of single-phase ground (SPG) fault which accounts for the majority of all faults that occurred in medium-voltage (MV) distribution networks in the past. The zero-sequence current in the impedance induced between the lines and ground will pass through the SPG fault branch as fault current. This article transfers the flow path of the zero-sequence current from the SPG fault branch to the power electronic branch connected between the faulty phase and ground involved in the construction of hybrid ac–dc system, thereby limiting SPG fault branch current and reducing fault node potential. This helps to suppress fault arc and provides engineers with safe conditions to clear faulty elements from the SPG fault branch. The power electronic carries this zero-sequence current instead of SPG fault branch and therefore absorb energy from the distribution networks in the same way as SPG fault, but the energy is not lost but routed back to the hybrid ac–dc system for reuse. Simulations and experiments validate the proposal.**

***Index Terms*—Active fault arc suppression, energy recovery, energy router, fault current limitation, hybrid ac–dc active distribution networks, single-phase ground (SPG) fault, solid state transformer.**

I. Introduction

With the penetration of distributed resources, active distribution networks have a tendency to develop toward hybrid ac–dc systems constructed by a great quantity of power electronics [1]. In this case, the magnitude and direction of power may change randomly at any time [2], which may lead to the potential insensitivity of usual protection, thereby increase the negative impacts of faults [3]. According to statistics, the majority of all faults that occurred in medium-voltage (MV) distribution networks in the past were single-phase ground (SPG) faults, which may be accompanied by arcing, resulting in fires, electrocution of life, and widespread power outages [4], [5]. Thus, the active MV distribution networks are urgently needed to improve their capabilities of self-healing and self-recovery from SPG fault [6], [7].

SPG fault branch typically contains a large amount of capacitive fault current and a small amount of resistive fault current caused by the impedance induced between the lines and ground. Paul [8] provides a detailed analysis of SPG fault current via the symmetrical component method, where a phasor diagram of currents was drawn to make it easy to follow, and the flow path of the capacitive and resistive components of the SPG fault current was clarified. In [9], the experimental measurement of SPG fault current for various fault causes was conducted, and the real SPG fault current waveform data were collected for analysis and comprehending. The experimental results align well with those measured by other authors in other distribution networks mentioned in this literature, even if they applied simplified measuring circuits.

If the SPG fault current is large and persistent, a series of derivative problems may be caused. For examples, when the SPG fault current increases, the electrical potential of the ground may increase due to the thermal and mechanical stresses of grounding grid, and the protection provided by the grounding grid against step and contact potential may become insufficient [10]. Based on the analysis in Pons et al. [11], the fault current distribution between grounding electrodes and cables sheaths was considered as the main factor affecting the safety of grounding grid, and a simulation model was built to further analyze the negative impacts of different factors on the fault current distribution. Temporary overvoltage is another serious problem that may arise from SPG fault, and an experiment proved that the temporary overvoltage may exceed 2.3 p.u. in distribution networks with isolated neutral, sometimes may evolving into cross-phase faults [12]. Therefore, the SPG fault current and fault potential should be limited to a safe range, avoiding energy loss from fault in form of thermal energy and serious life-threatening electrocution [13]. Moreover, this helps to extinguish the fault arc and has a high probability of restoring the distribution networks on its own, or provides engineers with

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Bin-Long Zhang, Mou-Fa Guo, and Ze-Yin Zheng are with the College of Electrical Engineering and Automation, Fuzhou University, Fuzhou 350108, China (e-mail: belongz@foxmail.com; gmf@fzu.edu.cn; zhengzeyin@fzu.edu.cn).

Qiteng Hong is with the Department of Electronic and Electrical Engineering, University of Strathclyde, G1 1XQ Glasgow, U.K. (e-mail: q.hong@strath.ac.uk).

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safe conditions to clear faulty elements from the SPG fault branch in time, avoiding power outage to loads.

Among the latest applications, superconductor is considered to be one of the desired fault current limiter as it is lossless during the normal operation but an intrinsic high resistance can be induced during a fault to limit the high fault current, and it can be applied to different parts of ac and dc power systems, such as power generation, power transmission, and power distribution [14]. However, the cost of superconducting fault current limiter with design, manufacture, and operation is high compared to conventional current limiting solutions, and a low temperature operating environment is required so that it has not been fully accepted by the power system researchers and engineers and is therefore not applied on a large scale in industry [15]. It could be a very promising application in the future after addressing these problems.

At present, in dc system, current-limiting reactors are still commonly accepted, they suppress the surge of fault current when a fault occurs and contains resistors for further current limiting, but may deteriorate the system stability and dynamic responsiveness, the rapid fault current clearing, and system recovery. With the maturity of thyristor technology, fault current limiters based on power electronics have better cost performance. In [16] and [17], power electronic switches were applied to control the rapid opening and closing of reactor branch, mitigating the negative impacts of reactors on the system. However, reactors may saturate during fault current limiting and they can only limit the surge of fault current but not the peak. Consequently, Li et al. [18] presented to provide additionally virtual reactance controlled by modular multilevel converter that interconnects ac and dc systems at the converter station to assist the reactor in limiting fault current, avoiding reactor saturation and additional current limiting devices. Zheng et al. [19] applied a standalone controlled voltage source converter to completely replace reactors so that the negative impacts of reactors are completely eliminated, with better current limiting performance, but it is additionally installed. Similarly, in ac system, inductive Peterson coils are still the accepted fault current limiters commonly, but they may cause negative impacts on the system, such as resonance overvoltage and long transient process. Accordingly, power electronics were connected to the neutral point to work with inductive Peterson coils to regulate away from the resonance point, mitigating the negative impacts and further limiting the residual component of the SPG fault current [20], [21]. Moreover, the adjustable current-limiting coils combined with active converters were presented to reduce the capacity of inverters and improve the dynamic performance of inductive Peterson coils in [22] and [23]. However, the transient process is still long and the coil may affect the stability of converters. Thus, the authors in [24], [25], [26], and [27] applied the standalone single-phase or three-phase converters to limit the fault current, completely eliminating the negative impacts of inductive coils, with faster dynamic response and better stability, but the converters are also additionally installed, with high costs.

In the available research reported in literature, the main research gap between fault current limiters based on power electronics in ac and dc system is that dc fault current limiters take into account the energy interaction with the fault during the fault current limiting process, i.e., the flexible fault current limiter can recover fault energy for dc system [28], [29], but the recovered energy was consumed directly, not stored or reused. Therefore, Chen et al. [30] proposed a secondary active dc fault current limiter topology which not only has excellent secondary active current limiting performance, but also can recover and store fault energy for reuse. As for ac fault current limiters, the corresponding research reported in literature in this field is deficient, and the energy recovery technology is only available in rail transit [31], [32], [33], where the energy is usually generated by train braking and recovered via power electronics for reuse.

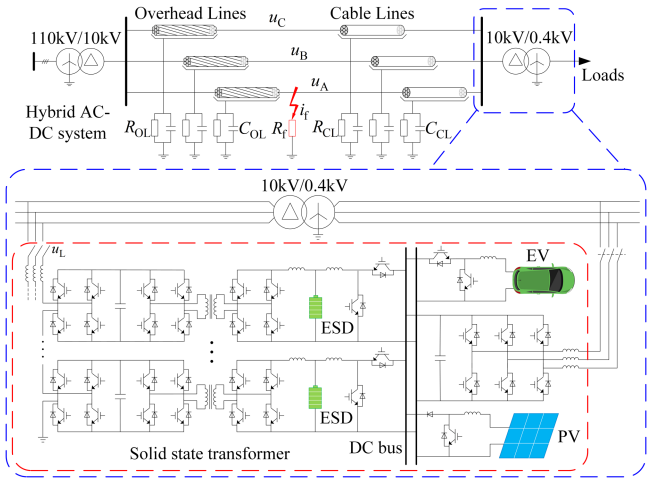

Fig. 1. Topology of hybrid AC–DC system with MV and LV interconnections based on solid state transformer.

As mentioned at the beginning, active distribution networks may develop in the future into complicated hybrid ac–dc systems constructed by many power electronics. Depending on the voltage level, hybrid ac–dc systems can be classified as low-voltage (LV) ac–dc system [34], [35], MV ac–dc system [36], [37], and high-voltage (HV) ac–dc system [38], as well as hybrid ac–dc system with MV and LV interconnections [39], [40] and MV and HV interconnections via solid state transformers [41]. They come in a variety of topologies, but operate in a large similar way. Of these, hybrid MV and LV ac–dc systems typically carry more distributed resources penetration due to the matching of voltage levels, including photovoltaic power (PV), wind power, energy storage devices (ESD), and electric vehicles (EV) that can be considered as sources or loads, thus the power electronics that interconnect multiple ac and dc systems are also considered as energy routers with multiple ports [42], [43], which can simultaneously manage the voltage, current, and power flow of hybrid ac–dc system.

Given the flexibility and availability of power electronics in ac–dc system, this article takes a hybrid ac–dc system with MV and LV interconnections based on solid state transformer as an example, applying the power electronics in the hybrid ac–dc system to limit the SPG fault branch current in the MV distribution networks while recovering the corresponding energy. As shown in Fig. 1, the topology of power electronic connected between the MV distribution networks and ground is a cascaded H-bridge

(CHB), where the dc-link of each H-bridge module contains a capacitor and is connected to the ESD of the dc system via isolated dc converter. All ESD are connected to the common dc bus of the dc system in parallel via nonisolated dc converters, and the distributed resources and loads, such as PV and EV are also connected in the dc bus via nonisolated dc converter. The dc bus is connected to the LV distribution networks via three-phase converter, building the hybrid ac–dc system with interconnection of the MV and LV distribution networks.

The implementation of this application is that when an SPG fault occurs in MV distribution networks, the CHB connected between the faulty phase and ground is controlled as a branch of zero-sequence circuit, transferring the flow path of the zero-sequence current in the impedance branch induced between the distribution networks and ground, from the SPG fault branch to the CHB branch, thereby limiting SPG fault branch current and reducing fault node potential, because this zero-sequence current is the main cause of SPG fault branch current. During this period, the CHB branch is connected between the faulty phase and ground in the same way as the SPG fault branch and carries this zero-sequence current instead of the SPG fault branch, and will therefore absorb energy from the MV distribution networks in the same way as a SPG fault. However, the absorbed energy is not lost like an SPG fault but is absorbed and temporarily stored in the dc capacitors. The isolated dc converters that interconnect the dc capacitor and the ESD in the dc system provide an energy routing path for the absorbed energy so that it can be immediately recovered and stored in the ESD for a long time or supplied directly to the LV distribution network loads via three-phase converter for reuse, while maintaining the dc capacitance voltage stable.

The contributions of this proposal are that it does not cause resonant overvoltage and long transient process as inductive Peterson coil does. In addition to limiting the fault current to avoid energy loss from the SPG fault branch, it also reduces the fault node potential at the same time, thus the fault arc can be extinguished due to the combustion conditions not being met, which also meets the safe conditions for engineers to clear faulty elements at the location of SPG fault, without power outage to loads. In addition, the problem of energy interaction between the SPG fault branch and the fault current limiter branch has been addressed to fill the research gap, and the power electronics are readily available in hybrid ac–dc active distribution networks, so that no additional fault current limiting devices are required, without high costs.

Moreover, this type of topology has good prospects for other application. During the normal operation of distribution networks, it serves as an energy router with multiple ports that can distribute power to loads to share the strain on distribution transformer. Especially in the case of charging EV in clusters at night, the power can be transmitted to the EV from both paths, the distribution transformer and the power electronics, avoiding overload operation of the distribution transformer, and the ESD can profit from the difference between peak-valley price by peak-load shifting. During this period, the power electronics can also convert the asymmetrical three-phase components in the MV distribution networks to the dc system and then reconvert them to symmetrical three-phase components for the LV distribution networks by controlling the CHB as a negative or zero-sequence circuit, which can symmetrize both the three-phase voltage and current in the MV and LV distribution networks. These are well worth studying for researchers at present and may be very useful for active distribution networks in the future.

It is worth emphasizing that the proposal is not limited to the specific topology referred to herein. The key to limiting SPG fault current for power electronics is that the topology has a zero potential point and is connected to ground, which can provide a flow path to the zero-sequence current induced between the distribution networks and ground to flow, so that preventing it from passing through the SPG fault branch, i.e., if a power electronic structure is open to zero-sequence current, it can be used to the proposal. In addition, it should have sufficient capability and is fully four-quadrant controllable. Moreover, any such power electronics capable of limiting the SPG fault current will absorb energy in the process of limiting the fault current, the absorbed energy can be recovered, and stored or fed back in the form of dc energy routing. The main contributions of this article are summarized as follows:

1) The characteristics of SPG fault current caused by the zero-sequence current induced between the MV distribution networks and ground are analyzed, whereby the characteristics of active power loss from the SPG fault caused by the zero-sequence current with different fault resistances is summarized.
2) By the zero-sequence circuit analysis in MV distribution networks, it is proposed to transfer the flow path of the zero-sequence current from SPG fault branch to power electronic branch. The vectors analysis shows that the active power will also be transferred to be absorbed by power electronic branch.
3) The coordinated control is designed to regulate the zero-sequence current while recovering the absorbed active power to distribution networks via energy routing based on power electronics. The simulations and experiments are carried out to verify the feasibility and effectiveness of the proposal.

The rest of the article is organized as follows. The principles of SPG fault current limiting with energy recovery are introduced in Section II. The control and implementation are presented in Section III. The simulation and experimental results are collected and discussed in Sections IV and V, respectively. Finally, Section VI concludes this article.

II. Principles of SPG Fault Branch Current Limiting With Energy Recovery

A. Analysis of SPG Fault Branch Current and Its Energy Loss

Taking the simplified 10 kV distribution networks with an SPG fault in Fig. 1 as an example for analysis. The feeder types include overhead lines and cable lines. The line impedance is temporarily neglected and only the phase-to-ground impedance is considered. Assume that the three-phase-to-ground impedance is symmetrical. R_{OL} and C_{OL} are the

phase-to-ground leakage resistance and capacitance of the overhead lines, respectively, and R_{CL} and C_{CL} are the phase-to-ground leakage resistance and capacitance of the cable lines, respectively, which all are induced between the distribution networks and ground and can be measured [5], [20]. u_{A}, u_{B}, and u_{C} are the three phase to ground voltages at the fault node, respectively. The grid frequency f is 50 Hz. The initial phase angle of the phase A voltage is assumed to be zero. The SPG fault occurs in the phase A, and the fault resistance is R_{f}, and the fault branch current is i_{f}.

According to Kirchhoff's current law (KCL), the SPG fault branch current can be expressed as

$$\begin{aligned} -i_{\mathrm{f}} = {} & u_{\mathrm{A}}\left(\frac{1}{R_{\mathrm{OL}}}+\mathrm{j}\omega C_{\mathrm{OL}}+\frac{1}{R_{\mathrm{CL}}}+\mathrm{j}\omega C_{\mathrm{CL}}\right) \\ & + u_{\mathrm{B}}\left(\frac{1}{R_{\mathrm{OL}}}+\mathrm{j}\omega C_{\mathrm{OL}}+\frac{1}{R_{\mathrm{CL}}}+\mathrm{j}\omega C_{\mathrm{CL}}\right) \\ & + u_{\mathrm{C}}\left(\frac{1}{R_{\mathrm{OL}}}+\mathrm{j}\omega C_{\mathrm{OL}}+\frac{1}{R_{\mathrm{CL}}}+\mathrm{j}\omega C_{\mathrm{CL}}\right). \end{aligned} \tag{1}$$

Let

$$R_0 = \frac{R_{\mathrm{OL}}R_{\mathrm{CL}}}{3\left(R_{\mathrm{OL}}+R_{\mathrm{CL}}\right)}, \tag{2}$$

$$C_0 = 3\left(C_{\mathrm{OL}}+C_{\mathrm{CL}}\right). \tag{3}$$

The SPG fault branch current i_{f} can be rewritten as

$$i_{\mathrm{f}} = \frac{u_{\mathrm{A}}}{R_{\mathrm{f}}} = \frac{e_{\mathrm{A}}+u_0}{R_{\mathrm{f}}} = -u_0\left(\frac{1}{R_0}+\mathrm{j}\omega C_0\right) = -i_0 \tag{4}$$

where e_{A} is the line-to-neutral voltage at the fault node phase A; u_0 is the zero-sequence voltage; and i_0 is the zero-sequence current in the impedance induced between the distribution networks and ground. This means that the zero-sequence current in the impedance induced between the distribution networks and ground is the main cause of SPG fault branch current. Further, u_0 can be expressed as

$$u_0 = \frac{-R_0 e_{\mathrm{A}}}{R_{\mathrm{f}}+R_0+\mathrm{j}\omega R_{\mathrm{f}}R_0C_0}. \tag{5}$$

Replacing (5) into (4), the SPG fault branch current can be restated as

$$i_{\mathrm{f}} = -i_0 = \frac{e_{\mathrm{A}}\left(1+\mathrm{j}\omega R_0C_0\right)}{R_{\mathrm{f}}+R_0+\mathrm{j}\omega R_{\mathrm{f}}R_0C_0}. \tag{6}$$

The active power p_{L} consumed by the SPG fault can be expressed as

$$p_{\mathrm{L}} = i_{\mathrm{f}}^2R_{\mathrm{f}} = i_0^2R_{\mathrm{f}} = \frac{|e_{\mathrm{A}}|^2|1+\mathrm{j}\omega R_0C_0|^2R_{\mathrm{f}}}{|R_{\mathrm{f}}+R_0+\mathrm{j}\omega R_{\mathrm{f}}R_0C_0|^2}. \tag{7}$$

From (7), the active power loss p_{L} is related to the fault resistance R_{f}, and the order of R_{f} in the denominator is higher than that in the numerator. The other parameters are constants. Take a medium-sized MV distribution networks in a suburb of China as an illustrative example, the typical constant parameters are $|e_{\mathrm{A}}| = 10/\sqrt{3}\,\mathrm{kV}$, $R_0 = 2000\ \Omega$, and $C_0 = 19.5\,\mu\mathrm{F}$, accordingly, the relationship between the active power loss p_{L} and the fault resistance R_{f} can be shown in Fig. 2.

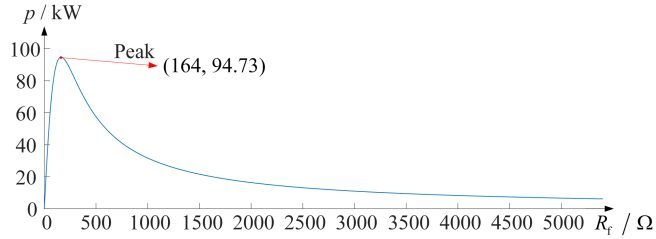

Fig. 2. Active power loss from the SPG fault under different fault resistances.

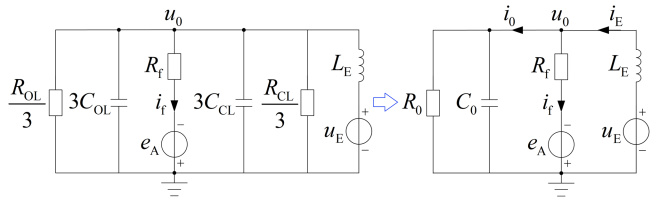

Fig. 3. Equivalent zero-sequence circuit of active MV distribution networks during an SPG fault.

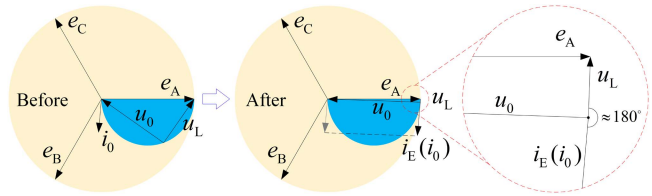

Fig. 4. Vector diagram of grid-connected voltage and output current of CHB in active MV distribution networks.

When R_{f} is between 17 and 1612 Ω, the active power loss exceeds 20 kW. In this case, the temperature of the fault branch will rise with time, resulting in serious heating, which may cause serious accidents, such as fires and electrocution of life. When $R_{\mathrm{f}} = 164\ \Omega$, the active power loss is the largest, which is 94.73 kW. If the SPG fault branch current i_{f} can be rapidly reduced to zero, the fault branch can be equivalent to an open circuit and R_{f} is equivalent to an infinite resistance. In this case, $p_{\mathrm{L}} = 0$ according to (7), and the fault energy loss and corresponding negative impacts can be eliminated.

B. Principles of SPG Fault Branch Current Limiting With Energy Recovery Via Power Electronics

As shown in Fig. 1, when an SPG fault occurs, the current of the CHB branch connected to the fault phase is regulated to bypass the SPG fault branch. The fault phase can be identified via the fault phase selection algorithm that has been studied to identify SPG fault phase for fault current limiters to adapt to asymmetric distribution networks [24]. In this case, the zero-sequence equivalent circuit of the MV distribution networks can be drawn, as shown in Fig. 3.

Where u_{E} and i_{E} are the output voltage and output current of the CHB branch, respectively; and L_{E} is the filter inductor. From Fig. 4, if $i_{\mathrm{E}} = i_0$, $i_{\mathrm{f}} = 0$ according to KCL and $u_0 = -e_{\mathrm{A}}$ according to Kirchhoff's voltage law. The output current of CHB

branch i_{E} is described as

$$i_{\mathrm{E}} = i_0 = u_0\left(\frac{1}{R_0} + \mathrm{j}\omega C_0\right) = -e_{\mathrm{A}}\left(\frac{1}{R_0} + \mathrm{j}\omega C_0\right). \quad (8)$$

The parameters R_0 and C_0 can be obtained in many ways [5], [20], so the reference current of CHB can be calculated by (8). In this way, the flow path of i_0 is transferred from the SPG fault branch to the CHB branch, so that the SPG fault branch current i_{f} is regulated to zero and R_{f} is equivalent to an infinite resistance, $p_{\mathrm{L}} = 0$ according to the analysis in Part A above, avoiding energy loss from the SPG fault branch caused by the zero-sequence i_0, and there are no fault current limiting devices that need to be additionally installed.

During this process, since the flow path of i_0 is transferred from the SPG fault branch to the CHB branch, there is energy interaction between them, i.e., the energy caused by the zero-sequence i_0 will also be transferred from the SPG fault branch to be absorbed by the CHB converter. The active power output by CHB converter branch p_{O} can be expressed as

$$p_{\mathrm{O}} = |u_{\mathrm{L}} \cdot i_{\mathrm{E}}| = |u_{\mathrm{A}} \cdot i_0| = |u_{\mathrm{A}}| \cdot |i_0| \cos\alpha. \quad (9)$$

where u_{L} is the voltage at the connection point between the CHB branch and fault phase of MV distribution networks, and α is the phase angle difference between u_{L} and i_0. The active power output by the CHB converter should ideally be zero because the fault node potential is reduced to $u_{\mathrm{A}} = u_0 + e_{\mathrm{A}} = 0$. Consequently, the fault arc can be extinguished due to the combustion conditions not being met, which also meets the safe conditions for engineers to clear faulty elements at the location of SPG fault, without power outage to loads, and other negative impacts can also be minimized.

However, u_{L} is different from u_{A} due to the existence of line impedance in practice, so the active power output by the CHB converter is typically not zero. The vectors u_{L} and i_0 before and after the SPG fault current is limited can be drawn in Fig. 4.

According to Fig. 4, although the amplitude of u_{L} is not very large after the SPG fault current is limited, the phase angle difference α between u_{L} and i_0 is close to $180°$. Therefore, $\cos\alpha \approx -1$, and (9) can be represented as

$$p_{\mathrm{O}} = |u_{\mathrm{L}} \cdot i_{\mathrm{E}}| = |u_{\mathrm{L}} \cdot i_0| = |u_{\mathrm{L}}| \cdot |i_0| \cos\alpha \approx -|u_{\mathrm{L}}| \cdot |i_0|. \quad (10)$$

It can be seen that the CHB converter will absorb active power. This is because it is connected between the faulty phase and ground in the same way as the SPG fault branch, and carries this zero-sequence current in the impedance branch induced by the distribution networks and ground instead of SPG fault branch, and will therefore absorb active power from the MV distribution networks in the same way as an SPG fault, which indicated that the CHB converter absorbs the energy that would otherwise be lost by the SPG fault branch. The energy absorbed by the CHB converter will be stored in the dc capacitors, resulting in the dc-link voltages of the CHB to rise, affecting the CHB performance. With the help of isolated dc converters, the energy absorbed by the CHB converter is immediately recovered via dc capacitor energy routing, it can be stored in the distributed ESD for a long time or supplied directly to the LV loads via the three-phase converter for reuse so as to keep the dc-link voltages of the CHB stable. Thus, the research gap of energy interaction between the SPG fault and the fault current limiter can be filled.

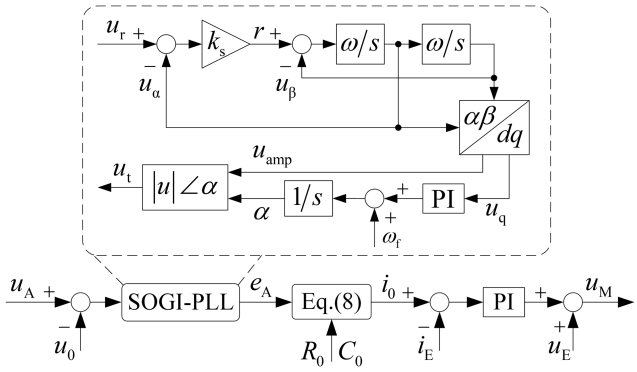

Fig. 5. Schematic diagram of reference value acquisition and control for CHB converter.

III. Control and Implementation

A. Coordinated Control

The control objective of CHB converter connected between the fault phase of MV distribution networks and ground is its output branch current i_{E}, whose reference value is the zero-sequence current in the impedance induced between the MV distribution networks and ground, which can be calculated using (8), and the purpose is to transfer the flow path of the zero-sequence current from SPG fault branch to CHB branch, limiting the SPG fault branch current. However, the key to calculating the reference current value is to obtain accurate e_{A} which cannot be measured directly but is obtained by subtracting u_{A} and u_0 that can be measured directly, i.e., $e_{\mathrm{A}} = u_{\mathrm{A}} - u_0$. To accurately extract e_{A}, a second-order generalized integral and a phase-locked loop (SOGI–PLL) are designed, as shown in Fig. 5, where u_{r} is the input signal whose amplitude and phase angle at the fundamental frequency need to be extracted; and u_α and u_β are quadrature signals decomposed from u_{r}. k_{s} is the gain coefficient of the SOGI; ω is the fundamental angular frequency; u_{amp} is the amplitude obtained at the fundamental frequency; and α is the phase angle obtained at the fundamental frequency. u_{t} is the output signal composed of u_{amp} and α. After the reference current value i_0 is calculated by (8), a proportional–integral (PI) controller is used to regulate the output current of the CHB converter i_{E}.

The control objectives of isolated dc converters connected between the dc-link of CHB and the ESD of dc system are the dc-link capacitor voltages of CHB, the aim is to route the energy absorbed by the CHB converter and maintaining the dc-link voltages of CHB. In order to adaptively regulate the size and direction of energy routing, single phase-shift control method is adopted. The two H-bridges of each isolated dc converter are, respectively, given a square wave with frequency of 1000 Hz and pulsewidth of 50% as trigger signal. The phase angle of square wave of the H-bridge on the dc-link capacitor side is $0°$, and that on the other side is shifted to θ which is adjusted by

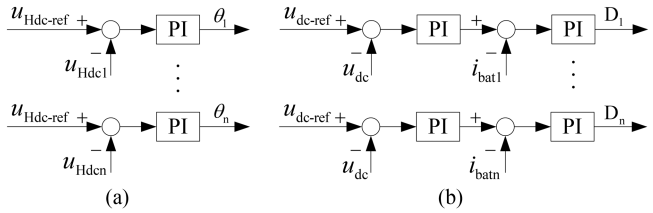

Fig. 6. Control schematic diagram of isolated DC converters and nonisolated DC converters: (a) isolated DC converters for maintaining DC-link voltages of CHB and (b) nonisolated DC converters for supporting common DC bus voltage.

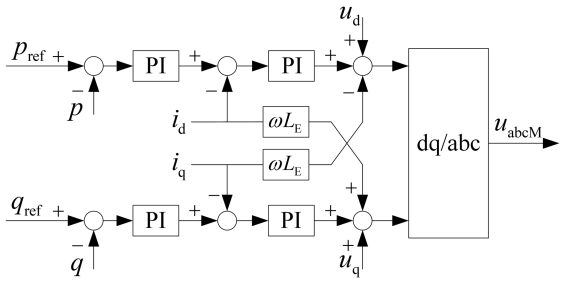

Fig. 7. Control schematic diagram of three-phase converter for suppling active power and reactive power to LV distribution networks.

a PI controller, as shown in Fig. 6(a), where u_{Hdcn} and θ_{n} are the dc-link voltage and phase-shift angle of the nth H-bridge module, respectively, $n = 1, 2, 3\ldots$; $u_{\text{Hdc}-\text{ref}}$ is the reference voltage of the dc-links of the CHB.

The control objective of the nonisolated dc converters connected between the ESD and the common dc bus in dc system is the dc bus voltage u_{dc}, to support its stability, as shown in Fig. 6(b), where $u_{\text{dc}-\text{ref}}$ is the reference voltage of the dc bus; i_{batn} and D_{n} are the output current from the ESD to the dc bus and duty cycle signal of the nth ESD, respectively, $n = 1, 2, 3\ldots$. The two PI controllers in series are adopted to manage u_{dc} and i_{batn}, respectively.

The control objectives of three-phase converter connected between the dc bus of dc system and the LV distribution networks are active power and reactive power output to the LV distribution networks. The control schematic diagram for the three-phase converter is shown in Fig. 7, where p_{ref} and q_{ref} are the reference active and reactive power, respectively; i_{d} and i_{q} are the output currents on the d-axis and q-axis, respectively; and u_{d} and u_{q} are the output voltage on the d-axis and q-axis, respectively. The modulated voltage signal u_{abcM} can be obtained by Park inverse transformation.

B. Implementation Process

The implementation flowchart of the coordinated control is shown in Fig. 8. During the normal operation of distribution networks, the insulation parameters can be measured in real time [5], [20]. When an SPG fault occurs, the fault phase can be identified rapidly [24], and then the fault phase voltage and zero-sequence voltage are sampled and the difference between them is calculated in real time. Through the control system shown in Fig. 5, the line-to-neutral voltage of the fault phase can be extracted from the difference by means of SOGI–PLL so

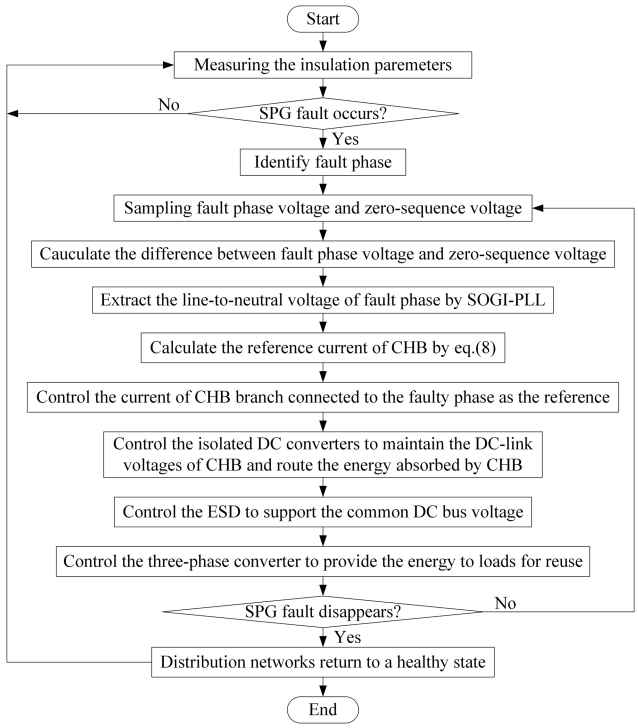

Fig. 8. Implementation flowchart of SPG fault limiting with energy recovery based on power electronics in hybrid AC–DC system.

that the reference current of the CHB can be calculated by (8). Then, the output current of CHB branch connected to the faulty phase is regulated as the reference current value to limit the SPG fault branch current and absorb the corresponding energy. Meanwhile, by using the control system shown in Fig. 6, the isolated dc converters are controlled to maintain the dc-link voltages of CHB so that the energy absorbed by the CHB is immediately routed to the ESD for long-term storage or provided directly to support common dc bus voltage and then to loads for reuse. Until the SPG fault arc is extinguished and the faulty elements are cleared, the distribution networks return to normal operation and this process is terminated.

IV. Simulation and Discussion

A. Simulation Parameters

A simulation model was built on the Simulink platform of Matlab-2017 b. The simulation type is discrete with the solver type being variable-step and the max step size being 100 μs. The line type is three-phase PI section with overhead lines and cable lines. The battery type is lithium-ion, and the module type of PV array is 1STH-230-P, with 10 series-connected modules per string and 20 parallel strings. The parameters in the simulation model are shown in Table I.

B. Performances of Fault Current Limiting

Assuming an SPG fault occurs at $t = 0.1$ s. To compare the situations before and after the fault current limitation, 0.4 s after the SPG fault occurred and the output current of CHB branch

TABLE I
SIMULATION PARAMETERS

Parameters	Value
Sample time	100 [μs]
Phase-to-phase voltage	10 [kV]
Capacitance to ground C_0	19.5 [μF]
Resistance to ground R_0	2 [kΩ]
Number of H-bridges in CHB N	10
DC-link voltage of H-bridge u_{Hdc}	1000 [V]
DC-link capacitor of H-bridge	4700 [μF]
Filter inductance of CHB L_{E}	0.05 [H]
Frequency of dc isolated transformer	1000 [Hz]
Winding ratio of dc isolated transformer	4:1
Nominal ESD voltage	300 [V]
Rated ESD capacity	500 [Ah]
Initial state-of-charge (SOC)	50 [%]
DC bus voltage u_{dc}	380 [V]
Sun irradiance of PV system	1000 [W/m^2]
Cell temperature of PV system	25 [°C]
Maximum output voltage of PV system	300 [V]
Maximum output power of PV system	45.75 [kW]

connected between the faulty phase and ground is controlled as i_0, so that the flow path of the zero-sequence current in the impedance induced between the distribution networks and ground is transferred from the SPG fault branch to the CHB branch. Fig. 9 shows the performances, including the active power loss from the SPG fault p_{L} and the SPG fault branch current i_{f}, when $R_{\text{f}} = 1\ \Omega$ and $R_{\text{f}} = 50\ \Omega$, respectively.

At the initial period of the SPG fault, the SPG fault branch current has a large impulse. The maximum impulse current reaches 1913 A in the case of $R_{\text{f}} = 1\ \Omega$, accordingly, the active power loss from the SPG fault has a large impulse. The impulse decreases as the fault resistance increases. The maximum impulse current is 74 A in the case of $R_{\text{f}} = 50\ \Omega$. Before the SPG fault branch currents are limited, although the fault branch currents in steady state 35.23 and 32.93 A are very close when $R_{\text{f}} = 1\ \Omega$ and $R_{\text{f}} = 50\ \Omega$, respectively, the active power losses 2.24 and 54.22 kW are very different. Because p_{L} is related to R_{f} according to (7), and the curve slope in Fig. 2 is large when R_{f} is small. After the SPG fault branch currents are limited, the fault branch currents decrease to 0.93 and 0.86 A when $R_{\text{f}} = 1\ \Omega$ and $R_{\text{f}} = 50\ \Omega$, respectively. Meanwhile, the active power losses drop to less than 0.1 W, approaching 0 kW.

When $R_{\text{f}} = 164\ \Omega$, the performances of the active power loss from the SPG fault p_{L} and SPG fault branch current i_{f} are shown in Fig. 10. They have not the current impulse and active power loss impulse at the initial period of the SPG fault. The active power loss in steady state almost reaches the maximum value 94.26 kW, which aligns well with the consequence shown in Fig. 2. After the SPG fault branch current is limited, the residual current of the faulty branch is only 0.67 A, and the active power loss is also less than 0.1 W, close to zero.

When R_{f} is greater than 164 Ω, the active power loss from the SPG fault decreases. Fig. 11 shows the performances in the cases of $R_{\text{f}} = 500\ \Omega$ and $R_{\text{f}} = 2000\ \Omega$, respectively. Because

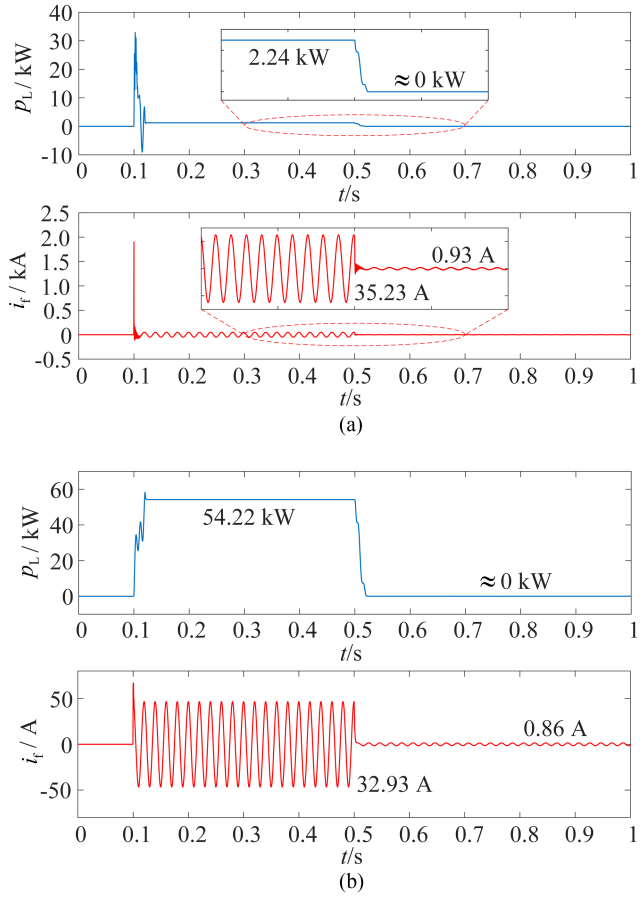

Fig. 9. Simulation waveforms of active power loss from the SPG fault p_{L} and SPG fault branch current i_{f} in the cases of different fault resistances: (a) $R_{\text{f}} = 1\ \Omega$ and (b) $R_{\text{f}} = 50\ \Omega$.

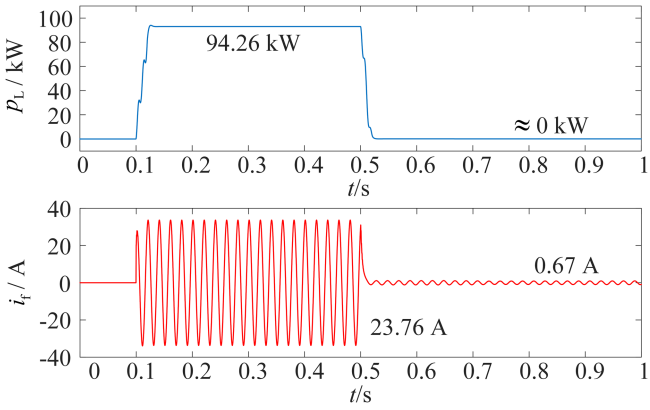

Fig. 10. Simulation waveforms of active power loss from the SPG fault p_{L} and SPG fault branch current i_{f} in the case of $R_{\text{f}} = 164\ \Omega$.

R_{f} is large enough, they have not the current impulse and active power loss impulse. Moreover, although the SPG fault branch currents in steady state 10.64 and 2.83 A are relatively small, the active power losses reach 56.34 and 16.02 kW, respectively, which align well with the theoretical analysis conclusion of (7) and Fig. 2. After the SPG fault branch currents are limited, the residual currents of the faulty branch are 0.35 and 0.09 A,

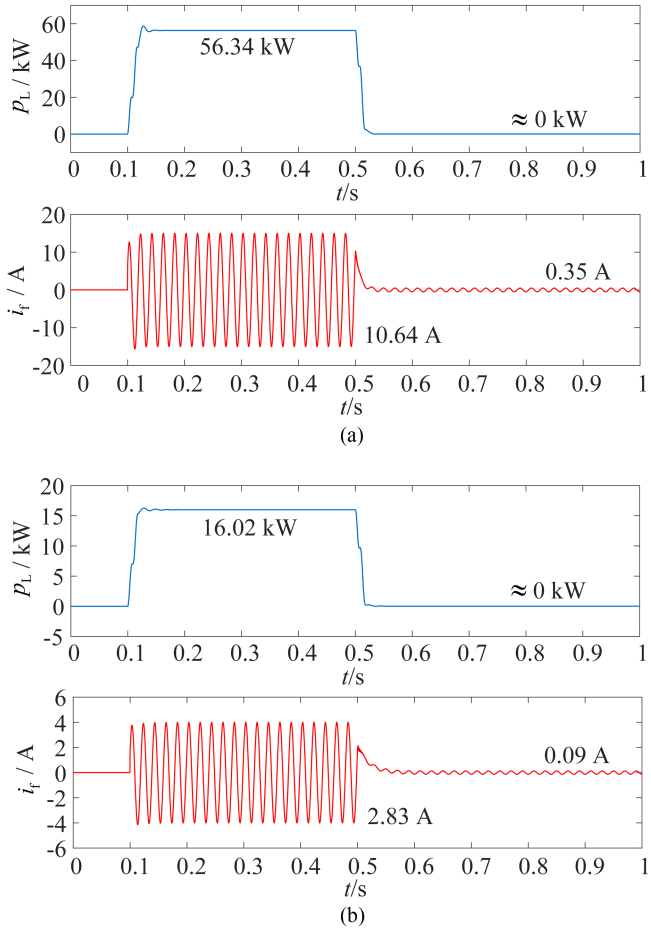

Fig. 11. Simulation waveforms of active power loss from the SPG fault p_{L} and SPG fault branch current i_{f} in the cases of different fault resistances: (a) $R_{\mathrm{f}} = 500\ \Omega$ and (b) $R_{\mathrm{f}} = 2000\ \Omega$.

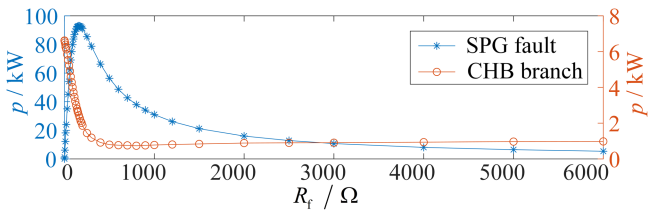

Fig. 12. Active power lost by the SPG fault and active power absorbed by the CHB converter under different fault resistance conditions.

respectively, and the active power losses will also reduce to less than 0.1 W, near zero.

The active power curves are fitted in Fig. 12 by discrete points under different fault resistance conditions, including the active power loss from the SPG fault branch and the active power absorbed by the CHB branch during fault current limitation. The statistical results show that the active power loss curve from the SPG fault is consistent with Fig. 2. The active power absorbed by the CHB converter is large when R_{f} is small, but it becomes small when R_{f} is large. Because the active power loss after the fault current limitation does not exceed 0.1 W, shown in Figs. 9–11, while the active power absorbed by the CHB converter exceeds

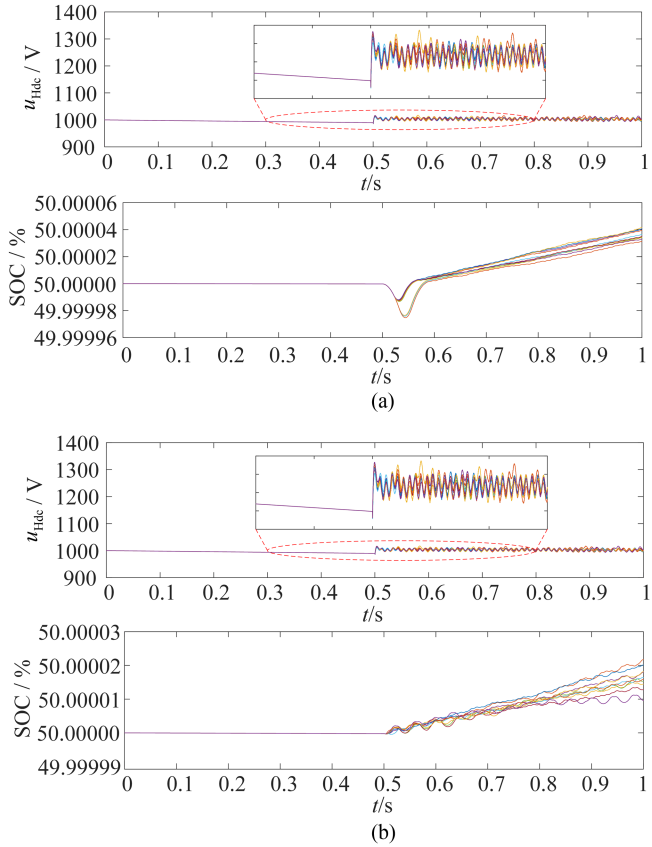

Fig. 13. DC-link voltages of CHB converter and SOC of ESD in the cases of different fault resistances: (a) $R_{\mathrm{f}} = 10\ \Omega$ and (b) $R_{\mathrm{f}} = 100\ \Omega$.

1 kW, which is evident by Fig. 12, thus the percentage of active power loss is no more than $0.1/1000 = 0.01\%$ of the total at this time, i.e., the recovered active power can reach over 99.99%.

In summary, through CHB converter, for a wide range of R_{f} that has been tested, the SPG fault branch current can be limited effectively, and the active power loss from the SPG fault can be minimized, i.e., close to 0 kW. After the flow path of the zero-sequence current is transferred from the SPG fault branch to the CHB branch, the negative impacts of the SPG fault are eliminated, which prompts the distribution networks to resume normal operation. Meanwhile, the active power absorbed by the CHB converter can be stored in the ESD for a long time or supplied directly to loads for reuse, the following shows their simulation performances.

C. Performances of Energy Recovery

Fig. 13 shows the performances, including the dc-link voltages of the CHB converter and the SOC of ESD, when $R_{\mathrm{f}} = 10\ \Omega$ and $R_{\mathrm{f}} = 100\ \Omega$, respectively.

At the beginning, the SOC is 50%, and the dc-link voltages of the CHB are 1000 V. Before $t = 0.5$ s, the isolated dc converters do not work, and the dc-link voltages of the CHB converter drop slightly due to dc-link loss. After $t = 0.5$ s, the SPG fault branch current is transferred to the CHB branch, so that the energy caused by the SPG fault branch current is also transferred to the CHB converter, and only the energy absorbed by the CHB

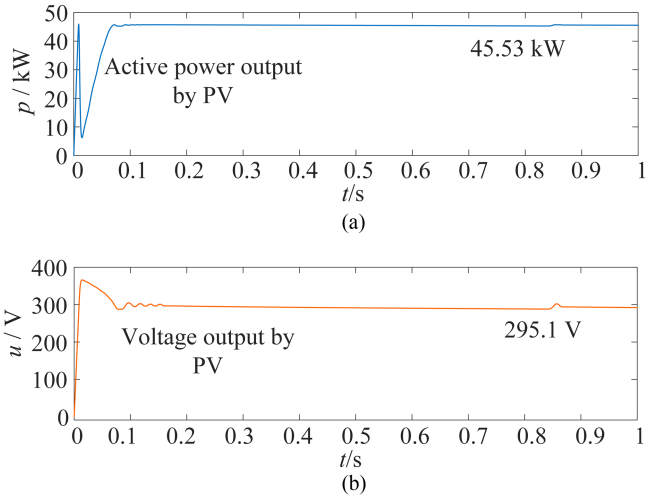

Fig. 14. Simulation waveforms of PV system. (a) Active power output by PV system. (b) Voltage output by PV system.

converter during this period is stored in the ESD. The dc-link voltages of the CHB are restored and maintained at 1000 V. The SOC rise from 50%, and the rising speed in the case of $R_{\mathrm{f}} = 10\,\Omega$ is about twice that in the case of $R_{\mathrm{f}} = 100\,\Omega$, because the active power absorbed by the CHB converter in the case of $R_{\mathrm{f}} = 10\,\Omega$ is twice as much as that in the case of $R_{\mathrm{f}} = 100\,\Omega$ according to Figs. 2 and 12. In the cases, although the SOC of the ESD is uneven, they can be evenly redistributed via the common dc bus.

The ESD is used to support the common dc bus voltage u_{dc} by controlling the nonisolated dc converters connected between the ESD and the common dc bus in parallel, and the three-phase converter connected between the common dc bus and the LV distribution networks is responsible for converting the energy from the PV system and the ESD to LV distribution networks for reuse, their performances are shown in Figs. 14 and 15. Because the LV distribution networks only need the three-phase converter to convert active power 20 kW, but the active power generated by the PV system is close to the maximum. Therefore, without dc load power, the ESD will store the surplus active power 25.37 kW to maintain the dc bus voltage at 380 V. When the active power generated by the PV system is insufficient, the ESD will serve as backup power source to output active power to support the dc bus voltage.

V. Experiment and Discussion

A. Experimental Prototype

The proposed SPG fault current limitation with energy recovery is verified on a physical experimental system, as shown in Fig. 16.

Where the specifications of distribution network cabinets and CHB industrial prototype are shown in Table II. The separate FPGA in each H-bridge module is used to receive switch drive signals from the master CPU with operation system, control the output of H-bridge module, and collect and provide feedback on operation information about the H-bridge module to the master

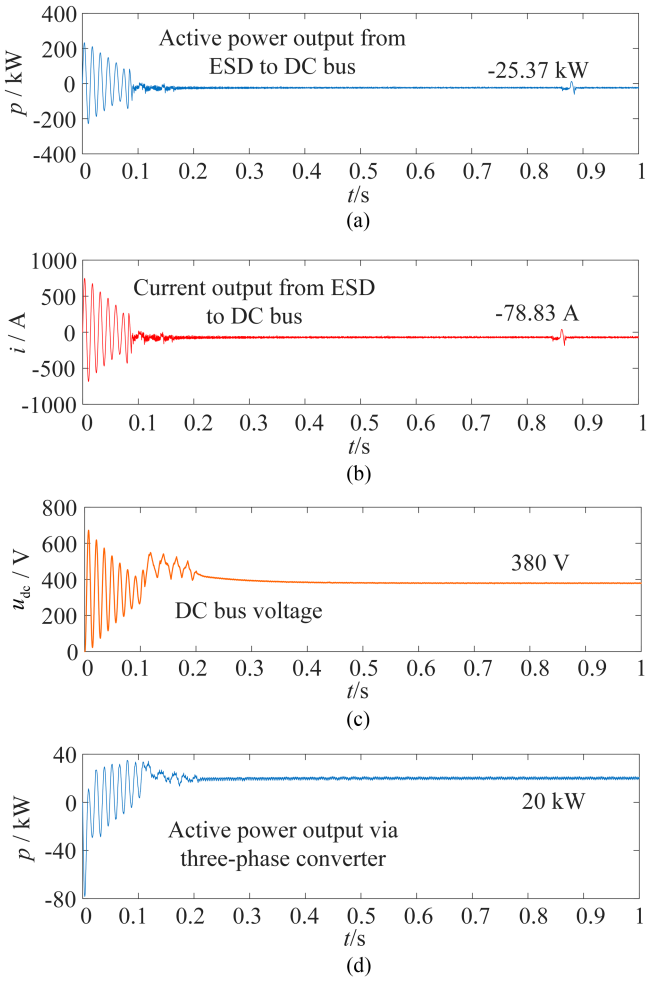

Fig. 15. Simulation waveforms of DC system. (a) Active power output from ESD to DC bus. (b) Current output from ESD to DC bus. (c) DC bus voltage. (d) Active power converted from DC system to LV distribution networks via three-phase converter.

TABLE II
Specifications of Distribution Network Cabinets and CHB Industrial Prototype

Parameters	Value
Sample frequency	6 [kHz]
Phase to phase voltage	380/380 [V]
Phase to ground capacitance	13.92 [μF]
Phase to ground resistance	800 [Ω]
DC-link voltage of H-bridge u_{Hdc}	40 [V]
DC-link capacitor of H-bridge	600 [μF]
Filter inductance of CHB L_{E}	58.33 [mH]
DC bus voltage u_{dc}	120 [V]
Number of H-bridges	12

CPU which communicates with the FPGA via optical fiber. The output current and voltage of CHB branch, and the three-phase voltage and current of distribution networks are sampled by Hall sensors as feedback signals of the master CPU, the specifications of sensors are shown in Table III, and the hardware working schematic of the experiment system is shown in Fig. 17. The

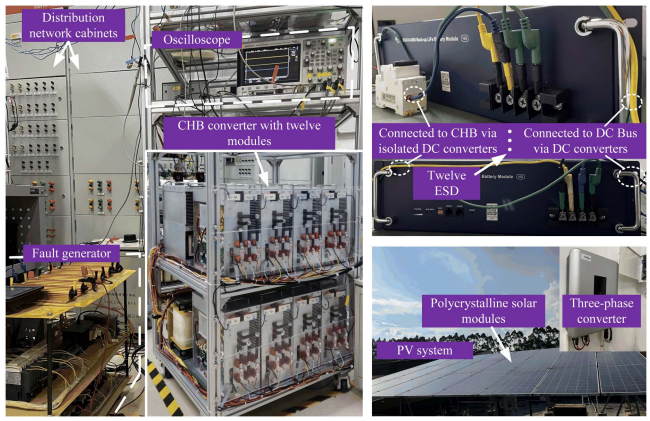

Fig. 16. Photos of physical prototype of hybrid AC–DC system.

TABLE III
SPECIFICATIONS OF SENSORS

Parameters	Value
Rated input of voltage sensor	400 [V]
Measuring range of voltage sensor	0–±480 [V]
Measuring resistance of voltage sensor	>10 [kΩ]
Rated output of voltage sensor	5 [V]
Accuracy of voltage sensor	±1.0 [%]
Supply voltage of voltage sensor	±12 [Vdc]
Frequency range of voltage sensor	0–20 [kHz]
Rated input of current sensor	15 [A]
Measuring range of current sensor	0–±48 [A]
Rated output of current sensor	2.5±0.625 [V]
Accuracy of current sensor	±0.7 [%]
Supply voltage of current sensor	+5 [VDC]
Frequency range of voltage sensor	0–100 [kHz]

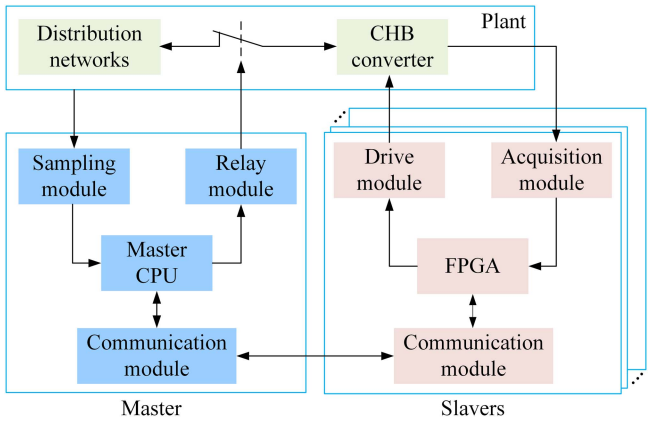

Fig. 17. Hardware working schematic of distribution networks and CHB.

CHB is connected to the distribution networks via contactor controlled by the master CPU with fault phase selection algorithm [24], and the specifications of contactor are shown in Table IV. The fault generator contains resistors with different resistance values (10, 50, 100, 200, 500, 1000, 2000, 5000 Ω) which are opened and closed by silicon-controlled rectifier controlled via MCU to simulate different fault resistors, and the schematic is

TABLE IV
SPECIFICATIONS OF CONTACTOR

Parameters	Value
Thermal stability current	125 [A]
Rated insulation voltage	690 [V]
Utilization category	AC-3
Rated voltage at single-phase	220/230 [V]
Rated power at single-phase	25 [kW]
Rated voltage at three-phase	380/660 [V]
Rated power at three-phase	45 [kW]

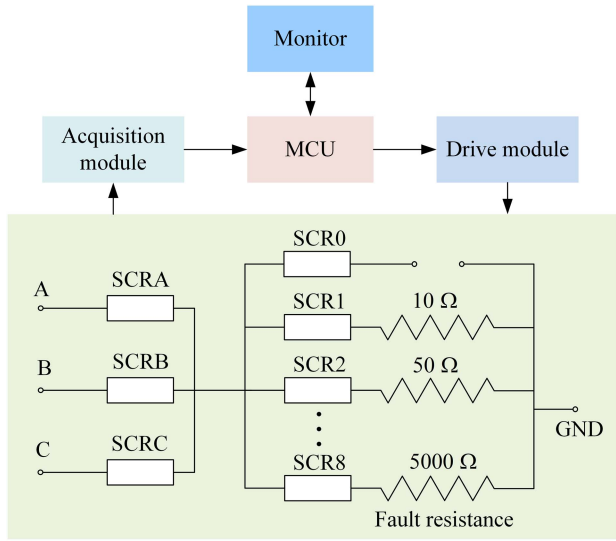

Fig. 18. Fault generator schematic.

TABLE V
SPECIFICATIONS OF ESD

Parameters	Value
Normal voltage per battery	48 [V]
Rated capacity per battery	50 [Ah]
Operating voltage range per battery	40–56.4 [V]
Maximum charging voltage per battery	60.4 [V]
Maximum charging current per battery	10 [A]
Maximum discharge voltage per battery	55 [V]
Maximum discharge current per battery	50 [A]
Discharge cut-off voltage	40 [V]
Number of batteries	12

drawn in Fig. 18. The type of ESD is lithium iron phosphate battery with operational protection, and its specifications are shown in Table V. In addition, the module type of PV system is TP660P polycrystalline solar module with 60 cell series, and the specifications are shown in Table VI.

B. *Performances of Fault Current Limiting*

Figs. 19–21 show the experimental results of SPG fault branch current limiting, including the voltage waveforms of CHB, the current waveforms of SPG fault branch, and the output current

TABLE VI
SPECIFICATIONS OF PV SYSTEM

Parameters	Value
Maximum power per module	275 [W]
Operating voltage per module	31.7 [V]
Operating current per module	8.69 [A]
Open-circuit voltage per module	38.7 [V]
Short-circuit current per module	9.17 [A]
Module efficiency	16.8 [%]
Number of modules in PV system	6
Number of series-connected modules per string	3
Number of parallel strings	2
Number of series-connected PV module	3
Maximum power of PV system	1.65 [kW]
Maximum voltage of PV system	95.1 [V]

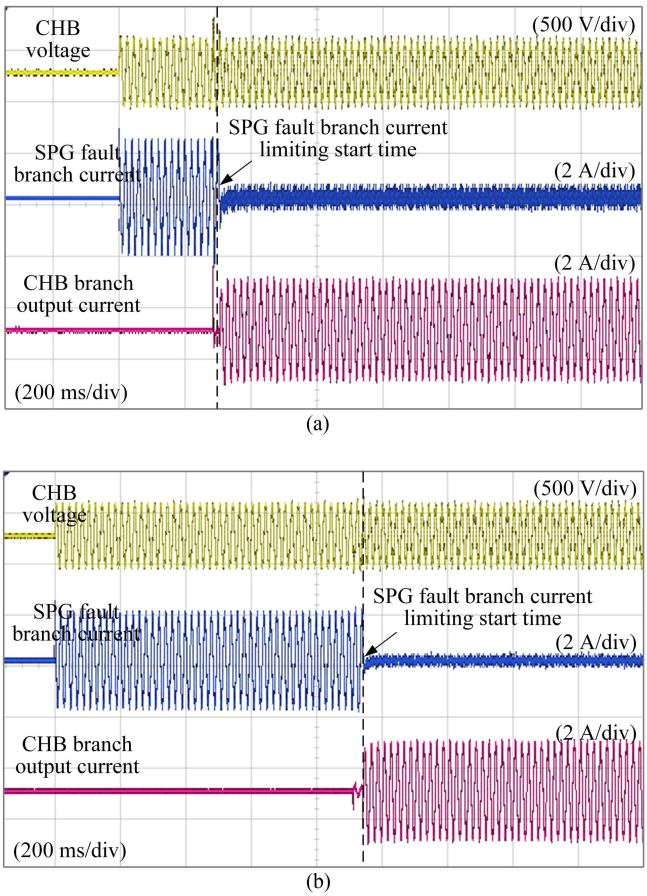

Fig. 19. Experimental waveforms of SPG fault branch current limiting in the cases of different fault resistances: (a) $R_{\mathrm{f}} = 10\ \Omega$ and (b) $R_{\mathrm{f}} = 50\ \Omega$.

waveforms of CHB branch, in the cases of different fault resistances ($R_{\mathrm{f}} = 10\ \Omega$, $50\ \Omega$, $100\ \Omega$, $500\ \Omega$, $2000\ \Omega$, and $5000\ \Omega$).

As shown in Fig. 19, when R_{f} is small, because the fault phase voltage drops to near zero and u_0 is close to $-e_{\mathrm{A}}$, so the SPG fault branch current is large which is consistent with (6). After the current in the SPG fault branch is transferred to the CHB branch successfully, the residual current in the SPG fault branch is close to zero, thus, the active power loss from the SPG fault

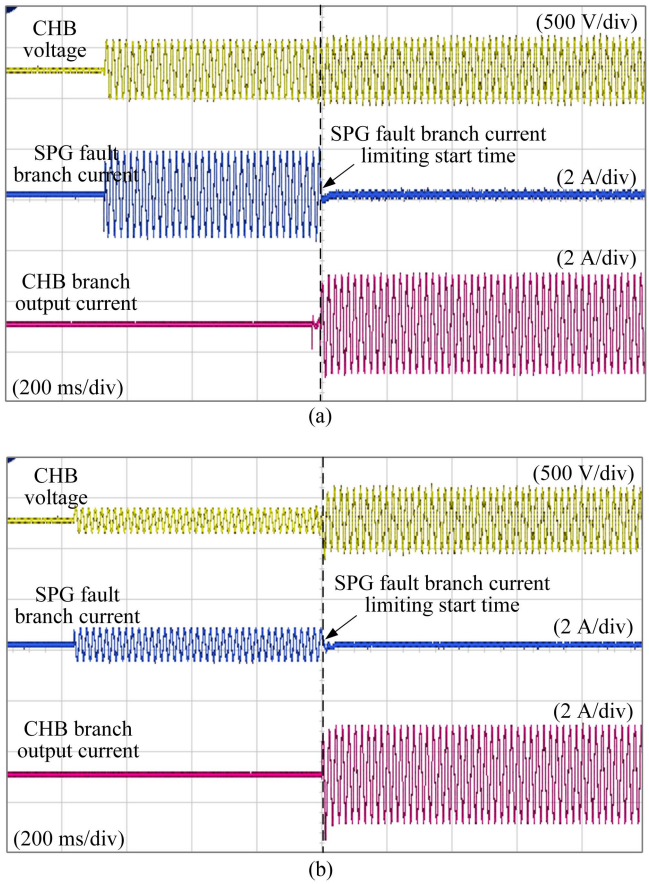

Fig. 20. Experimental waveforms of SPG fault branch current limiting in the cases of different fault resistances: (a) $R_{\mathrm{f}} = 100\ \Omega$ and (b) $R_{\mathrm{f}} = 500\ \Omega$.

caused by the current can be reduced. From Figs. 20 and 21, when R_{f} is large, the SPG fault branch current is small because the fault phase voltage does not significantly drop and u_0 is not very large. However, the current transferred to the CHB branch is large, which is due to that after the SPG fault branch current is transferred, the fault phase voltage is further reduced to near zero and u_0 increases to near $-e_{\mathrm{A}}$ according to (8) and Fig. 4. When R_{f} is large enough, the SPG fault branch current is small enough and the residual current of the faulty branch is closer to zero after the current limiting. The current transferred to CHB branch is always large, and is always the same value calculated by (8).

C. Performances of Energy Recovery

The experimental results of recovering the energy absorbed by the CHB converter are shown in Fig. 22, including the dc-link voltage of an H-bridge module, the voltage, and current of an ESD charging. For a clear analysis, only the active power absorbed by the CHB converter is stored in the ESD. In the cases of $R_{\mathrm{f}} = 100\ \Omega$ and $R_{\mathrm{f}} = 500\ \Omega$, respectively, the charging currents of the ESD are different due to the different active power absorbed by the CHB converter, but the dc-link voltages can be maintained at 40 V.

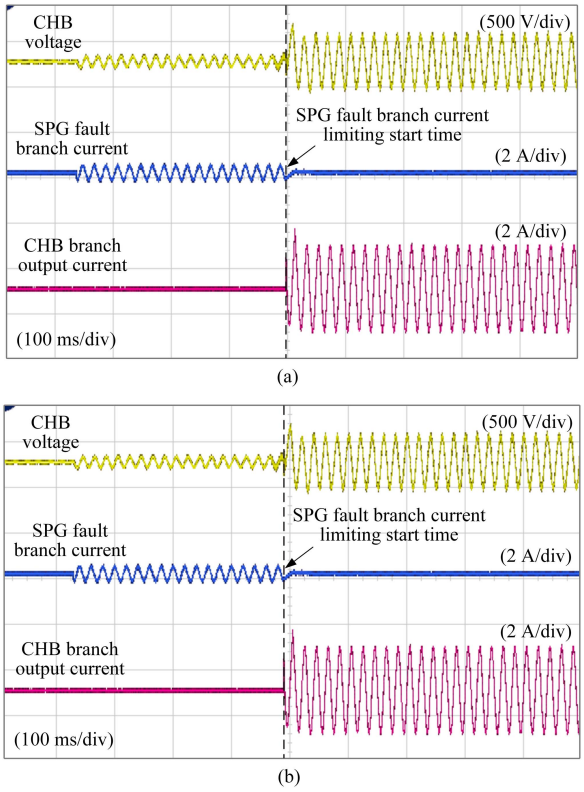

Fig. 21. Experimental waveforms of SPG fault branch current limiting in the cases of different fault resistances: (a) $R_f = 2000\ \Omega$ and (b) $R_f = 5000\ \Omega$.

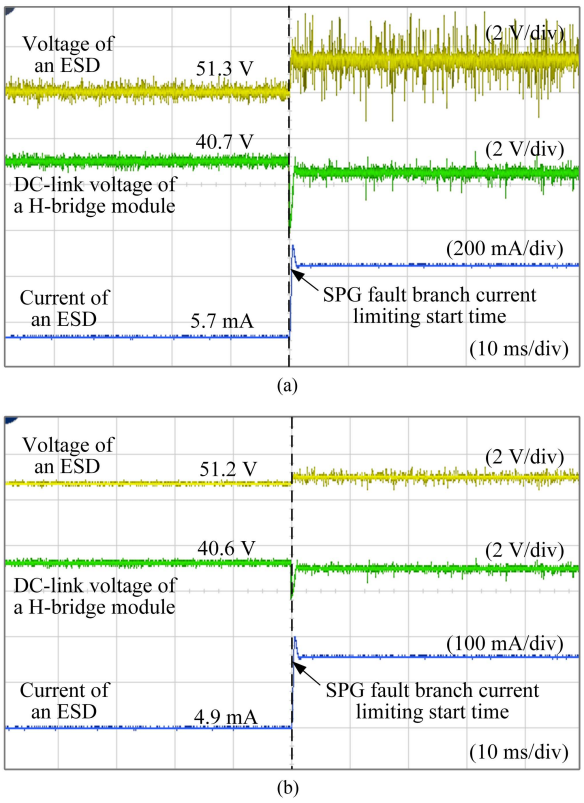

Fig. 22. Experimental waveforms of ESD for storing active power absorbed by CHB under different fault resistances: (a) $R_f = 100\ \Omega$ and (b) $R_f = 500\ \Omega$.

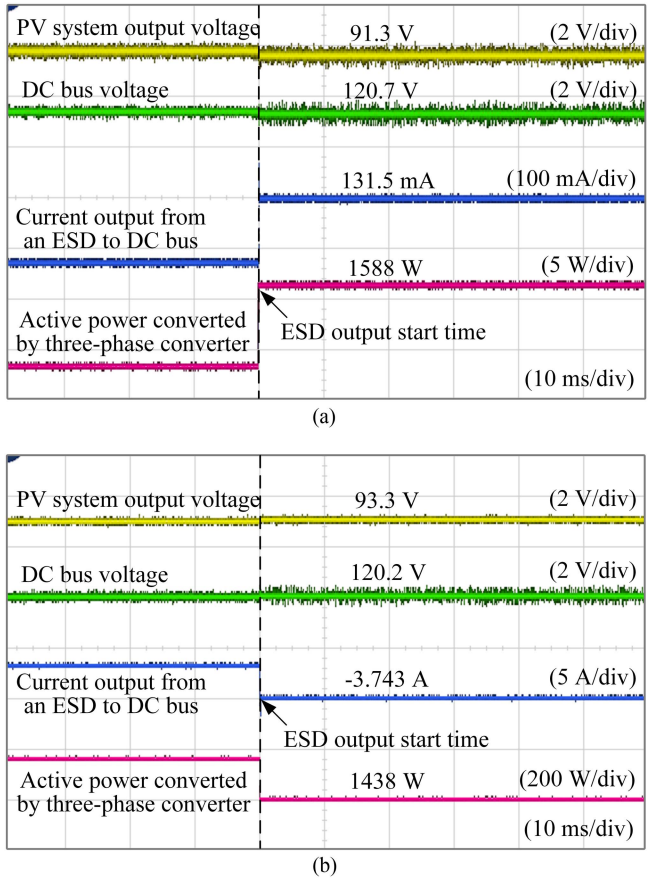

Fig. 23. Experimental waveforms of DC system in different cases. (a) Active power output by PV system is surplus. (b) Active power output by PV system is not enough.

Fig. 23 shows the experimental results of the dc system, including the PV system output voltage, the dc bus voltage, the current output from an ESD to the dc bus, and the active power converted by three-phase converter. The PV system is close to the maximum output point. According to Fig. 23(a), if the active power generated by the PV system is insufficient, the ESD provides active power to support the dc bus voltage at 120 V, accordingly, the energy absorbed by the CHB during the SPG fault branch current limiting is routed back to the distribution networks via the three-phase converter for reuse. On the contrary, when the active power generated by the PV system is surplus, the ESD stores the residual active power to maintain the dc bus voltage, as shown in Fig. 23(b).

VI. Conclusion

To improve the self-healing and self-recovery capabilities of MV active distribution networks from SPG fault and avoid the potential negative impacts of SPG fault, this article has analyzed the characteristics of SPG fault current caused by the zero-sequence current in the impedance induced between the MV distribution networks and ground, and has summarized that the active power loss from the SPG fault caused by the

SPG fault current is different in the case of different fault resistances and the variation follows a certain pattern. Considering the tendency of active distribution networks to develop toward hybrid ac–dc systems constructed by large amount of power electronics, combined with the analysis of zero-sequence circuit in MV distribution networks, it is proposed to control the power electronic involved in the construction of hybrid ac–dc system to transfer the flow path of the zero-sequence current in the impedance induced between the MV distribution networks and ground from the SPG fault branch to the power electronic branch for limiting the SPG fault branch current. During this period, the power electronic connected between the faulty phase and ground in the same way as the SPG fault branch will carry the zero-sequence current instead of the SPG fault branch. The vectors analysis shows that the power electronic will therefore absorb active power from the MV distribution networks in the same way as an SPG fault. The coordinated control for the power electronic cluster is designed to route the absorbed energy back to the hybrid ac–dc system. Based on the simulations and experiments, this proposal can avoid the energy loss from the SPG fault branch. This helps to suppress the fault arc due to the combustion conditions not being met, and provides engineers with the safe conditions to clear faulty elements from the SPG fault branch, without power outage to loads.

REFERENCES

[1] M. Kouki, B. Marinescu, and F. Xavier, "Exhaustive modal analysis of large-scale interconnected power systems with high power electronics penetration," *IEEE Trans. Power Syst.*, vol. 35, no. 4, pp. 2759–2768, Jul. 2020.

[2] K. E. Antoniadou-Plytaria, I. N. Kouveliotis-Lysikatos, P. S. Georgilakis, and N. D. Hatziargyriou, "Distributed and decentralized voltage control of smart distribution networks: Models, methods, and future research," *IEEE Trans. Smart Grid*, vol. 8, no. 6, pp. 2999–3008, Nov. 2017.

[3] M.-F. Guo, X.-D. Zeng, D.-Y. Chen, and N.-C. Yang, "Deep-learning-based earth fault detection using continuous wavelet transform and convolutional neural network in resonant grounding distribution systems," *IEEE Sensors J.*, vol. 18, no. 3, pp. 1291–1300, Feb. 2018.

[4] S.-J. Huang and H.-H. Wan, "A method to enhance ground-fault computation," *IEEE Trans. Power Syst.*, vol. 25, no. 2, pp. 1190–1191, May 2010.

[5] Z.-Y. Zheng, M.-F. Guo, T. Jin, and J.-H. Liu, "A novel method of insulation parameters measurement based on hybrid flexible arc suppression device in distribution networks," *Int. J. Elect. Power Energy Syst.*, vol. 130, Sep. 2021, Art. no. 106982.

[6] I. Colak, R. Bayindir, and S. Sagiroglu, "The effects of the smart grid system on the national grids," in *Proc. 8th Int. Conf Smart Grid*, 2020, pp. 122–126.

[7] X. Fang, S. Misra, G. Xue, and D. Yang, "Smart grid—The new and improved power grid: A survey," *IEEE Commun. Surv. Tut.*, vol. 14, no. 4, pp. 944–980, Oct./Dec. 2012.

[8] D. Paul, "Phase-ground fault current analysis and protection of a high-resistance grounded power system," *IEEE Trans. Ind. Appl.*, vol. 56, no. 4, pp. 3306–3314, Jul./Aug. 2020.

[9] Y.-L. Liang, K.-J. Li, Z. Ma, and W.-J. Lee, "Typical fault cause recognition of single-phase-to-ground fault for overhead lines in nonsolidly earthed distribution networks," *IEEE Trans. Ind. Appl.*, vol. 56, no. 6, pp. 6298–6306, Nov./Dec. 2020.

[10] M. Mitolo, P. E. Sutherland, and R. Natarajan, "Effects of high fault currents on ground grid design," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1118–1124, May/Jun. 2010.

[11] E. Pons, P. Colella, R. Napoli, and R. Tommasini, "Impact of MV ground fault current distribution on global earthing systems," *IEEE Trans. Ind. Appl.*, vol. 51, no. 6, pp. 4961–4968, Nov./Dec. 2015.

[12] A. Cerretti, F. M. Gatta, A. Geri, S. Lauria, M. Maccioni, and G. Valtorta, "Ground fault temporary overvoltages in MV networks: Evaluation and experimental tests," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1592–1600, Jul. 2012.

[13] J. L. P. Pinto de Sa and M. Louro, "On human life risk-assessment and sensitive ground fault protection in MV distribution networks," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2319–2327, Oct. 2010.

[14] B. Shen, Y. Chen, C. Li, S. Wang, and X. Chen, "Superconducting fault current limiter (SFCL): Experiment and the simulation from finite-element method (FEM) to power/energy system software," *Energy*, vol. 234, Nov. 2021, Art. no. 121251.

[15] X. Chen et al., "Superconducting fault current limiter (SFCL) for a power electronic circuit: Experiment and numerical modelling," *Supercond. Sci. Technol.*, vol. 35, no. 4, Apr. 2022, Art. no. 045010.

[16] H. Lyu et al., "An improved hybrid DC circuit breaker with self-adaptive fault current limiting capability," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4730–4741, Apr. 2022.

[17] S. Zhang, G. Zou, X. Wei, and C. Zhang, "Bridge-type multiport fault current limiter for applications in MTDC grids," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 6960–6972, Jul. 2022.

[18] X. Li et al., "HVdc reactor reduction method based on virtual reactor fault current limiting control of MMC," *IEEE Trans. Ind. Electron.*, vol. 67, no. 12, pp. 9991–10000, Dec. 2020.

[19] F. Zheng, J. Zhang, J. Lin, C. Deng, and J. Huang, "A novel flexible fault current limiter for DC distribution applications," *IEEE Trans. Smart Grid*, vol. 13, no. 2, pp. 1049–1060, Mar. 2022.

[20] K. Yu, S. Liu, X. Zeng, H. Peng, F. Liu, and Z. Wang, "A novel insulation parameter online measuring technique based on two voltage transformers for distribution networks," *IEEE Trans. Power Del.*, vol. 36, no. 6, pp. 3383–3392, Dec. 2021.

[21] K. Liu et al., "Flexible grounding system for single-phase to ground faults in distribution networks: A systematic review of developments," *IEEE Trans. Power Del.*, vol. 37, no. 3, pp. 1640–1649, Jun. 2022.

[22] B. Fan et al., "Principle and control design of a novel hybrid arc suppression device in distribution networks," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 41–51, Jan. 2022.

[23] P. Wang, B. Chen, C. Tian, B. Sun, M. Zhou, and J. Yuan, "A novel neutral electromagnetic hybrid flexible grounding method in distribution networks," *IEEE Trans. Power Del.*, vol. 32, no. 3, pp. 1350–1358, Jun. 2017.

[24] M.-F. Guo, W.-Q. Cai, Z.-Y. Zheng, and H. Wang, "Fault phase selection method based on single-phase flexible arc suppression device for asymmetric distribution networks," *IEEE Trans. Power Del.*, vol. 37, no. 6, pp. 4548–4558, Dec. 2022.

[25] W. Wang, X. Zeng, L. Yan, X. Xu, and J. M. Guerrero, "Principle and control design of active ground-fault arc suppression device for full compensation of ground current," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4561–4570, Jun. 2017.

[26] Y. Hou et al., "Adaptive active voltage-type arc suppression strategy considering the influence of line parameters in active distribution network," *IEEE Trans. Ind. Electron.*, vol. 70, no. 5, pp. 4799–4808, May 2023.

[27] Z. Huang et al., "A non-neutral alternate arc suppression method for single phase grounding fault in active distribution network," *Int. J. Elect. Power Energy Syst.*, vol. 152, May 2023, Art. no. 109182.

[28] H. Chen, J. Yuan, H. Zhou, S. Xu, C. Zou, and F. Chen, "A novel fast energy storage fault current limiter topology for high-voltage direct current transmission system," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5032–5046, May 2022.

[29] H. Chen, J. Yuan, F. Chen, and Z. Zhang, "A new type of fast-response fault current limiter topology for HVDC application," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 11576–11586, Nov. 2021.

[30] H. Chen, J. Yuan, S. Xu, C. Zou, and Y. Hong, "Research on a secondary active limiting DC fault current limiter topology," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14547–14561, Dec. 2022.

[31] M. Kim and M. Youn, "An energy feedback control of series resonant converter," *IEEE Trans. Power Electron.*, vol. 6, no. 3, pp. 338–345, Jul. 1991.

[32] W. Liu, J. Zhang, H. Wang, T. Wu, Y. Lou, and X. Ye, "Modified AC/DC unified power flow and energy-saving evaluation for urban rail power supply system with energy feedback systems," *IEEE Trans. Veh. Technol.*, vol. 70, no. 10, pp. 9898–9909, Oct. 2021.

[33] A.-L. Allègre, A. Bouscayrol, P. Delarue, P. Barrade, E. Chattot, and S. El-Fassi, "Energy storage system with supercapacitor for an innovative subway," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4001–4012, Dec. 2010.

[34] B. Liu, Y. Peng, J. Xu, C. Mao, D. Wang, and Q. Duan, "Design and implementation of multiport energy routers toward future energy internet," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 1945–1957, May/Jun. 2021.

[35] X. Zhao et al., "Multimode operation mechanism analysis and power flow flexible control of a new type of electric energy router for low-voltage distribution network," *IEEE Trans. Smart Grid*, vol. 13, no. 5, pp. 3594–3606, Sep. 2022.

[36] S. Ouyang, J. Liu, Y. Yang, X. Chen, S. Song, and H. Wu, "DC voltage control strategy of three-terminal medium-voltage power electronic transformer-based soft normally open points," *IEEE Trans. Ind. Electron.*, vol. 67, no. 5, pp. 3684–3695, May 2020.
[37] J. Zhang et al., "A modular multilevel converter station with multiple MVac ports," *IEEE Trans. Ind. Electron.*, vol. 70, no. 9, pp. 8655–8665, Sep. 2023.
[38] A. Rodríguez-Cabero, J. Roldán-Pérez, M. Prodanovic, J. A. Suul, and S. D'Arco, "Coupling of AC grids via VSC-HVDC interconnections for oscillation damping based on differential and common power control," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6548–6558, Jun. 2020.
[39] J. Zhang, Y. Zhang, J. Zhou, J. Wang, G. Shi, and X. Cai, "Control of a hybrid modular solid-state transformer for uninterrupted power supply under MVdc short-circuit fault," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 76–87, Jan. 2023.
[40] L. Chen et al., "Study on resistive SFCL for fault ride-through fulfillment of power electronic transformer interconnecting MV and LV power systems," *IEEE Trans. Appl. Supercond.*, vol. 31, no. 8, Nov. 2021, Art. no. 5402106.
[41] Y. Li, X. Pei, M. Yang, X. Lin, and Z. Li, "An advanced fault control of transformerless modular multilevel converters in AC/DC hybrid distribution networks under the single-phase grounding fault," *IEEE Trans. Power Del.*, vol. 36, no. 2, pp. 932–942, Apr. 2021.
[42] Y. Xia, W. Wei, M. Yu, X. Wang, and Y. Peng, "Power management for a hybrid AC/DC microgrid with multiple subgrids," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3520–3533, Apr. 2018.
[43] D. D. Atkar, P. Chaturvedi, H. M. Suryawanshi, P. P. Nachankar, and D. Yadeo, "Optimal design of solid state transformer-based interlink converter for hybrid AC/DC micro-grid applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 4, pp. 3685–3696, Aug. 2022.

Bin-Long Zhang (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from the Fuzhou University, Fujian, China, in 2020. He is currently working toward the Ph.D. degree in electrical engineering with the Fuzhou University.

His research interests include the protection and control of power system with a high penetration of renewable energy resources with power electronics.

Mou-Fa Guo (Member, IEEE) was born in Fujian province, China, in 1973. He received the B.S. and M.S. degrees in electrical engineering from the Fuzhou University, Fuzhou, China, in 1996 and 1999, respectively, and the Ph.D. degree in electrical engineering from the Yuan Ze University, Taoyuan, Taiwan, in 2018.

Since 2000, he has been with the Fuzhou University, where he is currently a Professor with the College of Electrical Engineering and Automation. His research interests include the information processing, protection control, and flexible arc suppression of single-line-to-ground fault in distribution networks.

Ze-Yin Zheng (Member, IEEE) received the B.S. degree in electrical engineering from the Fuzhou University, Fuzhou, China, in 2014, and the Ph.D. degree in electrical engineering from the Fuzhou University and the Yuan Ze University, Taoyuan, Taiwan, in 2021.

He is currently an Associate Professor with the Fuzhou University, Fuzhou, China. His research interests include power distribution system automation, flexible active arc suppression of singe-phase ground fault, protection, and control of distribution systems.

Qiteng Hong (Senior Member, IEEE) received the B.Eng. (Hons.) and Ph.D. degrees in electronic and electrical engineering from the University of Strathclyde, Glasgow, U.K., in 2011 and 2015, respectively.

He is currently a Senior Lecturer (Associate Professor) with the University of Strathclyde, Glasgow, U.K. His research interests include power system protection and control in future networks with high penetration of renewables.

Dr. Hong is a member of IEEE Working Group P2004 and IEEE Task force on Cloud-Based Control and Co-Simulation of Multi-Party Resources in Energy Internet, and he also was a Regular Member of the completed CIGRE WG B5.50.