Decoupled Modeling and Wide-Range Power Distribution Strategy for the Multisource Inverter in Microgrids

Lijie Liu, Dehong Zhou, *Senior Member, IEEE*, Jianxiao Zou, *Member, IEEE*, and Weijun Wang

***Abstract*—Multisource inverter (MSI) provides a low-cost and high-power-density solution for microgrids (MGs) applications due to the removal of the dc/dc converter, which offers direct power flow between the dc-side and the ac-side. The existing modulation strategies for the MSI transplanted from those of multilevel inverters experience a limited power distribution range due to the finite control freedom of degree provided by redundant vectors. Moreover, the power distribution between the dc ports is highly coupled with the vector synthesis, this is especially true when the voltages of the dc port are unbalanced. To address the aforementioned issue, this article proposes a decoupled modeling method and a wide-range power distribution strategy for the MSI. The decoupled model is proposed to simplify the modulation implementation process and power distribution analysis. In the proposed model, the reference voltage vector of the MSI is proportionally decomposed into two decoupled parts, which can be generated independently. As a result, it can not only avoid complex modulation calculations but also ensure decoupled power distribution. Moreover, detailed theoretical analysis indicates that the proposed solution can offer an expanded power distribution range by increasing the switching actions in one switching cycle. Finally, the effectiveness of the porposed power distribution strategy is verified by islanded MGs experimental tests.**

***Index Terms*—Decoupled modeling, hybrid energy systems, multisource inverter (MSI), multiple-carrier modulation, power distribution.**

NOMENCLATURE

V_H, V_L	DC voltages of high-voltage and low-voltage ports.
V_1, V_2	DC voltages of upper and lower dc-side capacitors.
i_H, i_L	Output currents of high-voltage and low-voltage ports.
$S_{x1}, \ldots, S_{x4}$	Switching states in phase x.
D_{xu}, D_{xl}	Duty cycles of S_{x1} and S_{x2}.
$V_{\text{out}x}$	Output voltage vector in phase x.
V_{Uy}, V_{Ly}	Output voltage vectors of modeled upper and lower inverters.
$V_{g\text{ref}}, f_{g\text{ref}}$	Rated grid voltage and current.
$V_{\text{ref}}, I_{\text{ref}}$	Reference voltage and current vectors.
P_1, P_2	Output power of high-voltage and low-voltage ports.
$P_{1\text{ref}}$	Reference power of high-voltage ports.
P_U, P_L	Output power of modeled upper and lower inverters.
P, Q	Active power and reactive power of ac-side.
$P_{\text{ref}}, Q_{\text{ref}}$	Reference active power and reactive power of the ac side.
ξ	Proportionality factor of reference voltage vector decomposition.
$\xi_{\min}, \xi_{\max}$	Minimum and maximum value of ξ.
K_P, K_I	Proportional-integral (PI) controller parameters in the power control loop.
T_{Uz}, T_{Lz}	Dwell time in modeled upper and lower inverters.
d_{xu}, d_{xl}	Duty cycles in modeled upper and lower inverters.
d_{ou}, d_{ol}	Zero-sequence injections in modeled upper and lower inverters.
$d_{u\min}, d_{l\max}$	Minimum of and d_{xu} and maximum value of d_{xl}.
d'_{xl}, d'_{xl}	Modified duty cycles in modeled upper and lower inverters.
η_1, η_2	Output power ratio of high-voltage and low-voltage ports.
P_{total}	Total output power of two dc ports.
η_s	System efficiency.

Manuscript received 20 December 2022; revised 11 May 2023; accepted 6 June 2023. Date of publication 12 June 2023; date of current version 1 September 2023. This work was supported in part by the National Natural Science Foundation of China under Grant 62173067, in part by the Natural Science Foundation of Sichuan Province under Grant 2023NSFSC0298, and in part by the Shenzhen Science and Technology Program under Grant JCYJ20220530165001003. Recommended for publication by Associate Editor D. Mahinda. *(Corresponding author: Dehong Zhou.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3285008.

Digital Object Identifier 10.1109/TPEL.2023.3285008

I. INTRODUCTION

RENEWABLE energy sources (RESs) such as wind and photovoltaic (PV) play significant roles in tackling the fossil energy source shortage and environmental pollution challenges [1], [2]. However, high penetration of RESs is more likely to cause power/frequency fluctuations, voltage deviations, and

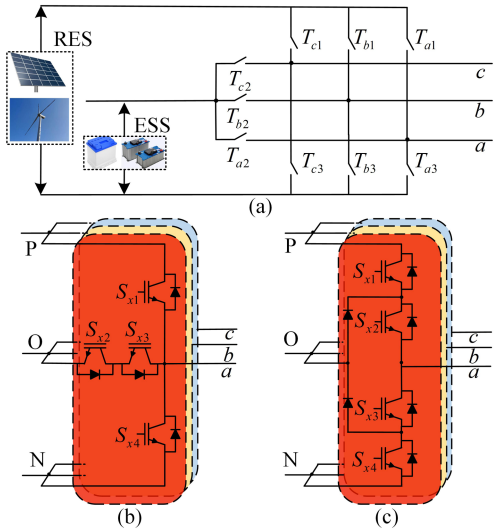

Fig. 1. Configurations of the MSI. (a) Concept with ideal switches. (b) T-NPC type. (c) I-NPC type.

even system instability in microgrids (MGs) applications [3]. To tackle the aforementioned challenges, an attractive solution is called energy storage technology, which can absorb or release energy on demand [4]. An energy storage system (ESS) contributes to the integration of RESs into the MGs by power quality improvement and smoothing power fluctuations. Multisource systems composed of the RES and ESS can meet the ac MGs/load demand with high reliability and at moderate costs [5]. Hence, multisource systems have gained considerable attention in recent years [6], such as PV-battery hybrid systems [7], [8].

The multisource inverter (MSI) is a promising solution for the integration of RES and ESS in MGs applications, which directly transfers power from RES/ESS to the ac-side without any dc/dc converters or magnetic elements [9], [10], [11], [12]. Fig. 1(a) shows its concept with ideal switches. The motivation of the MSI is to improve the system efficiency and power density [13]. As shown in Fig. 1(a), MSI offers one-stage power conversion from RES/ESS to the ac-side. The RES dc port is unidirectional, such as PV generation is adopted. And the ESS dc port is bidirectional, for instance, the battery should be charged/discharged to compensate for the system power difference. In Fig. 1(a), the MSI topology essentially is a variant of a three-level inverter. The three-level inverter is an attractive solution used as the MSI due to it offering low voltage/current stresses and high power quality. The topology of the MSI can be constructed from the conventional three-level neutral-point-clamped (NPC) inverter by adding a dc port. Fig. 1(b) and (c) give the T-NPC type and I-NPC type implementations of the MSI. The T-NPC circuit is utilized to connect different level dc voltages in [14] and [15]. And the I-NPC circuit is adopted to integrate two dc sources in [16].

Though outstanding advantages could be achieved by the MSI, it is challenging to design a modulation for the MSI due to the unbalanced port voltage feature. Unbalanced port voltages are caused by intermittent RES generation and variable state of charge (SOC) in the ESS. As a result, output voltage vectors of MSI distribute asymmetrically. Therefore, the conventional modulation strategies for a three-level converter could not be adopted in the MSI. Numerous advanced modulation strategies have been investigated for three-level converters with unbalanced port voltages. A simplified pulsewidth modulation (PWM) strategy for a three-level converter with unbalanced dc-link was proposed to achieve high-quality output voltages and maximize the linear modulation range [17]. A two-stage modulation strategy is proposed to produce the undistorted current even in the presence of unevenly distributed space vectors [18]. To suppress output harmonics and maximize the linear modulation region, as well as to reduce switching losses, an analytical discontinuous space vector PWM is proposed for three-level inverters with unbalanced dc links [19]. To reduce the common-mode voltage and obtain high-quality output current, a carrier-based modulation is proposed for a three-level converter with unbalanced neutral-point voltage conditions [20]. A hybrid PWM strategy composed of carried-based PWM and discontinuous PWM is proposed to generate high-quality ac voltages [21]. A carrier-based PWM strategy is proposed to improve the power conversion efficiency [22]. Although the aforementioned modulation strategies are effective under unbalanced port voltages and have achieved a beneficial system performance, they could not be directly transplanted to the MSI because the major modulation target for the MSI is to achieve flexible power control under unbalanced port voltages.

To realize the flexible power flow in the MSI, the dc-port power should be decoupled to meet the demand of RES/ESS, e.g., maximum power point tracking for PV modules. In addition, an expanded power distribution range is required so that more RES generated energy can be harvested. Some previous studies have made useful explorations for decoupled port power control. A unified model predictive control scheme is proposed for the desirable port power management of the multiport inverter [23]. However, the power distribution range is not addressed. A general control scheme is proposed for realizing independent port power tracking of the dual-input three-level inverter [24]. This method enhances the power distribution range effectively but brings the time-consuming control design. The modulation-based power-sharing strategies can regulate port power effectively and show clear physical meaning [25], [26], [27], [28], [29], [30]. Power sharing between two dc ports can be regulated by altering the small vectors in [25] and [26]. Unfortunately, the power-sharing capacity is not discussed in [25] and [26]. Decoupling port power distribution has been achieved by regulating the dwell time of positive/negative small vectors in [27] and [28] and zero vector in [29] and [30]. Moreover, the detailed power distribution range is given in [27], [28], [29], and [30]. However, the power distribution range is limited due to the freedom of degree provided by the redundant small/zero vector being finite in the modulation process. This calls for a wide-range power distribution strategy for the MSI to increase the energy harvested by RES and stored by the ESS.

To obtain flexible power control under unbalanced port voltages, this article proposes a decoupled model, in which the reference voltage vector is proportionally decomposed into two

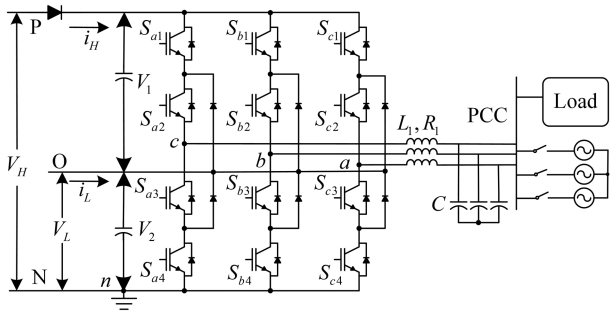

Fig. 2. Topology of the MSI with I-NPC-based circuit.

TABLE I
SWITCHING STATES AND OUTPUT VOLTAGES IN EACH PHASE

Switching state S_x	$S_{x1}S_{x2}S_{x3}S_{x4}$	Output voltage
P	1100	V_H
O	0110	V_L
N	0011	0

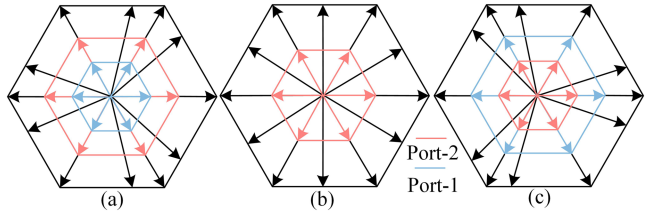

Fig. 3. Output voltage vectors of the MSI: (a) $V_2 > V_1$, (b) $V_2 = V_1$, and (c) $V_2 < V_1$.

independent parts. With the proposed modeling method, the MSI is modeled as two two-level inverters to generate the decomposed voltage. As a result, not only complex modulation problems caused by unbalanced dc-link can be avoided, but also independent port power control can be achieved. On top of that, a multiple-carrier modulation is proposed for the equivalent models to output the decomposed voltage. By increasing the switching actions in one switching cycle, the power distribution range is expanded. The effectiveness of the proposed solution is verified by detailed theoretical analysis and islanded MGs experimental tests.

The rest of this article is organized as follows. The MSI and proposed modeling method are illustrated in Section II. Section III provides the proposed multiple-carrier modulation and power distribution strategy. Power distribution analysis is given in Section IV. The experimental tests are conducted in Section V. Finally, Section VI concludes this article.

II. MSI AND PROPOSED MODELING METHOD

This section first introduces the topology and operation modes of the MSI. Then, a decoupled modeling method for the MSI is proposed.

A. Topology and Operation Modes of the MSI

The topology of the MSI with the I-NPC-based circuit is shown in Fig. 2. In this study, the I-NPC-type MSI is selected and adopted for MGs applications. The MSI connects to ac MGs with an *LC* filter. The voltages of two dc inputs are V_H and V_L. The dc port connected between P and N is defined as high-voltage port-1, and another dc port connected between O and N is defined as low-voltage port-2. In general, the dc-port voltages are unbalanced due to unpredictable RES generation and variable SOC of ESS. Then, the dc-side capacitor voltages can be calculated as $V_1 = V_H - V_L$ and $V_2 = V_L$. And the output currents of high-voltage port-1 and low-voltage port-2 are i_H and i_L.

To describe the operating principle of the MSI clearly, Table I gives the switching states and output voltages in each phase. The switching state in each phase S_x =P, O, N ($x = a, b, c$) is determined by the combinations of switching function $S_{x1}S_{x2}S_{x3}S_{x4}$ (1 means closed and 0 means open). Output voltages corresponding to the three switching states are V_H, V_L, and 0, respectively. Fig. 3 shows output voltage vectors of the MSI: (a) $V_2 > V_1$, (b) $V_2 = V_1$, and (c) $V_2 < V_1$. Output voltage vectors of the MSI are distributed unevenly due to the unbalanced port voltages.

In this study, the high-voltage port-1 is connected to a unidirectional dc-source, such as PV. While the low-voltage port-2 is connected to a bidirectional dc-source, such as battery ESS. Therefore, the following three operation modes of the MSI are considered.

1) Mode I: Only high-voltage port-1 supports the ac-side.
2) Mode II: High-voltage port-1 and low-voltage port-2 support the ac-side together.
3) Mode III: High-voltage port-1 not only supports the ac-side but also charges to low-voltage port-2.

In summary, the MSI has two system problems, i.e., unevenly distributed voltage vectors caused by unbalanced port voltages and coupled port power caused by complex operation modes. The modulation strategy of the conventional 3L-NPC could not be transplanted to the MSI directly. Hence, an effective strategy is required to solve the aforementioned problems simultaneously.

B. Decoupled Modeling Method for the MSI

To achieve flexible port power control under unbalanced port voltages, the decoupled modeling for the MSI is proposed in Fig. 4. The modeling principle is given as follows. To simplify the analysis, the duty cycles for S_{x1} and S_{x2} are defined as D_{xu} and D_{xl} ($x = a, b, c$). Then, the output voltage vector of the MSI can be expressed as follows:

$$V_{\text{out}x} = D_{xu}V_H + (D_{xl} - D_{xu})V_L \tag{1}$$

where $V_{\text{out}x}$ is the output voltage vector in phase x. Moreover, (1) can be rewritten as follows:

$$\begin{aligned} V_{\text{out}x} &= D_{xu}(V_H - V_L) + D_{xl}V_L \\ &= D_{xu}V_1 + D_{xl}V_2. \end{aligned} \tag{2}$$

It can be concluded that the output voltage vector of the MSI can be generated by two inverters with dc-link voltages V_1 and V_2.

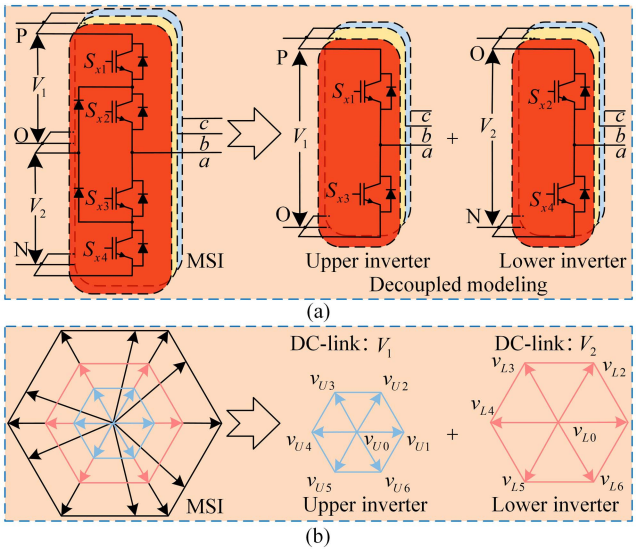

Fig. 4. Decoupled modeling method for the MSI. (a) Equivalent circuit of modeled inverters. (b) Space vector diagram of modeled inverters.

TABLE II
EQUIVALENT OUTPUT VOLTAGE VECTORS OF THE LOWER/UPPER INVERTER AND RESPONDING SWITCHING STATES OF THE MSI

V_L	Switching state	V_U	Switching state
V_{L1}	ONN	V_{U1}	POO
V_{L2}	OON	V_{U2}	PPO
V_{L3}	NON	V_{U3}	OPO
V_{L4}	NOO	V_{U4}	OPP
V_{L5}	NNO	V_{U5}	OOP
V_{L6}	ONO	V_{U6}	POP

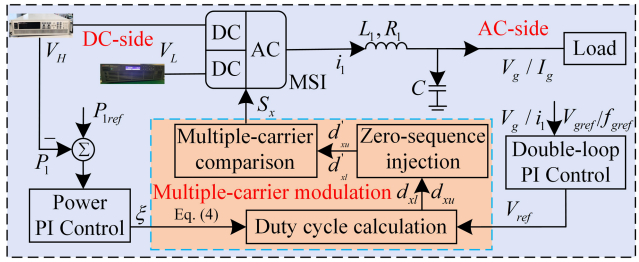

Fig. 5. Multiple-carrier modulation-based power distribution strategy.

Hence, the MSI is decoupled into the upper and lower inverters in this study.

Modeling the three-level converter into the two-level one is an existing method, which is effective to reduce the computational burden. A three-level converter has conversed into a two-level one through the coordinate transformation in [31] and [32]. Based on the vector-shifted method, the three-level NPC can be simplified as a two-level converter in [33]. However, the proposed decoupled method is essentially different from the existing methods in [31], [32], and [33]. The existing methods are based on the mathematical transformation [31], [32], [33]. On the contrary, the proposed method shows clearly physical meaning. As shown in Fig. 4, The dc sources of the MSI can be considered as two independent ones with voltages V_1 and V_2. By separating the two virtual dc sources, the MSI is modeled as two independent two-level inverters, i.e., the upper inverter and the lower inverter. Fig. 4(a) shows the equivalent circuit of modeled inverters. The dc-link voltages of the upper and lower inverters are V_1 and V_2, respectively. Considering that V_1 only supports the ac-side in the case of $S_{x1} = 1$, while V_2 only supports the ac-side in the case of $S_{x2} = 1$, the equivalent switching tubes for the upper inverter and lower inverter are selected as S_{x1}/S_{x3} and S_{x2}/S_{x4}. Hence, the output switching states of the upper and lower inverters can be regarded as N/O and O/P. Fig. 4(b) gives the space vector diagram of modeled inverters, where V_{Uy} and V_{Ly} $(y = 0, 1, 2, 3, 4, 5, 6)$ are the equivalent output voltage vectors of the upper/lower inverter, respectively. The equivalent output voltage vectors of the lower/upper inverter and responding switching states of the MSI are shown in Table II.

Based on the proposed modeling method, the reference voltage vector is decomposed into two parts, which can be generated by the upper/lower inverter. Then, compared to conventional modulation calculation in the three-level converter frame, the number of switching states is reduced from 27 to 16. Moreover, complicated triangle-function calculation under unbalanced port voltages is avoided as the synthesis of reference voltage vector can be conducted in the two-level converer frame. Hence, the complexity of the modulation strategy is greatly reduced with this modeling method. In addition, decoupled port power can be obtained by decomposing the reference voltage vectors. Detailed reference voltage vector distribution and responding port power analysis would be discussed in Section III.

III. PROPOSED MULTIPLE-CARRIER MODULATION-BASED POWER DISTRIBUTION STRATEGY

The multiple-carrier modulation-based power distribution strategy is shown in Fig. 5. The MSI is operated in an islanded MG mode. In this study, the double-loop proportional-integral (PI) control is adopted to track rated grid voltage/frequency $V_{g\text{ref}}/f_{g\text{ref}}$ and generate reference voltage vector V_{ref}. The double-PI control is composed of the voltage control loop and current control loop. And this method has been widely adopted in MGs applications, the detailed block diagram can be found in [34]. On the dc-side, a power PI control is utilized to track port-1 reference power $P_{1\text{ref}}$, where $P_{1\text{ref}}$ can be obtained from the MGs power management strategy [35]. The output of the power PI controller is parameter ξ, which plays an important role in reference voltage vector distribution. Then, V_{ref} would be synthesized by the multiple-carrier modulation.

As analyzed in Section II, the modulation design can be simplified by the power-decoupled model. Thus, the multiple-carrier modulation is derived based on the decoupled model. The target of modulation is to achieve flexible power control under unbalanced port voltages. Hence, decoupled port power analysis based on the modeled inverters is first proposed. Then, multiple-carrier modulation is proposed for the modeled inverters thanks to its natural advantages, i.e., generating the decomposed voltage vector independently. The proposed modulation includes the following parts: duty cycle calculation for the upper/lower inverter in the two-level converter frame, zero-sequence injection

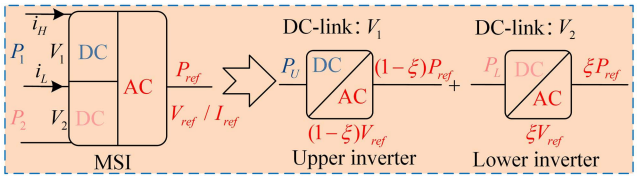

Fig. 6. Results of reference voltage vector distribution and responding active power.

for modifying the duty cycle, and multiple-carrier comparison for switching states generation. The detailed implementation process of each part is shown in the following text.

A. Decoupled Port Power Analysis Based on Modeled Inverters

Fig. 6 gives the results of reference voltage vector distribution and responding active power. For the unit power factor condition, the voltage reference V_{ref} is always synchronous with the current reference I_{ref}. To ensure the reactive power remains zero, the voltage reference V_{ref} is proportionally distributed to the upper and lower inverters. The reference voltage of the lower inverter is set as ξV_{ref}, and the reference voltage of the upper inverter is set as $(1-\xi)V_{\text{ref}}$, where ξ is the proportionality factor. To avoid the overmodulation problem of the upper/lower inverter, ξ should satisfy the following equation:

$$\begin{cases}(1-\xi)V_{\text{ref}} \le \frac{V_1}{\sqrt{3}} \\ \xi V_{\text{ref}} \le \frac{V_2}{\sqrt{3}}.\end{cases} \tag{3}$$

Then, the domain of ξ can be obtained as follows:

$$\xi_{\min} \le \xi \le \xi_{\max} \tag{4}$$

where

$$\begin{cases}\xi_{\min} = 1 - \frac{V_1}{\sqrt{3}V_{\text{ref}}} \\ \xi_{\max} = \frac{V_2}{\sqrt{3}V_{\text{ref}}}.\end{cases} \tag{5}$$

Reference vectors V_{ref} can be generated by superimposing $(1-\xi)V_{\text{ref}}$ and ξV_{ref} of the upper and lower inverter.

Fig. 6 also gives the active power distribution of the MSI, upper inverter, and lower inverter. In this study, the reactive power remains zero. Hence, only the active power has been further analyzed. After some simplifications, the ac-side active power of the MSI can be calculated as

$$P_{ref} = 1.5(V_{\text{ref}\alpha}I_{\text{ref}\alpha} + V_{\text{ref}\beta}I_{\text{ref}\beta}) \tag{6}$$

where P_{ref} is the reference ac-side active power, $V_{\text{ref}\alpha}/I_{\text{ref}\alpha}$ and $V_{\text{ref}\beta}/I_{\text{ref}\beta}$ are the real and imaginary parts of the reference voltage/current vector. The active power equation of the MSI can be expressed as

$$P_1 + P_2 = P_{\text{ref}} \tag{7}$$

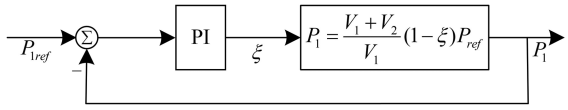

Fig. 7. Block diagram of the power control loop.

where P_1/P_2 is the dc-side high-/low-voltage port active power. P_1/P_2 can be calculated as

$$\begin{cases}P_1 = (V_1+V_2)i_H = (V_1+V_2)\sum\limits_{x=a,b,c}(D_{xu}i_x) \\ P_2 = V_2 i_L = V_2\sum\limits_{x=a,b,c}[(D_{xl}-D_{xu})i_x]\end{cases} \tag{8}$$

where $i_x(x=a,b,c)$ is the ac-side current. Due to the equivalent switching tubes for the upper inverter and lower inverter being considered as S_{x1}/S_{x3} and S_{x2}/S_{x4}, the active power of the upper/lower inverter P_U/P_L can be represented as

$$\begin{cases}P_U = V_1\sum\limits_{x=a,b,c}(D_{xu}i_x) \\ P_L = V_2\sum\limits_{x=a,b,c}(D_{xl}i_x).\end{cases} \tag{9}$$

Then, relationship between P_1/P_2 and P_U/P_L can be derived from (8) and (9) as

$$\begin{cases}P_1 = \frac{V_1+V_2}{V_1}P_U \\ P_2 = -\frac{V_2}{V_1}P_U + P_L.\end{cases} \tag{10}$$

Due to the MSI and upper/lower inverter sharing the same current I_{ref}, it can be concluded from (6) that the active power of the upper/lower inverter is proportional to the voltage vector, i.e., P_U/P_L is determined by ξ as

$$\begin{cases}P_U = (1-\xi)P_{\text{ref}} \\ P_L = \xi P_{\text{ref}}.\end{cases} \tag{11}$$

Therefore, flexible power control of P_U/P_L can be achieved by regulating ξ. Based (10) and (11), decoupled dc-port power P_1 and P_2 can be realized by designing ξ. And vice versa, the proportionality factor ξ can be obtained by controlling the dc-port powers P_1 and P_2. In the case of constant grid active power, desired ξ can be obtained by only regulating P_1. The relationship between P_1 and ξ can be expressed as

$$P_1 = \frac{V_1+V_2}{V_1}(1-\xi)P_{\text{ref}}. \tag{12}$$

Hence, a negative feedback control about port power P_1 is adopted to generate the proportionality factor ξ. Fig. 7 gives the block diagram of the power control loop. The closed-loop transfer function can be expressed as

$$\begin{aligned}\Phi(s) &= \frac{P_1(s)}{P_{1\text{ref}}(s)} \\ &= \frac{C_1/P_{1\text{ref}}(s) - C_1 G_{\text{PI}}(s)}{1 - C_1 G_{\text{PI}}(s)}\end{aligned} \tag{13}$$

where $C_1 = \frac{V_1+V_2}{V_1}P_{\text{ref}}$ is a constant, $G_{\text{PI}}(s) = K_P + \frac{K_I}{s}$ is the transfer function of the PI controller. Then, the system pole s_1 can be obtained. To guarantee the stability of the system, $s_1 < 0$

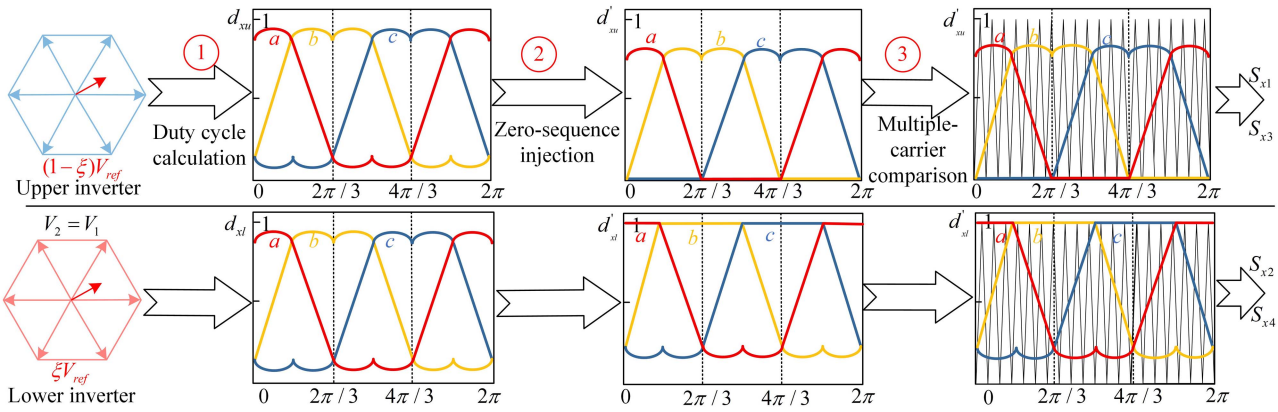

Fig. 8. Multiple-carrier modulation and its implementation process.

should be satisfied. As a result, the following system stability condition can be achieved:

$$K_P > \frac{1}{C_1}. \tag{14}$$

This system stability condition can be adopted as the guideline to design the parameters of the PI controller. According to the aforementioned analysis, the power control system is stable.

B. Duty Cycle Calculation for Upper and Lower Inverters

To generate the decomposed reference voltage vector $(1-\xi)V_{\text{ref}}/\xi V_{\text{ref}}$, Fig. 8 gives the multiple-carrier modulation and its implementation process. The first step is to calculate the duty cycle for upper and lower inverters according to the conventional space vector modulation strategy. For the lower inverter, to synthesize the reference voltage vector ξV_{ref} in sector I, three nearest vectors V_{L0}, V_{L1}, and V_{L2} are selected. The dwell time of each vector can be calculated as

$$\begin{cases} T_s \xi V_{\text{ref}} = T_{L1} V_{L1} + T_{L2} V_{L2} + T_{L0} V_{L0} \\ T_s = T_{L1} + T_{L2} + T_{L0} \end{cases} \tag{15}$$

where T_s is the switching period. And the dwell time $T_{Lz} (z = 0, 1, 2)$ are expressed as

$$\begin{cases} T_{L1} = \frac{\sqrt{3} T_s}{2 V_2} \left(\sqrt{3} \xi V_{\text{ref}\alpha} - \xi V_{\text{ref}\beta} \right) \\ T_{L2} = \frac{\sqrt{3} T_s}{V_2} \xi V_{\text{ref}\beta} \\ T_{L0} = T_s - T_{L1} - T_{L2}. \end{cases} \tag{16}$$

Similarly, dwell time $T_{Uz} (z = 0, 1, 2)$ for the upper inverter can be achieved as follows:

$$\begin{cases} T_{U1} = \frac{\sqrt{3} T_s}{2 V_1} \left[\sqrt{3} (1-\xi) V_{\text{ref}\alpha} - (1-\xi) V_{\text{ref}\beta} \right] \\ T_{U2} = \frac{\sqrt{3} T_s}{V_1} (1-\xi) V_{\text{ref}\beta} \\ T_{U0} = T_s - T_{U1} - T_{U2}. \end{cases} \tag{17}$$

Then, the duty cycle for each phase can be obtained based on the traditional seven-segment PWM strategy

$$\begin{cases} d_{al} = \frac{1}{T_s} (T_{L1} + T_{L2} + \frac{T_{L0}}{2}) \\ d_{bl} = \frac{1}{T_s} (T_{L2} + \frac{T_{L0}}{2}) \\ d_{cl} = \frac{1}{T_s} \frac{T_{L0}}{2} \end{cases} \tag{18}$$

where $d_{xl} (x = a, b, c)$ is duty cycle for the lower inverter. Similarly, $d_{xu} (x = a, b, c)$ for the upper inverter can be achieved as

$$\begin{cases} d_{au} = \frac{1}{T_s} (T_{U1} + T_{U2} + \frac{T_{U0}}{2}) \\ d_{bu} = \frac{1}{T_s} (T_{U2} + \frac{T_{U0}}{2}) \\ d_{cu} = \frac{1}{T_s} \frac{T_{U0}}{2}. \end{cases} \tag{19}$$

C. Zero-Sequence Injection for Modifying Duty Cycle

There are three different switching states of the MSI, i.e., 1100, 0110, and 0011. It can be concluded that $d_{xu} > d_{xl}$ $(x = a, b, c)$ would result in unwanted switching states. To ensure $d_{xu} < d_{xl}$, the zero-sequence injection method is adopted. The injected zero-sequence components for the upper inverter d_{ou} and lower inverter d_{ol} are designed as follows:

$$\begin{cases} d_{ou} = -1 - d_{u\min} \\ d_{ol} = 1 - d_{l\max} \end{cases} \tag{20}$$

where

$$\begin{cases} d_{u\min} = \min \left(d_{au}, d_{bu}, d_{cu} \right) \\ d_{l\max} = \max \left(d_{al}, d_{bl}, d_{cl} \right) \end{cases} \tag{21}$$

are the minimum and maximum value of the original duty cycle, respectively. Then, the modified duty cycle with the zero-sequence injection can be expressed as

$$\begin{cases} d'_{xu} = d_{xu} - 1 - d_{u\min} \\ d'_{xl} = d_{xl} + 1 - d_{l\max}. \end{cases} \tag{22}$$

Afterward, the modified duty cycle in sector I of upper/lower inverter can be rewritten as

$$\begin{cases} d'_{au} = \frac{1}{T_s} (T_{U1} + T_{U2}) \\ d'_{bu} = \frac{1}{T_s} T_{U2} \\ d'_{cu} = 0 \end{cases} \tag{23}$$

$$\begin{cases} d'_{al} = \frac{1}{T_s} (T_{L1} + T_{L2} + T_{L0}) \\ d'_{bl} = \frac{1}{T_s} (T_{L2} + T_{L0}) \\ d'_{cl} = \frac{1}{T_s} T_{L0}. \end{cases} \tag{24}$$

Then, the modified duty cycle d'_{xl}/d'_{xu} would be adopted as modulation waveforms to obtain the switching sequences.

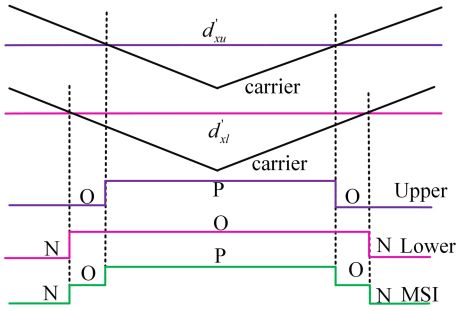

Fig. 9. Results of multiple-carrier comparison: Switching states for the upper inverter, lower inverter, and MSI.

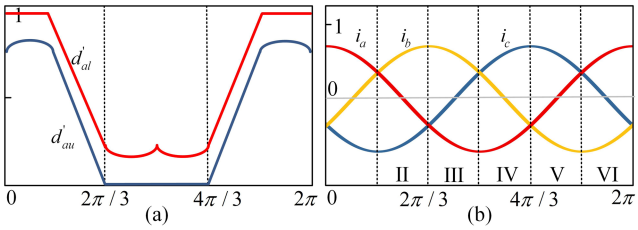

Fig. 10. Modified duty cycle in phase a and AC-side current. (a) Modified duty cycles of the upper and lower inverters. (b) AC-side current in one period.

D. Multiple-Carrier Comparison for Switching States Generation

Fig. 9 shows the results of multiple-carrier comparison: switching sequences for upper inverter, lower inverter, and MSI. Switching sequences of upper/lower inverters are derived from multiple-carrier comparison. d'_{xu} products two states (P and O), which are adopted to control switches S_{x1} and S_{x3}, d'_{xl} products two states (O and N), which are adopted to control switches S_{x2} and S_{x4}. Afterward, the switching sequence of the MSI can be constructed by superimposing those of upper/lower inverters. Hence, the MSI outputs a three-level switching sequence. Then, four switching actions in one switching cycle are unavoidable. One drawback of the proposed modulation is higher switching losses in comparison to the previously modulations. It can be concluded from Fig. 9 that this disadvantage is caused by the modified duty cycle. However, the modified duty cycle provides a wider power distribution range, which would be discussed in Section IV.

IV. Power Distribution Analysis

In this section, the active power of two dc ports is first calculated. Then, the power distribution range and its influence factors are discussed.

A. DC-Port Active Power Calculation

Fig. 10 shows the modified duty cycle in phase a and ac-side current. For the sake of simplicity, only modified duty cycle and ac-side current in sector I are adopted to calculate dc-port power.

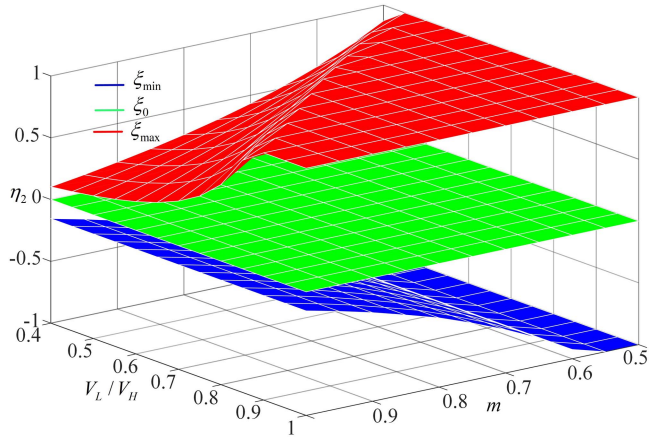

Fig. 11. Port power ratio η_2 with different modulation index m and different port voltage ratio V_L/V_H.

The active power of high-voltage port-1 can be calculated as

$$P_1 = (V_1 + V_2)(d'_{au} i_a + d'_{bu} i_b + d'_{cu} i_c). \tag{25}$$

Substituting (23) into (25), P_1 can be rewritten as

$$P_1 = \frac{V_1 + V_2}{T_s}(T_{U1} i_a - T_{U2} i_c). \tag{26}$$

In sector I, $i_a > 0$ and $i_c < 0$ are considered. Hence, $P_1 > 0$ should be satisfied. This is consistent with the preset in Section II, i.e., the high-voltage port-1 is unidirectional.

The active power of low-voltage port-2 can be calculated as

$$P_2 = V_2[(d'_{al} - d'_{au}) i_a + (d'_{bl} - d'_{bu}) i_b + (d'_{cl} - d'_{cu}) i_c]. \tag{27}$$

Substituting (23) and (24) into (27), P_2 can be rewritten as

$$P_2 = \frac{V_2}{T_s}[(T_{L1} - T_{U1}) i_a + (-T_{L2} + T_{U2}) i_c]. \tag{28}$$

Based on (16) and (17), (28) can be rewritten as

$$P_2 = \frac{V_2}{T_s}[(T_{L1} - M T_{L1}) i_a + (-T_{L2} + M T_{L2}) i_c] \tag{29}$$

where M is defined as $M = \frac{(1-\xi)V_2}{\xi V_1}$. Especially, $P_2 = 0$ can be achieved when $M = 1$. In this case, ξ can be obtained as

$$\xi = \xi_0 = \frac{V_2}{V_1 + V_2} = \frac{V_L}{V_H}. \tag{30}$$

This condition can be considered as the MSI operates in mode I, and the output power of low-voltage port-2 is zero.

B. Discussion of Power Distribution Range

Fig. 11 shows port power ratio η_2 with different modulation index m and different port voltage ratio V_L/V_H. The port power ratio is defined as

$$\eta_1 = \frac{P_1}{P_{\text{total}}}, \eta_2 = \frac{P_2}{P_{\text{total}}} \tag{31}$$

where $P_{\text{total}} = P_1 + P_2$ is the total output power of two dc ports. Ignoring the power losses, P_{total} can be formulated as

$$P_{\text{total}} = 3 V_{\text{ref}} I_{\text{ref}}. \tag{32}$$

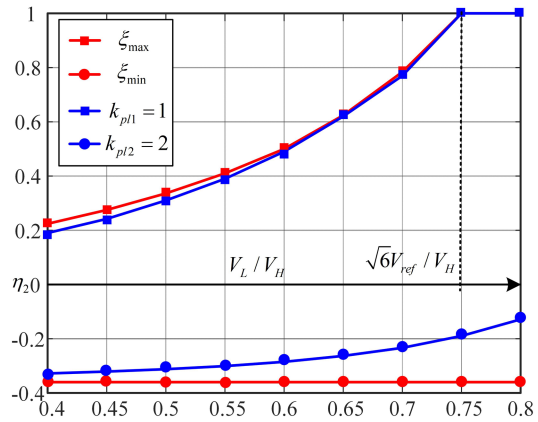

Fig. 12. Port power ratio η_2 with different port voltage ratio V_L/V_H under modulation index $m = 0.86$: Proposed strategy (red line), power distribution strategy in [28] (blue line).

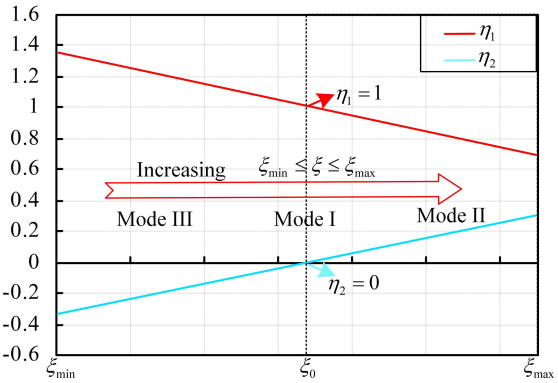

Fig. 13. Port power ratio with different ξ under balanced port voltages.

In Fig. 11, with the increasing modulation m, the power distribution range decreases. With the decreasing modulation m, the power distribution range increases but its maximum is limited. In this study, the modulation index is set as 0.86.

Fig. 12 shows a port power ratio η_2 with different port voltage ratio V_L/V_H under modulation index $m = 0.86$: proposed strategy (red line), power distribution strategy in [28] (blue line). All ac-side power can be supported by port-2 when $V_L \ge \sqrt{6}V_{\text{ref}}$. The power distribution range increases as V_L/V_H increases. It can be concluded from Fig. 12 that the power distribution range of the proposed strategy is wider than that of the power distribution strategy in [28]. The wider power distribution range of the proposed strategy is realized by increasing the switching actions in one switching cycle. Though more switching losses are caused, larger power control capability can be obtained by the proposed strategy.

Fig. 13 shows the port power ratio with different ξ under balanced port voltages. To explore the influence of ξ, balanced port voltage conditions are considered to simplify analysis. As shown in Fig. 13, the output power P_2 increases as ξ increases, and the output power P_1 decreases as ξ increases. On the condition of balanced port voltages, (29) can be expressed as

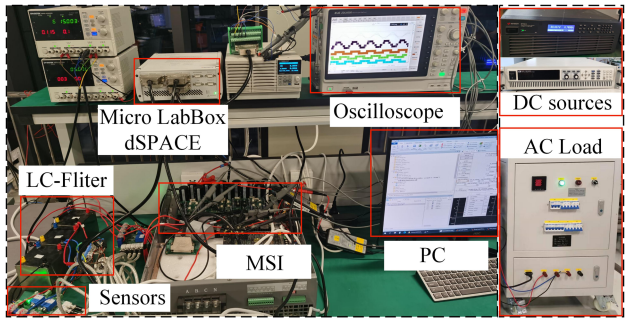

Fig. 14. Experimental test plant.

TABLE III
PARAMETERS OF THE TEST SYSTEM

Low voltage	$V_L = 140$–220 V
High voltage	$V_H = 360$ V
LC-filter inductance	$L_1/R_1 = 3\,m$H/0.4 Ω
LC-filter capacitance	$C = 15\,\mu$F
Sampling time/frequency	$T_s = 100\,\mu$s/$f_s = 10$ kHz
Rated grid voltage	$V_{gref} = 110$ V
Rated grid frequency	$f_{gref} = 50$ Hz
Rated active power	$P_{\text{ref}} = 1$ kW
Rated reactive power	$Q_{\text{ref}} = 0$var

$$\begin{aligned} P_2 &= \frac{V_2}{T_s}\left[\left(T_{L1}-\frac{1-\xi}{\xi}T_{L1}\right)i_a+\left(-T_{L2}+\frac{1-\xi}{\xi}T_{L2}\right)i_c\right] \\ &= (2\xi-1)\left[\frac{\sqrt{3}}{2}\left(\sqrt{3}V_{\text{ref}\alpha}-V_{\text{ref}\beta}\right)i_a-\sqrt{3}V_{\text{ref}\beta}i_c\right] \\ &= k\xi + C \end{aligned} \tag{33}$$

where $k > 0$, and C is independent of ξ. It can be concluded that P_1/P_2 is a monotonically decreasing/increasing function about ξ. Hence, decoupled port power distribution can be achieved by regulating ξ, i.e., proportionally distributing reference vectors to lower/upper inverters. On the condition of $\xi = \xi_0$, the MSI operates at mode I, $\eta_1 = 1$ and $\eta_2 = 0$ have been obtained. In addition, the MSI operates at mode III when $\xi_{\min} \le \xi \le \xi_0$ and operates at mode II when $\xi_0 \le \xi \le \xi_{\max}$.

V. Experimental Results

As shown in Fig. 14, to verify the effectiveness of the proposed strategy, an islanded MGs experimental test plant is established in the laboratory. Parameters of the test system are given in Table III. Two programmable dc sources are used to output high/low voltage. They are directly connected to the MSI. Due to the experimental tests being conducted in islanded MG conditions, the MSI connects the ac load via an LC filter. The proposed control method is implemented in the dSPACE MicroLabBox DS1202 controller, the total execution time is about 20 μs composed of the ad/da conversion and algorithm performing. The input signals of the controller are the voltage/current variables measured by the sensors. The sampling frequency is set to 10 kHz, and the PWM generation and analog-to-digital

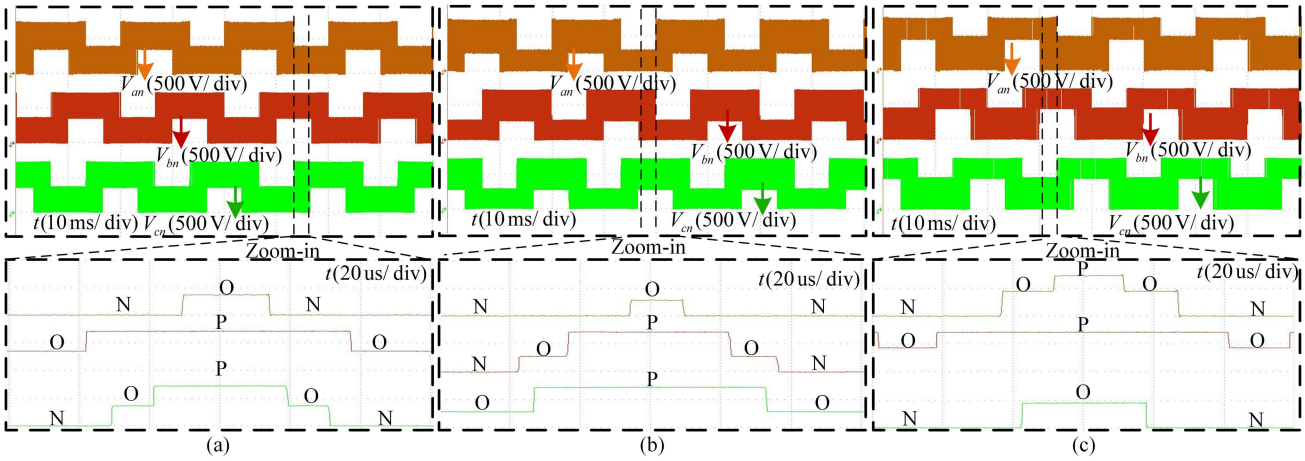

Fig. 15. Switching sequences of the MSI under variable port voltages. (a) $V_1 = V_2$. (b) $V_1 > V_2$. (c) $V_1 < V_2$.

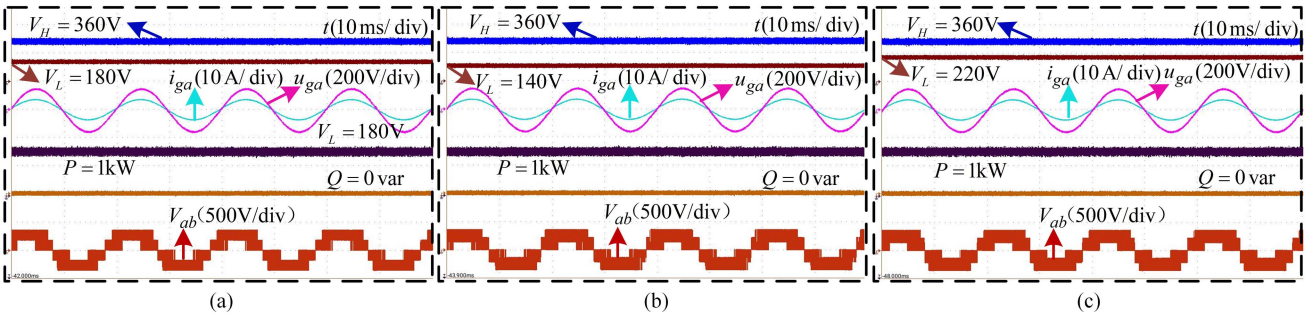

Fig. 16. Steady-state performance under variable port voltages. (a) $V_1 = V_2$. (b) $V_1 > V_2$. (c) $V_1 < V_2$.

conversion are realized by FPGA. The MSI is implemented by insulated-gate bipolar transistors (IGBTs), and the switching frequency is also set to 10 kHz. And an eight-channel oscilloscope is adopted to capture experimental variables.

The following experimental tests are conducted in islanded MGs mode, including the steady-state performance under variable port voltages, results of power distribution, the dynamic performance of mode/power change tests, and comparison with the conventional strategy.

A. Steady-State Tests

The steady-state tests under variable port voltages are conducted to verify the effectiveness of the proposed modeling and modulation methods. On the dc-side, the high voltage is set as $V_H = 360$ V. And the low voltage is set as $V_L = 180$ V, 140 V, and 220 V, which reflects the conditions of $V_1 = V_2$, $V_1 > V_2$, and $V_1 < V_2$. The switching sequences, steady-state performance, and dc/ac side current of the MSI are given as follows.

Fig. 15 illustrates the switching sequences of the MSI under variable port voltages: (a) $V_1 = V_2$, (b) $V_1 > V_2$, and (c) $V_1 < V_2$. As shown in Fig. 15, the MSI outputs desirable phase voltage under variable port voltages. In the zoom-in part, there is a three-level switching sequence in one phase. As discussed in Section III, the three-level switching states of the MSI can be considered as the superposition of those of upper and lower inverters. And the switching sequences of the upper and lower inverters are determined by d'_{xu} and d'_{xl}, separately. Hence, the proposed modeling method is effective, i.e., the MSI can be equivalent to two independent inverters. As four switching actions in one phase are inevitable, the proposed modulation would cause more switching losses.

Fig. 16 demonstrates results of steady-state performance with under variable port voltages: (a) $V_1 = V_2$, (b) $V_1 > V_2$, and (c) $V_1 < V_2$. From top to bottom: waveform is high/low port voltage V_H/V_L, grid-side voltage/current u_{ga}/i_{ga}, grid-side active/reactive power P/Q, and line-to-line voltage V_{ab}. The unbalanced line-to-line voltage V_{ab} is caused by variable port voltages V_H/V_L. Fig. 16 indicates that the proposed strategy achieves desirable grid-side voltage/current tracking performance under variable port voltage conditions. Moreover, the active/reactive power P/Q is regulated as desired, i.e., $P = 1$ kW, $Q = 0$ var. Although the port voltages are different in these three conditions, the results of grid-side voltage/current are almost the same.

Fig. 17 shows results of dc/ac side current: (a) mode I and (b) mode II. From top to bottom: waveform is high-voltage port current i_H, low-voltage port current i_L, and grid-side current i_{ga}. The dc-side currents i_H and i_L are stably controlled with small ripples in both mode I and mode II. Fig. 17 also gives the total harmonic distortions (THDs) of the grid-side current, and

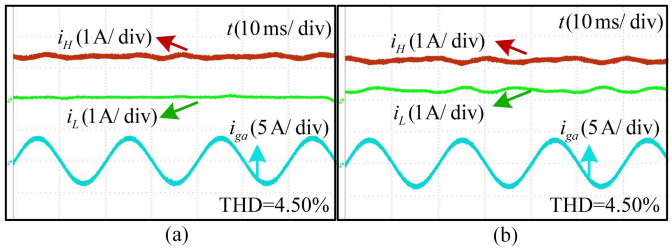

Fig. 17. Results of the DC/AC side current. (a) mode I. (b) mode II.

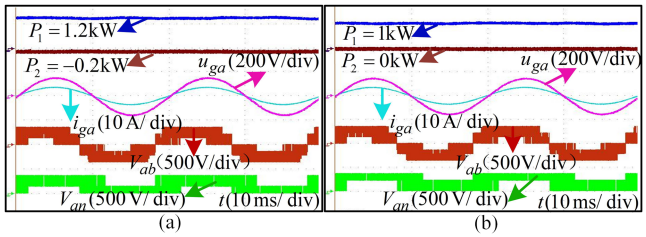

Fig. 18. Power distribution results under unbalanced port voltages. (a) $V_1 > V_2$. (b) $V_1 < V_2$.

the THDs of these two conditions are around 4.50%. Therefore, the proposed strategy shows a beneficial current quality.

Figs. 15–17 verify that the proposed strategy is effective for variable port voltages and has obtained desirable steady-state performance.

B. Results of Power Distribution

1) Power Distribution Under Unbalanced Port Voltages: Power distribution results under unbalanced port voltages are given in Fig. 18. The low voltage is set as $V_L = 140$ V and $V_L = 220$ V in Fig. 18(a) and (b), respectively. Fig. 18(a) shows the results under $V_1 < V_2$, $P_1 = 1.2$ kW and $P_1 = -0.2$ kW are obtained. Fig. 18(b) shows the results under $V_1 > V_2$, $P_1 = 1$ kW and $P_1 = 0$ kW are obtained. Moreover, the quality of output voltage/current is guaranteed. Therefore, the proposed strategy has achieved flexible port power distribution under unbalanced port voltages.

2) Power Distribution Under Balanced Port Voltages: Fig. 19 shows the power distribution results under balanced port voltages: (a) mode I, (b) mode II, and (c) mode III. In mode I, $\xi = \xi_0$ is selected. As shown in Fig. 19(a), the output power of low-voltage port-2 is zero, and all the ac-side power is supplied by port-1 ($P_1 = 1$ kW, $P_2 = 0$ kW). In mode II, high-voltage port-1 and low-voltage port-2 support the ac-side together ($P_1 = 0.7$ kW, $P_2 = 0.3$ kW). In mode III, high-voltage port-1 supplies the ac-side, while charging low-voltage port-2 ($P_1 = 1.35$ kW, $P_2 = -0.35$ kW). In the aforementioned three operation modes, beneficial results of grid-side voltage/current and line-to-line/voltage have been obtained. Therefore, the multimode operation of the MSI and its flexible power distribution have been realized.

3) Power Distribution Discussion: To verify the power distribution analysis in Section IV, the variable parameter ξ tests are carried out. Fig. 20 gives the port power ratio results with different ξ under balanced port voltages. There are seven sets of experimental data in Fig. 20. As shown in Fig. 20, experimental results indicate that η_1/η_2 monotonically decreases/increases as ξ increases. The experimental results are consistent with the theoretical analysis in Section IV. Hence, the decoupled port power can be achieved by designing proper ξ.

C. Dynamic Performance

Fig. 21 shows the results of the mode variation tests: (a) from mode I to mode III, and (b) from mode III to mode I. The mode change tests are conducted under balanced port conditions with constant ac power. When the operation mode changes, the port power P_1/P_2 changes to reference quickly. As shown in Fig. 21(a), high-voltage port-1 output power P_1 changes from 1 to 1.35 kW, and low-voltage port-2 output power P_2 changes from 0 to -0.35 kW. Although the operation mode has changed, the grid-side voltage/current and line-to-line/phase voltage keep stable.

Fig. 22 shows the results of the ac power variation tests: (a) power steps up tests, and (b) power steps down tests. Due to the ac power change tests being conducted in mode I, low-voltage port-2 output power P_2 remains at 0 kW as desired. High-voltage port output power P_1 and grid-side current change rapidly as the power steps up and down. As shown in Fig. 22(a), P_1 changes from 1 to 2.25 kW quickly when ac power steps up. Although ac power has been changed, grid-side voltage and line-to-line/phase voltage remain stable.

Figs. 21 and 22 suggest that the proposed strategy has fast and smooth dynamic performance.

D. Comparison With the Conventional Strategy

To verify the effectiveness of the proposed strategy, the comparison between the conventional strategy in [28] and the proposed strategy is carried out. The power losses and system efficiency are discussed first. Then, the power distribution range comparison is given. Finally, the evaluation of the comparison is carried out.

1) Power Losses and System Efficiency: As shown in Fig. 15, the proposed strategy generates nine-segment PWM signals. While the conventional strategy generates five-segment or seven-segment PWM signals. Hence, the power losses of the proposed strategy are higher than that of the conventional strategy, i.e., the system efficiency of the proposed strategy is lower than that of the conventional strategy. The power analyzer WT1800 is adopted to test the system efficiency. The system efficiency test circuit is shown in Fig. 23, where W_1 and W_2 are the dc-side input powers, and W_3 and W_4 indicate the ac-side output powers. Then, the system efficiency η_s can be calculated as

$$\eta_s = \frac{W_1 + W_2}{W_3 + W_4}. \tag{34}$$

Fig. 24 shows the system efficiency of the conventional strategy [28] and proposed strategy under different port voltage ratios V_L/V_H. The efficiency of the proposed strategy is approximately 0.5% lower than that of the conventional strategy, i.e., the proposed strategy causes higher power losses. However, the

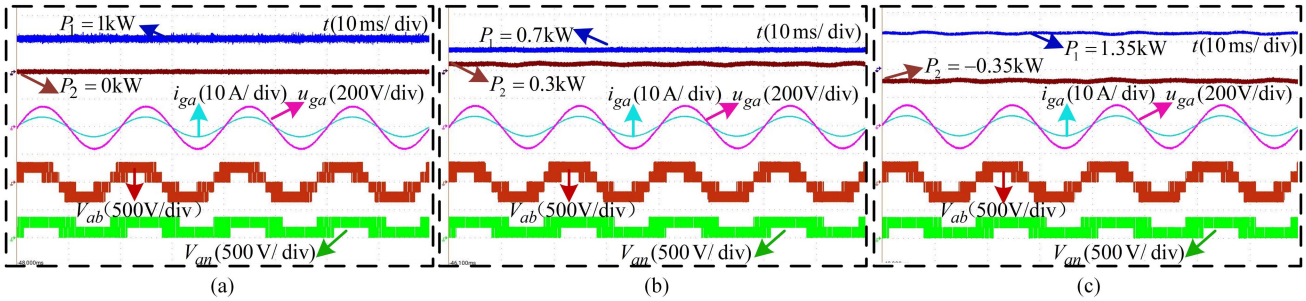

Fig. 19. Power distribution results under balanced port voltages. (a) Mode I. (b) Mode II. (c) Mode III.

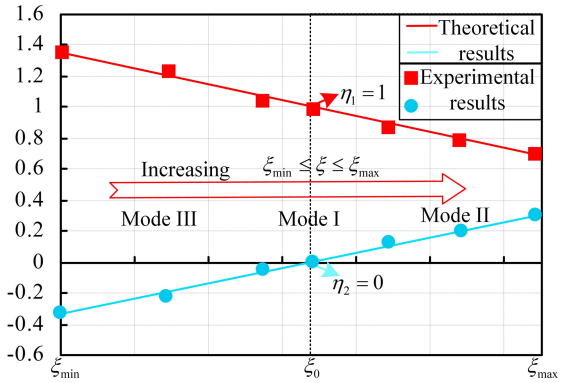

Fig. 20. Port power ratio results with different ξ under balanced port voltages.

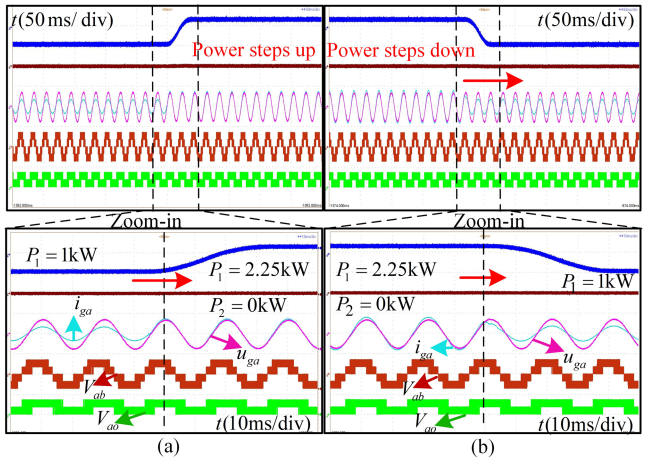

Fig. 22. Results of the AC power variation tests. (a) Power steps up tests. (b) Power steps down tests.

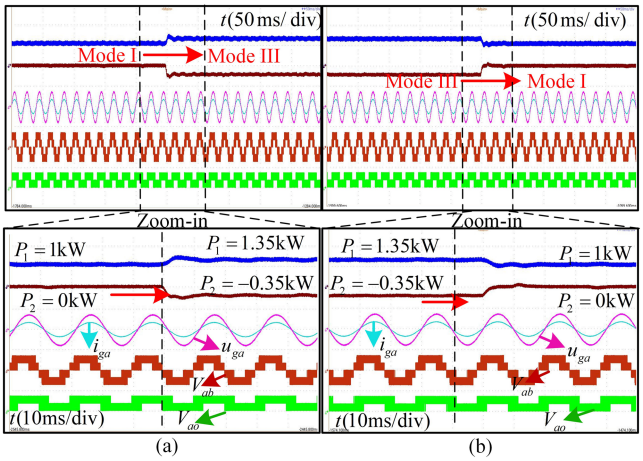

Fig. 21. Results of the operation mode variation tests. (a) From mode I to mode III. (b) From mode III to mode I.

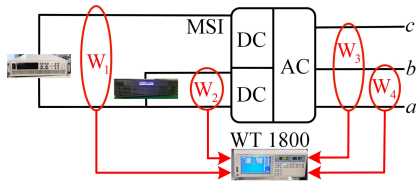

Fig. 23. System efficiency test circuit.

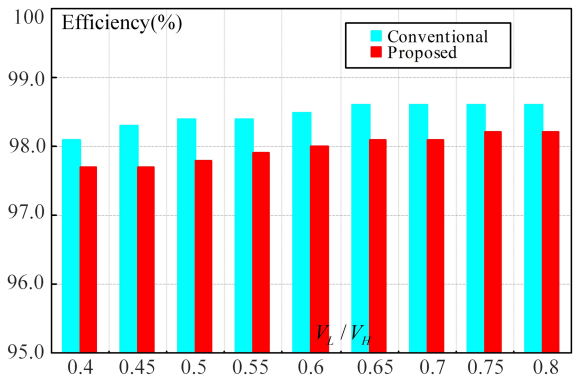

Fig. 24. System efficiency of the conventional strategy [28] and proposed strategy under different port voltage ratios V_L/V_H.

efficiency of the proposed solution is still higher than that of the two-stage structure due to the removal of the dc/dc converter.

2) Power Distribution Range: Fig. 25 shows the power distribution results of the conventional strategy [28] (blue line) and the proposed strategy (red line) under different port voltage ratio V_L/V_H. The experimental results are consistent with the theoretical results in Section IV. It can be concluded from Fig. 25 that the proposed strategy shows a wider power distribution range than that of the conventional strategy.

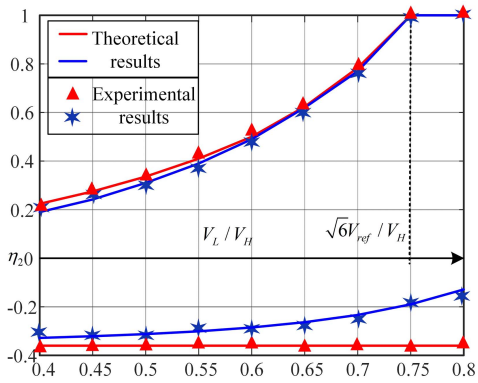

Fig. 25. Power distribution results of the conventional strategy [28] (blue line) and proposed strategy (red line) under different port voltage ratio V_L/V_H.

To be concluded, the proposed strategy generates a wider power distribution range at the expense of higher switching losses. Though the system efficiency is reduced, more RES power can be harvested and more ESS power can be stored. Moreover, the proposed strategy realizes decoupled port power control, which offers clear power distribution guideline.

VI. Conclusion

The MSI directly connects RES and ESS to the ac-side without dc/dc converter, which helps to reduce system cost and improve the efficiency in MGs applications. To simplify the modulation implementation process and power distribution analysis, a decoupled model for the MSI is proposed. Then, a multiple-carrier modulation-based strategy is proposed to obtain a wider power distribution range. The proposed strategy has the following features:

1) the modeling and modulation methods for the MSI are effective for variable port voltage conditions;
2) flexible power flow between dc ports and ac-side has been realized.

The detailed theoretical analysis and experimental tests illustrate that the proposed strategy offers a wider power distribution range in comparison to the previously published counterparts. Furthermore, experimental results under different scenarios show that the proposed strategy could achieve beneficial voltage/current tracking capability in both steady-state and dynamic conditions. The MSI with the proposed strategy provides an attractive solution for low-cost and high-integration MGs applications.

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