Analysis and Modeling of Self-Powered Cascaded Resonant Switched Capacitor Power Supply for Medium-Voltage DC Systems

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***Abstract*—DC power grid is considered as the future trend for distribution networks. However, the pure medium-voltage direct current (MVdc) grid faces great challenges in designing power supplies with high-voltage input but small power output requirements. The continuous power supply from the MVdc bus typically requires power converters with complex circuit structures and control algorithms. This article presents a power supply with a simple circuit structure for MVdc systems. The proposed power supply is comprised of cascaded standardized submodules to cope with high-voltage input and reduce the isolation requirement, and the voltage balance of all dc-link capacitors can be ensured with submodules operating independently. A start-up strategy and a simple self-powering strategy for the proposed converter are proposed in this article, and the average current model is established to characterize the proposed power supply. To verify the analysis, an average model and a switching model are constructed and simulated in Simulink and a 600-W prototype comprised of five submodules is built and tested to validate the design, and the maximum input voltage can reach 2700 V.**

***Index Terms*—Medium-voltage direct current (MVdc) system, modular converter, resonant switched capacitor converter, small power supply.**

I. Introduction

DC POWER grid is considered the development trend of distribution networks in the future because of its advantages, such as the reduction of power systems' weight and cost, no need for phase angle synchronization and reactive voltage drop compensation, and simple interface to renewable energy generations and dc loads [1], [2]. Pure medium-voltage direct current (MVdc) grid without any ac power link has been applied to applications, such as urban distribution systems and subsea power systems. Several pure MVdc projects can be found for both research purposes and real applications [3], [4].

For all kinds of dc systems, power electronic converters are indispensable for voltage conversion regardless of their power rating. This brings a major issue for all pure MVdc grid systems: how to generate small power in high-voltage systems. In classic ac grids, a small passive transformer is enough to provide small power without using complex high-voltage power converters. However, in pure MVdc grids, every small amount of power requires a power converter. Typical scenarios are given as follows.

1) Auxiliary power supply (APS) that provides energy for controllers and drivers in high-power MVdc power converters [5]. Before the main converter works, no energy can be derived from its low-voltage (LV) side.
2) Power supplies for detection and condition monitoring devices in power systems. Such devices are usually close to the primary side of MVdc grids, and it will be difficult for the power supply to draw power from LVdc networks [6], [7].
3) Power supplies that generate an LV power link for control networks [8]. Even if there are energy storage modules in the whole system, the initial energy should still come from the MVdc bus.

The requirements of such small power converters include the following.

1) *High step-down capability:* The input voltage of such converters can be as high as tens of thousands of volts. The output voltage should be standard 48 V or several hundred volts, which can be converted into a lower voltage with another regular dc–dc converter.
2) *Simple control structure:* Complex control structures require the use of large-scale controllers, such as DSPs or FPGAs, also complex communication structures are needed to support synchronization. However, this will bring the need for smaller power supplies that require power from the MVdc side again.
3) *Simple isolation design:* Because of the high input voltage, the isolation of the system becomes critical. Complex

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isolation design will bring huge size and also potential risks, especially if the power supply is used for the controllers of MVdc systems.

4) *Self-powering feature:* Because no external transformer or converter is applied, the controller or other circuits in the small power supply should easily draw power from its internal LV bus. Only in this way, the difficulty of designing a power supply for this converter is avoided.

Among all power electronic converter solutions, the increasing voltage rating of the power converters can be realized on both device level and circuit level. To the best of the authors' knowledge, the existing solutions can be divided into following three categories correspondingly.

1) Single-stage converter using high-voltage power devices [9], [10], [11], [12].
2) Converters with series-connected power devices [13], [14].
3) Modular converters with input-series structure [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25].

In [9], a 4000-V MOSFET is used in a single-ended flyback converter. However, such a scheme cannot be applied to MVdc systems with dc-link voltage up to 10 kV because of the low breakdown voltage of power devices. Even though SiC power devices show great potential in MVdc applications and several converters have been constructed with 15-kV SiC MOSFETs [10] or 20-kV SiC IGBTs [11], applications of ultrahigh voltage SiC devices are still in the laboratory research stage, and the rated voltage of available commercial IGBT is only 6.5 kV [12]. Besides, although a high step-down ratio and simple control structure can be achieved, the transformer in such schemes will withstand a high dc-link voltage, and isolation design will be a big problem. In addition, these schemes also need an additional small power supply with high-voltage input and high-voltage isolation ability for controllers and driver circuits.

Using series-connected power devices, the shortcoming of the low breakdown voltage of available commercial power devices can be improved, and the input voltage range of power converters can be expanded. In [13], five 1700-V SiC MOSFETs are connected in series to construct a single-stage flyback converter that can withstand 4-kV input, and a tapped-inductor buck converter with series-connected high side switches, which can withstand 3-kV input, is constructed in [14]. However, the self-powering problem for control blocks and the high requirement for isolation design still exist. Apart from that, driver signals of power devices should be highly synchronous to ensure voltage sharing of power devices in series connection, thus control strategy and driver structure will be complex.

Modular converters have also been reported several times for medium-voltage applications. A flyback-based input series output parallel (ISOP) structure converter is adopted in [15], and both the voltage stress of each submodule and isolation requirement for drivers are greatly reduced. But for such a converter, control strategies should be taken to ensure input voltage sharing (IVS) of submodules [16]. To achieve IVS, feedback control with a central controller is used in [17] and an inverse droop control strategy without central controllers is proposed in [18]. In these control strategies, isolated sampling is needed and the control structure or control strategy is usually complex. For simplicity, common duty cycle control can be adopted [14], [19], but a central controller is still needed so that submodules can operate synchronously with the same duty cycle. Besides, the output isolation requirement is still high. For similar reasons, modular multilevel converter [20], which is commonly used in MVdc systems and multicell series–parallel converter [21], is not suitable for the scenarios described in this article.

To simplify the system design, some researchers also use a two-stage structure instead of realizing IVS and regulated output in a single stage as ISOP converters. In [22], an input-series structure power supply is proposed, a resonant switched capacitor converter is used as the voltage balance stage to realize the IVS of dc-link capacitors, and single-ended flyback converters are used as the second stage to provide galvanic isolation and regulated output. This scheme can realize IVS even if the converters in the second stage operate asynchronously with different duty cycles, and the isolation requirement can be reduced by placing the flyback converters in an appropriate position. However, the power devices used in the voltage balance stage still need to operate synchronously and a central controller is still needed, which brings difficulties in controller design and self-powering strategy for the central controller. Besides, standard modularization is not realized in the voltage balance stage, thus the scalability of the scheme is poor.

To cope with the problems mentioned earlier, cascade structure converters are used in [23], [24], and [25]. Two LLC-based cascade structure converters proposed in [23] and [24] can realize IVS of dc-link capacitors without a central controller, and they have low isolation requirement and good scalability. But the power supplies in [23] and [24] need a high-voltage commercial APS module for the control block and large power transformers, leading to a large volume overhead.

In this article, a self-powered cascade structure power supply based on the resonant switched capacitor converter is proposed for MVdc systems, standard modularization is achieved to simplify the system design process, and isolation requirement is greatly reduced. All submodules can operate independently while realizing ZCS of power devices and IVS of dc-link capacitors, thus no central controller is needed. The control structure and control strategy of the proposed power supply are quite simple, only a local controller is used in each submodule and no voltage detection is required. According to the voltage level of the target application, the proposed power supply can be flexibly extended by adding more submodules. Benefiting from the self-powering strategy and switched capacitor structure, the proposed supply also has a lower volume overhead of power passive components.

The rest of this article is organized as follows. In Section II, the overall structure and operation principle of the proposed power supply will be given. As the two most important elements, start-up strategy and self-powering strategy will also be introduced. In Section III, the average current and analysis of the start-up process are presented, and simulation results are given to prove the analysis. In Section IV, a 600-W prototype is designed and tested, and a comparison with several other small power supplies is given. Finally, Section V concludes this article.

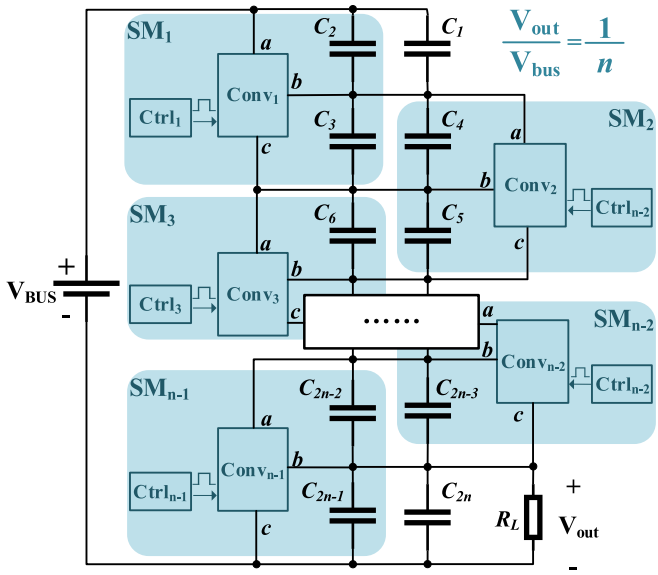


Fig. 1. Overall structure of the proposed power supply.

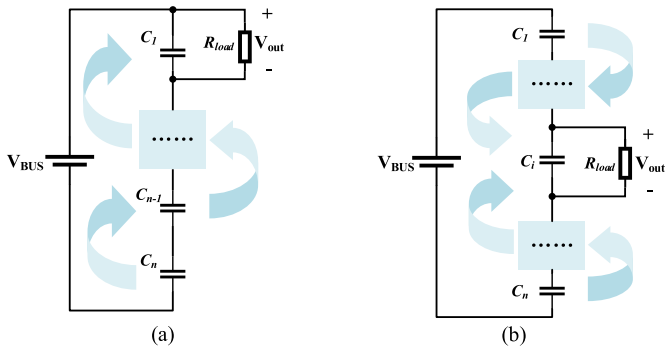


Fig. 2. (a) Energy is transferred from the bottom to the top. (b) Energy is transferred from two ends to the middle.

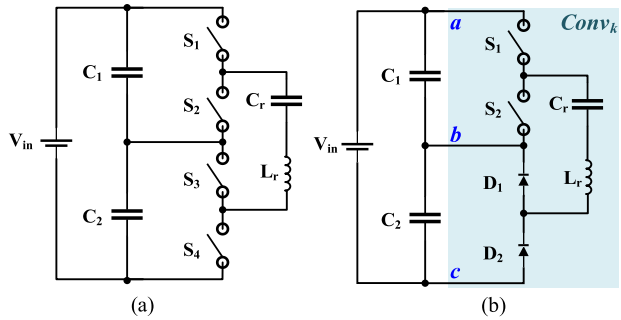


Fig. 3. (a) Basic cell of resonant switched capacitor converter. (b) Topology adopted by a single submodule in this article.

II. System Configuration and Operation Principle

A. Overall Structure of the Proposed Power Supply

The structure of the proposed power supply with n-1 submodules (SM_1, SM_2, …, SM_{n-1}) is given in Fig. 1, each submodule has three ports, a, b, and c, two identical dc-link capacitors C_{2k} and C_{2k+1} ($1 \le k \le n$-1), and one local controller $Ctrl_k$. Among these, C_{2k} is the input capacitor and C_{2k+1} is the output capacitor. Port a of SM_1 is connected to the positive end of the MVdc bus and port c of SM_{n-1} is connected to the negative end of the MVdc bus. Cascade connection is adopted among submodules, i.e., the output side of SM_i ($1 \le i \le n$-2) is connected to the input side of SM_{i+1}, and the load R_L is in parallel connection with the bottom capacitor. In practice, two additional capacitors are used to improve the voltage balance performance of dc-link capacitors, one is connected to the input side of SM_1 and the other is connected to the output side of SM_{n-1}, thus there are $2n$ identical dc-link capacitors in total.

In the proposed power supply, the energy is transferred to the load stage by stage from the top capacitors to the bottom capacitors with the help of converter $Conv_k$ in each submodule. Besides, energy can also be transferred from the bottom capacitor to the top capacitor, thus there are two other different power flow paths, as are shown in Fig. 2(a) and (b). The system structure is selected mainly based on the polarity of the MVdc bus.

The local controller $Ctrl_k$ in each submodule is only responsible for controlling $Conv_k$, no intercommunication among submodules is applied. The converter $Conv_k$ in each submodule is responsible for the voltage balance of two adjacent dc-link capacitors. If the voltage of dc-link capacitor C_k is V_{Ck}, this can be presented by the following equation:

$$V_{C2k} = V_{C2k+1}. \tag{1}$$

Therefore, the voltage balance of all dc-link capacitors is achieved, and a system with a step-down ratio of n is obtained, which can be represented by the following equation:

$$V_{C1} = V_{C2} = \cdots = V_{C2n} = V_{\text{out}} = V_{\text{bus}}/n \tag{2}$$

where V_{out} and V_{bus} are defined in Fig. 1.

B. Operation Principle of a Single Submodule

As mentioned earlier, the converter in each submodule is used to ensure the voltage balance of two adjacent dc-link capacitors. Considering the complexity of topology, control strategy, and ability of soft switching, the resonant switched capacitor converter is adopted here. A basic cell of the resonant switched capacitor converter is shown in Fig. 3(a), and bidirectional energy transmission can be achieved because four switches are used. For the structure used in this article, the load is connected to the bottom capacitors of the system, and the energy only needs to be transferred from C_1 to C_2, thus S_3 and S_4 in Fig. 3(a) are replaced with two diodes for simplicity, as is shown in Fig. 3(b).

The control strategy of the topology shown in Fig. 3(b) is quite simple, S_1 and S_2 only need to work complementarily a 50% duty cycle and the voltage self-balance of dc-link capacitors can be realized. The operation process of the topology can be divided into two stages, and the equivalent circuits and theoretical waveforms are shown in Fig. 4. To simplify the analysis of voltage balance process, ignore the effect of L_r and assume the following.

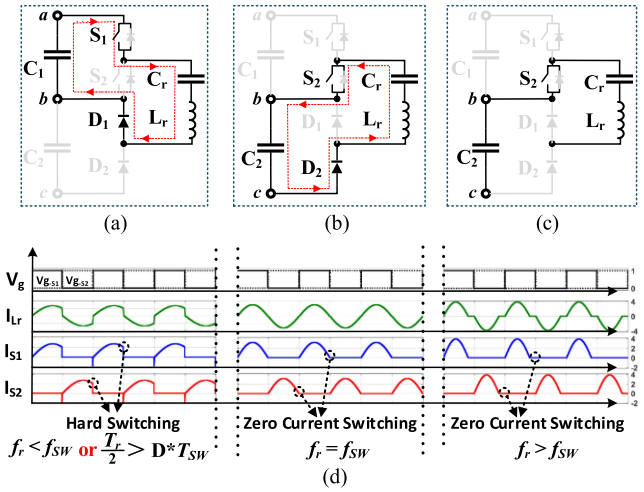


Fig. 4. Operation process of a single submodule. (a) Operation stage 1. (b) Operation stage 2 when $V_{C1} > V_{C2}$. (c) Operation stage 2 when $V_{C1} < V_{C2}$. (d) Theoretical waveforms of a single submodule.

1) All the devices used here are ideal.
2) Capacitance of the dc-link capacitor is much larger than the resonant capacitor C_r.

If $V_{C1} > V_{C2}$, when S_1 is turned ON and S_2 is turned OFF in stage 1, C_r will be charged by C_1 until V_{Cr} is equal to V_{C1}, as shown in Fig. 4(a). In stage 2, S_1 is turned OFF and S_2 is turned ON, and C_r will charge C_2 because $V_{Cr} > V_{C2}$, as shown in Fig. 4(b). This process will cause a voltage drop in C_1 and a voltage rise in C_2 until V_{C1} is equal to V_{C2}.

If $V_{C1} < V_{C2}$, V_{Cr} is also smaller than V_{C2} in stage 2, and C_r will not charge C_2 because D_2 will not be conductive, as shown in Fig. 4(c). Considering C_2 will be connected to a load in practice, the energy stored in C_2 will be continuously consumed, and C_1 and C_r will be charged by the input source until V_{C1} and V_{Cr} are equal to V_{C2}. In this way, the voltage balance of two dc-link capacitors is achieved.

Inductor L_r is used to limit the slew rate of the current to realize the ZCS operation of power devices. For the topology used in this article, because D_1 and D_2 can prevent reverse charging between a dc-link capacitor and the resonant capacitor, the resonant current will drop to zero and stay at this value as long as the resonant frequency f_r is larger than the switching frequency f_{sw}. Theoretical waveforms at different f_r and f_{sw} are shown in Fig. 4(d).

For parameters design, power flow analysis is needed. Assume that the rated output power is P_N, the power balance relationship can be represented by the following equation:

$$P_N = \frac{V_{\text{in}}}{T_s}\int_t^{t+T_s} I_{\text{in}}(\tau)d\tau = \frac{V_{\text{out}}}{T_s}\int_t^{t+T_s} I_o(\tau)d\tau \quad (3)$$

where T_s represents the switching period and the other variables are defined in Fig. 5(a). Because V_{out} is half of V_{in}, the periodic average value of I_{in} is half of I_o. According to the fact that the periodic average value of the current in a capacitor is zero in steady state, the average current of C_r in stage 1 is equal to the periodic average value of I_{in}, and the corresponding power flow is $P_N/2$, and this portion of power will be transferred to the load in the second operation stage.

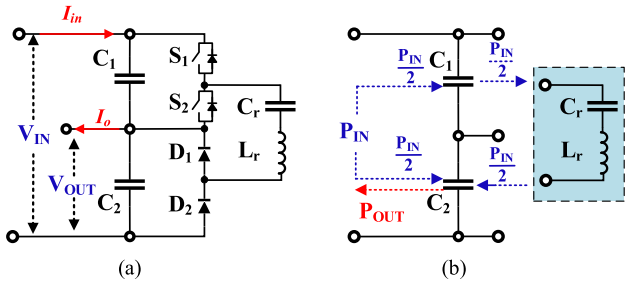


Fig. 5. (a) Definition of input and output variables of a single submodule. (b) Sketch map of power flow in a single submodule.

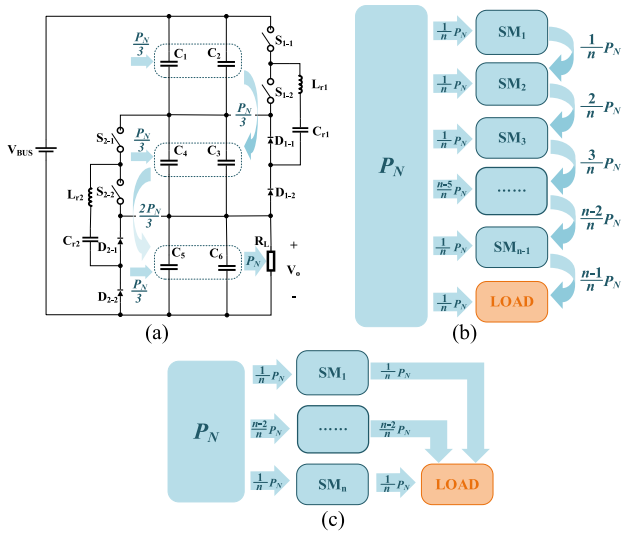


Fig. 6. (a) Operation process of a proposed power supply with two submodules. (b) Power flow diagram of a proposed power supply with *n-1* submodules. (c) Power flow diagram of an ISOP converter with *n* submodules.

Therefore, the output power is comprised of two portions, one portion is given by the input source directly, and the other portion is first transferred from the input source to C_r, and then from C_r to the load. The sketch map of the power flow in a single submodule is given in Fig. 5(b).

C. Operation Principle of Whole Power Supply

Practically, a power supply is often comprised of serval submodules, and a power supply with two submodules is taken as an example to illustrate the operation principle of the cascaded system, as shown in Fig. 6(a).

In steady state, the load R_L will continuously consume energy and cause a voltage drop in C_5 and C_6, then C_3 and C_4 will charge C_5 and C_6 through Cr_2 to keep the voltage balance, and a similar process will occur in SM_1. In this way, energy is delivered stage by stage from the top submodule to the load, and the corresponding power flow is marked in Fig. 6(a). Similarly,

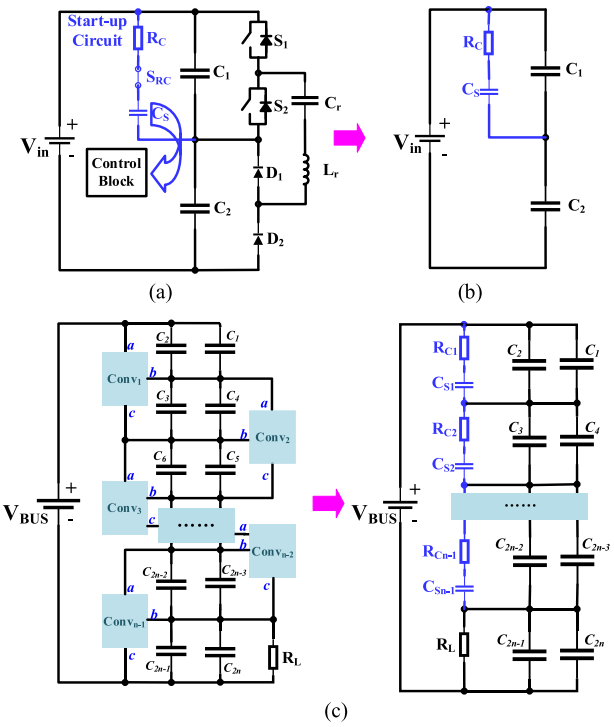


Fig. 7. (a) Single submodule with a start-up circuit. (b) Equivalent circuit of a single submodule during the start-up process. (c) Equivalent circuit of a proposed power supply with *n-1* submodules during the start-up process.

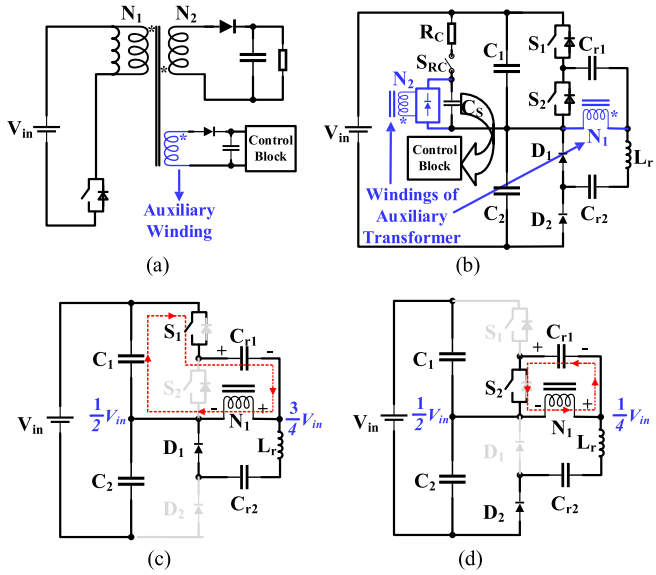


Fig. 8. (a) Flyback converter with an auxiliary winding. (b) Single submodule with start-up circuit and self-powering circuit. (c) Operation stage 1 of the self-powering circuit. (d) Operation stage 2 of the self-powering circuit.

we can get the power flow of a system with *n-1* submodules, as is shown in Fig. 6(b).

A more intuitive understanding of power flow can be derived by comparing the proposed power supply with an ISOP converter. For an ISOP converter with n submodules, the output sides of submodules are directly connected to the load, thus it can be considered that every submodule receives $1/n$ rated power P_N from the input source and then transfers this portion of power to the load directly, and its power flow diagram is shown in Fig. 6(c). For the proposed converter, each submodule also receives $1/n$ rated power P_N from the input source, but the power received by each submodule is transferred to the input side of its adjacent submodule due to the cascade connection adopted here, and this leads to a linear growth of power flow from the top submodule to the load.

D. Start-Up Strategy and Self-Powering Strategy

For the application scenarios described in this article, except for the MVdc bus, no additional LV bus is available for the control blocks of submodules. Therefore, self-starting ability and self-powering ability are essential.

The start-up circuit in a submodule is shown in Fig. 7(a), which is mainly constructed by three parts: a charging resistor R_C, a switch S_{RC}, and an energy storage capacitor C_S. During the start-up process, S_{RC} is driven by a Zener diode, then C_S will be charged. When the voltage of C_S reaches a threshold value, C_S will begin to provide energy for the control block to get the submodule running.

Besides, as shown in Fig. 7(b), the start-up circuit can be seen as a snubber circuit in parallel connection with the dc-link capacitor C_1 during the start-up process. As a result, for a proposed power supply with *n-1* submodules, except for C_{2n-1} and C_{2n}, every dc-link capacitor has a snubber circuit in parallel connection with it, as shown in Fig. 7(c). This helps improve the voltage balance of dc-link capacitors during the start-up process.

Because the start-up circuit is of poor efficiency, it should be turned OFF in steady state and a self-powering circuit with higher efficiency is needed. Compared with using a commercial APS module, it is simpler to add an auxiliary winding to the power transformer or power inductor so that the control block can derive energy from the switching action, and a flyback converter with an auxiliary winding is given as an example in Fig. 8(a). However, in the proposed power supply, the power flow increases from the top submodule to the bottom submodule, which leads to a variation of inductor voltage in each submodule and brings difficulties to auxiliary winding design and standardization of the submodule.

To provide self-powering ability in a relatively simple way without influencing the standardization of submodules, the resonant capacitor C_r in Fig. 3(b) is divided into two identical Cr_1 and Cr_2 in Fig. 8(b). Additionally, an auxiliary transformer with two windings N_1 and N_2 is added to provide galvanic isolation and high step-down conversion. The two operation stages of the proposed self-powering strategy are shown in Fig. 8(c) and (d). For simplicity, assume the following.

1) The power consumption of the control block is small and the excitation inductance of the transformer is large enough, thus the current in N_1 can be neglected.
2) Ignore the effect of inductor L_r.
3) Capacitors are considered to be voltage sources.

When S_1 is turned ON and S_2 is turned OFF, the electric potential at the left end of N_1 is clamped at $V_{\text{in}}/2$, and the voltage

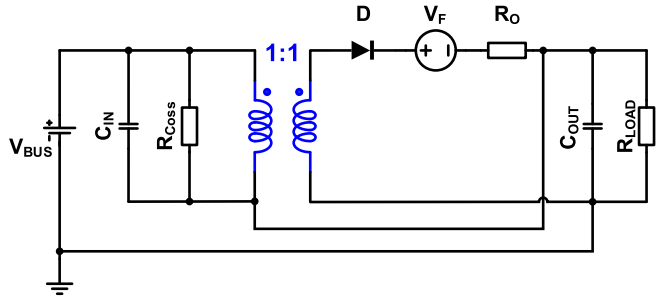


Fig. 9. Average current model of a converter comprised of one submodule.

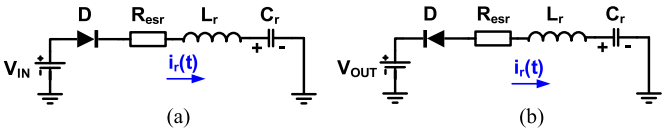


Fig. 10. Equivalent circuits of a single submodule in two operation stages. (a) Stage 1. (b) Stage 2.

of each resonant capacitor is $V_{\rm in}/4$, thus it can be calculated that the voltage of N_1 is $+V_{\rm in}/4$ according to the polarity marked in Fig. 8(c). When S_1 is turned OFF and S_2 is turned ON, the electric potential at the right end of N_1 changes to $V_{\rm in}/4$, and the voltage of N_1 is -$V_{\rm in}/4$. Therefore, an ac square wave with an amplitude of $V_{\rm in}/4$ is applied at the primary winding N_1 of the auxiliary transformer. Then, through the transformer and a diode rectifier, an LV dc bus is derived.

III. Modeling and Simulation

A. Average Current Model of Proposed Power Supply

In this section, the average current model will be given to characterize the proposed converter. First, a converter with one submodule is modeled, as shown in Fig. 9. The turn ratio of the ideal transformer represents the ideal voltage ratio of V_{CIN} and V_{COUT}, R_O represents the ohmic loss of the power converter, V_F represents the loss caused by the conduction voltage of power devices, R_{Coss} represents the loss caused by output capacitors of power switches, and D is an ideal diode.

1) $\rm R_O$ *Calculation:* Equivalent circuits of a single submodule in two operation stages are shown in Fig. 10 and the conduction voltage of power device is ignored here. The ohmic loss of one submodule can be expressed by the following equation:

$$P_{\rm ohm} = f_{sw} \int_0^{T_{sw}} i_{Lr}^2(t) R_{esr} dt \tag{4}$$

where R_{esr} is the sum of the series resistance of all components in the power loop and $i_r(t)$ is the resonant current of the series *RLC* branch

$$i_r(t) = \begin{cases} Ae^{\frac{-R_{esr}}{2L_r}t}\sin(\omega_r t + \phi), & 0 \le t \le \frac{T_r}{2} \\ -Ae^{\frac{-R_{esr}}{2L_r}t} & \\ \quad \sin(\omega_r(t - \frac{T_{sw}}{2}) + \phi), & \frac{T_{sw}}{2} \le t \le \frac{T_{sw}+T_r}{2} \\ 0, & \frac{T_r}{2} \le t \le \frac{T_{sw}}{2} \\ & \cup \frac{T_{sw}+T_r}{2} \le t \le T_{sw} \end{cases}. \tag{5}$$

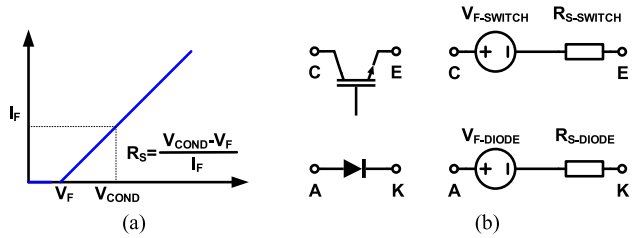


Fig. 11. (a) Typical output characteristic of IGBTs and diodes. (b) Equivalent model of IGBTs and diodes.

Usually, the quality factor of the series *RLC* branch is high enough, and the amplitude of the resonant current can be approximately expressed by $A = \Delta V_i \times \sqrt{C_r/L_r}$, where ΔV_i is the voltage difference between V_{IN} and $V_{\rm Cr}$ at the beginning of each switching cycle. Since the resonant current at the beginning of each switching cycle is 0, we have $\phi = 0$.

In the average current model, the ohmic loss is calculated by the following equation:

$$P_{\rm ohm} = I_{\rm aver}^2 R_{\rm eff} \tag{6}$$

where $I_{\rm aver}$ is

$$I_{\rm aver} = \frac{\int_0^{\frac{T_{SW}}{2}} i_r(t)dt}{T_{SW}} = \Delta V_i f_{sw} C_r \left(1 + e^{-\frac{\pi R_{esr}}{2L_r\omega_r}}\right). \tag{7}$$

From (4) to (7), it can be derived that

$$R_o = \frac{\tanh\left(\frac{\pi}{4Q}\right)}{f_{sw}C_r} \tag{8}$$

where Q is the quality factor of the series *RLC* branch and $Q = \frac{1}{R_{esr}}\sqrt{\frac{L_r}{C_r}}$.

2) $\rm V_F$ *Calculation:* Assume that the power switches used here are IGBTs, the output characteristic of IGBTs and diodes can be represented by the curve shown in Fig. 11(a), and a constant voltage source and a resistor in series connection can be used to characterize the power devices, as shown in Fig. 11(b). The loss calculation of the constant voltage source in the switching model is the same as that in the average current model, thus V_F in Fig. 9 can be derived by the following equation:

$$V_F = 2 \times (V_{F-\rm SWITCH} + V_{F-\rm DIODE}). \tag{9}$$

3) $\rm R_{Coss}$ *Calculation:* R_{Coss} represents the loss caused by the output capacitance of switching devices. In a submodule, the output capacitance loss P_{Coss} can be calculated by the following equation:

$$P_{Coss} = 2 f_{SW} C_{OSS} {V_{CIN}}^2. \tag{10}$$

And R_{Coss} in Fig. 9 can be derived as

$$R_{Coss} = \frac{{V_{CIN}}^2}{P_{Coss}} = \frac{1}{2 f_{SW} C_{OSS}}. \tag{11}$$

Considering that the loss caused by the output capacitance of diodes is usually small and the reverse recovery loss is negligible because of ZCS operation, these are ignored in the average current model.

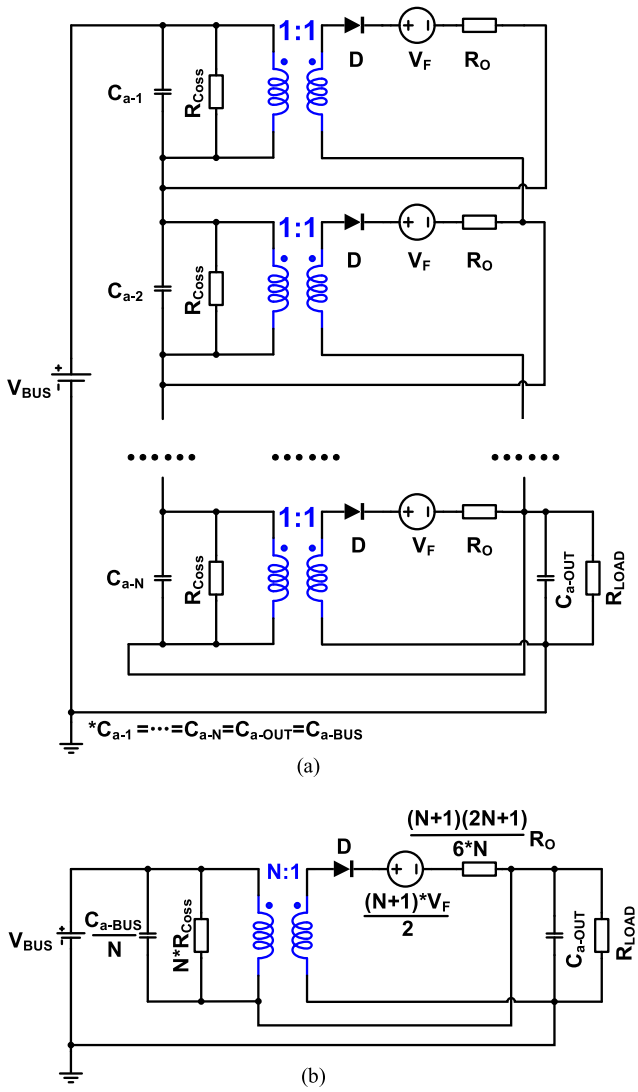


Fig. 12. Average current model of a converter with n submodules. (a) Cascade structure model. (b) Unified model.

4) Average Current Model of Multisubmodule Converter: Through cascade connection, the average current model of a converter with N submodules can be derived, as shown in Fig. 12(a). Such a model can be used to analyze the steady-state dc voltages of each submodule. The model in Fig. 12(a) can be simplified as a unified average current model shown in Fig. 12(b), which can be used to calculate the conversion ratio of the whole converter.

B. Analysis of the Start-Up Process

1) Current Overshoot and Voltage Overshoot: Before the start-up process, the voltage of the resonant capacitor is zero, if a 50% duty cycle is applied during the start-up process, current overshoot and voltage overshoot can be observed in the resonant tank. Assume that the voltages of dc-link capacitors are balanced, the equivalent circuit of a single submodule during the start-up process can be derived in Fig. 13. From Fig. 13, it is easy to get that the maximum voltage of resonant capacitor $V_{Cr\text{-max}}$ and the maximum resonant current $I_{Lr\text{-max}}$ appear

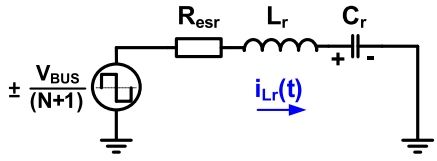


Fig. 13. Equivalent circuit of a single submodule during the start-up process.

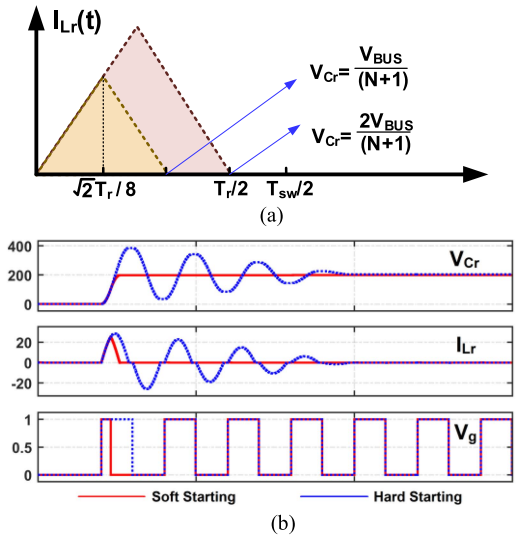


Fig. 14. (a) Duty cycle design for the start-up process. (b) Comparison of soft starting and hard starting.

in the first switching cycle, which can be calculated by the following equation:

$$V_{Cr-\max}=\frac{2V_{\rm BUS}}{N+1}\,,\ I_{Lr-\max}=\frac{2V_{\rm BUS}}{N+1}\sqrt{\frac{C_r}{L_r}}. \tag{12}$$

To suppress the overvoltage and overcurrent, a proper duty cycle is needed to realize a soft start-up. The recommended range of duty cycle can be obtained from Fig. 14. In Fig. 14(a), a triangular wave is used to approximately replace the sine wave to get the solution. The area of the triangular wave is the amount of charge received by the resonant capacitor. Obviously, precharging of the resonant capacitor can be completed within a switching cycle without overvoltage when the duty cycle meets the following restriction:

$$D_{HS-\text{cycle1}}=\frac{\sqrt{2}\times T_r}{8\times T_S}. \tag{13}$$

Define that $D'=4T_sD_{HS-\text{cycle1}}/T_r$, the maximum resonant current in such situation can be approximately calculated by the following equation:

$$I_{Lr-\max-ss}=D'\,I_{Lr-\max}\,. \tag{14}$$

If a smaller current overshoot is preferred during start-up process, a smaller D' can be used.

2) Voltage Balance Analysis During Start-Up Process: In the start-up circuit, C_S begins to power the control block when its voltage V_{CS} reaches a threshold value V_{SET}. However, because

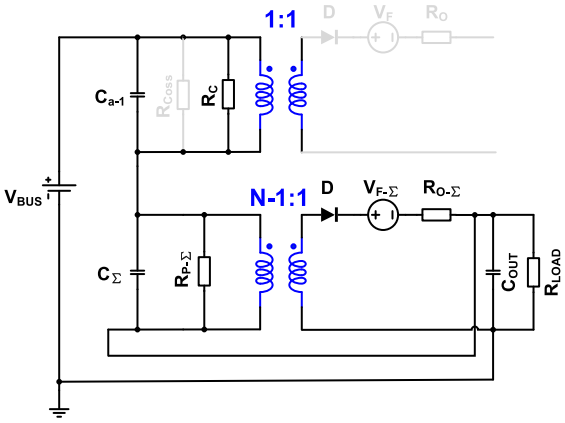


Fig. 15. Equivalent circuit in the worst case.

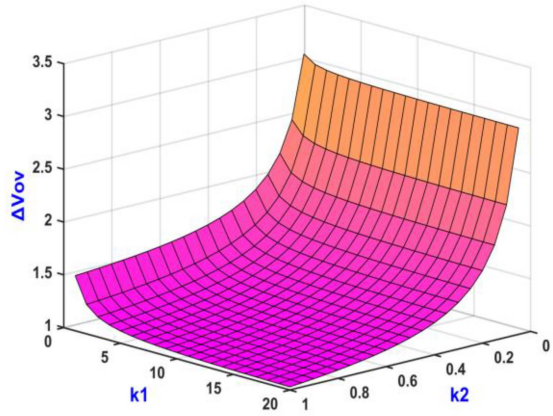


Fig. 16. Voltage balance degree in the worst case.

of the tolerance of passive components, the start-up time varies in different submodules. It is necessary to analyze the influence of the unsynchronized start-up time on the voltage balance of dc-link capacitors to ensure that the system can work safely.

The voltage balance of the dc-link capacitors during the start-up process is related to their equivalent parallel impedance, and this can be analyzed by using the average current model derived in Fig. 12. For simplicity, assume the following.

1) $C_{\text{bus}} >> C_r$.
2) Ignore the influence of V_{CS} on the equivalent parallel impedance of dc-link capacitors.

For the proposed power supply, the worst situation in the start-up process is that the first submodule has not been started, whereas the other submodules have been started. At this time, the input capacitor of the first submodule $C_{a\text{-}1}$ will have the highest voltage, and the equivalent circuit of the proposed power supply is shown in Fig. 15. According to the circuit in Fig. 15, the voltage of $V_{Ca\text{-}1}$ can be calculated by the following equation:

$$V_{Ca-1} = \frac{b_2 V_{\text{bus}} + b_1 V_{F-\Sigma}}{a_1 b_2 + a_2 b_1} \times R_C \tag{15}$$

where

$$a_1 = R_C + R_{P-\Sigma} + R_{\text{LOAD}},\ b_1 = (N-1)\ R_{\text{LOAD}} - R_{P-\Sigma}$$
$$a_2 = \frac{R_{P-\Sigma}}{N-1} - R_{\text{LOAD}},\ b_2 = \frac{R_{P-\Sigma}}{N-1} + (N-1) \times (R_{O-\Sigma} + R_{\text{LOAD}})$$
$$R_{P-\Sigma} = (N-1) \times \frac{R_C \times R_{Coss}}{R_C + R_{Coss}},\ V_{F-\Sigma} = V_F \times \frac{N}{2}$$
$$R_{O-\Sigma} = \frac{N(2N-1)}{6(N-1)} \times R_O.$$

For simplicity, ignore the effect of $R_{O-\Sigma}$ and $V_{F-\Sigma}$ and define that

$$R_{Coss} = k_1\ R_C,\ R_{\text{LOAD}} = k_2\ R_C,\ \Delta V_{OV} = \frac{V_{Ca-1}}{\frac{V_{\text{BUS}}}{N+1}} \tag{16}$$

where ΔV_{OV} indicates the voltage unbalance degree of dc-link capacitors in the worst case. The closer the ΔV_{OV} is to 1, the better the voltage balance is.

Substitute (16) into (15), the relationship among ΔV_{OV}, $k1$, and $k2$ can be represented by Fig. 16. It can be gotten from Fig. 16 that if the following two conditions are met, the voltage balance of dc-link capacitors can be ensured even in the worst case.

TABLE I
SIMULATION PARAMETERS OF SWITCHING MODEL

Parameters	Values	Parameters	Values
Maximum Bus Voltage V_{bus}	3000 V	Number of submodules N	4
Switching Frequency f_{sw}	50 kHz	DC-link capacitors C_k	14 μF
$V_{\text{F-IGBT}}$	0.8 V	$V_{\text{F-DIODE}}$	1.3 V
$R_{\text{S-IGBT}}$	60 mΩ	$R_{\text{S-DIODE}}$	45 mΩ
L_r	18.8 μH	C_{r1} and C_{r2}	820 nF
$R_{esr\text{-}Lr}$	40 mΩ	$R_{esr\text{-}Cr}$	20 mΩ
$Coss$	100 pF	R_C	6 kΩ

1) $R_{Coss} >> R_C$.
2) R_L is as close as possible to R_C.

In the physical sense, when the aforementioned two conditions are met, whether the submodule works will not significantly change the equivalent parallel impedance of its dc-link capacitors, and there is no significant voltage unbalance during the start-up process. Besides, it should be pointed out that the value calculated by (15) only occurs when the start-up time difference among the submodules is large enough, thus ΔV_{OV} will be smaller in practice.

C. Simulation Verification

1) Start-Up Process Simulation: A proposed power supply with four submodules is built in Simulink to verify the aforementioned analysis, the schematic of a single submodule in the switching model is shown in Fig. 8(b), and its simulation parameters are shown in Table I. The average current model of a single submodule used in the simulation is shown in Fig. 17, and its parameters calculated by (8), (9), and (11) are shown in Table II.

The start-up process is simulated with an input voltage of 1300 V and a 4-kΩ load, and voltage waveforms of dc-link capacitors and resonant capacitors are shown in Fig. 18(a). By applying the duty cycle calculated by (13) in the first few switching cycles, there is nearly no overvoltage on resonant capacitors during the start-up process.

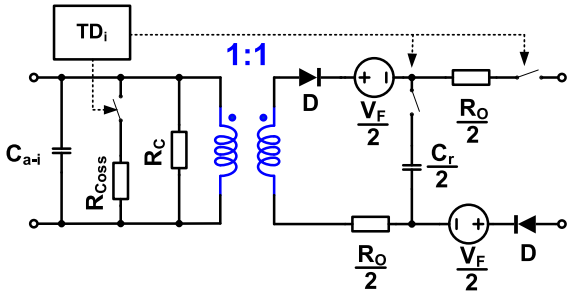


Fig. 17. Average current model used in the simulation.

TABLE II
SIMULATION PARAMETERS OF AVERAGE CURRENT MODEL

Parameters	Values	Parameters	Values
V_F	4.2 V	R_O	962 mΩ
R_{Coss}	100 kΩ	$C_{a\text{-}i}$	28 μF
TD_1	0.42 s	TD_2	0.34 s
TD_3	0.16 s	TD_4	0.07 s

*TD_i is the start-up delay of the ith submodule.

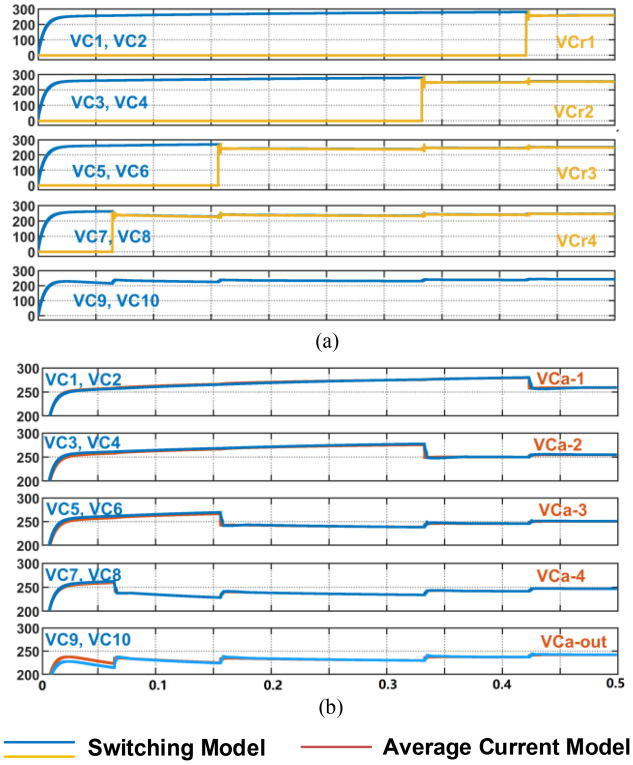


Fig. 18. Simulation results of the start-up process. (a) Voltage waveforms of DC-link capacitors and resonant capacitors. (b) Detailed views of voltage waveforms of DC-link capacitors in switching model and average current model.

Detailed views of voltage waveforms of dc-link capacitors in the switching model and average current model are given in Fig. 18(b), it can be gotten that ΔV_{OV} is only 1.07 and the average current model reflects the dc characteristics of the power supply very well.

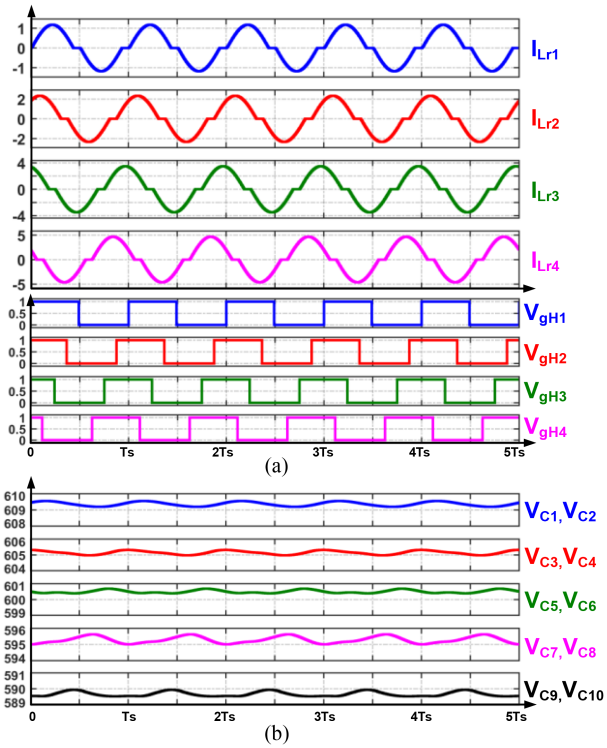


Fig. 19. Steady-state simulation results of switching model. (a) Driver signals of high-side power switches and resonant current waveforms. (b) Voltages of DC-link capacitors.

2) Steady-State Simulation: The driver signals of the high-side power switches in submodules are shown in Fig. 19(a), when the high-side switches are turned ON, the resonant current i_{Lr} increases from zero. Because the resonant frequency is larger than the switching frequency, i_{Lr} falls to zero before the power switches are turned OFF, and the ZCS operation of power devices is realized. Owing to the cascade structure used here, the power flow increases from SM_1 to SM_4.

Simulation results of dc-link capacitors are given in Fig. 19(b), it is obvious that voltage balance of dc-link capacitors is achieved even though all submodules work independently. The slight voltage unbalance is mainly contributed by the conduction voltage of power devices.

IV. DESIGN CONSIDERATIONS AND EXPERIMENTAL RESULTS

A 600-W prototype comprised of five submodules is designed here, the input voltage range is 1300 to 2700 V. Design considerations and experimental results are given in this section.

A. Design Considerations

1) Voltage and Current Rating of Components: For a converter with N submodules, the rated output power of each submodule P_N should meet the following equation for standard modulization:

$$P_N = \frac{N}{N+1} P_{\text{OUT}} \tag{17}$$

where P_{OUT} is the rated output power of the whole converter.

Because voltage balance of dc-link capacitors is realized, voltage stress of power devices $V_{\text{stress-}p}$ and resonant capacitors $V_{\text{stress-}r}$ can be calculated by the following equations:

$$\mathrm{V}_{\text{stress}-p} = \frac{V_{\text{BUS}-\max}}{N+1}\ ,\ V_{\text{stress}-r} = \frac{V_{\text{BUS}-\max}}{2\,(N+1)} \tag{18}$$

where $V_{\text{BUS}-\max}$ is the maximum voltage of the MVdc bus.

In this article, the voltage rating of a component is two to three times of its voltage stress. Besides, the rated ac voltage of a resonant capacitor should be larger than its voltage ripple, and the peak-to-peak value of a resonant capacitor's voltage ripple is

$$\Delta V_{Cr} = \frac{N P_{\text{OUT}}}{C_r f_s V_{\text{BUS}-\min}} \tag{19}$$

where $V_{\text{BUS}-\min}$ is the minimum voltage of the MVdc bus.

As long as the power rating and voltage stress is determined, the current stress of the power devices $I_{\text{stress-}p}$ and the resonant components $I_{\text{stress-}r}$ can be calculated by the following equations:

$$I_{\text{stress}-p} = \frac{\pi}{2}\,\frac{N \times P_{\text{OUT}}}{V_{\text{BUS}-\min}}\sqrt{\frac{f_r}{f_{SW}}},\ \ I_{\text{stress}-r} = \sqrt{2}\,I_{\text{rate}-p}. \tag{20}$$

The current rating of a component should be larger than its current stress. Besides, saturation current of L_r should meet the following requirement:

$$I_{SAT-Lr} > \max\left\{I_{Lr-\max-ss}, \frac{\pi f_r N P_{\text{OUT}}}{f_{sw} V_{\text{BUS}-\min}}\right\} \tag{21}$$

where $I_{Lr-\max-ss}$ is defined in (14).

2) Resonant Frequency: For ZCS operation, resonant frequency f_r should be larger than the switching frequency f_{sw}, so we have

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \geq f_{sw}. \tag{22}$$

For lower conduction loss of power devices, it will be better that f_r is as close as possible to f_{sw} to reduce the rms current. However, considering the tolerance of passive components, the parasitic inductance of packages, and parameter drift caused by the long-time operation, a design margin is needed. In this article, the maximum tolerance of the passive components is 10%, and an additional 5% design margin is left for the other factors

$$f_r = 1.15 \times f_{SW}. \tag{23}$$

3) Resonant Components: As the rated power and resonant frequency are determined, the peak value of the resonant current in the steady state is also determined. Usually, reducing the inductance of the resonant inductor L_r can improve the power density of the system. On the other hand, if L_r is too small, f_r is more sensitive to the parasitic inductance of the converter, and a smaller duty cycle is required during the start-up process to suppress the current overshoot in the resonant tank to prevent the device from being damaged.

In this article, an 18.8-μH inductor and two 820-nF capacitors are used, and the volume of the resonant capacitors is similar to that of the resonant inductor in this condition, which is convenient for the PCB layout, and the current overshoot in the start-up process is also within the acceptable range.

4) Start-Up Circuit: The charging resistor R_C is related to voltage balance during the start-up process, it is recommended that R_C is 1/10–1/20 of R_{Coss}. In this article, R_{Coss} of the selected power switch is about 100 kΩ, so R_C used here is 6 kΩ.

The appearance of a single submodule is shown in Fig. 20 and the parameters of the whole prototype are given in Table III.

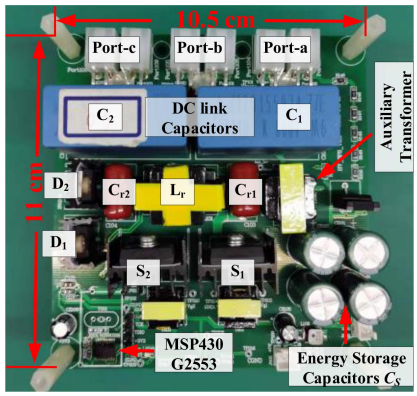


Fig. 20. Appearance of a single submodule in the prototype.

TABLE III
PARAMETERS OF WHOLE POWER SUPPLY

Parameters	Values
Input voltage range V_{bus}	1300−2700 V
Rated output voltage V_o	400 V
Rated Output Power	600 W
Power switches S_1 and S_2	IGW25N120H3
Diodes D_1 and D_2	STTH1210DI
DC- link capacitor C_k	14 μF
Resonant Capacitor C_{r1} and C_{r2}	820 nF
Resonant Inductor L_r	18.8 μH
Switching frequency f_{sw}	50 kHz
Turns ratio of auxiliary transformer N_1: N_2	12:1

B. Experimental Results of a Single Submodule

The start-up process of a single submodule at 400-V input is tested at first, and a 1-kΩ resistor is used as the load. The voltage waveforms of the energy storage capacitor V_{CS}, input source V_{bus}, and output voltage V_{out} are shown in Fig. 21(a).

During the start-up process, the energy storage capacitor C_s will be charged at first, then it begins to power the control block of the submodule when its voltage reaches 13 V, and the voltages of dc-link capacitors will be balanced after that. Because energy storage capacitor C_s also acts as the output filter capacitor of the diode rectifier connected to the auxiliary transformer, the voltage of C_s will finally equal the output voltage of the diode rectifier.

Start-up waveforms of a single resonant capacitor's voltage and the resonant current in a submodule with a 6-kΩ load are shown in Fig. 21(b). By applying the duty cycle calculated by

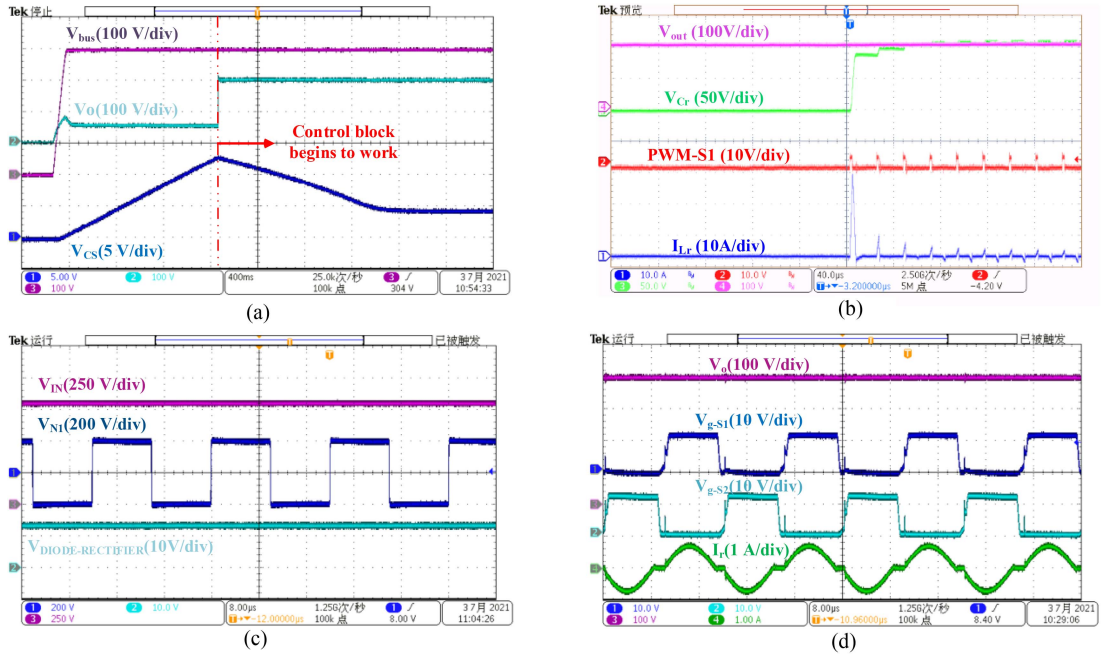


Fig. 21. Experiment results of a single submodule. (a) Start-up process with a 1-kΩ load. (b) Start-up process with a 6-kΩ load. (c) Voltage waveforms of the self-powering circuit. (d) Waveforms of driver signals and resonant current.

(13) in the start-up process, there is nearly no overvoltage in the resonant capacitor, and the maximum resonant current is limited to an acceptable range.

Steady-state waveforms at 800-V input are shown in Fig. 21(c) and (d). At this time, the start-up circuit has been turned OFF and the auxiliary transformer will provide energy for the control block. As shown in Fig. 21(c), an ac square wave with an amplitude of 200 V is applied at the primary winding of the auxiliary transformer, and an internal LV bus is derived at the output port of the diode rectifier. To regulate the output voltage of the diode rectifier, a commercial buck converter LMR16030 is used. Waveforms of power switches' driver signals and resonant current are shown in Fig. 21(d), and it is obvious that the ZCS operation is realized.

Thermal test at 800-V input and 396-V/1055-W output is conducted with a cooling fan. The ambient temperature is 25.5 °C, and a thermal imager UTi384G and an anemometer AR866A are used. After working for 10 min, the thermal performance of a single submodule is shown in Fig. 22. The maximum temperature is 46.4 °C and the wind speed near the heat sinks of IGBTs is about 3.7 m/s.

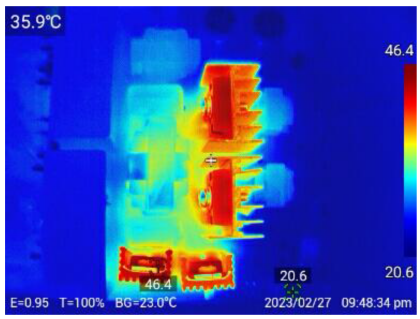


Fig. 22. Thermal performance of a single submodule at 800-V input and 396-V/1055-W output.

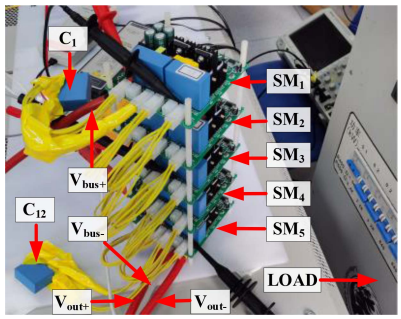


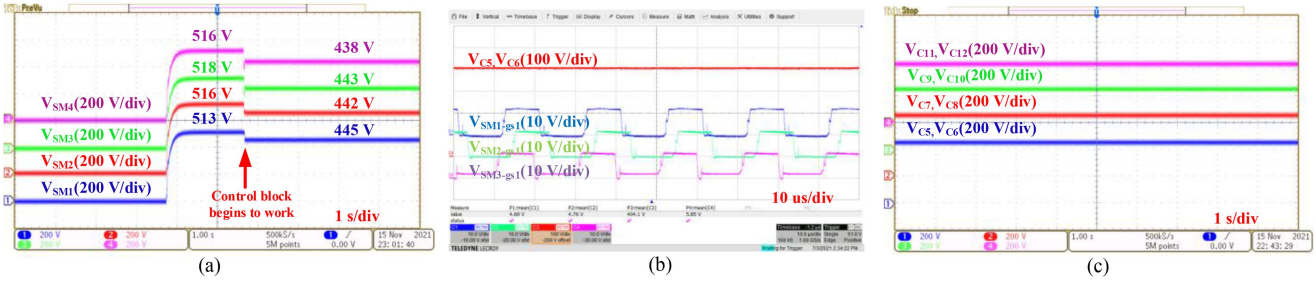
Fig. 23. Appearance of the whole prototype.

C. Experimental Results of the Whole Power Supply

The appearance of a prototype with five submodules is shown in Fig. 23. Except for an MVdc bus, no extra power supply lines are used, and no communication among submodules or central controller is applied.

Voltage waveforms of submodules during the start-up process at 1300-V input are shown in Fig. 24(a). There is no significant overvoltage of dc-link capacitors during the start-up process.

Driver signals of high-side power switches in the first three submodules at 2400-V input are shown in Fig. 24(b). The driver signals are asynchronous, but it has no impact on the operation of the prototype.



(a) (b) (c)

Fig. 24. Experiment results of the whole prototype with a 1-kΩ load. (a) Start-up process at 1300-V input. (b) Driver signals of high-side power switches in the first three submodules at 2400-V input. (c) Voltages of DC-link capacitors at 2700-V input.

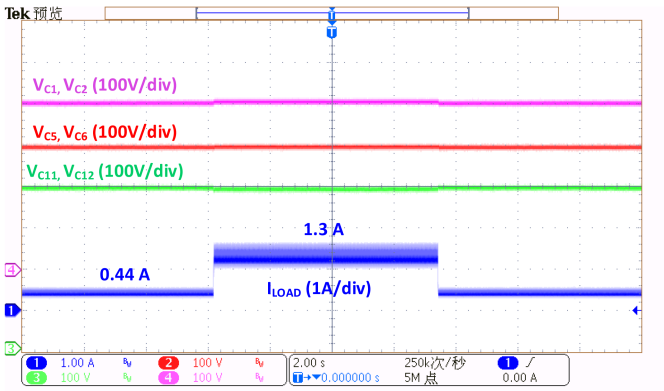


Fig. 25. Load step response from 170 to 510 W at 2400-V input.

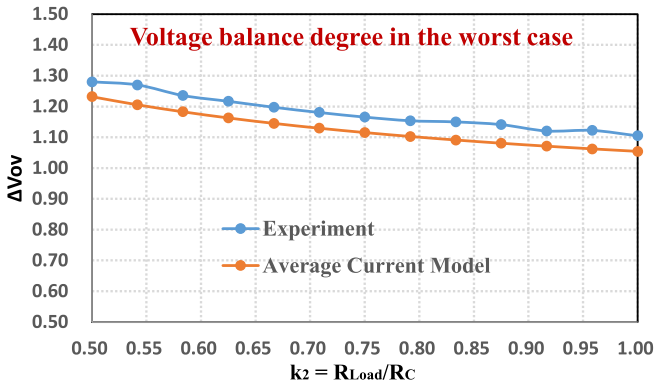


Fig. 26. Voltage balance degree of a prototype with four submodules in the worst case.

Voltage waveforms of dc-link capacitors at 2700-V input are shown in Fig. 24(c). Ignoring the conduction voltage of power devices and measurement error of voltage probes, the voltages of dc-link capacitors are balanced in steady state.

The load step response from 170 to 510 W at 2400-V input is shown in Fig. 25, and a 20-V voltage fluctuation can be observed at the output port of the prototype.

Voltage balance degree in the worst case is tested with a prototype with four submodules at 800-V input, and the control block of the first submodule is disabled in the experiment. The measured value of the relationship between voltage balance degree and load is shown with a blue curve in Fig. 26.

According to the datasheets of components, the voltage balance degree calculated by (15) and (16) is shown with an orange curve in Fig. 26. The maximum error between the experiment and theoretical analysis is about 5%, which is acceptable.

The efficiency curves of the prototype with five submodules are given in Fig. 27, the prototype reaches an efficiency of 82.3% at 2400 V and 83.2% at 1800 V.

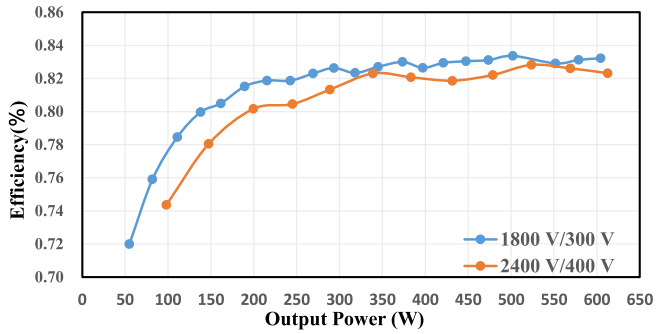


Fig. 27. Efficiency curve of the whole prototype with five submodules.

D. Performance Comparison

Performance comparison with other state-of-the-art small power supplies is summarized in Table IV. For the converter with series-connected power switches [13] or input series structure converter [19], [22], a central controller is needed, this makes the converter more complex and is unfavorable for modular design. Besides, the isolation requirement for drivers or power transformers is high. But in this article and in [23], [24], and [25], the problems mentioned earlier can be solved by adopting the cascade structure converter.

It is simpler to use a buck–boost type cascade structure power supply [25] because the components needed in each submodule are the least. However, considering that the voltage stress of power devices is twice the voltage of a dc-link capacitor, more submodules are needed at the same voltage level, and soft switching operation is not realized. In this article, ZCS operation is realized and power devices have a lower voltage stress.

TABLE IV
COMPARISON WITH OTHER STATE-OF-THE-ART SMALL POWER SUPPLIES

Performance / Works	Isolation requirement for drivers	Central controller	Self-powering ability	Soft Switching Type	Voltage stress of HV power devices ①	Power Rating	Switching Frequency	Volume of Power Passive Components②
This article	Low	Not Needed	Yes	ZCS	$V_{BUS}/(N+1)$	2.4kV/600 W	50 kHz	27.5 cm^3 per submodule
TPEL 2023 [25]	Low	Not Needed	-	Hard Switching	$2V_{BUS}/(N+1)$	0.75 kV/100 W	100 kHz	23 cm^3 per submodule
TPEL 2022 [23]	Low	Not Needed	No	ZC/ZVS	$V_{BUS}/(N+1)$	0.3 kV/150 W	100 kHz	280 cm^3 per submodule
JESTPE 2022 [24]	Low	Not Needed	No	ZC/ZVS	$V_{BUS}/(N+1)$	10 kV/1 kW		
TPEL 2020 [22]	Low	Needed	No	ZCS	$V_{BUS}/(N+1)$	1 kV/125 W	17 kHz	-
ECCE-Asia 2016 [13]	High	Needed	-	Hard Switching	$2V_{BUS}/N$	2400 V/60 W	10 kHz	-
APEC 2015 [19]	Low	Needed	Yes	Hard Switching	$2V_{BUS}/N$	4300 V/60 W	50 kHz	-

①. N is the number of series-connected power switches for a converter with series-connected power switches; for a modular converter, N is the number of submodules.
②. DC-link capacitors are not included.

The power switches in *LLC*-based cascade structure power supply also have lower voltage stress and realize ZC/ZVS operation in [22] and [23]. But compared with the power supply proposed in this article, a high-voltage commercial APS is needed in [22] and [23] because the self-powering ability is not realized. Besides, large power transformers are needed in the *LLC*-based converter. The volume of the resonant capacitors and the power transformer (500-V input/500-V output) of a single module in [23] and [24] is about 280 cm^3. While in this article, because switched capacitor structure is used, the volume of the resonant tank is only 27.5 mm^3 at a lower switching frequency, and it will be no larger than 110 mm^3 if the voltage rating and power rating of a single submodule are increased to the same level with Liu et al. [22] and Xiao et al. [23].

Theoretically, a better voltage balancing performance or load step response can be achieved in those closed-loop approaches, but the slight voltage unbalance of the proposed converter is mainly caused by the conduction voltage of the power device, and a comparable voltage balancing performance can be achieved by replacing IGBTs with MOSFETs and applying a synchronous rectification structure in the proposed power supply. Besides, an LV converter with closed-loop control can be applied to the output port of the proposed power supply to improve the load step response.

V. CONCLUSION

A switched capacitor-based cascade structure power supply for MVdc systems is proposed in this article. The whole power supply is constructed by standard submodules, each submodule works independently and no central controller is needed. The control strategy for the power supply is quite simple, no voltage detection or current detection is needed. The operation principle and power flow of the proposed power supply are analyzed, and a self-powering strategy for switched capacitor converter is proposed. The average model of the proposed converter is established in this article and the start-up process is analyzed based on this model. A 600-W prototype comprised of five submodules is manufactured and several experiments are conducted. Besides, a comparison with other small power supply schemes is made to highlight the advantages of the proposed power supply.

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