An Improved Bidirectional Dual-Output Multilevel Buck PFC Rectifier With Wide Load Scalability and Stability

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***Abstract*—Power converters with multiobjective functionality have ample scope of research in the power electronics field. As a consequence, a bidirectional multilevel buck rectifier (BMBR) is proposed for power factor correction applications. Unlike the existing bidirectional multilevel rectifiers, the proposed BMBR has excellent load scalability and stability. In addition, the proposed BMBR synthesizes multilevel voltage across its input terminals to shape the supply current and reduce its harmonic content. Further, the proposed BMBR eliminates the need for an additional output voltage sensor. Also, its continuous current mode operation reduces the requirement for capacitive and inductive filter at its input and output sides, respectively. All the power switches in the proposed BMBR operate at a lower switching frequency and have equal peak inverse voltage. In addition, the BMBR is capable of feeding single as well as double similar/dissimilar loads simultaneously without compromising converter stability. Through experimental findings, the superiority of proposed BMBR has been confirmed under steady-state and dynamic operations.**

***Index Terms*—Active rectifier, buck power factor correction (PFC), load scalability, multilevel bidirectional converter, stability, switched capacitors.**

I. Introduction

IN PARTICULAR, rectification of ac supply can be actively performed by utilizing a variety of power factor correction (PFC) rectifiers, including typical two-stage bridge integrated dc–dc converter type rectifiers, bridgeless rectifiers (BLRs), and unidirectional multilevel rectifiers (UMLRs) and bidirectional multilevel rectifiers (BMLRs). Nonetheless, IEC/EN 61000-3-2 harmonic limitation guidelines are often followed when designing all these rectifiers [1], [2], [3], [4], [5], [6], [7], and [8]. Due to increased conduction losses caused by voltage drop across bridge diodes, conventional two-stage active rectifiers are less efficient. However, input diode bridge requirements are reduced and fewer switches are permitted in the current conduction path with BLRs [2]. This significantly lowers conduction losses compared with conventional active rectifiers. However, because of the indirect connection between the supply phases and the load terminals, BLRs have a problem with common mode noise [3].

Ultimately, boost converter cell-derived active PFC rectifiers surpass all other rectifiers in prominence because of their exceptional performance. These rectifiers can readily generate 400 V of output voltage from a 230-V ac source, which is essential for the dc-link of large electric vehicle (EV) batteries [4]. However, typical operating voltages for hybrid and pure EV battery systems range between 200 and 800 V. Although, small EVs such as e-bicycles, e-bikes, e-rickshaws, and small electric cars require batteries with a voltage rating of 36, 48, 72, 120, 250, and 300 V. Similarly, compact devices, such as LED drivers and laptop adapters, need a reduced voltage range [5]. However, boost PFC rectifiers cannot be utilized to supply low-voltage applications, since it only produces voltage greater than the peak of its supply voltage [6]. Conversely, only buck PFC rectifiers can generate lower level battery voltages for small EVs. Generally, the buck PFC rectifiers are known for wider output voltage regulation. However, they suffer from the issue of dead zones while operating in the region where the output voltage is higher than the instantaneous value of input voltage [7]. Nonetheless, a buck–boost PFC rectifier possesses both buck and boost PFC rectifier characteristics. Meanwhile, Sepic and Cuk PFC rectifiers accomplish the buck–boost operation and have the capability of effectively isolating the input and the output [8]. However, PFC rectifiers devised from dc–dc converter cells tend to operate at higher switching frequencies (50–100 kHz) and sustain heavy current and voltage burden, especially when in discontinuous conduction mode. In spite of that, all these rectifiers are mandated to have an input-side electromagnetic interference (EMI) filter [7], [8].

The abovementioned issues can be resolved using multilevel rectifiers (MLRs). The MLRs have a greater scope of operating at unity power factor (UPF) by introducing multilevel voltage across its supply terminals. Power switches of these converters usually operate under lesser voltage and current stress. The MLRs have scant scholarly attention. However, various MLRs have been reported in literature for EV charging, high-voltage direct current (HVDC) applications, and power quality supplementary services, including modular multilevel converter (MMC), cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor type. In MMCs, more voltage sensors and feedback control are required to coordinate the capacitor voltage in each submodule [9]. The CHB type

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rectifiers are renowned for its modularity and simplicity, but due to the multiple dc outputs, balancing the capacitor voltages requires additional sensors and complex control strategy [10]. The large number of power switches in NPC converter increases the possibility of switch failure. So, the open-circuit fault detection method for the switches in three-level NPC rectifiers has been investigated in [11]. Further, filterless resonant NPC BLR with reduced switching and conduction loss is given in [12].

The PFC UMLRs based on switched/flying capacitors for multilevel operation are presented in [13], [14], [15], [16], [17], [18], and [19]. All of these MLRs are only intended for use in boost mode. However, UMLRs given in [15] and [16] are derived from two interleaved boost cells by eliminating input diode bridge. These rectifier uses three active switches, six diodes, and split capacitor structure to synthesize five-level (5L) voltage waveform. Lange et al. [17] discussed various 5L UMLRs that use two capacitors, multiple switches, and diodes, which makes the MLR system bulky and costly, whereas the MLRs in [18] yield 5Ls utilizing four switched capacitors and many switching devices. Further, the topology outlined in [19] comprises two capacitors, four switches, and four diodes. Furthermore, switched capacitor-based three-level boost PFC UMLR with reduced voltage gain is presented in [20], which uses two controlled switches, seven diodes, and two switched capacitors. However, all these UMLRs exhibit only rectification operation in the expense of numerous switching components and capacitors.

On the other hand, BMLRs offer a strong advantage in terms of bidirectional power flow. These rectifiers are also capable of functioning as multilevel inverters [21], and have desirable operation of grid to vehicle and vehicle to grid in EVs. In addition, MLRs perform the task of UPF operation with a lower switching frequency than conventional and BLRs [22]. Also, it lessens the need for a large inductive and capacitive filter on the output and input sides, respectively. Although, BMLR of [21] operates in boost mode, while all other BMLRs presented in [22], [23], [24], [25], [26], [27], [28] and [29] does the buck operation. However, BMLR of [21] uses input EMI filter capacitor and two inductors. Subsequently, the authors in [22], [24], [25], and [26] presented packed U-cell (PUC)-derived Buck PFC BMLRs with multiple outputs, including Hani PUC (HPUC) and Packed E-cell (PEC) MLRs, respectively. With integrated basic PUC structure and fewer active switching devices, these BMLRs yield 5L, seven-level, and nine-level voltages. However, controlling the BMLRs necessitates the use of more output voltage sensors and complex control strategy. Furthermore, capacitor voltage balancing is indeed poor, when the loads are of different magnitudes. Hence, their stable operating region is incredibly limited due to lack of self-balancing capability. Also, two switches of these BMLRs have a voltage burden of $2V_{\rm dc}$. Although, BMLR of [25] and [26] implemented for triple output and power quality conditioning operation, which utilizes three output voltage sensors and a model predictive control scheme for capacitor voltage balancing. Further, Jain et al. [27], [28], [29] recently published a buck PFC BMLRs for EV application. For 5L operation, the BMLRs in these literature's employ ten switches and two capacitors. Furthermore, the authors claimed that the proposed topology can be extended to a three-phase rectifier and has self-balancing capabilities. Although, these BMLRs are designed for a single/multiple loads, but the load has to bring across the capacitors by switching actions. This might introduce switching ripples in the output voltage. Some of the inverter topologies that have self-balancing and bidirectional power flow capabilities are given in [30], [31] and [32]. The capacitors in existing Buck MLRs charge together but discharge independently. Since the loads are always connected across the capacitors of MLRs, unequal loads cause the capacitor voltages to be out of balance, which is especially noticeable if the MLR is supplying more than one load, which limits the MLRs' working range for their stable operation. As a result, it should be acknowledged that capacitor voltages can only be balanced when it charges and discharges together.

Consequently, this work proposes a bidirectional multilevel buck rectifier (BMBR) with dual output that addresses the aforementioned issue and possesses the following properties.

1) It performs the PFC operation.
2) It poses 5L voltage across the rectifier's input terminals, which shapes the supply current and improves the total harmonic distortion (THD).
3) It has the capability to feed single or double loads simultaneously with extended load scalability and stability.
4) It requires power switches of equal voltage rating ($V_{\rm dc}$) due to equal peak inverse voltage (PIV) across all the switches.
5) It abolishes the need for input-side capacitive filter and output-side inductive filter because of its operation in continuous conduction mode.
6) Unlike most active rectifiers, it can work at a lower switching frequency.
7) It allows power flow in both directions and can also be used as a multilevel inverter.
8) It can balance capacitor voltages by appropriate switching actions, hence further reduces the requirement of complex control strategy.
9) A single voltage sensor is adequate to control the output voltage since the voltages of the capacitors are held constant by switching actions.

To accomplish these goals, this article is investigating the attributes of switched capacitors-based BMBR, which has heretofore been proposed as an inverter in [31].

II. Proposed Rectifier and Its Topological States

The proposed single-phase dual output BMBR with its control is shown in Fig. 1. It comprised an ac voltage source ($V_{\rm ac}$), an input-side inductor (L_i), two capacitors (C_1 and C_2) with parallelly connected resistive dc loads (R_a and R_b), and nine unipolar bidirectional power switches (S_1–S_8 and S_M), which could either MOSFETs or IGBTs. The proposed BMBR is capable of yielding a maximum of 5L voltage at its input terminals, although this number can be raised by optimizing the more intermediate switching cell units. Here, S_3–S_6 and S_M switches compose the intermediate switching cell. The switch S_M is intended to connect two capacitors in series and charge together from an ac source, resulting in maximum voltage ($\pm 2V_{\rm dc}$) across

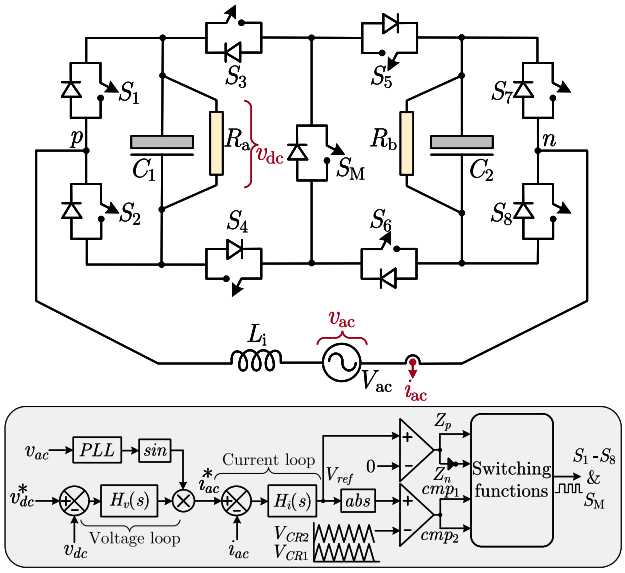

Fig. 1. Proposed bidirectional multilevel Buck PFC rectifier and its control.

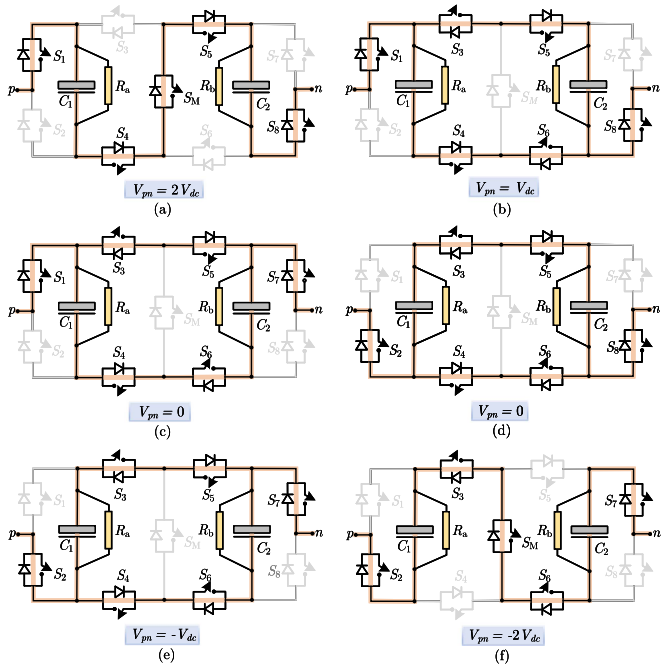

Fig. 2. Topological states of proposed PFC BMBR.

the supply terminals p and n. It is worth noting that capacitors are always held in parallel to discharge through the loads in $\pm V_{\rm dc}$ and zero states. To prevent short circuits of the switches with capacitors, the switch pairs (S_1–S_2), (S_3–S_4, S_M), (S_5–S_6, S_M), and (S_7—S_8) should not be switched ON together. Indeed, switches S_1–S_2 and S_7–S_8 are complementary in nature, and one of these pairs always operates at fundamental frequency, which further reduces switching loss. Also, switch pairs S_3, S_6 and S_4, S_5 are driven from the same triggering pulse, respectively.

A. Discussion on Topological Switching States

The various switching states of the proposed rectifier are detailed as follows.

1) *First topological state (V_{pn}=2$V_{\rm dc}$):* During positive half-cycle of input supply, the switches S_1, S_4, S_M, S_5, and S_8 are turned ON, as shown in Fig. 2(a). Both capacitors (C_1 and C_2) are charging from the input source and yield a maximum $2V_{\rm dc}$ voltage across terminals p and n.
2) *Second topological state (V_{pn}=$V_{\rm dc}$):* During positive half-cycle of input supply, the switches S_1, S_3–S_6, and S_8 are turned ON, as shown in Fig. 2(b). In this case, both capacitors are connected in parallel and discharge to loads R_a and R_b. The voltages across the capacitors are maintained at $V_{\rm dc}$, which reflect at rectifiers' supply terminals.
3) *Third topological state (V_{pn}=0):* During this state, a zero voltage will be flashed across the p and n terminals by utilizing redundant switching states. Either S_1, S_3–S_6, and S_7 or S_2, S_3–S_6, and S_8 are turned ON to attain this state [as shown in Fig. 2(c) and (d)]. Hence, both capacitors are arranged in parallel again, so that their voltages remain equal, and together provide power to the connected loads.
4) *Fourth topological state (V_{pn}=$-V_{\rm dc}$):* In negative half-cycle of input supply, the switches S_2, S_3–S_6, and S_7 are turned ON, as shown in Fig. 2(e). Both capacitors remained in the parallel to feed loads R_a and R_b. The voltage across the capacitors is kept at $V_{\rm dc}$.
5) *Fifth topological state (V_{pn}=$-2V_{\rm dc}$):* During negative half-cycle of input supply, the switches S_2–S_3, S_M, S_6, and S_7 are turned ON, as shown in Fig. 2(f). Both capacitors C_1 and C_2 are organized in series, and hence charge from the input source and acquire a maximum voltage of $-2V_{\rm dc}$ between terminals p and n.

TABLE I
SWITCHING STATES OF THE PROPOSED PFC BMBR

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_M	V_{pn}
1	0	0	1	1	0	0	1	1	$2V_{\rm dc}$
1	0	1	1	1	1	0	1	0	$V_{\rm dc}$
1	0	1	1	1	1	1	0	0	0
0	1	1	1	1	1	0	1	0	0
0	1	1	1	1	1	1	0	0	$-V_{\rm dc}$
0	1	1	0	0	1	1	0	1	$-2V_{\rm dc}$

B. Pulsewidth Modulation (PWM) Control Strategy

Table I demonstrates the switching set needed to execute 5L voltage at rectifiers input terminals. The input 1 implies that a specific switch is turned ON, whereas 0 implies that it is OFF. It is important to generate the required gating signals in order to mimic the correct multilevel voltage at rectifier input terminals. The active switches for producing desired voltage levels are shown in Fig. 2. This is accomplished by using a rectified sinusoidal reference signal and two level-shifted high-frequency carriers signals, as shown in Fig. 3. Suitable logic actions are applied to the comparator outputs to develop switching functions. The reference signal used for comparison is given as follows:

$$V_{\rm ref} = V_m \sin \omega t \tag{1}$$

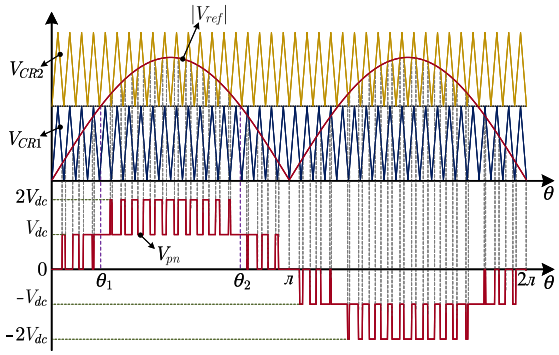

Fig. 3. PWM control strategy.

TABLE II
SWITCHING FUNCTIONS FOR THE SWITCHES OF PROPOSED BMBR

Switches	Switching functions
S_1	Z_p
S_2	Z_n
S_3, S_6	$Z_p \times \overline{cmp_2} + Z_n$
S_4, S_5	$Z_p + Z_n \times \overline{cmp_2}$
S_7	Z_p x $(\overline{cmp_1} + \overline{cmp_2}) + Z_n$ x cmp_1
S_8	Z_p x $cmp_1 + Z_n$ x $(\overline{cmp_1} + \overline{cmp_2})$
S_M	$Z_p \times cmp_2 + Z_n \times cmp_2$

where V_m is the magnitude of reference signal. Its absolute value is obtained as

$$V_{\text{ref,abs}} = |V_{\text{ref}}|\,. \tag{2}$$

The positive and negative half cycles of the reference signal are identified with the help of variables Z_p and Z_n as

$$Z_p = V_{\text{ref}} \geq 0 \text{ and } Z_n = V_{\text{ref}} \leq 0. \tag{3}$$

The level-shifted high-frequency carrier signals (V_{CR1} and V_{CR2}) are compared with (2), resulting in

$$cmp_1 = V_{\text{ref,abs}} \geq V_{\text{CR1}} \text{ and } cmp_2 = V_{\text{ref,abs}} \geq V_{\text{CR2}}. \tag{4}$$

Using (3) and (4), the switching functions for individual switches are derived and detailed in Table II.

C. Capacitor Voltage-Balancing and PFC Control

The charging of capacitors in series with the source and discharging in parallel with the loads enables self-voltage balancing. It can be seen from Fig. 2 that, during $\pm 2V_{\text{dc}}$ state, C_1 and C_2 are arranged in series to charge from the source, whereas in $\pm V_{\text{dc}}$ and 0 states, both the capacitors are connected in parallel using the switching actions to feed the loads. Assuming negligible effective series resistances of the capacitors and the parasitic of the switches in the charging paths, both the capacitors will hold equal voltage in $\pm V_{\text{dc}}$ and 0 states. Hence, the proposed rectifier does not require voltage sensors to balance capacitor voltages. However, one voltage sensor at the output side is sufficient for output voltage regulation. Meanwhile, the control scheme employed for output voltage regulation and PFC operation is shown in Fig. 1, while a proportional resonant (PR) controller has been implemented for inner current control loop for better PFC operation and a proportional–integral (PI) controller for outer voltage control loop. It, thus, improves proposed BMBR control since the PR controller performs better at sinusoidal reference tracking.

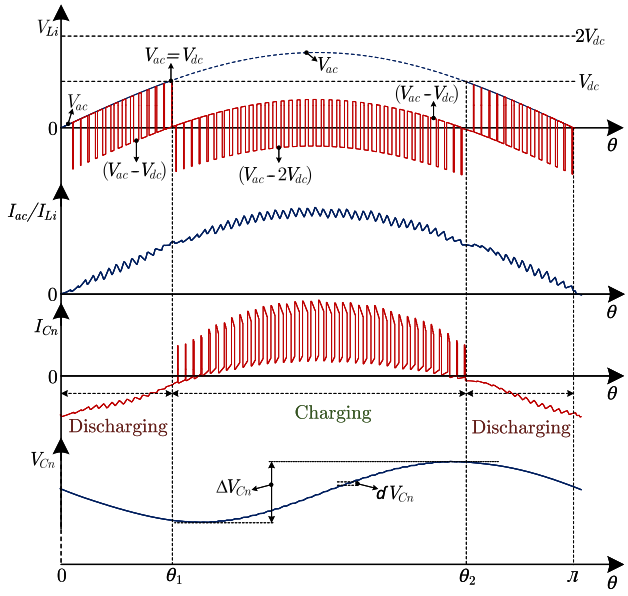

Fig. 4. Waveforms depicting charging and discharging of the capacitors during positive half cycle.

D. Charging and Discharging of the Capacitors

The charge and discharge of the capacitors are described in detail based on inductor voltage and capacitors current waveform during positive half cycle of source voltage, as shown in Fig. 4. The switching frequency (f_s) in the rectifier is assumed to be much greater than the supply frequency (ω). An inductor and the capacitors of the rectifier are considered to be substantial enough to store/supply energy during its respective transition periods. In addition, it is supposed that both the loads are of equal magnitude. The charge and discharge of capacitors are discussed in relation to the modulation index (M) and explained beneath.

When M sin $\theta < 0.5$: In zero-switching states, the source voltage V_{ac} is applied across the L_i to energize it. During this time, both capacitors provide energy to their respective loads (R_a, R_b). However, in V_{dc} states, as shown in Fig. 4, the defluxing voltage ($V_{\text{ac}} - V_{\text{dc}}$) across the L_i is constantly decreasing as the V_{ac} is increasing. Therefore, the addition of source voltage and defluxing voltage across the L_i is insufficient to charge the capacitors. As a result, during $M\sin\theta < 0.5$, the capacitors are constantly discharging to feed the loads. If t_1 and t_2 are the switching periods of zero and V_{dc} states, respectively, for $M\sin\theta < 0.5$ interval, it can be obtained from volt–second balance theory as

$$V_{\text{ac}} dT_s + (V_{\text{ac}} - V_{\text{dc}})(1-d)T_s = 0 \tag{5}$$

where T_s is a switching period, and $V_{ac} = V_{ac,pk} \sin\theta$. By solving abovementioned equation for d, the t_1 and t_2 are calculated as

$$t_1 = (1 - 2M \sin\theta)T_s \text{ and } t_2 = (2M \sin\theta)T_s. \quad (6)$$

When $M sin\theta > 0.5$: In this interval, the value of V_{ac} exceeds the capacitors voltage V_{dc}. In V_{dc} states, the voltage across the inductor is $(V_{ac} - V_{dc})$, and in $2V_{dc}$ states, it is $(V_{ac} - 2V_{dc})$. It can be seen from Fig. 4 that the inductor defluxing voltage $(V_{ac} - 2V_{dc})$ is added to the source voltage to charge the capacitors during $M\sin\theta > 0.5$ interval. Hence, the capacitors' current is positive. However, looking from the inductor current waveform, the energizing and deenergizing periods of inductors seem to be approximately equal for $M > 0.75$. If t_3 and t_4 are the switching periods of V_{dc} and $2V_{dc}$ states, respectively, for $M\sin\theta > 0.5$ interval, it can be obtained as

$$t_3 = (2 - 2M \sin\theta)T_s, t_4 = (2M \sin\theta - 1)T_s. \quad (7)$$

Meanwhile, the capacitors' voltage variation in a single switching cycle is given as

$$\delta V_{C_n} = \frac{\delta Q_{C_n}}{C_n} = \frac{I_{ac,pk} \sin\theta \times (t_4 - t_3)}{C_n}, n = 1, 2 \quad (8)$$

where δQ_{C_n} is the charge stored by the capacitors during T_s, and $I_{ac,pk}$ is the peak of source current. Also, the maximum capacitor voltage ripple (ΔV_{C_n}) is calculated as follows:

$$\Delta V_{C_n} = \int_{\theta_1}^{\theta_2} \delta V_{C_n} d\theta. \quad (9)$$

The value of θ_1 and θ_2 are obtained as

$$\theta_1 = \sin^{-1}\left(\frac{1}{2\,M}\right), \theta_2 = \pi - \theta_1. \quad (10)$$

It can be seen from the capacitor voltage ripple of Fig. 4 that the resultant capacitor voltages increase during θ_1 to θ_2, i.e., in $M\sin\theta > 0.5$ interval, and decreases after θ_2 in $M\sin\theta < 0.5$ period. This is owing to the capacitors' charging/discharging actions, as well as oscillations caused by the double-frequency power component. Importantly, the charging and discharging events of capacitors are considerably influenced by the load characteristics. If the single load is present in the rectifier, then unloaded capacitor is used to supply its energy for a loaded capacitor to feed its load and vice versa.

III. Rectifiers Buck Operation and Its Design Considerations

The proposed topology is used as a buck rectifier by optimizing its input terminal voltage (V_{pn}), which should always be greater than the source peak voltage $(V_{ac,pk})$. V_{pn} must be 5L voltage, with its highest level being $\pm 2V_{dc}$, and this can be achieved by appropriate control of output voltage. The relationship between input–output voltage, boosting factor (α), and modulation index (M) is given as

$$V_{ac,pk} = M \times \alpha \times V_{dc}. \quad (11)$$

The proposed BMBR has a boosting factor of 2, whenever it works as a multilevel inverter [31]. In the rectifier case, the output voltage is expressed as

$$V_{dc} = \frac{V_{ac,pk}}{2\,M}. \quad (12)$$

According to (12), the proposed BMBR operates in buck mode only for M greater than 0.5 $(0.5 < M < 1)$; otherwise, if M is less than 0.5, it will behave like a boost MLR and maximum voltage levels $\pm 2V_{dc}$ will not be seen across p and n.

A. Capacitors Sizing

At UPF operation, the power transferred by the rectifier is segregated into two components, i.e., average and oscillatory power. The average power is transferred to the loads, whereas double-frequency oscillatory power is required to compensate by both the capacitors. Hence, the value of capacitor (C_n) needed to allow an admissible voltage ripples (ΔV_{C_n}) for a given load (R) and supply frequency (ω) is obtained as

$$C_n \geq \frac{V_{dc}}{2\omega R \Delta V_{C_n}}, n = 1, 2. \quad (13)$$

B. Inductor Sizing

The rectifier's input-side inductor shapes supply current and reduces current ripples. Its value primarily depends on the rectifier switching frequency (f_s) and permissible input current ripple (ΔI_{Li}). Assuming negligible inductor parasitic resistance, the voltage across the inductor obtained as

$$L_i \frac{dI_{Li}}{dt} = V_{ac} - V_{pn}. \quad (14)$$

From (14), the value of an input inductor can be calculated for T_s and duty ratio (d) as

$$L_i = \frac{V_{ac} - V_{pn}}{\Delta I_{Li}} d.T_s. \quad (15)$$

The ripples in inductor current are caused by the effect of switching transition $(0 \Rightarrow \pm V_{dc} \Rightarrow \pm 2V_{dc})$ and indirectly the value V_{pn}. However, V_{pn} is approximated to V_{dc}, if M is optimal and the duty ratio of the rectifier becomes 50%. With reference to (12), the input-inductor value is obtained as

$$L_i \geq \frac{V_{ac,pk}\left(1 - \frac{1}{2\,M}\right)}{2 f_s \Delta I_{Li}}. \quad (16)$$

Therefore, better input current with reduced THD and constant output voltage are achieved with the appropriate selection of input inductor and output capacitors.

IV. Load Scalability and Stability Analysis

The proposed BMBR has the capability of supply power to either one or two distinct loads at the same time without disturbing the system stability. Although, in contrast to the HPUC BMBR, the proposed BMBR offers increased load scalability. Further, the stability of the rectifier is determined by equally balanced capacitor/load voltages and phase synchronization between supply voltage and current. As shown in Fig. 5, the proposed BMBR relies on two H-bridge structures, and an additional switch to produce higher voltage level and charge

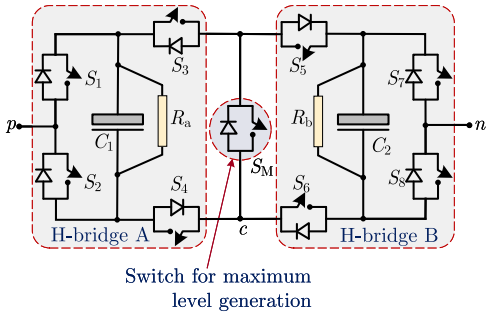

Fig. 5. Proposed BMBR structure comprising two H-bridges and a switch.

the capacitors. Although, each H-bridge produces a constant voltage of $V_{\rm dc}$ to feed their connected loads. Also, due to shared switches and common current paths, each H-bridge cannot operate independently. The voltage V_{pn} at input terminals of rectifier is observed as

$$V_{pn} = V_{pc} + V_{cn} \tag{17}$$

where voltages V_{pc} and V_{cn} are the terminal voltages of H-bridges with respect to their common point c. However, individual H-bridge yields three-level voltage waveform $(0, \pm V_{\rm dc})$ at their respective terminals. The rms voltage of each bridge is obtained as [22]

$$V_{\rm pc,rms} = 0.7797 \times V_{\rm pc,pk}, V_{\rm cn,rms} = 0.7797 \times V_{\rm cn,pk}. \tag{18}$$

Here, peak values of $V_{\rm pc,pk}$ and $V_{\rm cn,pk}$ are possibly reached to $V_{\rm dc}$. Although, these rms voltages decides the maximum power that can be delivered to loads R_a and R_b, respectively. The maximum power that individual H-bridge can generate is determined as

$$P_{A\,\max} = \frac{V_{\rm pc,rms}}{V_{\rm ac}} \times P, P_{B\,\max} = \frac{V_{\rm cn,rms}}{V_{\rm ac}} \times P \tag{19}$$

where $V_{\rm ac}$ is the input rms voltage and P is total power supplied by the rectifier. Since both the capacitors (C_1, C_2) are connected in parallel during the zero and $\pm V_{\rm dc}$ topological states, both the H-bridges operate together to generate required power for the loads. In such a circumstance, one of the load (either R_a or R_b) can be reduced to zero (disconnect from the rectifier), while other load can be increased to maximum power delivering capability of the rectifier. So

$$P_{R_a\,\min} = 0, P_{R_b\,\max} = P \tag{20}$$

and

$$P_{R_a\,\max} = P, P_{R_b\,\min} = 0. \tag{21}$$

Therefore, switching operations in the proposed rectifier will not permit H-bridges to operate independently, which helps to enhance the rectifier stability under unequal loading conditions. In addition, self-balancing capability of the rectifier maintains constant voltage at the load terminals. In contrast, BMBRs presented in the existing literature [22], [23], [24], [25], [26] suffer from instability because of unequal loading over the capacitors.

In Fig. 6, along with a system phasor diagram, the stability region and load scaling of the proposed and the existing HPUC

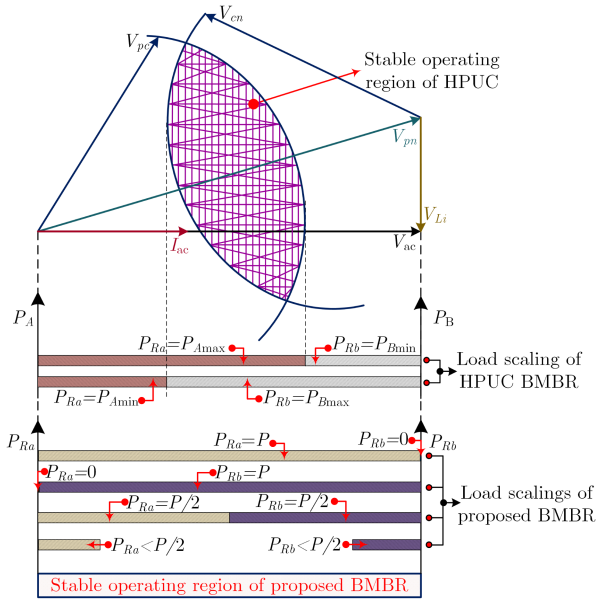

Fig. 6. Stability region and load scaling in HPUC and proposed BMBR.

BMBR are depicted. For HPUC BMBR to operate in stable region, both the capacitors must have predefined loading. If one H-bridge is loaded to its maximal power-delivering capability, the minimum load required for other H-bridges to take over in HPUC BMBR is calculated as

$$P_{A\min} = \frac{(V_{\rm ac} - V_{\rm cn,rms})}{V_{\rm ac}} \times P, P_{B\min} = \frac{(V_{\rm ac} - V_{\rm pc,rms})}{V_{\rm ac}} \times P. \tag{22}$$

From (19) and (22), it is noted that the HPUC BMBR has a confined load resistance ratio, which is given as

$$\frac{R_b}{R_a} = \frac{P_{A\,\max}}{P_{B\,\min}}. \tag{23}$$

Operation beyond this ratio could lead the HPUC BMBR in an unstable state. In addition, this ratio will differ based on the power and voltage ratings of the BMBR. Nonetheless, the proposed BMBR can operate above this confined load resistance ratio without compromising converter stability. Importantly, the proposed BMBR can also reliably supply a single load.

V. Performance Evaluation of the Proposed BMBR

The performance of the proposed BMBR has been verified through simulation and experimental methods. Further, both dynamic and steady-state performance are being assessed. Table III lists the rectifier parameters which are considered for simulation and hardware studies.

A. Hardware Results

The parameters given in Table III are used to conduct experimental tests on the prototype built in the laboratory. In Fig. 7, a snapshot of the hardware setup is shown. A proposed BMBR circuit is constructed using IRFP460 MOSFETs and TLP-250-based gate drivers. In conjunction with RT-Lab software, an OPAL-RT

TABLE III
INPUT AND DESIGN SPECIFICATIONS OF THE PROPOSED BMBR

Parameters	Specifications
Supply voltage	230 V , 50 Hz
Power rating	2 kW
Output voltages	200 V
Switching frequency	6.5 kHz
Input inductor (L_i)	4 mH
Capacitors (C_1, C_2)	2200 μF
Ripples in inductor current	25%
Ripples in output voltage	2%

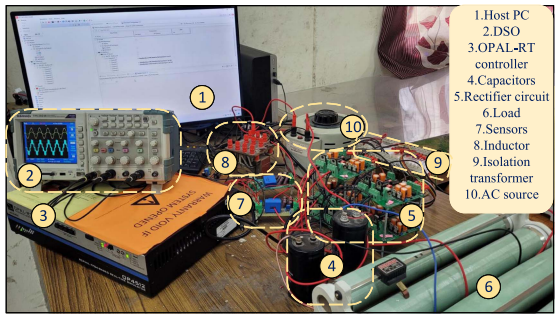

Fig. 7. Photo of experimental prototype.

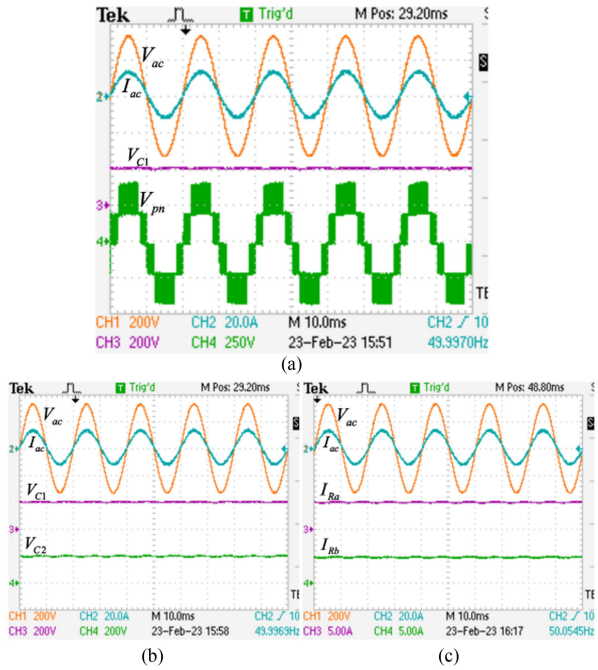

Fig. 8. Experimental results under steady-state and rated condition. (a) V_{ac}, I_{ac}, V_{C1}, V_{pn}. (b) V_{ac}, I_{ac}, V_{C1}, V_{C2}. (c) V_{ac}, I_{ac}, I_{Ra}, I_{Rb}.

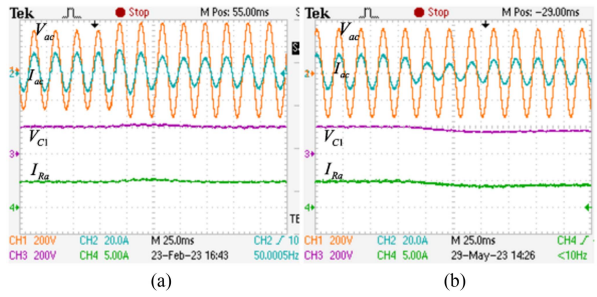

Fig. 9. Experimental results under dynamic conditions. (a) During input voltage change from 200 to 250 Vrms. (b) During output voltage change from 200 to 170 V.

OP4512 real-time controller has been used to generate the gate signals for the switches. An appropriate dead band (2 μs) is given between switching of the complementary switches to prevent short circuiting across the capacitors. An inductor of inductance 4 mH is used at input side, while two capacitors of capacitance 2200 μF are used at the output side of BMBR. However, the output voltage and power factor (PF) are regulated using two Hall effect-based voltage sensors (LEM LV25-P) and one current sensor (LEM LA 55-P).

The experimental results under steady-state and rated conditions are shown in Fig. 8(a)–(c). The input current (I_{ac}) is sinusoidal and in-phase with supply voltage V_{ac}, as shown in Fig. 8(a), while capacitor voltage V_{C1} has a constant magnitude of 200 V and BMBR terminal voltage (V_{pn}) of 5Ls with a 400-V peak value, thus demonstrating the bucking capability of proposed BMBR. Fig. 8(b) and (c) indicates capacitor voltages (V_{C1}, V_{C2}) and load currents (I_{Ra}, I_{Rb}) along with supply voltage and current at rated condition, respectively. However, capacitor voltages are maintained to fixed-voltage reference of 200 V and load resistances (Ra, Rb) of 40 Ω allow 5 A current pass through it. Further, the experimental results under dynamic conditions during input voltage change of 200–250 Vrms and output voltage change of 200–170 V are shown in Fig. 9(a) and (b), respectively. However, change in voltage reference (input/output) does not affect the nature of the current drawn by the BMBR and the output voltage is kept fixed even during input voltage change.

The load scalability of the proposed BMBR is verified in Fig. 10 while dynamic change in the load resistance of R_b. The waveforms of V_{ac}, I_{ac}, I_{Ra}, and I_{Rb} with fixed R_a of 40 Ω are shown in Fig. 10(a)–(c). When R_b is changed from 40 to 80 Ω, I_{Rb} reduced to 2.5 A, as shown in Fig. 10(a), while output voltage remains unaffected. If R_b is again increased to 400 Ω, I_{Rb} is decreased to value 0.5 A, and the results are shown in Fig. 10(b). In Fig. 10(c), I_{Rb} reduced to zero if R_b is disconnected from BMBR. Even capacitor voltages (V_{C1}, V_{C2}) also remain unaffected due to sudden changes in I_{Rb}, which is clearly indicated in Fig. 10(d). Remarkably, proposed BMBR has outstanding load scalability and stability, which has been validated through the results of Fig. 10(a)–(d). The results of Fig. 10 reveal that the supply current remains sinusoidal even when the loads are imbalanced. It implies that the power quality remains unaffected. In spite of this, switching devices are subject to different current stresses when loads are imbalanced. The experimental outcomes of Fig. 11(a) and (b) demonstrate that the proposed BMBR can operate at rated power with a single load. Without R_a, increasing the load R_b from 1500 to 2000 W has no effect on the capacitor voltages or the PFC operation of the rectifier. The proposed rectifier is also tested as an inverter to ensure its bidirectional functioning. The capacitor C_1 is replaced with a 200 V dc source, and by executing the switching states of Table I, the 5L voltage is obtained at the inverter output side. With the M of 0.8 and resistive load of 60 Ω, the capacitor

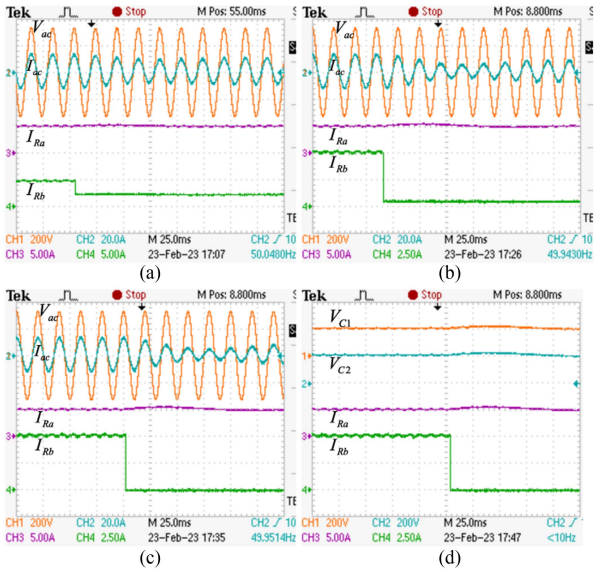

Fig. 10. Experimental results under dynamic conditions. (a) V_{ac}, I_{ac}, I_{Ra}, and I_{Rb} when load R_b reduced to half ($R_b/R_a = 2$). (b) V_{ac}, I_{ac}, I_{Ra}, and I_{Rb} when load R_b reduced to 10% ($R_b/R_a = 10$). (c) V_{ac}, I_{ac}, I_{Ra}, and I_{Rb} when R_b disconnected ($R_b/R_a = \infty$). (d) V_{C1}, V_{C2}, I_{Ra}, and I_{Rb} when R_b disconnected.

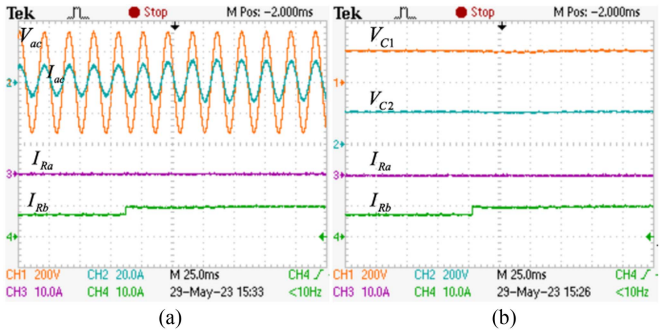

Fig. 11. Experimental results under dynamic conditions when R_a is disconnected and P_{R_b} increased from 1500 to 2000 W. (a) V_{ac}, I_{ac}, I_{Ra}, and I_{Rb}. (b) V_{C1}, V_{C2}, I_{Ra}, and I_{Rb}.

voltage (V_{C2}), 5L inverter output voltage (V_{pn}), voltage after the inductive filter, i.e., load voltage (V_{ac}), and load current (I_{ac}) are shown in Fig. 12(a). Further, the experimental results for the load change of 60 to 40 Ω are shown in Fig. 12(b).

B. Performance Analysis

The real semiconductor model has been used to simulate proposed BMBR switches using PLECS simulator for loss and thermal analysis. In addition, each inductor and capacitor of the rectifier are connected with the practical values of equivalent series resistance (ESR) of 15 and 20 mΩ, respectively. The cumulative losses in the rectifier are calculated as 70.84 W, of which 0.56 W are attributable to capacitors ESR losses and 1.31 W to inductor ESR loss. Meanwhile, the rectifier has an efficiency of 96.57% at full load and a peak efficiency of 97.73%. The efficiency curves of proposed and existing MLRs at different output power are shown in Fig. 13. At the rated load, Fig. 14 shows the power loss and junction temperature of each switching device. The heat sink module is placed over the switches for

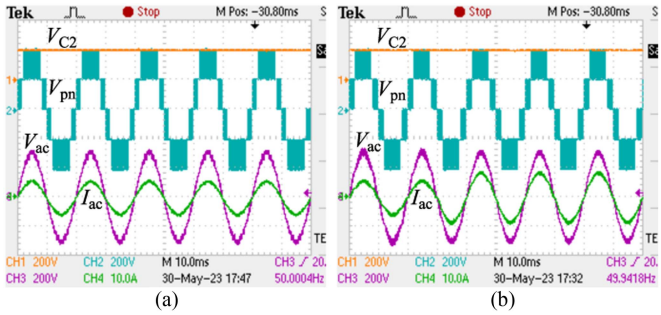

Fig. 12. Experimental results when proposed BMBR operates as an inverter. (a) V_{C2}, V_{pn}, V_{ac}, and I_{ac} for the restive load of 60 Ω. (b) V_{C2}, V_{pn}, V_{ac}, and I_{ac} for the change in load of 60 to 40 Ω.

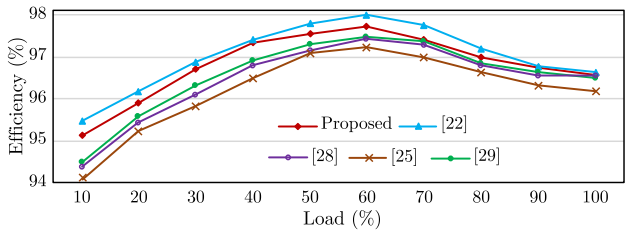

Fig. 13. Simulated efficiency of different MLR topologies.

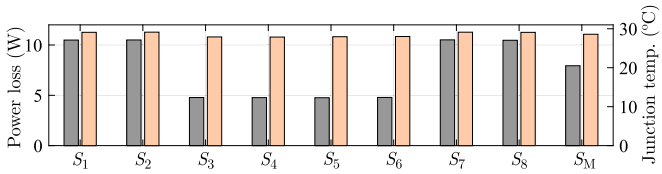

Fig. 14. Power losses and junction temperatures in the switching devices of proposed rectifier at rated load.

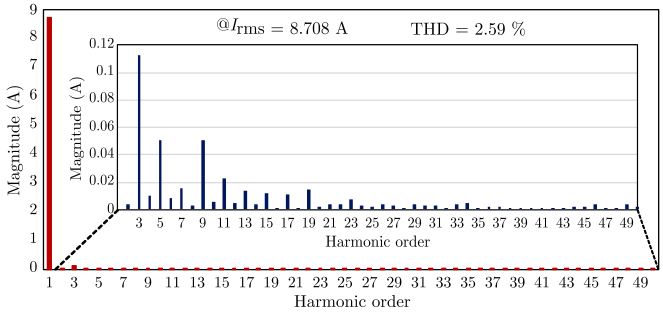

Fig. 15. Harmonic profile of the input current at rated load.

thermal assessment, and the junction temperature of each switch is computed based on the heat sink's ambient temperature of 25 °C.

Further, the experimental tests are conducted to measure power losses at different output power levels. The Yokogawa WT1804E power analyzer was used for power quality and efficiency analysis. Fig. 15 shows the harmonic profile of the input current, which is obtained through harmonic component with an order up to 50 at the rated load. The THD of input current is measured as 2.59% and the PF is achieved as 0.996. In addition, the peak efficiency of the proposed rectifier is 96.68%, and the full-load efficiency is measured as 95.77%. The efficiency curve

TABLE IV
COMPARATIVE ANALYSIS BETWEEN PREVAILING AND PROPOSED MULTILEVEL PFC RECTIFIERS

Parameters	[13]	[15]	[16]	[17]	[18]	[21]	[20]	[22]	[23]	[24]	[25]	[27]	[28]	[29]	Proposed
No. of switches (N_{SW})	2	3	3	4	3	6	2	6	6	6	8	10	10	10	9
No. of diodes (N_D)	4	8	6	6	8	2	7	0	0	0	0	0	0	0	0
No. of inductors (N_L)	1	2	1	1	1	2	1	1	1	1	1	1	1	1	1
No. of capacitors (N_C)	3	2	2	2	4	2	2	2	2	2	3	3	3	2	2
No. of voltage levels (N_{VL})	3	5	5	5	5	5	3	5	5	7	9	7	5	5	5
Input rms voltage (V_{ac}) (V)	220	220	120	220	127	115	220	120	230	120	120	230	230	230	230
Output voltage (V_{dc}) (V)	800	400	200	380	400	170	200	125	300	150/75	180/90	120	200	200	200
PIV ($\times V_{dc}$)	0.5	1	1	1	0.5	1	2	2	1.5	1.5	2	3	1	1	1
TSV ($\times V_{dc}$)	3	8.5	6.5	9	3.25	6	14	8	6	6	9	18	10	10	9
No. of voltage sensors (N_{VS})	2	2	2	2	2	2	2	3	1	3	4	2	2	2	2
No. of current sensors (N_{CS})	1	1	1	1	1	1	1	1	1	3	1	1	1	1	1
No. of outputs (N_O)	1	1	1	1	1	1	1	2	1	2	3	1	3	1	1/2
Operating mode	Boost	Boost	Boost	Boost	Boost	Boost	Buck	Buck	Buck	Buck	Buck	Buck	Buck	Buck	Buck
Bidirectional capability	No	No	No	No	No	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Load scalability	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	Yes	Yes	Yes
Measured efficiency (%)	97.06	98.3	-	98.6	95.13	96.2	96.5	-	94.3	-	-	-	-	-	96.68
Simulated efficiency (%)	-	-	97.34	-	-	-	-	98	-	-	97.1	-	97.5	97.5	97.73
THD (%)	2.6	3.7	1.3	2.18	5.6	1.4	4.6	3.1	2.25	1.6	3.21	NA	2.9	3.1	2.59
PF	UPF	UPF	UPF	0.99	UPF	0.99	UPF	0.989	UPF	UPF	UPF	UPF	0.996	0.99	0.996
Power rating (kW)	1	1	1.07	3	1	1	1	0.525	0.3	0.5	0.9	1	1	2	2
Switching frequency (kHz)	100	20	5	140	50	20	50	2	10	2.8	6	10	10	10	6.5

† NA: Not available. UPF: Unity power factor.

TABLE V
PRICE ANALOGY BETWEEN PROPOSED AND EXISTING MULTILEVEL PFC RECTIFIERS

Element	Details	Price/item (₹)	[22]	[24]	[25]	[27]	[28]	[29]	Proposed
MOSFET	IRFP21N60LPBF (600 V, 21 A)	362	724	724	724	1448	-	-	-
	IRFP460 (500 V, 20 A)	211	844	422	844	-	2110	2110	1899
	IRFP240PBF (200 V, 20 A)	116	-	232	232	696	-	-	-
Capacitor	VFL2G222YC109 (2200 μF, 400 V)	2319	4638	2319	2319	6957	6957	4638	4638
	LLG2D222MELC40 (2200 μF, 200 V)	452	-	452	904	-	-	-	-
Inductor	710-7448062105 (5 mH, 21 A, 10 kHz)	1750	1750	1750	1750	1750	1750	1750	1750
Gate driver circuit	TLP-250	300	1800	1800	2400	3000	3000	3000	2700
Voltage sensor	LEM LV 25-P	4521	13563	13563	18084	9042	9042	9042	9042
Current sensor	LEM LA 25-NP	1522	1522	4566	1522	1522	1522	1522	1522
		Total Cost (₹)	24841	25828	28779	24415	24381	22062	21551

Reference: digikey.com, mouser.in, element14.com, *Product price is subject to market demand.

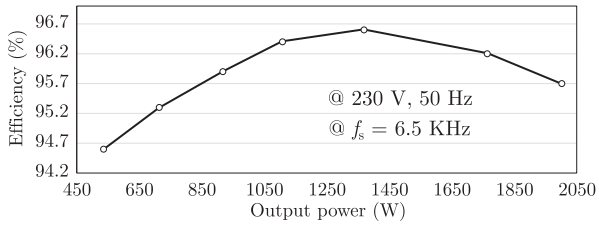

Fig. 16. Measured efficiency of the proposed BMBR at different output power.

is shown in Fig. 16. Thus, the proposed BMBR has improved the power quality performance.

C. Comparative Analysis

The proposed BMBR is compared against a variety of literature PFC MLRs in order to thoroughly assess its distinguished qualities. Table IV provides a comprehensive comparison of the various PFC MLRs. It can be observed that the proposed BMBR requires nine switches, whereas the MLRs of [15], [17], [18], [28] and [29] use more semiconductor devices to generate 5L voltage, indicating that the proposed BMBR is less expensive. Furthermore, the proposed BMBR requires no diodes, whereas the MLRs in [15], [16], [17], [18], [20] and [21] require additional diodes for the same levels. The PIV and total standing voltage (TSV) in the MLRs are determined from its output voltage. All the switches of proposed BMBR have equal PIV of 200 V, whereas the switches in the MLRs of [13], [15], [17], [20], [22], [23], [24], [25] and [27] have higher PIVs. Also, TSV is comparatively lesser than MLRs of [13], [15], [17], [20], [27], [28] and [29]. MLR of [22], [24], and [25] requires more voltage sensors for capacitor voltage balancing, whereas the proposed BMBR needs only one for output voltage regulation due to its self-balancing capability. Although the proposed BMBR can offer either one or two outputs, but the MLRs in [22], [23], [24], and [25] do not have this option. Similar to other BMLRs, the proposed BMBR has a reduced static voltage gain of 0.5 and can operate in buck mode. However, UMLRs only perform the boost operation and have higher voltage gain. Most importantly, in contrast to all MLRs, the proposed BMBR offers stable operation and have wide range of load scaling. In addition, efficiency of the proposed rectifier is higher than MLRs presented in [18], [20], [21], [23], [25], [28], and [29]. Moreover, THD of input current in the proposed topology is lesser than the MLRs of [15], [18], [20], [22], [25], [28], and [29]. Besides that, the power rating and operating switching frequency of all MLRs are also given in Table IV.

It is obvious that, only component count comparison is inadequate to analyze MLRs unique merits. Hence, a detailed cost analysis is required to evaluate and thereby verify the merits of the MLRs. Specifications given in Table III have been used as a case study to demonstrate the economic benefits of the proposed BMBR. Table V describes the general ratings of the components considered for cost analysis of BMBRs. It should be noted that the proposed BMBR has less cost than others because it employs low voltage rating MOSFETs and only requires two voltage sensors. Hence, the requirement of low voltage rated switches, capacitors, voltage sensors, and current sensors in the proposed BMBR has a substantial impact on its lesser pricing.

Notably, similar to BMLRs of [21], [22], [23], [24], [25], [26], [27], [28], and [29], the solid connection between source and loads is not possible in the proposed topology, which might generate common mode noise and introduce EMI in the system. Hence, suitable modulation technique or modifications in the proposed topology is required to overcome these issues.

VI. Conclusion

In this article, a PFC BMBR with its distinct features of load scalability and stability has been proposed. The topological switching states of the proposed rectifier auto-balances the capacitor voltages and hence reduces the requirement of additional output voltage sensor. The proposed BMBR has been controlled using a conventional level-shifted-based PWM strategy rather than a complex control for other BMBRs. In addition, proposed BMBR offers an option of flexible loading's (single/double). The extensive component- and cost-based comparison has confirmed the supremacy of the proposed BMBR in contrast to other existing MLRs for a PFC applications. The load scalability and stability of proposed rectifier has been analyzed and further verified through experimental outcomes.

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