# An Asymmetrical Active-Neutral-Point-Clamped Five-Level H-bridge Inverter for Open-Winding Motor Applications With Its Modulation Strategy

Kefeng Li, Fei Xiao, Jilong Liu, Zhiqin Mai, and Zhuangzhi Dai

***Abstract*—Asymmetrical active-neutral-point-clamped five-level H-bridge (ANPC5L-HB) inverter has reduced switch count and fewer high-frequency switches compared with other existing five-level H-bridge topologies. However, multiphase ANPC5L-HB inverter for open-winding motor applications is rarely researched. In this article, a three-phase ANPC5L-HB inverter for open-winding motor applications is proposed. The modulation and neutral point (NP) voltage balance strategies for the inverter are also proposed. By using the proposed modulation strategy, transitions between different switching states are constrained to avoid unexpected intermediate states. Meanwhile, zero voltage switching (ZVS) of low-frequency switches could be achieved. For the NP voltage balance problem, optimal switching states are selected by using the MPC approach, and a better NP control performance is realized compared with the classical method. The effectiveness and high efficiency of the inverter are validated by a 25-kW experimental prototype. And a peak efficiency of 98.685% is confirmed under 10 kHz switching frequency. The good performances of the proposed strategies have been fully verified.**

***Index Terms*—Asymmetrical active neutral point clamped (ANPC) inverter, H-bridge, model predictive control (MPC), open-winding motor, pulse width modulation (PWM).**

## I. Introduction

MULTILEVEL inverters (MLIs) have experienced fast-growing attention in the last decade due to their superior characteristics like high voltage capability, lower total harmonic distortion, reduced switching stress and smaller filter size compared with conventional inverters [1], [2], [3], [4]. In open-winding motor drive applications, MLI systems have also been recently developed. And it has been applied as a solution for electric vehicles, ship electric propulsion, etc. Among various MLI topologies, cascaded H-bridge (CHB), modular multilevel converter (MMC), neutral-point-clamped (NPC), and floating capacitor (FC) are four classical and basic MLI topologies that are widely used in the industry [5], [6].

Due to their special structures, MLIs with isolated dc sources, such as CHB and its derived topologies, may not suitable for open-winding drive systems which are based on medium-voltage dc (MVDC) configuration or require high power density and flexibility, such as electric vehicles and ship electric propulsion systems [7], [8], [9]. Compared with MLIs with isolated dc sources, MLIs with a common dc bus have simple structure, reduced size, and weight, which is promising for improving the power density, efficiency, and harmonic performance at the same time [10], [11]. And it has been widely adopted due to their superior characteristics [8], [12].

Among MLIs with a common dc bus, MMC configuration allows it to be expanded to any number of voltage levels and different power ratings by employing only one dc bus and components with the same voltage and current rating [7]. However, the large component count and the large fluctuation of capacitor voltage especially in low-frequency conditions are two main limitations of MMC. NPC H-bridge (NPN-HB), FC H-Bridge (FC-HB), and ANPC H-Bridge (ANPC-HB) are all promising symmetrical MLI topologies in open-winding drive applications [13], [14], [15], [16]. More voltage levels could be obtained by feeding an H-bridge arm at both ends of a phase winding of the open-winding motor. However, in this kind of symmetrical H-bridge topology, a large number of switches is needed. And their efficiency is expected to be further improved [17]. By focusing on efficiency and better performance, multilevel H-bridge inverter with reduced switch count and enhanced functionality has become a heated topic, and a concept of asymmetrical H-bridge MLI is proposed [8], [17].

Asymmetrical MLIs have been recently investigated due to the reduced number of switches [18], [19]. In asymmetrical five-level (5L) topologies, the H-bridge usually consists of a three-level (3L) arm and a two-level (2L) arm. Two asymmetrical NPC-based 5L topologies were proposed in [20], [21], and [22]. Two asymmetrical ANPC-based (A-ANPC) 5L topologies introduced in [23], [24] and [17], [25] are shown in Fig. 1(a) and (b), respectively. Because the ANPC arm has more active switches, more switching states could be obtained to balance the loss distribution [26], [27], [28], [29], [30]. In Fig. 1(a), eight switches are utilized to produce a five-level output voltage, where six switches operate at the switching frequency [23]. In

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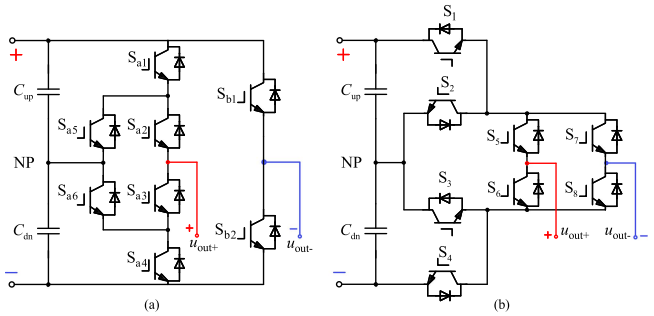


Fig. 1. Asymmetrical ANPC-based 5L topologies. (a) A-ANPC topology proposed in [23]. (b) ANPC5L-HB topology proposed in [17], [25].

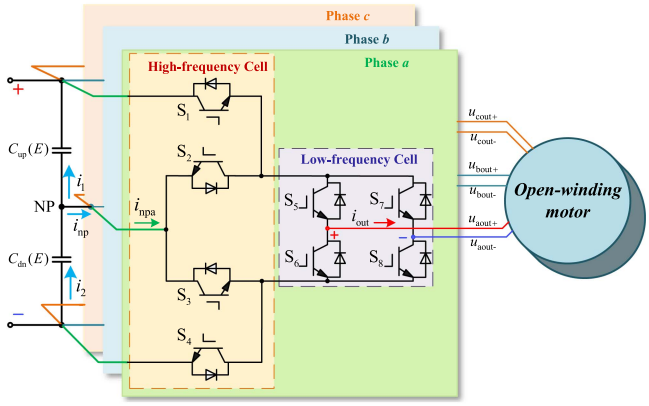


Fig. 2. Topology of the three-phase ANPC5L-HB inverter.

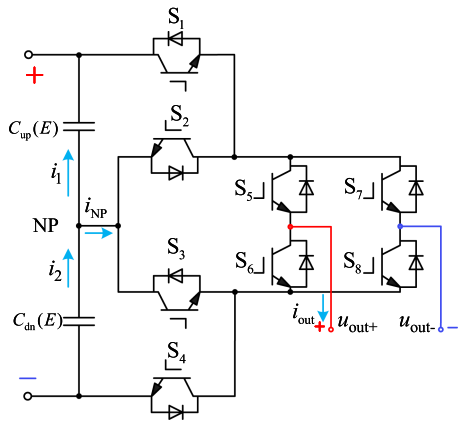

Fig. 3. Topology of a single-phase ANPC5L-HB arm.

Fig. 1(b), only four switches operate at the switching frequency [17], [25]. So, the ANPC5L-HB topology has a reduced switch count and fewer high-switching switches compared with the other abovementioned topologies. Besides, it has high control flexibility on the neutral point (NP) voltage and could operate at a hybrid switching frequency [17], [31].

In [17], a single-phase ANPC5L-HB topology was studied. By utilizing two different switch technologies (Si and SiC MOSFET) and a hybrid modulation strategy, the advantages of the inverter could be highlighted [17], [31]. However, the study of this topology is still limited to the single-phase structure, and its application scenario almost stays in photovoltaic [32]. When the single-phase ANPC5L-HB topology is expanded to multiphase topology and meets the needs of the open-winding motor drive applications, a promising multiphase ANPC5L-HB inverter could be generated.

In the multiphase ANPC5L-HB inverter, all the arm cells are fed by a common dc bus. The number of switching states increases exponentially, and the NP voltage is affected by each ANPC5L-HB arm. So, the fluctuation property of the NP voltage is different from that of the single-phase inverter. The multiphase ANPC5L-HB inverter inherits superior characteristics of its single-phase structure, and it is suitable for systems with a common dc bus. To further explore its performance in open-winding drive applications, modulation and NP voltage balance strategies should be carefully designed to ensure a good performance for the multiphase ANPC5L-HB inverter.

Based on the above research, a three-phase ANPC5L-HB inverter for open-winding motor drive applications is proposed in this article. IGBTs are adopted as switches. First, the operating principle and the characteristic of the inverter are analyzed. Then, a single-carrier-based PWM strategy for the three-phase ANPC5L-HB inverter is proposed. In the proposed PWM strategy, a transition rule of switching states is introduced to avoid unexpected intermediate switching states (parasitic states) and realize the ZVS of low-frequency switches. Pulse patterns are symmetrically distributed in a carrier cycle, which ensures a good output harmonic performance. Based on the proposed PWM strategy, an effective NP voltage balance strategy is proposed. Proper switching states are selected through the model predictive control (MPC) method, which shows a good control performance on the NP voltage. In this article, experiments with $RL$ load and open-winding motor drive are conducted to verify the effectiveness of the topology and the proposed strategies.

The rest of this article is organized as follows. The working principle and characteristics of the three-phase ANPC5L-HB inverter are introduced in Section II. The proposed PWM and NP voltage balance strategies for the three-phase ANPC5L-HB inverter are illustrated in Section III. The experimental verification is presented in Section IV. Finally, Section V concludes the article.

## II. Operating Principle and Characteristics of the ANPC5L-HB Topology

### A. Operating Principle

The topology of the three-phase ANPC5L-HB inverter is shown in Fig. 2. The inverter consists of three ANPC5L-HB arms, and each arm shares a common dc bus. $C_{\rm up}$ and $C_{\rm dn}$ are the upper and lower dc-link capacitors, respectively. NP represents the neutral point of the dc bus. Each H-bridge arm has eight IGBTs and two output ports, $u_{\rm out+}$ and $u_{\rm out-}$. Five voltage levels could be generated between the two ports.

To illustrate clearly, a single-phase ANPC5L-HB arm is shown in Fig. 3. In Fig. 3, $i_1$ and $i_2$ represent the current of $C_{\rm up}$, $C_{\rm dn}$, respectively. $i_{\rm out}$ represent the output current. Assuming

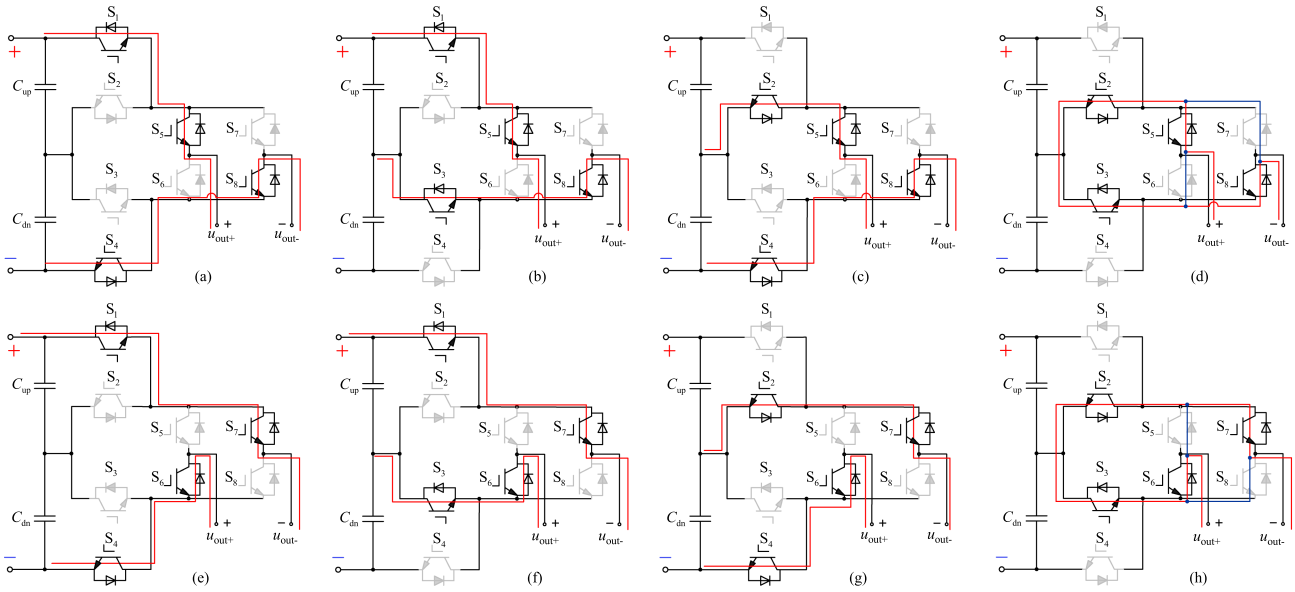


Fig. 4. Eight switching states of an ANPC5L-HB arm with current paths. (a) 2E. (b) EP. (c) EN. (d) OP. (e) –2E. (f) –EP. (g) –EN. (h) ON.

TABLE I
SWITCHING STATES OF A SINGLE-PHASE ANPC5L-HB ARM

| Switching state of switches | | | | | | | | $u_{\mathrm{out}}$ | $i_{\mathrm{np}}$ | $S$ |
|---|---|---|---|---|---|---|---|---|---|---|
| $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | | | |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | $2E$ | 0 | 2E |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | $E$ | $-i_{\mathrm{out}}$ | EP |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | $E$ | $i_{\mathrm{out}}$ | EN |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | OP |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | ON |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | $-E$ | $i_{\mathrm{out}}$ | –EP |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | $-E$ | $-i_{\mathrm{out}}$ | –EN |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | $-2E$ | 0 | –2E |

that the dc-link voltage is $2E$, the dc-link capacitors voltage should be controlled at $E$. If NP is referred as the zero potential, each phase can output five voltage levels ($2E$, $E$, 0, $-E$, $-2E$). Among the switches $S_1$∼$S_8$, $S_1$ and $S_2$ are complimentary, so do $S_3$ and $S_4$, $S_5$ and $S_6$, $S_7$ and $S_8$. Meanwhile, the switching states of $S_5$ and $S_7$ are consistent. So, only three independent control signals are needed in each phase, the switching states are summarized in Table I.

In Table I, 1 and 0 indicate the ON and OFF states of the switches, respectively. $u_{\mathrm{out}}$ represents the voltage between $u_{\mathrm{out}+}$ and $u_{\mathrm{out}-}$. $S$ represents the name of switching states. It could be concluded that switches $S_5$∼$S_8$ operate at the fundamental frequency, called low-frequency switches. $S_1$∼$S_4$ are called high-frequency switches. So, only half of the switches operate at the switching frequency and mainly bear the switching losses. Different switching states with the same output voltage level are called redundant states. Due to the redundant states having opposite effects on $i_{\mathrm{np}}$, NP voltage could be balanced by selecting different redundant states. It can be seen from Fig. 4 that the voltage stress of $S_1$∼$S_4$ is $U_{\mathrm{dc}}/2$ and the voltage stress of $S_5$∼$S_8$ is $U_{\mathrm{dc}}$ when the inverter operates normally. $U_{\mathrm{dc}}$ represents the dc-link voltage.

### B. Characteristic of the ANPC5L-HB Topology

To analyze the property of the ANPC5L-HB topology, a few 5L H-bridge topologies including the symmetrical ANPC (S-ANPC) topology in [15], the asymmetrical NPC-based (A-NPC) topology in [22] and the asymmetrical ANPC-based (A-ANPC) topology in [23] and [24] are selected as comparison objectives. The above topologies are depicted in Fig. 5. The switch count, switching frequency, and voltage stress among the above topologies are compared and listed in Table II.

It can be seen from Table II, the symmetrical topology has more switches compared with asymmetrical topologies. In terms of the switching frequency, all switches in the A-NPC topology operate at a high frequency. In the A-ANPC topology, by using the strategy in [23] and [30], the number of high-frequency switches is reduced compared with A-NPC topology, half of the switches operate at two times the fundamental frequency ($2f_{\mathrm{l}}$). By using strategies in [23], the conduction loss of the A-ANPC arm is optimized. However, the equivalent switching frequency is increased.

Based on the above analysis, the advantages of the ANPC5L-HB topology could be summarized as follows. It has fewer switches compared with the other H-bridge MLI topologies. Meanwhile, only four switches operate at $f_{\mathrm{h}}$ for every half cycle, the other switches operate at the fundamental frequency and could achieve ZVS by using the proposed modulation strategy. Thus, a higher efficiency could be achieved. Besides, it has high control flexibility on the neutral point (NP) voltage, which could ensure voltage integrity and operation stability. A limitation of

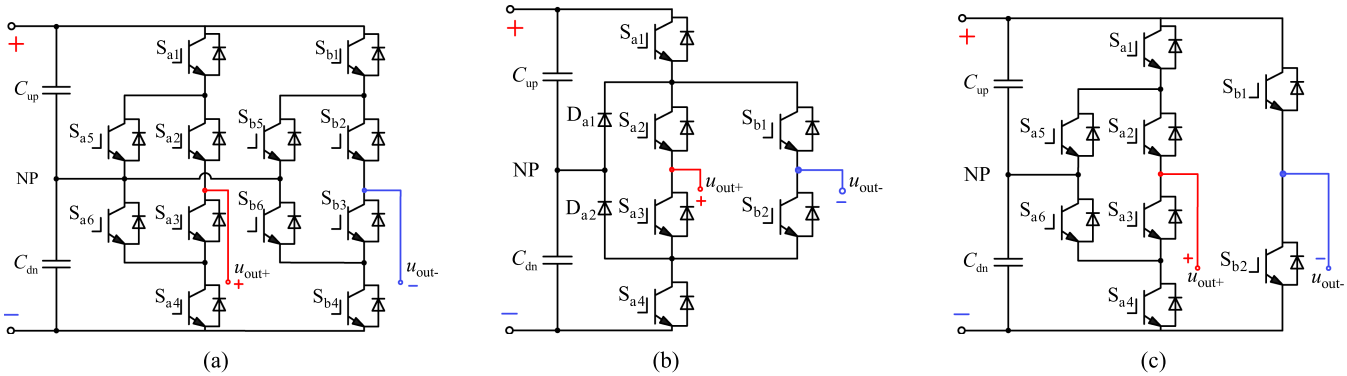


Fig. 5. Three existing 5L H-bridge topologies used for comparison. (a) S-ANPC topology. (b) A-NPC topology. (c) A-ANPC topology.

TABLE II
COMPARISON OF THE SWITCH COUNT, VOLTAGE STRESS, AND SWITCHING FREQUENCY OF FOUR 5L H-BRIDGE TOPOLOGIES

| Topology | Switch count | | Switches under different switching frequencies | | | Voltage stress | | Reference |
|---|---|---|---|---|---|---|---|---|
| | Active switch | Diode | $f_h$ | $f_l$ | Other frequency | $U_{dc}/2$ | $U_{dc}$ | |
| S-ANPC | 12 | – | 4 | 8 | 0 | 12 | 0 | [15] |
| A-NPC | 6 | 2 | 4 and 4(for half cycle) | 0 | 0 | 4 | 4 | [22] |
| A-ANPC | 8 | – | 2 | 2 | 4 ($2f_l$) | 6 | 2 | [30] |
| | | | 4 (for half cycle) | 2 | 2 ($2f_h$) | | | [23] |
| ANPC5L-HB | 8 | – | 4 (for half cycle) | 4 | 0 | 4 | 4 | Studied |

the topology is that the voltage stress of four low-frequency switches is the dc-link voltage.

## III. PROPOSED MODULATION AND NP VOLTAGE BALANCE STRATEGIES FOR THE THREE-PHASE ANPC5L-HB INVERTER

When the ANPC5L-HB topology is expanded to three-phase, a three-phase ANPC5L-HB inverter which is suitable for open-winding drive applications could be obtained. Three-phase ANPC5L-HB inverter inherits the superior characteristics of its single-phase structure, and it is suitable for systems with a common dc bus. Besides, the three-phase ANPC5L-HB inverter has a better self-balance ability on NP voltage because of the symmetry of the three phases.

The topology of the three-phase ANPC5L-HB is shown again in Fig. 6. In the three-phase ANPC5L-HB inverter, the number of switching states increases to $8^3 = 512$, which is much higher than that of the single-phase inverter. Meanwhile, the NP voltage is affected by three ANPC5L-HB arms. So, the ripple property of the NP voltage is different from that of the single-phase inverter.

### A. Neutral-Point Voltage Fluctuation Analysis

In this part, the NP voltage fluctuations of the ANPC5L-HB inverter are analyzed in two time-scales: 1) carrier period; and 2) fundamental period. The fluctuation at the fundamental period

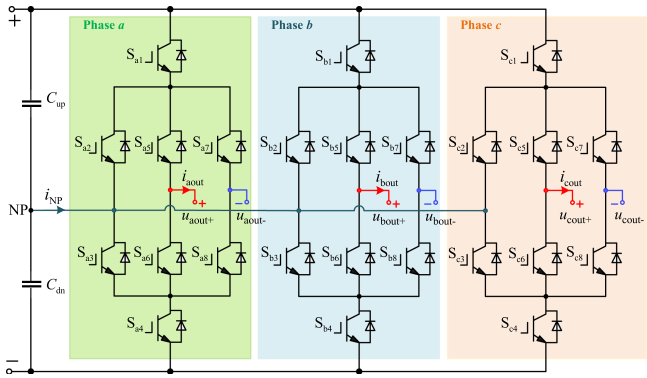


Fig. 6. Topology of the three-phase ANPC5L-HB inverter.

represents the worst working conditions and is used to guide the design of the dc-link capacitor.

*1) NP Voltage Ripple in a Carrier Period:* According to Table I, proper redundant switching states could be selected to balance the NP voltage. So, in a carrier period, the NP voltage ripple of the single-phase and the three-phase ANPC5L-HB inverter, $\Delta v_{\mathrm{CdcSp}}$ and $\Delta v_{\mathrm{CdcTp}}$, could be derived as (1) and (2), respectively. It could be concluded that the ripples are proportional to the carrier period $T_s$ and inversely proportional to the dc-link capacitance $C_{dc}$. For the three-phase inverter, the NP voltage balance may be more complex because it is influenced

by all H-bridge arms.

$$\Delta v_{\mathrm{CdcSp}} = \frac{i_{\mathrm{NP}} \cdot T_{\mathrm{s}}}{2C_{\mathrm{dc}}} \leq \frac{i_{\mathrm{out}} \cdot T_{\mathrm{s}}}{2C_{\mathrm{dc}}} \tag{1}$$

$$\Delta v_{\mathrm{CdcTp}} = \frac{(i_{\mathrm{NPa}} + i_{\mathrm{NPb}} + i_{\mathrm{NPc}}) \cdot T_{\mathrm{s}}}{2C_{\mathrm{dc}}} \leq \frac{(|i_{\mathrm{outa}}| + |i_{\mathrm{outb}}| + |i_{\mathrm{outc}}|) \cdot T_{\mathrm{s}}}{2C_{\mathrm{dc}}}. \tag{2}$$

*2) Maximum NP Voltage Fluctuation at the Fundamental Period:* The design of $C_{\mathrm{dc}}$ determines the NP voltage fluctuation, and the worst working condition should be taken into consideration. In this case, no closed-loop NP voltage control is applied, the NP voltage is balanced by the inverter itself and would fluctuate at the fundamental frequency. So, an analysis is conducted to give guidance on the design of dc-link capacitor. Assuming that the output power is applied from $C_{\mathrm{up}}$ when the output voltage is $E$, and is applied from $C_{\mathrm{dn}}$ when the output voltage is $-E$, the NP voltage fluctuation of the single-phase and the three-phase ANPC5L-HB inverter could be derived as (3) and (4), respectively, according to the method in [33].

$$\Delta v'_{\mathrm{CdcSp}} = k \cdot \frac{V_{\mathrm{m}} I_{\mathrm{m}}}{2\omega C_{\mathrm{dc}} V_{\mathrm{dc}}} \cdot \pi \tag{3}$$

$$\Delta v'_{\mathrm{CdcTp}} = k \cdot \frac{V_{\mathrm{m}} I_{\mathrm{m}}}{2\omega C_{\mathrm{dc}} V_{\mathrm{dc}}} \left(\sqrt{3} - \frac{\pi}{3}\right) \tag{4}$$

$$k = \begin{cases} 1 & m \in (0, 0.5] \\ \frac{2}{\pi}(\pi - \theta_1 - 2m\cos\theta_1) & m \in (0.5, 1). \end{cases} \tag{5}$$

In the above equations, $\theta_1 = \sin^{-1}(\frac{1}{2m})$. $V_m$, $I_m$ are the amplitudes of the output voltage, output current, respectively. $\omega$ is the angular frequency. $k$ represents the duty cycle of the voltage level $E$ (or $-E$) among the non-zero voltage over half a fundamental period. $m$ represents the modulation index.

Evidently, the voltage fluctuation in (4) is smaller than that in (3) under the same working condition. It could be concluded that if no closed-loop NP voltage control is applied, the three-phase topology has a better self-balance ability on the NP voltage because of the symmetry of the three phases. The dc-link capacitance could be designed according to (4), where $\omega$ is usually set to the rated frequency.

### B. Proposed Modulation Strategy

*1) Transition Rules of Switching States:* Switching states of each ANPC5L-HB arm should follow a few principles. On the one hand, the output voltage should be varied between adjacent levels to ensure a good output harmonic performance. On the other hand, parasitic states should not be generated during the deadtime. Meanwhile, switches $S_5$~$S_8$ should operate at the fundamental frequency to reduce the switching losses.

Based on the above principle, the transition diagram of eight switching states is depicted in Fig. 7. Among the diagram, if switching states EP and EN are switched between each other, parasitic states would be generated. So, the transition path between EP and EN is forbidden to avoid the parasitic states. In this case, only switches $S_5$ and $S_8$ are on. The parasitic states produced during the dead time are depicted in Fig. 7. If the output current $i_{\mathrm{out}}$ is positive, the parasitic state is OP. If $i_{\mathrm{out}}$ is negative, the parasitic state is 2E. The transition between –EP and –EN is similar to the above analysis, so it would not be analyzed in detail.

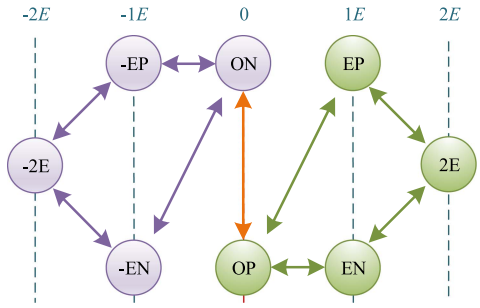


Fig. 7. Transition diagram of switching states for an ANPC5L-HB arm.

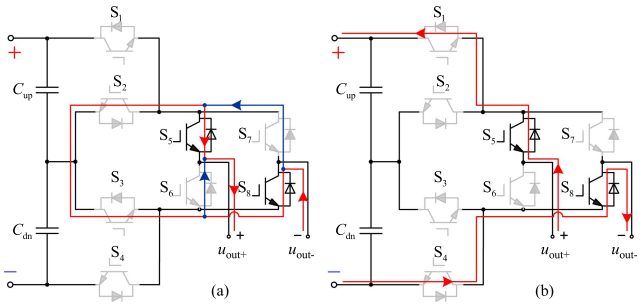


Fig. 8. Parasitic states produced by the transition between EP and EN. (a) When $i_{\mathrm{out}}$ is positive. (b) When $i_{\mathrm{out}}$ is negative. (a) OP. (b) 2E.

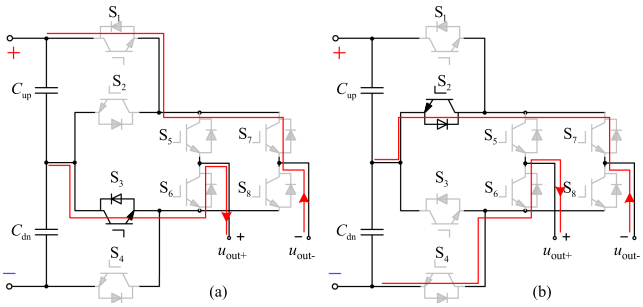


Fig. 9. Current paths in the two parasitic states. (a) Produced by the transition between ON and EP. (b) Produced by the transition between ON and EN. (a) -EP. (b) -EN.

To ensure switches $S_5$~$S_8$ operate at the fundamental frequency, the switching state ON is selected when the reference voltage is negative. Otherwise, OP is selected. In Fig. 8, the transition between ON and EP, OP and EN is forbidden to avoid extra switching loss and parasitic states. If the state is transited between ON and EP, only $S_3$ is switched-ON during the dead time. If $i_{\mathrm{out}}$ is positive, parasitic state –EP is generated. If the state is transited between ON and EN, only $S_2$ is switched-ON during the dead time. If $i_{\mathrm{out}}$ is positive, parasitic state –EN is generated. The current paths of the above two conditions are depicted in Fig. 9.

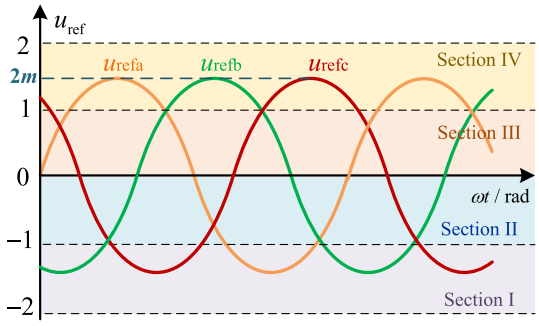


Fig. 10. Reference voltage waveforms of three-phase ANPC5L-HB inverter.

TABLE III
MODULATION PRINCIPLE OF THE PROPOSED STRATEGY

| Section | $u_{\mathrm{ref}}$ | $C_{\mathrm{mp}}$ | Switching states | |
|---|---|---|---|---|
| | | | $u_{\mathrm{c}} < C_{\mathrm{mp}}$ | $u_{\mathrm{c}} > C_{\mathrm{mp}}$ |
| I | [–2, –1] | $-(1+u_{\mathrm{ref}})$ | –2E | –EP or –EN |
| II | (–1, 0] | $-u_{\mathrm{ref}}$ | –EP or –EN | 0 |
| III | (0, 1] | $1-u_{\mathrm{ref}}$ | 0 | EP or EN |
| IV | (1, 2] | $2-u_{\mathrm{ref}}$ | EP or EN | 2E |

*2) Voltage Vector Synthesis and Pulse Generation:* In the three-phase ANPC5L-HB inverter, there is no common connection between loads in each phase, and the output voltages of each phase are relatively independent. The three-phase reference voltage could be defined as (6). $m \in (0,1)$ represents the modulation index.

$$\begin{cases} u_{\mathrm{refa}} = 2m \cdot \sin(\omega t) \\ u_{\mathrm{refb}} = 2m \cdot \sin(\omega t - \frac{2}{3}\pi) \\ u_{\mathrm{refc}} = 2m \cdot \sin(\omega t + \frac{2}{3}\pi). \end{cases} \tag{6}$$

Each ANPC5L-HB arm has five output voltage levels (–2$E$, –$E$, 0, $E$, 2$E$). Assuming that the output voltage only varies between adjacent levels, the reference signal could be divided into four sections, shown in Fig. 10. The reference signal contains two kinds of information. The integer part represents the variation range of the output voltage, and the difference between the reference signal and the lower limit of the interval represents the duty cycle of the high voltage level in the specific section.

For each phase, the modulation principle of the proposed strategy is summarized in Table III. $u_{\mathrm{c}}$ represents the triangular carrier signal, which range is [0,1]. As can be seen from Table III, in the four sections below, when the carrier signal is smaller than the compared value $C_{\mathrm{mp}}$, the low voltage level in this section is output. When the carrier signal is larger than $C_{\mathrm{mp}}$, the high voltage level is output. When the output voltage level is $E$ or $-E$, switching states should be selected from the two alternatives according to the NP voltage balance method.

Output voltage sequences in a switching period are depicted in Fig. 11. By using the proposed strategy, only one triangular carrier signal is needed to make a comparison with the specific reference signal, and output the corresponding switching state.

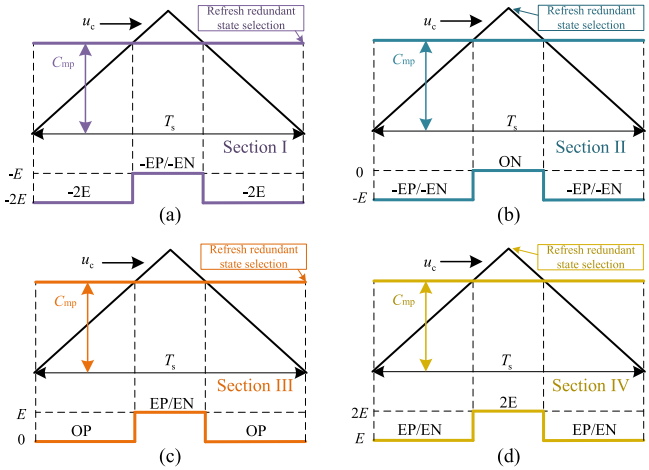


Fig. 11. Voltage sequences in a switching period. (a) Section I. (b) Section II. (c) Section III. (d) Section IV.

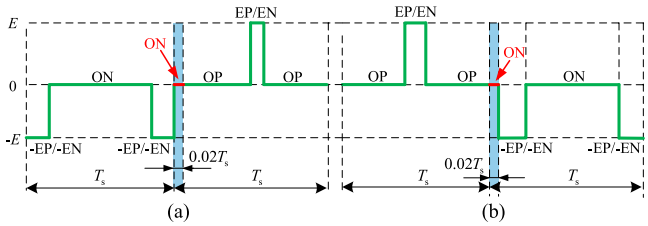


Fig. 12. Switching sequences when $u_{\mathrm{ref}}$ crosses zero. (a) From negative to positive. (b) From positive to negative.

In each section, the refresh time of the redundant state should be constrained to ensure the transition rules in Fig. 7 are followed. In Fig. 11(a) and (c), the selection of redundant states should be refreshed at the bottom of the carrier signal (at the end of the switching period). In Fig. 11(b) and (d), the selection of redundant states should be refreshed at the top of the carrier signal (in the middle of the switching period). In this way, the transitions between EP and EN, –EP and –EN are avoided. So, the parasitic states could be avoided.

*3) Switching Sequences Design During the Zero-Crossing Process:* The switching sequences when the output voltage crosses zero should be treated specially. When the output voltage is positive over zero, the switching state should be switched to ON, then the normal switching sequence could be carried out. When the output voltage is reversed over zero, the switching state should be switched from OP to ON, then the normal switching sequence could be carried out. The switching sequences during the process are shown in Fig. 12. To ensure the inserted state (ON) has less influence on the output voltage, the duration time of the state should be short as possible. It is controlled at $0.02T_{\mathrm{s}}$ manually in our application.

By using the abovementioned switching sequences, switching states only could be switched between OP and ON when $u_{\mathrm{ref}}$ crosses zero. The current paths during the dead time are depicted in Fig. 13. As can be seen from Fig. 13, due to the output voltage being zero in the above two states, whether switches $S_5 \sim S_8$ is

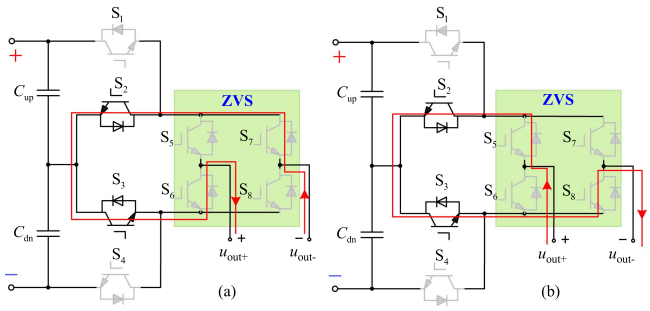


Fig. 13. Current paths during the dead time when switching state is transited between OP and ON. (a) When $i_{\rm out}$ is positive. (b) When $i_{\rm out}$ is negative.

ON or OFF, of which the voltage is zero. So, ZVS for $S_5$~$S_8$ could be realized. It could be approximated that the loss on the low-frequency switches is only conduction loss, which could further improve the efficiency of the inverter.

### C. NP Voltage Balance Strategy

Due to several ANPC5L-HB arm cells sharing a common dc bus, each arm cell has an influence on the NP voltage. So, the NP voltage control for the three-phase ANPC5L-HB inverter is more complicated compared with the single-phase structure. Based on the proposed modulation strategy, an NP voltage balance method based on the MPC approach is proposed.

*1) Fluctuation Model of Neutral Point Voltage:* Assuming that the dc-link voltage $U_{\rm dc}$ keeps constant, the current through NP $i_{\rm NP}$ could be expressed as (7). $i_1$ and $i_2$ are the current of the dc-link capacitor $C_{\rm up}$ and $C_{\rm dn}$, respectively, where $U_{\rm up}$ and $U_{\rm dn}$ are the voltage of the dc-link capacitor $C_{\rm up}$ and $C_{\rm dn}$, respectively.

$$i_{\rm NP} = i_2 - i_1 = -C_{\rm dn}\frac{dU_{\rm dn}}{dt} + C_{\rm up}\frac{dU_{\rm up}}{dt} = -2C_{\rm dn}\frac{dU_{\rm dn}}{dt}. \tag{7}$$

Assuming that the current in a switching period remains constant, (7) could be discretized in a switching period to obtain the variation of dc-link capacitors, shown in (8).

$$\Delta U_{\rm dn} = -\frac{i_{\rm NP}\cdot\Delta t}{2C_{\rm dn}}. \tag{8}$$

In the three-phase ANPC5L-HB inverter, $i_{\rm NP}$ could be decomposed into the sum of the components in each phase. So, (8) could be written as (9). Where $d_{\rm a}$, $d_{\rm b}$, and $d_{\rm c}$ represent the duty cycles of switching states $E$ or $-E$.

$$\Delta U_{\rm dn} = -\frac{(d_a i_{{\rm NP}a} + d_b i_{{\rm NP}b} + d_c i_{{\rm NP}c})T_{\rm s}}{2C_{\rm dn}}. \tag{9}$$

*2) Classical NP Voltage Balance Method:* According to Table I in Section II, the redundant state which could produce the required polarity of $i_{\rm NP}$ should be selected. By sampling the NP voltage and output current, the corresponding switching states could be selected. Define the NP voltage as half of the difference between $U_{\rm up}$ and $U_{\rm dn}$, shown in (10). The principle of the classical NP voltage balance method is shown in Fig. 14.

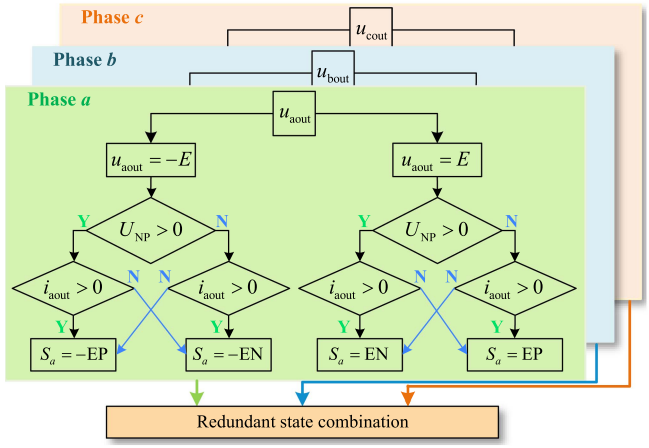


Fig. 14. Flowchart of the classical NP voltage balance method.

$$U_{\rm NP} = \frac{1}{2}\cdot(U_{\rm dn} - U_{\rm up}). \tag{10}$$

When the redundant states of the three-phase ANPC5L-HB inverter are all selected according to Fig. 14, $i_{\rm NP}$ could be expressed by the sum of the product of the absolute output current values with their action times. The variation of $U_{\rm dn}$ in a switching period $\Delta U_{\rm dn\_c}$ could be expressed by (11).

$$|\Delta U_{\rm dn\_c}| = \frac{(d_{\rm a}\,|i_{\rm aout}| + d_{\rm b}\,|i_{\rm bout}| + d_{\rm c}\,|i_{cout}|)\cdot T_{\rm s}}{2C_{\rm dn}}. \tag{11}$$

Due to the three components in the numerator of (11) being positive, NP voltage would have a large fluctuation by using this kind of method. It should be noted that, if the state selecting principle of one or two phases is reversed, the fluctuation of NP voltage may be reduced. If the absolute current value of phase $A$ is minimum among the three phases, and the redundant state selecting principle of phase $A$ is reversed, the variation of $U_{\rm dn}$ in a switching period, $\Delta U'_{\rm dn\_c}$, could be expressed as (12).

$$|\Delta U'_{\rm dn\_c}| = \frac{(-d_{\rm a}\,|i_{\rm aout}| + d_{\rm b}\,|i_{\rm bout}| + d_{\rm c}\,|i_{\rm cout}|)\cdot T_{\rm s}}{2C_{\rm dn}}. \tag{12}$$

It can be concluded from (12), in some cases, $|\Delta U'_{\rm dn\_c}|$ is smaller than $|\Delta U_{\rm dn\_c}|$. As a result, NP voltage fluctuations could be reduced to some extent. So, in the three-phase ANPC5L-HB inverter, the state selecting principle in each phase may not be the same. To balance the NP voltage effectively, a precise control model should be established.

*3) An Optimal NP Voltage Balance Method Based on MPC:* Aiming at the characteristic of the three-phase ANPC5L-HB inverter, an optimal NP voltage balance method based on model predictive control is proposed. According to the proposed modulation strategy, the output voltage $E$ or $-E$ must occur in a switching period, and only one of them would occur. So, there are only two alternatives per phase for NP voltage control. In phase $X$ ($X$ represents phase $A$, $B$, or $C$), the redundant state selection with its influence on NP voltage is depicted in Fig. 15.

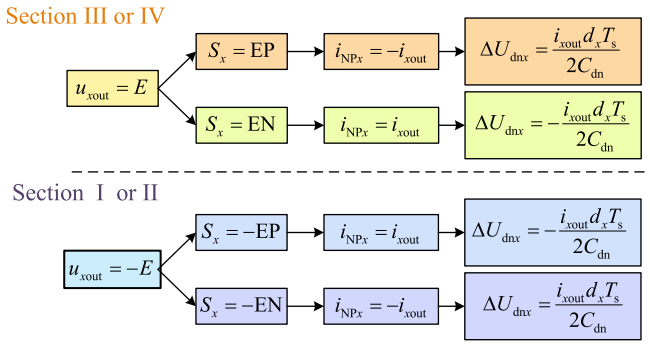


Fig. 15. Redundant switching state selection with its influence on NP voltage.

In the three-phase inverter, a total of $2^3 = 8$ combinations of the redundant state selection could be obtained. The influence on NP voltage can be expressed as (13). Among these combinations, one is the most favorable for the NP voltage balance. Therefore, the influences of the above combinations should be calculated. And a cost function $J$ is constructed, as shown in (14), to determine the most favorable switching state combination.

$$\begin{aligned}\Delta U_{\mathrm{dn}} &= \Delta U_{\mathrm{dna}} + \Delta U_{\mathrm{dnb}} + \Delta U_{\mathrm{dnc}} \\ &= -\frac{(d_a i_{\mathrm{NP}a} + d_b i_{\mathrm{NPb}} + d_c i_{\mathrm{NPc}}) \cdot T_{\mathrm{s}}}{2C_{\mathrm{dn}}} \end{aligned} \tag{13}$$

$$\begin{aligned} J &= |U_{\mathrm{dn}}(k+1) - U_{\mathrm{up}}(k+1)| \\ &= |U_{\mathrm{dn}}(k) - U_{\mathrm{up}}(k) + 2\Delta U_{\mathrm{dn}}(k)|\,. \end{aligned} \tag{14}$$

In (14), $U_{\mathrm{dn}}(k)$ and $U_{\mathrm{up}}(k)$ represent the sampling voltage value of $C_{\mathrm{dn}}$ and $C_{\mathrm{up}}$ at $k$ instant. $U_{\mathrm{dn}}(k+1)$ and $U_{\mathrm{up}}(k+1)$ represent the predicted value at $(k+1)$ instant. Based on the above analysis, the implementation of the proposed PWM and NP voltage balance strategies could be depicted in Fig. 16.

In Fig. 16, $J_{\min}$ represents the minimum cost function value among all the cost function values in the prediction process. As can be seen from Fig. 16, eight traversals are needed in each control cycle, but the calculation in the prediction process is simple. So the proposed method has a light computational burden, and is easy to realize in the digital control system.

## IV. Experimental Verification

To verify the effectiveness of the proposed strategies for the three-phase ANPC5L-HB inverter, a 25-kW three-phase ANPC5L-HB inverter prototype was built, and two types of experiments are conducted.

The experimental platform is shown in Fig. 17. The specifications are listed in Table IV. Scope recorder DL850E is used to record waveforms. Power analyzer WT1805E is used to evaluate the efficiency. Controllers of the platform include a central controller (based on DSP TMS320C6678) and three slave controllers (based on FPGA EP3C80F484I7). The central controller is responsible for sampling and executing algorithms, slave controllers are responsible for generating pulses.

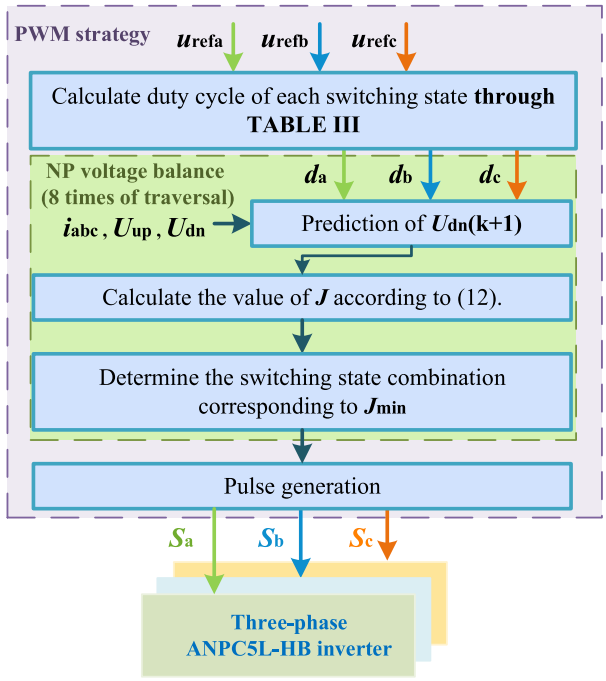


Fig. 16. Implementation process of the proposed NP voltage balance method.

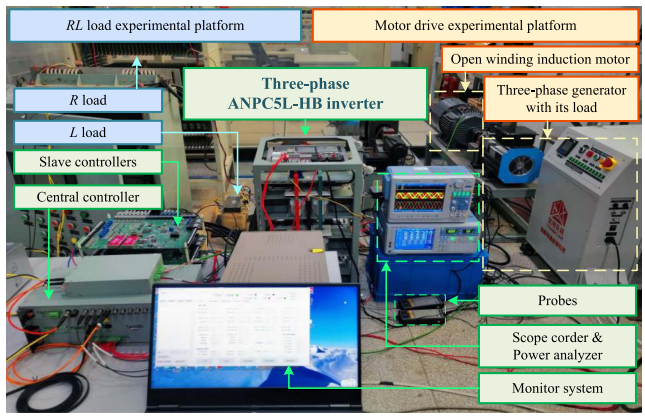


Fig. 17. Experimental platform.

TABLE IV
Specifications of the Experimental Platform

| Parameters | Values |
|---|---|
| DC-link voltage ($V_{\mathrm{dc}}$) | 600 V |
| DC-link capacitance ($C_{\mathrm{up}}$ $C_{\mathrm{dn}}$) | 1.41 mF |
| Load resistance ($R$) | 15 Ω |
| Load inductance ($L$) | 5 mH |
| Switching frequency ($f_{\mathrm{s}}$) | 10 kHz |
| IGBT (FF225R12ME4P) | 1200V / 225A |
| Dead time | 3 $\mu$s |

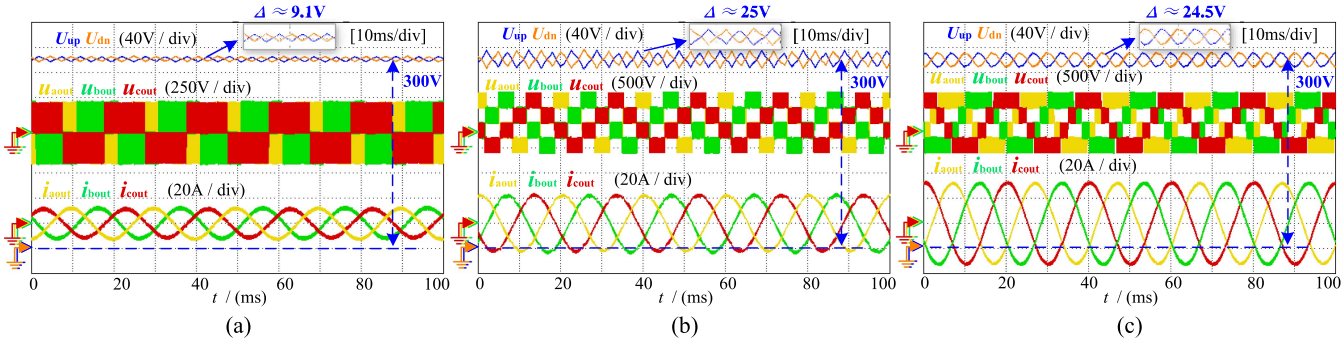


Fig. 18. Experimental results under steady-state conditions by using the classical NP voltage balance method. (a) $m = 0.3$. (b) $m = 0.6$. (c) $m = 0.9$.

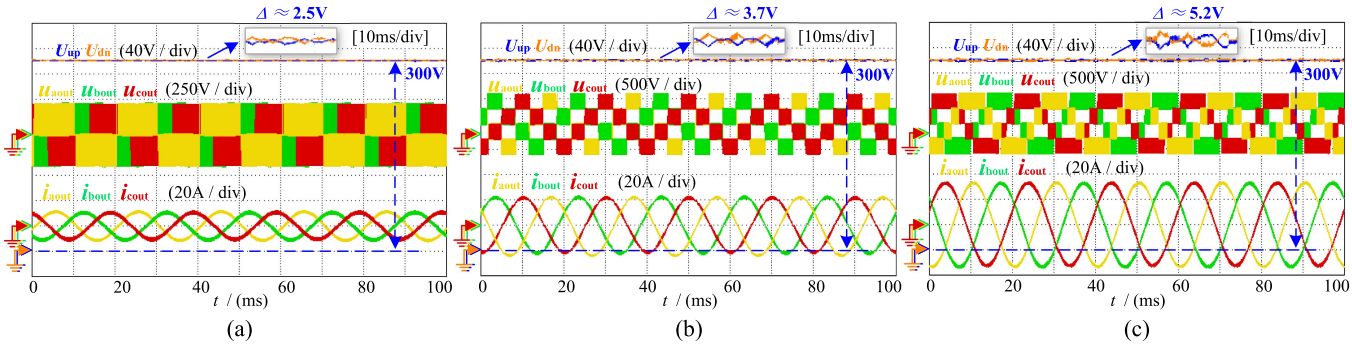


Fig. 19. Experimental results under steady-state conditions by using the proposed NP voltage balance method. (a) $m = 0.3$. (b) $m = 0.6$. (c) $m = 0.9$.

A star-shaped communication architecture is adopted between the central controller and slave controllers.

This experimental platform records experimental data in two ways. One is using the scope recorder, the other is saving the running data in the random access memory (RAM) of the controller. And the data in the RAM would be sent back to the monitor system through Ethernet after the inverter runs.

### A. *Experiments With RL Load*

*1) Steady-State Performance:* A few ANPC5L-HB inverter experiments under different modulation indices and different output frequencies are carried out to fully verify the effectiveness of the proposed strategy. Meanwhile, the NP voltage control performances of the proposed method and the classical method are compared and analyzed.

The steady-state performances of the ANPC5L-HB inverter by using the classical NP voltage balance method and the proposed method are depicted in Figs. 18 and 19, respectively. $\Delta$ represents the maximum difference between $U_{\rm dn}$ and $U_{\rm up}$. As can be seen from Figs. 18 and 19, when $m$ is smaller than 0.5, reference signals are located in Sections II and III, and output voltage levels are produced. When $m$ increases above 0.5, reference signals cover four sections, five output voltage levels are produced. In each section, the output voltage is changed between the two adjacent levels, and no parasitic state is produced. The effectiveness of the proposed modulation strategy is verified.

As for NP voltage control performance, it could be seen that the control performance of the proposed method is evidently superior to the classical method. When $m$ is 0.9, the $U_{\rm NP}$ fluctuation of the proposed method is only 2.6 V (0.87%), while the fluctuation amplitude of the classical method is 12.25 V (4.17%), which proves a better control performance of the proposed method.

*2) Dynamic Performance:* To verify the performance of the proposed strategy under dynamic working conditions, a series of comparative experiments are conducted. Experimental results under dynamic conditions by using the classical and the proposed NP voltage balance method are depicted in Figs. 20 and 21, respectively. The experiments include the rapid change of the modulation index ($m$) and the output frequency ($f$). In Figs. 20(a) and 21(a), $f$ is set to 50 Hz, and $m$ is sharply increased from 0.3 to 0.9. By using the proposed strategy, the NP voltage is kept well balanced, the fluctuation of $U_{\rm NP}$ is about 2.5 V (0.8%), while the $U_{\rm NP}$ fluctuation is almost five times larger (about 12.2 V) by using the classical method. The same results are shown in other subfigures of Figs. 20 and 21, where $m$ is set to 0.9. During this process, $f$ is sharply changed between 50 Hz and 25 Hz. Meanwhile, the proposed strategy always has a superior NP voltage balance performance. Based on the above analysis, the effectiveness and the superior performance of the proposed strategy are verified under dynamic working conditions.

*3) Low-Frequency Performance:* In motor drive applications, the torque of the motor may be non-zero when the rotor

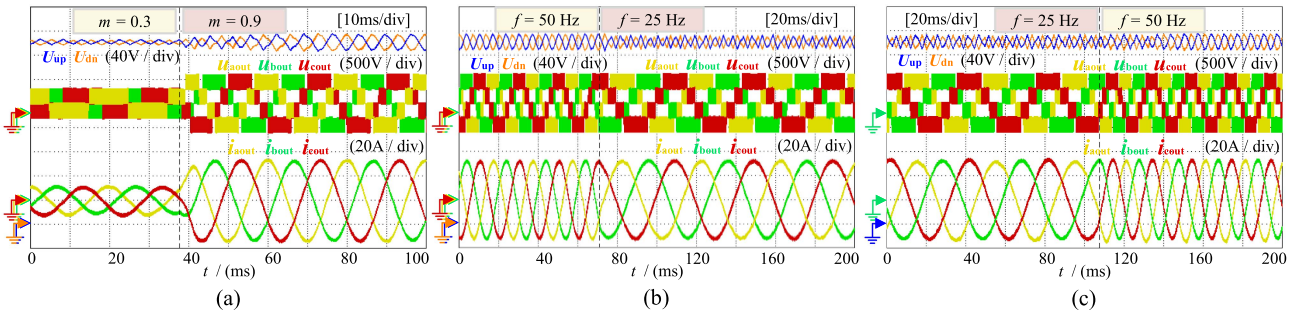


Fig. 20. Experimental results under dynamic conditions by using the classical NP voltage balance method. (a) When $m$ is sharply increased. (b) When $f$ is sharply changed from 50 to 25 Hz. (c) When $f$ is sharply changed from 25 to 50 Hz.

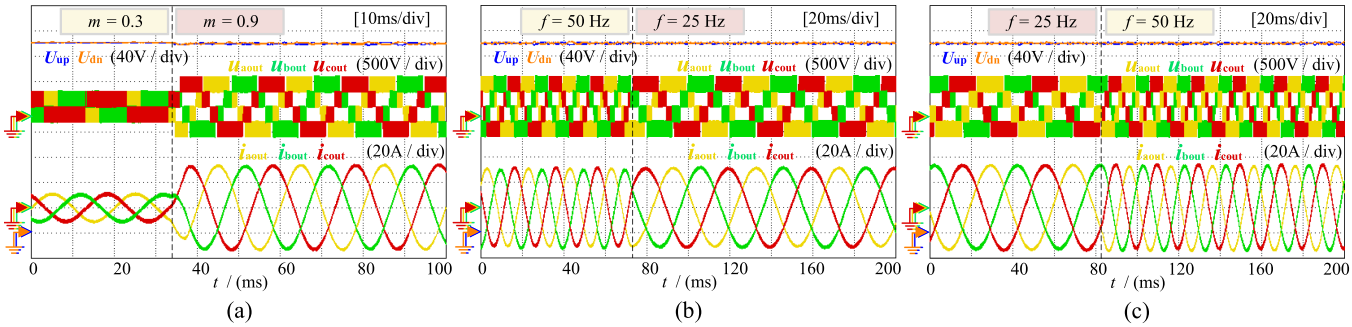


Fig. 21. Experimental results under dynamic conditions by using the proposed NP voltage balance method. (a) When $m$ is sharply increased. (b) When $f$ is sharply changed from 50 to 25 Hz. (c) When $f$ is sharply changed from 25 to 50 Hz.

speed is zero. So the NP voltage of the ANPC5L-HB inverter has to be kept balanced under zero output frequency working conditions. A frequency variation experiment is carried out to verify the zero frequency output ability of the ANPC5L-HB inverter. In the experiment, $m$ is set to 0.4, the output frequency is varied from 10 to 0 Hz. Due to the Rogowski current probe used in the platform could not acquire dc current, the experimental data is collected by the monitor system and plotted by MATLAB.

Fig. 22 shows the results when $f$ is varied from 10 to 0 Hz. It can be seen from Fig. 22, the NP voltage is kept well balance during the frequency variation process. When $f$ is varied to 0 Hz, output currents of three phases are keeping a constant value. ac current is transferred to dc current. The result proved the output ability of the inverter at 0 Hz and the effectiveness of the modulation and NP voltage balance strategies.

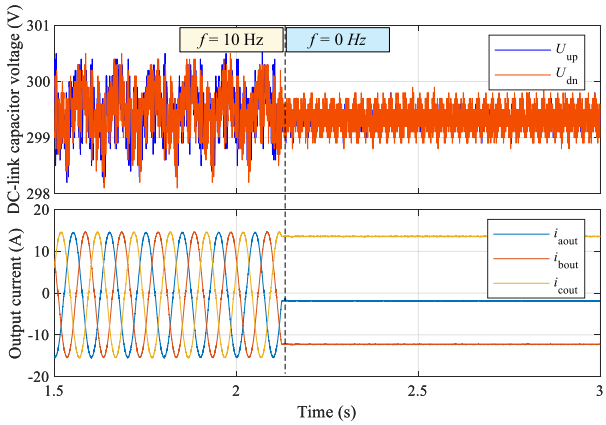


Fig. 22. Experimental results when $f$ is changed from 10 to 0 Hz.

## B. ZVS Characteristic and Efficiency Analysis

A switching loss comparison using the proposed modulation scheme is conducted based on PLECS thermal simulation, in which $m$ is gradually increased to 0.85, and $f$ is set to 50 Hz. In this case, the input power of the three-phase ANPC5L-HB inverter is about 25 kW. The simulation results of LFCs losses under two modulation schemes are depicted in Fig. 23. Compared with the undesigned modulation scheme, the loss of LFCs is reduced from 0.62% (155 W) to 0.5% (125 W) of the input power under the proposed modulation scheme, in which the switching losses of low-frequency IGBTs are almost zero.

Meanwhile, the ZVS of low-frequency IGBTs in the ANPC5L-HB inverter is verified in the experiment, relevant waveforms are depicted in Fig. 24. Take the low-frequency IGBT $S_{b6}$ as an example, the gate signal $V_{ge(Sb6)}$, and the collector-emitter voltage, $V_{ce(Sb6)}$, are depicted to verify the ZVS function. It could be seen from Fig. 24(b) and (c) that, the collector-emitter voltage is zero when the IGBT is turned

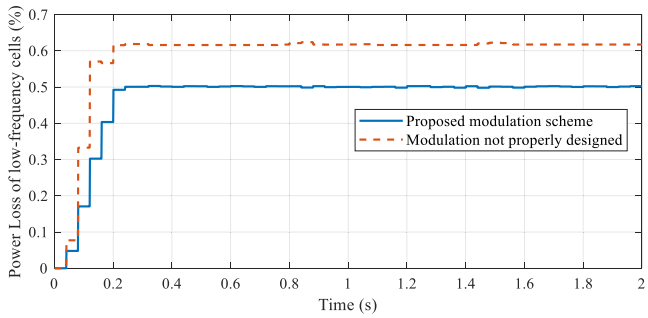


Fig. 23. Power losses of LFCs using different modulation schemes.

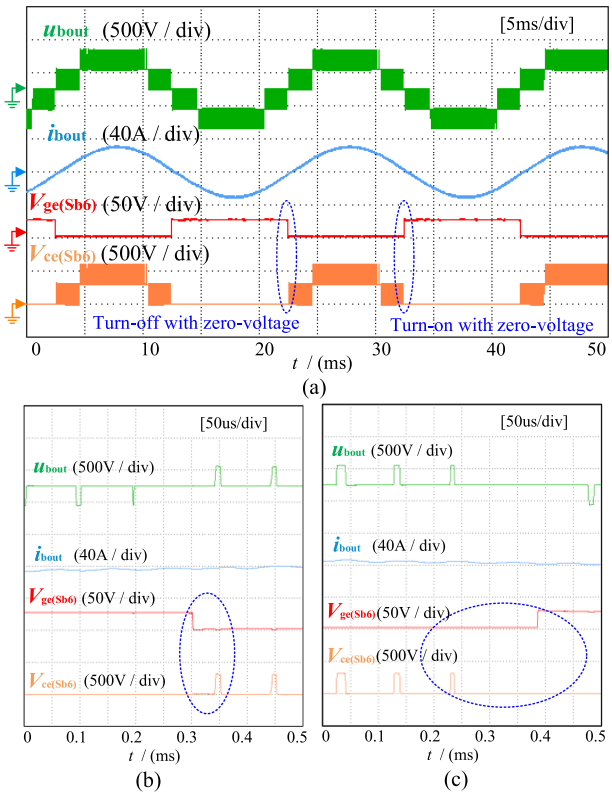


Fig. 24. ZVS waveforms by using the proposed modulation strategy. (a) Waveforms in the whole-time range. (b) Detailed waveforms of zero-voltage switching off. (c) Detailed waveforms of zero-voltage switching on.

ON and turned OFF. Enough time interval is reserved to ensure the effectiveness of the ZVS.

In the experiment, the efficiency of the ANPC5L-HB inverter is measured and depicted in Fig. 25. Fig. 25(a) represents the efficiency curve in the full output power range. Fig. 25(b) represents the peak efficiency (98.685%) measured near the rated power. In Fig. 25(b), $\eta_1$ marked by the red box represents the efficiency of the inverter. Element 1 represents the measured data of the dc input, and Elements 2∼4 represent the measured data of three ac outputs.

### C. Experiments With Open-Winding Motor Drive

Motor drive experiments are conducted to further verify the proposed strategies. The motor drive platform consists of an

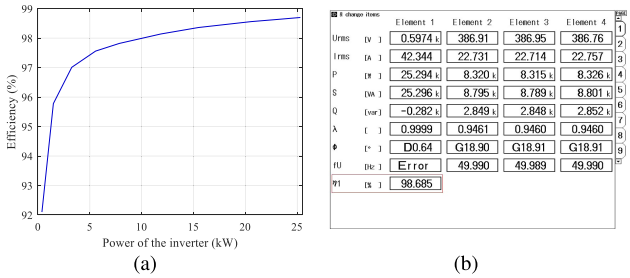


Fig. 25. Efficiency measurement of the ANPC5L-HB inverter. (a) Efficiency curve in the full power range. (b) Efficiency measurement at 25kW.

TABLE V
PARAMETERS OF THE OPEN-WINDING INDUCTION MOTOR

| Parameters | Value |
|---|---|
| Number of pole pairs | 1 |
| Stator resistance ($R_s$) | 1 Ω |
| Stator resistance ($R'_r$) | 0.9 Ω |
| Leakage inductance ($L_{ls}$ $L'_{lr}$) | 30 mH |
| Magnetizing inductance ($L_m$) | 300 mH |
| Rated frequency ($f$) | 45 Hz |

open-winding induction motor (IM) and a three-phase PMSM used as the generator. The output of the generator is connected to a three-phase resistance load. Parameters of the IM are listed as Table V.

*1) Steady-State Experiment:* An experiment under steady-state conditions is conducted. The reference rotor speed is set to 2500 r/min (rpm) and the load resistance of the generator is set to 10 kW, corresponding to 21.5 N·m load torque. Experimental results by using the classical and the proposed NP voltage balance strategy are depicted in Fig. 26(a) and (b), respectively.

It can be seen from Fig. 26 that the speed of the motor could be well controlled at around 2500 r/min and the NP voltage is balanced in this working condition. Compared with the classical method, the proposed NP voltage balance method has a better performance. The control accuracy of the NP voltage under the proposed method is ±1.05 V (0.35%), while that of the classical method is ±4.15 V (1.39%). In addition, with the improvement of NP voltage control accuracy, the rotor speed control accuracy is enhanced.

*2) Dynamic Experiments Under Abrupt Change of Load:* A dynamic experiment is carried out when the rotor speed is 2500 r/min. A 10-kW load is suddenly added and then removed in the process. The experimental results are depicted in Fig. 27. When no load is added, the output current amplitude is less than 10 A. During this time, the current is mostly composed of field current, and the torque current component is almost zero.

When the 10 kW load is added suddenly, the load torque is increased to 21.5 N·m, and the amplitude of the output current increases simultaneously. After about 2 seconds, the dynamic process ends, and the rotor speed and output current tend to be stabilized. When the load is added and removed, the rotor speed has fluctuations during the dynamic processes, which are

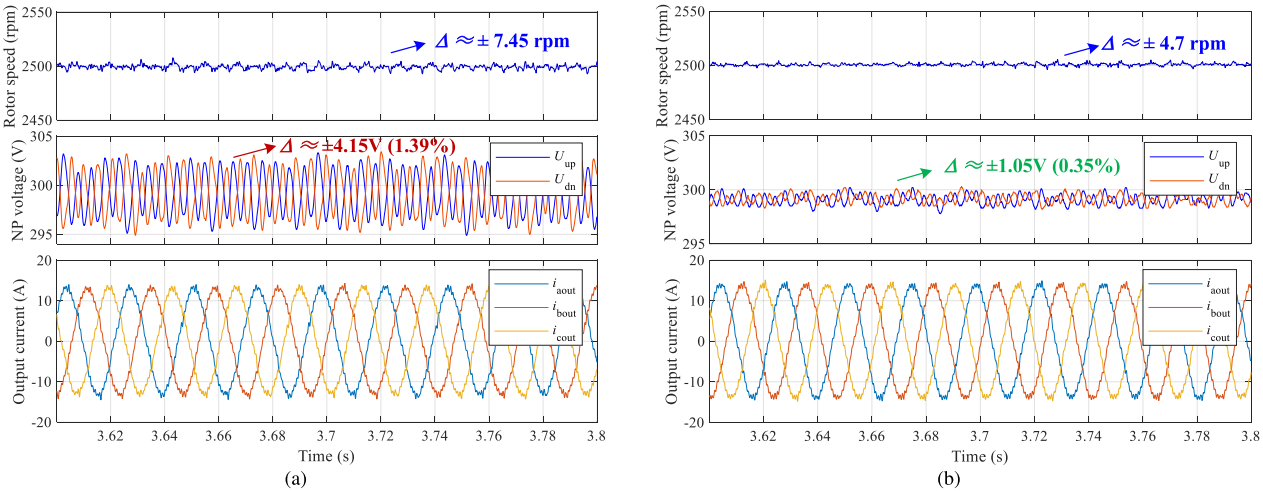


Fig. 26. Experimental results when the rotor speed is 2500 rpm. (a) Using classical NP voltage balance method. (b) Using the proposed method.

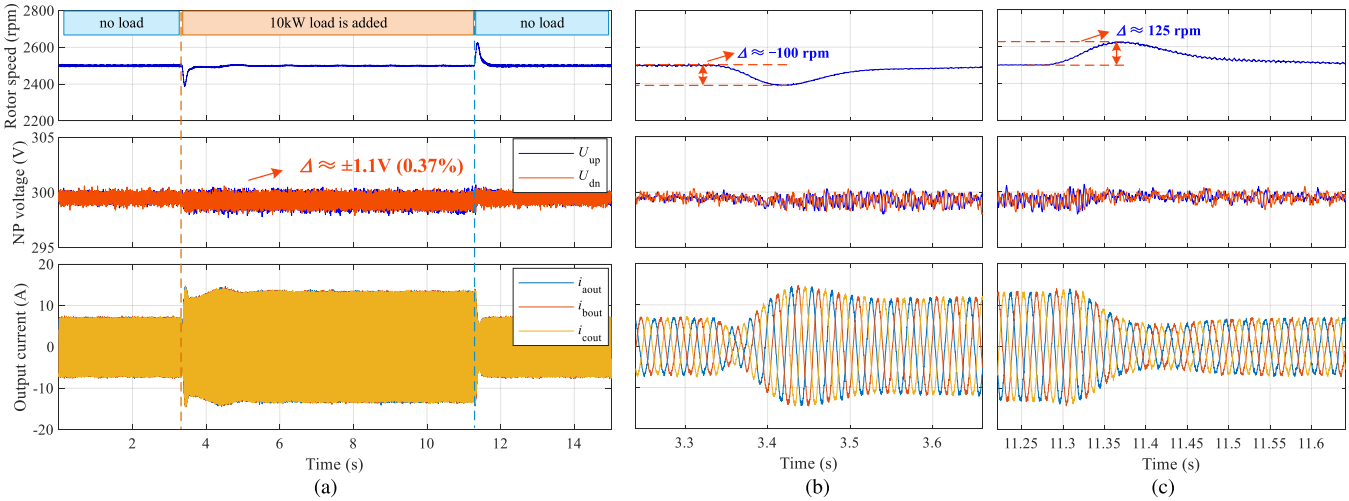


Fig. 27. Experimental results under abrupt changes of load. (a) Waveforms in the whole time range. (b) Details when load is added. (c) Details when load is removed.

depicted in Fig. 27(b) and (c), respectively. However, the rotor speed can be adjusted to the reference speed in less than 0.5 s. Meanwhile, the NP voltage is balanced well during the whole process. The maximum NP voltage fluctuation is only ±1.1 V (0.37%) during the load is added. The result represents that the proposed method has a good control performance on NP voltage.

Based on the above experiments, the effectiveness and good performance of the proposed modulation and NP voltage balance strategy for the ANPC5L-HB inverter are validated.

## V. Conclusion

A reduced switch count and high-efficiency three-phase ANPC5L-HB inverter for open-winding motor drive applications is proposed in this article. The modulation and NP voltage balance strategies for the three-phase ANPC5L-HB inverter are also proposed. The efficiency measurement is performed and confirmed the peak efficiency of 98.685% under 10-kHz switching frequency.

1) In the proposed PWM strategy, transitions between different switching states are constrained to avoid parasitic states. Meanwhile, the ZVS of low-frequency switches could be achieved by properly designing the voltage sequence, which reduces the switching loss and further improves the inverter efficiency.
2) Three arm cells all have influences on the NP voltage, which is beneficial to the self-balance of the NP voltage. In the proposed NP voltage balance strategy, the optimal switching state combination is selected by using the MPC approach. A better NP voltage control performance is realized compared with the classical method.
3) The effectiveness of the three-phase ANPC5L-HB inverter is validated by both $RL$ load and open-winding motor drive experiments. Meanwhile, the good performances of the PWM and NP voltage balance strategies are fully verified.

The strategies proposed in this article could also be applied to other multiphase ANPC H-bridge topologies.

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