Active Power Decoupling by Closed-Loop Control of Power Oscillations for a Bidirectional Single-Phase DC–AC Converter

Roberto A. Fantino, *Member, IEEE*, Claudio A. Busada, and Jorge A. Solsona, *Senior Member, IEEE*

***Abstract*—A control strategy for the active power decoupling in a single-phase full-bridge-based bidirectional dc–ac converter is proposed in this work. An ac-side auxiliary-circuit three-leg topology is used for the implementation. The proposal makes use of the instantaneous power theory for three-phase systems, applied to single-phase systems. A closed-loop control in the power domain is implemented, by matching the instantaneous power oscillations in the main circuit of the converter connected to the grid, with the instantaneous power oscillations in the auxiliary circuit. The control loop does not employ the measurement of the voltage or current on the dc-bus, nor the voltage on the auxiliary-circuit capacitor. Not requiring a calculation for the voltage reference on the auxiliary-circuit capacitor depending on the circuit parameters allows to eliminate the second harmonic power oscillations on the dc-bus even in the presence of parameteric uncertainty. Experimental and simulation results are presented to demonstrate the validity and effectiveness of the proposal.**

***Index Terms*—Distributed generation, full-bridge converter, power decoupling, single-phase voltage source converter.**

I. Introduction

SINGLE-PHASE converters are widely used in power electronics applications as an interface between a direct current (dc) power system and an alternating current (ac) power system. Among the most outstanding applications are the distributed power-generation systems [1], [2], battery chargers for electric vehicles [3], and light-emitting diode drivers [4]. One of the most used topologies for these applications is the four active switches full-bridge converter [5], [6]. Because of advantages in terms of efficiency, cost, and size, this topology is usually implemented without an isolation transformer.

In most applications, a constant power flow on the dc side of a single-phase converter is desirable. However, the ac side requires a constant power plus a pulsating power generated by the product of its sinusoidal voltage and current waveforms. This produces a power ripple on the dc-bus pulsating at twice the fundamental grid frequency, which degrades the system performance, for example, by reducing the efficiency of photovoltaic panels [2], [7], shortening the lifespan of fuel cells [8], or producing flickering effects on light-emitting diodes [4]. This issue can be addressed by methods generally called "power decoupling," which consist of adding to the basic converter topology, an auxiliary mechanism (generally, with a capacitor as main energy storage element) that provides the oscillatory component of the power required on the ac side, while the stationary power flow on the dc-bus is held constant. Typical passive methods of power decoupling make use of a large capacitor bank placed on the dc-bus [7], [9], which is desirable to eliminate or minimize since their implementation requires large electrolytic capacitors with a short lifespan and low reliability. As an alternative to reduce the dc-bus capacitance, many active power decoupling (APD) methods have been proposed and various reviews on this topic can be found in the literature [2], [7], [10], [11], [12], [13]. In general, the APD methods add to the main converter an auxiliary circuit made up of power electronic switches combined with small-size capacitors and/or inductors. The auxiliary circuit is an internal instantaneous power supply that must be controlled to provide the power oscillations to the ac side of the converter, decoupling them from the dc-bus.

In topological terms related to the place where the auxiliary circuit is connected, the APD methods can be classified into two main groups [12], [13], [14]: 1) dc-side arrangements, in which the auxiliary circuit is connected to the dc-bus [15], [16], [17], [18], and 2) ac-side (or mixed-type) arrangements, in which a part of the auxiliary circuit is connected to the ac side and part to the dc side of the converter [19], [20], [21], [22], [23], [24], [25], [26], [27], [28].

The APD in [24] uses two auxiliary capacitors at the ac side of a full-bridge converter, without extra power electronics. However, the utilization factor and stress on the switches can be greatly improved by adding an extra leg [12]. The ac-side auxiliary-circuit three-leg topology, initially proposed in [25], has become popular because of advantages, such as low control bandwidth requirement and high energy storage efficiency, since its auxiliary circuit operates with purely sinusoidal voltage and current waveforms. For this topology, in [27], it is shown that

Manuscript received 28 November 2022; revised 11 March 2023 and 26 May 2023; accepted 1 July 2023. Date of publication 6 July 2023; date of current version 1 September 2023. This work was supported in part by the Universidad Nacional del Sur, in part by the Consejo Nacional de Invertigaciones Científicas y Tecnicas (CONICET), and in part by the Agencia Nacional de Promocion Científica y Tecnologica (ANPCyT), Argentina. Recommended for publication by Associate Editor Q. Shafiee. *(Corresponding author: Roberto A. Fantino.)*

The authors are with the Instituto de Investigaciones en Ingeniería Eléctrica (UNS-CONICET) and Departamento de Ingeniería Eléctrica y de Computadoras, Universidad Nacional del Sur, Bahía Blanca 8000, Argentina (e-mail: roberto.fantino@uns.edu.ar; cbusada@uns.edu.ar; jsolsona@uns.edu.ar).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3292984.

Digital Object Identifier 10.1109/TPEL.2023.3292984

the current and voltage stress on the switches can be reduced by adopting space-vector pulsewidth modulation (SVM) technique. In [22], it is shown that this topology better aligns with power density and efficiency constraints in comparison with typical dc-side arrangements. In [26], a discontinuous pulsewidth modulation (PWM) strategy is proposed to reduce the converter switching losses. Regarding the control strategies proposed for this topology and other similar ones, most of the techniques in the literature implement a closed-loop control of the auxiliary circuit capacitor voltage. For this, they must estimate a capacitor voltage reference from a given ac-side pulsating power ripple. This reference is predicted based on the circuital model of the auxiliary circuit branch [13], [21], [22], [23], [25], [26], [27], [28], [29]. Then, the accuracy of such control strategies (in terms of second harmonic power ripple suppression) is affected by parameteric variations, since they depend on the exact knowledge of the capacitance, inductance, and resistance of the auxiliary circuit branch. Besides, in some cases the effect of the auxiliary-circuit inductor is neglected in the reference calculation process [22], [28], which can lead to greater error. The model-based feedback linearization control technique in [17] requires many sensors for full-state feedback, and its performance depends on the precise knowledge of all the system parameters. As is mentioned there, variations of the grid inductance can lead to steady-state tracking errors and a change in the control bandwidth [17]. There, the focus is placed on rectifier operation and, as in other control techniques [25], [28], a closed-loop control of the dc-bus voltage is implemented, with the aim of suppressing the ripple on this voltage, under the assumption that the dc current is a constant. This practice can lead to control issues if the dc-bus current or voltage is contaminated with ripple from other systems connected to the same dc-bus [23].

This work proposes a new control strategy to implement the APD in a bidirectional full-bridge-based single-phase dc–ac converter, employing an ac-side auxiliary-circuit three-leg topology [25]. The proposed control strategy makes use of the instantaneous power theory for three-phase systems applied to single-phase systems [5], [30]. The control loop does not require the measurement of the dc-bus voltage or current, nor the auxiliary-circuit capacitor voltage. A closed-loop control in the power domain is implemented, by matching the instantaneous power oscillations in the main circuit of the converter, with the instantaneous power oscillations in the auxiliary circuit, without the need to estimate a reference for the capacitor voltage depending on the circuit parameters. This allows to eliminate the second harmonic power oscillations on the dc-bus even in the presence of parameteric uncertainty. The validity and effectiveness of the proposed control strategy are demonstrated via experimental and simulation results.

II. System Description and Modeling

Fig. 1 shows the circuit diagram of the topology under study. The four main switches S_1, S_2, S_3, and S_4 make up a single-phase full-bridge converter, whose ac side is connected to a single-phase grid with voltage v_g and fundamental angular frequency ω_g, via an inductive filter with inductance L_g and

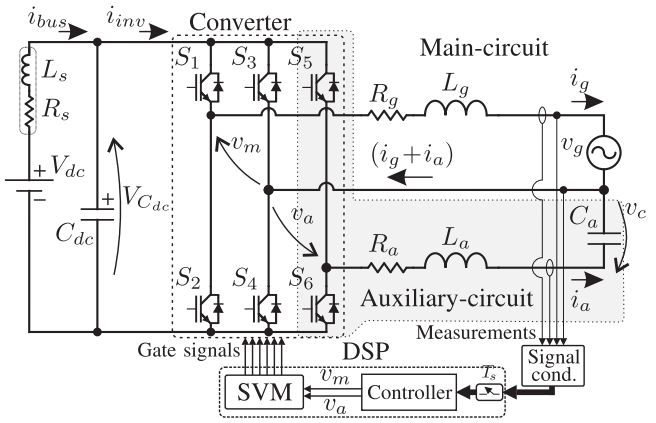


Fig. 1. Three-leg bidirectional single-phase DC–AC converter topology with ac-side auxiliary circuit.

parasitic resistance R_g. The auxiliary circuit (marked in gray) is composed of two switches S_5 and S_6, an inductive filter with inductance L_a and parasitic resistance R_a, and a storage capacitor with capacitance C_a, where v_c and i_a are the capacitor voltage and current, respectively. The dc side of the system is modeled here as a dc voltage source $V_{\rm dc}$ that supplies a current $i_{\rm bus}$, in series with a resistance R_s and an inductance L_s modeling the impedance of the connecting wires [31]. A parallel filtering capacitor $C_{\rm dc}$ of voltage $V_{C_{\rm dc}}$ is connected at the dc-bus to absorb the high-frequency ripple from the converter switching current $i_{\rm inv}$. The principal function of the auxiliary circuit is to provide the instantaneous power necessary to cancel out the power oscillations of fundamental frequency $2\omega_g$ in the instantaneous power $P_g = v_g i_g$ transferred to the grid, while the single-phase inverter injects a current i_g synchronized with v_g. In this way, the instantaneous power $P_i = V_{\rm dc} i_{\rm bus}$ supplied by $V_{\rm dc}$ results free of ripple of angular frequency $2\omega_g$. Note in Fig. 1 that the inductors are arranged in such a way that the main circuit and the auxiliary circuit can be controlled independently by means of the control actions v_m and v_a, respectively [25].

A. Main-Circuit Control and Auxiliary-Circuit Oscillatory Power Reference Generation

Indicated as "main-circuit control," Fig. 2(a) illustrates the controller usually used to regulate the current i_g injected to the grid by the converter. In the Laplace domain, the model of the main circuit in Fig. 2(a) is given by

$$i_g(s) = \frac{1}{R_g + sL_g}\left[v_m(s) - v_g(s)\right] \tag{1}$$

for which v_m represents the control action, while v_g represents a bounded disturbance signal. Based on the internal model principle [32], to copy a sinusoidal reference i_{g_r} of angular frequency ω_g, without steady-state error at ω_g, a proportional plus resonant (PR) regulator tuned to that frequency is used here, whose transfer function is given by

$$G_{{\rm PR}_m}(s) = K_{p_m}\left[1 + \frac{1}{T_{r_m}}\frac{s}{\left(s^2+\omega_g^2\right)}\right]. \tag{2}$$

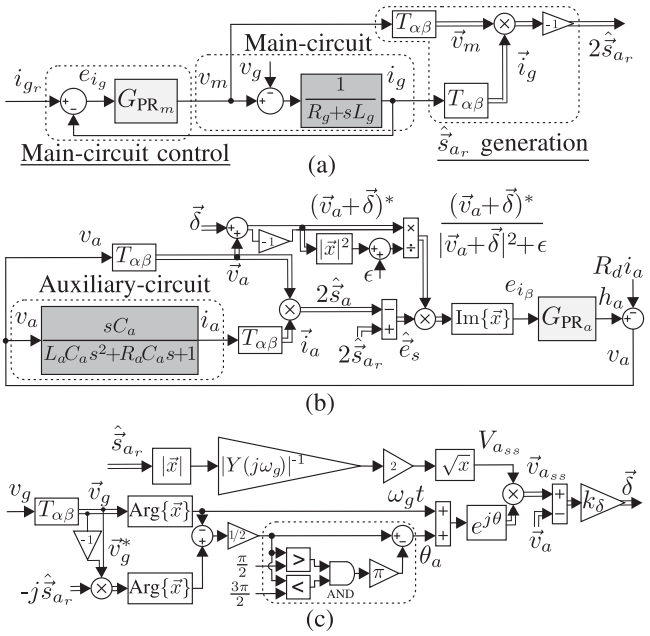


Fig. 2. Proposed control strategy. (a) Main-circuit control block diagram and generation of the oscillatory power reference $\hat{\vec{s}}_{a_r}$. (b) Auxiliary-circuit control block diagram. (c) Estimate of $\vec{v}_{a_{ss}}$ and computation of $\vec{\delta}$.

K_{p_m} and T_{r_m} in (2) can be designed according to the guidelines given in [33] and [34].

The blocks $T_{\alpha\beta}$ in Fig. 2(a) represent second-order generalized integrator–quadrature signal generator (SOGI-QSG) structures [5], tuned to ω_g. Let "x" be an arbitrary single-phase signal of angular frequency ω_g. By applying to x, the operator $T_{\alpha\beta}\{x\}$, a complex spatial vector with the form $\vec{x} = x_\alpha + jx_\beta$, is obtained, composed of a direct component "x_α" with the same magnitude and phase as "x," and its quadrature version x_β with the same magnitude but 90° lagging "x" [5]. The SOGI-QSG transfer functions, with respect to the components α and β, are given by [35]

$$T_\alpha(s) = \frac{k_s\omega_g s}{s^2 + k_s\omega_g s + \omega_g^2};\quad T_\beta(s) = \frac{k_s\omega_g^2}{s^2 + k_s\omega_g s + \omega_g^2} \tag{3}$$

where $k_s \in \mathbb{R}^+$. Thus, $T_{\alpha\beta}\{x\} = \mathcal{L}^{-1}\{T_{\alpha\beta}(s)X(s)\} = \mathcal{L}^{-1}\{T_\alpha(s)X(s)\} + j\mathcal{L}^{-1}\{T_\beta(s)X(s)\} = \vec{x}$, where $X(s) = \mathcal{L}\{x\}$ is the Laplace transform of "x."

Let $\vec{v}_m = T_{\alpha\beta}\{v_m\}$ and $\vec{i}_g = T_{\alpha\beta}\{i_g\}$ [see Fig. 2(a)]. Based on the instantaneous power theory for three-phase systems [5], [30], the instantaneous active power P_m and instantaneous reactive power Q_m, and the complex power vector $\vec{S}_m$ of the main circuit can be represented by

$$\begin{aligned} P_m &= v_{m_\alpha} i_{g_\alpha} \\ Q_m &= v_{m_\alpha} i_{g_\beta} \\ \vec{S}_m = P_m + jQ_m &= \underbrace{\frac{1}{2}\vec{v}_m^{\,*}\vec{i}_g}_{\bar{\vec{S}}_m = \bar{P}_m + j\bar{Q}_m} + \underbrace{\frac{1}{2}\vec{v}_m\vec{i}_g}_{\hat{\vec{s}}_m} \end{aligned} \tag{4}$$

where the symbol "$*$" indicates the conjugate operation. $\vec{S}_m$ in (4) is represented as the composition of a constant term $\bar{\vec{S}}_m = (\bar{P}_m + j\bar{Q}_m)$ and an oscillatory term $\hat{\vec{s}}_m$ of fundamental angular frequency $2\omega_g$ [5]. Following the same reasoning, the instantaneous complex power vector $\vec{S}_a$ of the auxiliary circuit in Fig. 1 can be represented by

$$\vec{S}_a = \underbrace{\frac{1}{2}\vec{v}_a^{\,*}\vec{i}_a}_{\bar{\vec{S}}_a} + \underbrace{\frac{1}{2}\vec{v}_a\vec{i}_a}_{\hat{\vec{s}}_a} \tag{5}$$

where $\bar{\vec{S}}_a$ and $\hat{\vec{s}}_a$ represent the constant and oscillatory terms of $\vec{S}_a$, with $\vec{v}_a = T_{\alpha\beta}\{v_a\}$ and $\vec{i}_a = T_{\alpha\beta}\{i_a\}$.

Let $(\vec{S}_m + \vec{S}_a)$ be the total instantaneous complex power of the system in Fig. 1. According to (4) and (5), for V_{dc} to supply constant power (free of second harmonic ripple), it must be $\hat{\vec{s}}_a = -\hat{\vec{s}}_m$. Thus, the oscillatory power of the auxiliary circuit must be controlled to copy a reference $\hat{\vec{s}}_{a_r}$ given by

$$\hat{\vec{s}}_{a_r} = -\hat{\vec{s}}_m = -\frac{1}{2}\vec{v}_m\vec{i}_g. \tag{6}$$

Indicated as "$\hat{\vec{s}}_{a_r}$ generation," Fig. 2(a) illustrates how $2\hat{\vec{s}}_{a_r}$ is generated based on (6).

B. Auxiliary-Circuit Control

Fig. 2(b) illustrates the block diagram proposed in this work to implement the closed-loop control of the instantaneous oscillatory power of the auxiliary circuit. The dark-gray block in Fig. 2(b) corresponds to the model of the auxiliary-circuit *LCR* branch in Fig. 1 of transfer function

$$\frac{i_a(s)}{v_a(s)} = \frac{sC_a}{L_aC_as^2 + R_aC_as + 1} = Y(s). \tag{7}$$

Voltage v_a must be regulated based on the measurement of i_a, to stabilize the auxiliary circuit and makes that $\hat{\vec{s}}_a$ in (5) copy to $\hat{\vec{s}}_{a_r}$ in (6). In Fig. 2(b), the calculation of the term $2\hat{\vec{s}}_a$ in (5) is implemented using v_a and i_a. A virtual resistance-based active damping of the auxiliary circuit [5] is implemented here to damp the *LC* resonance of (7). The need to implement the active damping is justified later in Section IV via Bode plot analysis. By adding the term $-R_di_a$ as is shown in Fig. 2(b), the following modified transfer function $H_m(s)$ with input signal h_a is obtained

$$H_m(s) = \frac{i_a(s)}{h_a(s)} = \frac{sC_a}{L_aC_as^2 + (R_a + R_d)C_as + 1} \tag{8}$$

where h_a is the output of the PR regulator in Fig. 2(b). The constant R_d represents a virtual resistance that can be selected as $R_d = (2\zeta\sqrt{L_a/C_a} - R_a)$, where ζ is the desired damping factor for the poles of (8). The signal h_a applied to (8) is obtained based on making zero the instantaneous oscillatory power error defined as

$$\hat{\vec{e}}_s = 2(\hat{\vec{s}}_{a_r} - \hat{\vec{s}}_a) = -\left(\vec{v}_m\vec{i}_g + \vec{v}_a\vec{i}_a\right) \tag{9}$$

in the complex instantaneous power domain [see Fig. 2(b)]. In order to map this error $\hat{\vec{e}}_s$ defined in the power domain, to an

error $\vec{e}_i$ in the current domain, let $\vec{e}_i$ be such that $\hat{\vec{e}}_s = \vec{v}_a \vec{e}_i$. Multiplying by $\vec{v}_a^*$ on both sides of this expression and solving it results

$$\vec{e}_i = \frac{\vec{v}_a^* \hat{\vec{e}}_s}{|\vec{v}_a|^2}. \tag{10}$$

Note in (10) that if the system starts with $\vec{v}_a = \vec{0}$, it will be $\vec{e}_i = 0$ regardless of the value of $\hat{\vec{s}}_{a_r}$. For this reason, it is necessary to add a signal $\vec{\delta}$ to $\vec{v}_a$, which provides the disturbance that allows the controller to start. In addition, to avoid the division by zero when $|\vec{v}_a| = 0$, a constant value $\epsilon > 0$ can be added to the denominator of (10). Thus, instead of (10), it is implemented here

$$\vec{e}_i = \frac{(\vec{v}_a + \vec{\delta})^*}{|\vec{v}_a + \vec{\delta}|^2 + \epsilon} \hat{\vec{e}}_s. \tag{11}$$

Another important aspect is that for each reference vector $\hat{\vec{s}}_{ar}$, there are two possible combinations of $\vec{v}_a$ and $\vec{i}_a$ that satisfy $\hat{\vec{e}}_s = \vec{0}$ in (9). Indeed, the value of $\hat{\vec{s}}_a$ resulting from the pair $\{\vec{v}_a, \vec{i}_a\}$ is identical to the value resulting from the pair composed of the same waveforms shifted 180°, $\{-\vec{v}_a, -\vec{i}_a\}$. These two pairs produce different results for the voltage $(v_m - v_a)$ and for the current $(i_g + i_a)$ (see Fig. 1). To avoid saturation of the control action, the pair that provides a smaller magnitude $|\vec{v}_m - \vec{v}_a|$ is selected in this work. The signal $\vec{\delta}$ in (11) is defined as

$$\vec{\delta} = k_\delta (\vec{v}_{a_{ss}} - \vec{v}_a) \tag{12}$$

where $0 < k_\delta < 1$ is a constant, and $\vec{v}_{a_{ss}}$ is the steady-state value for $\vec{v}_a$, corresponding to the selected steady-state pair $\{\vec{v}_{a_{ss}}, \vec{i}_{a_{ss}}\}$, whose estimate is given in Section II-C. Note in (12) that $\vec{\delta} \to \vec{0}$ at the steady state. Note also that if $\vec{v}_a = \vec{0}$, immediately after applying $\hat{\vec{s}}_{ar} = \vec{v}_{a_{ss}} \vec{i}_{a_{ss}} \neq 0$, the initial value $\vec{e}_{i_0}$ of $\vec{e}_i$ is

$$\vec{e}_{i_0} = \frac{k_\delta \vec{v}_{a_{ss}}^* \hat{\vec{s}}_{ar}}{|k_\delta \vec{v}_{a_{ss}}|^2 + \epsilon} \approx \frac{1}{k_\delta} \vec{i}_{a_{ss}}. \tag{13}$$

In this way, the initial error $\vec{e}_{i_0}$ has the initial orientation corresponding to the selected steady-state pair $\{\vec{v}_{a_{ss}}, \vec{i}_{a_{ss}}\}$. By symmetry, the complex error signal $\vec{e}_i$ in (11) is composed of two identical 90° phase-shifted error signals e_{i_α} and e_{i_β} of fundamental angular frequency ω_g. The closed-loop control of the auxiliary circuit is implemented here by using the imaginary component e_{i_β} of $\vec{e}_i$ given by

$$e_{i_\beta} = \mathrm{Im}\left\{ \frac{(\vec{v}_a + \vec{\delta})^*}{|\vec{v}_a + \vec{\delta}|^2 + \epsilon} \hat{\vec{e}}_s \right\}. \tag{14}$$

The stability of the auxiliary-circuit control using (14) is verified in Section IV via Bode plot analysis, based on the linearization of (14) developed in Section III. Finally, h_a is obtained by applying to e_{i_β}, a PR regulator tuned to ω_g, of transfer function

$$G_{\mathrm{PR}_a}(s) = K_{p_a} \left[1 + \frac{1}{T_{r_a}} \frac{s}{\left(s^2 + \omega_g^2\right)} \right] \tag{15}$$

where the controller constants K_{p_a} and T_{r_a} must be selected in order to guarantee the stability of the closed-loop system and obtain a proper dynamic response. It should be noted that the calculation of $\hat{\vec{e}}_s$ in (9) does not depend on the circuit parameters, since $\vec{v}_m$ and $\vec{v}_a$ are known control variables, and i_g and i_a are measured variables. Then e_{i_β} in (14) neither depends on the circuit parameters. Therefore, according to the internal model principle [32], as long as the system is stable in closed loop, the PR regulator will make the error e_{i_β} (and so $\hat{\vec{e}}_s$) zero even in the presence of parameteric uncertainty.

C. Estimate of $\vec{v}_{a_{ss}}$ From Steady-State Analysis

Here, an estimate for $\vec{v}_{a_{ss}}$ in (12) based on steady-state analysis of the auxiliary circuit is obtained. Consider for this analysis $R_a = 0$ and that (7) presents a capacitive behavior at ω_g (i.e., $L_a C_a \omega_g^2 < 1$). Taking as reference the grid voltage complex space-vector $\vec{v}_g = T_{\alpha\beta}\{v_g\}$ represented as

$$\vec{v}_g = V_g e^{j(\omega_g t)} \tag{16}$$

suppose the auxiliary circuit of Fig. 1 operating on a stable steady-state condition (subscript "ss") with applied voltage $v_{a_{ss}} = V_{a_{ss}} \cos(\omega_g t + \theta_a)$, being θ_a the phase-shift angle between $v_{a_{ss}}$ and v_g. In this condition, the complex space-vectors of voltage, current, and power oscillation in the auxiliary circuit are

$$\vec{v}_{a_{ss}} = V_{a_{ss}} e^{j(\omega_g t + \theta_a)} = v_{a_{\alpha_{ss}}} + j v_{a_{\beta_{ss}}} \tag{17}$$

$$\vec{i}_{a_{ss}} = V_{a_{ss}} |Y(j\omega_g)| e^{j(\omega_g t + \theta_a + \pi/2)} \tag{18}$$

$$\hat{\vec{s}}_{a_{ss}} = \frac{1}{2} V_{a_{ss}}^2 |Y(j\omega_g)| e^{j(2\omega_g t + 2\theta_a + \pi/2)} \tag{19}$$

where $Y(j\omega_g) = Y(s)|_{(s=j\omega_g)}$ is the complex steady-state admittance obtained by evaluating (7) at $s = j\omega_g$. Given $\hat{\vec{s}}_{a_r}$ computed with (6) and with the form

$$\hat{\vec{s}}_{a_r} = |\hat{\vec{s}}_{a_r}| e^{j(2\omega_g t + \theta_{sr})} \tag{20}$$

where θ_{sr} is an angle to be computed in the following. Using (20) and (16), it can be obtained that $-j\hat{\vec{s}}_{a_r} \vec{v}_g^* = |\hat{\vec{s}}_{a_r}| V_g e^{j(\omega_g t + \theta_{sr} - \pi/2)}$, from which

$$\theta_{sr} = \mathrm{Arg}\{-j\hat{\vec{s}}_{a_r} \vec{v}_g^*\} - \mathrm{Arg}\{\hat{\vec{v}}_g\} + \pi/2 \tag{21}$$

where $\mathrm{Arg}\{\vec{x}\} = \mathrm{atan2}\{\vec{x}\}$ represents the argument (or four-quadrant inverse tangent) of the complex vector $\vec{x}$ [36]. In order to (19) be equal to (20), it should be

$$V_{a_{ss}} = \sqrt{2 \frac{|\hat{\vec{s}}_{a_r}|}{|Y(j\omega_g)|}} \tag{22}$$

$$\theta_a = \frac{\theta_{sr} - \pi/2}{2} = \frac{\mathrm{Arg}\{-j\hat{\vec{s}}_{a_r} \vec{v}_g^*\} - \mathrm{Arg}\{\hat{\vec{v}}_g\}}{2}. \tag{23}$$

Fig. 2(c) illustrates how an estimate of (17) is obtained in practice based on (22) and (23), and how this estimate is used to obtain $\vec{\delta}$ in (12). Taking into account that $v_m \approx v_g$, $|\vec{v}_m - \vec{v}_a|$ can be approximated as $\sqrt{|\vec{v}_m|^2 - 2|\vec{v}_m||\vec{v}_a|\cos(\theta_a) + |\vec{v}_a|^2}$. Thus, to obtain the smaller magnitude $|v_m - v_a|$ between the two possible solutions for the estimate of θ_a in (23), it is selected that the one within the range $-\pi/2 \leq \theta_a \leq \pi/2$. The logic diagram

used to ensure that θ_a is within that range is illustrated enclosed in dashed lines in Fig. 2(c).

III. Linearization of the Auxiliary-Circuit Control

Consider for this analysis $\epsilon = 0$ in (14). Note in Fig. 2(b) that $(\vec{v}_a + \vec{\delta})/|\vec{v}_a + \vec{\delta}|^2$ is a nonlinear function of $\vec{v}_a$ involved in the auxiliary-circuit control. Next, a linearization of the control loop involving this nonlinear function is obtained.

At the steady-state operating point defined by (17)–(19), it is intended to linearize the complex function

$$\frac{(\vec{v}_a + \vec{\delta})}{|\vec{v}_a + \vec{\delta}|^2} = f_\alpha + j f_\beta \tag{24}$$

where, using (12)

$$\begin{cases} f_\alpha = \frac{v_{a_\alpha} + k_\delta (v_{a_{\alpha ss}} - v_{a_\alpha})}{|\vec{v}_a + k_\delta (\vec{v}_{a_{ss}} - \vec{v}_a)|^2} \\ f_\beta = \frac{v_{a_\beta} + k_\delta \left(v_{a_{\beta_{ss}}} - v_{a_\beta}\right)}{|\vec{v}_a + k_\delta (\vec{v}_{a_{ss}} - \vec{v}_a)|^2}. \end{cases} \tag{25}$$

In (25), f_α and f_β are nonlinear functions of v_{a_α} and v_{a_β}, which can be modeled as $f_\alpha = (f_{\alpha_{ss}} + \tilde{f}_\alpha)$ and $f_\beta = (f_{\beta_{ss}} + \tilde{f}_\beta)$. Being $f_{\alpha_{ss}} = v_{a_{\alpha ss}}/|\vec{v}_{a_{ss}}|^2$ and $f_{\beta_{ss}} = v_{a_{\beta ss}}/|\vec{v}_{a_{ss}}|^2$ steady-state components obtained by evaluating (25) at (17), considering that there is no error estimating $\vec{v}_{a_{ss}}$. The signals $\tilde{f}_\alpha$ and $\tilde{f}_\beta$ are small-signal components obtained as [37]

$$\begin{cases} \tilde{f}_\alpha = & a_{11}\tilde{v}_{a_\alpha} + a_{12}\tilde{v}_{a_\beta} \\ \tilde{f}_\beta = & a_{21}\tilde{v}_{a_\alpha} + a_{22}\tilde{v}_{a_\beta} \end{cases} \tag{26}$$

where $a_{11} = \partial f_\alpha/\partial v_{a_\alpha}|_{\vec{v}_{a_{ss}}}$, $a_{12} = \partial f_\alpha/\partial v_{a_\beta}|_{\vec{v}_{a_{ss}}}$, $a_{21} = \partial f_\beta/\partial v_{a_\alpha}|_{\vec{v}_{a_{ss}}}$, and $a_{22} = \partial f_\beta/\partial v_{a_\beta}|_{\vec{v}_{a_{ss}}}$ are the partial derivatives of f_α and f_β with respect to v_{a_α} and v_{a_β}, evaluated at $\vec{v}_{a_{ss}}$. Calculating (26) using (25) and (17), it results

$$\tilde{\vec{f}} = \tilde{\vec{v}}_a^* \frac{(k_\delta - 1)}{V_{a_{ss}}^2} e^{j(2\omega_g t + 2\theta_a)} \tag{27}$$

where $\tilde{\vec{f}} = (\tilde{f}_\alpha + j\tilde{f}_\beta)$ and $\tilde{\vec{v}}_a = (\tilde{v}_{a_\alpha} + j\tilde{v}_{a_\beta})$, being $\tilde{v}_{a_\alpha}$ and $\tilde{v}_{a_\beta}$ the small-signal components of v_{a_α} and v_{a_β}, respectively. Let i_r be a fictitious current reference such that $i_r = \text{Im}\{2\hat{\vec{s}}_{a_r}(\vec{v}_a + \vec{\delta})^*/|\vec{v}_a + \vec{\delta}|^2\}$ for the product involving $2\hat{\vec{s}}_{a_r}$ in Fig. 2(b). By considering the reference $\hat{\vec{s}}_{a_r}$ fixed at a steady-state condition $\hat{\vec{s}}_{a_{rss}} = \hat{\vec{s}}_{a_{ss}} \neq \vec{0}$, by using (19) and (27), it can be easily demonstrated that the linearization for i_r is given by

$$\tilde{i}_r = \text{Im}\left\{2\hat{\vec{s}}_{a_{rss}}\tilde{\vec{f}}^*\right\} = -(1 - k_\delta)|Y(j\omega_g)|\tilde{v}_{a_\alpha} \tag{28}$$

where $\tilde{i}_r$ is the small-signal component of i_r. Now, let i be a fictitious current such that $i = \text{Im}\{2\hat{\vec{s}}_a(\vec{v}_a + \vec{\delta})^*/|\vec{v}_a + \vec{\delta}|^2\}$ for the product involving $2\hat{\vec{s}}_a$ in Fig. 2(b). To linearize i, the following linearization for $\hat{\vec{s}}_a$ is used

$$\hat{\tilde{s}}_a = \frac{1}{2}\left(\vec{v}_{a_{ss}}\tilde{\vec{i}}_{a_{ss}} + \tilde{\vec{v}}_a\vec{i}_{a_{ss}} + \vec{v}_{a_{ss}}\tilde{\vec{i}}_a\right). \tag{29}$$

Using (25) and (29) to calculate $\text{Im}\{2(\hat{s}_{a_\alpha} + j\hat{s}_{a_\beta})(f_\alpha + jf_\beta)^*\}$, discarding the quadratic terms resulting from the products between small-signal components, the linearization for $\tilde{i}$ results

$$\tilde{i} = \tilde{i}_{a_\beta} + k_\delta |Y(j\omega_g)|\tilde{v}_{a_\alpha} \tag{30}$$

where $\tilde{i}$ represents the small-signal component of i. Using (28) and (30), the small-signal component $\tilde{e}_{i_\beta}$ of the error e_{i_β} in (14) can be calculated as

$$\tilde{e}_{i_\beta} = (\,\tilde{i}_r - \tilde{i}\,) = -\tilde{i}_{a_\beta} - |Y(j\omega_g)|\tilde{v}_{a_\alpha}. \tag{31}$$

Note that, in (31), the components proportional to k_δ are canceled out, resulting $\tilde{e}_{i_\beta}$ independent of this parameter. Fig. 3 illustrates the equivalent small-signal model for the nonlinear feedback of the auxiliary-circuit control in Fig. 2(b). By opening the path from e_{i_β} to $(\tilde{i}_r - \tilde{i})$, using (3), (8), and (15), the model can be simplified as the negative feedback of the open-loop transfer function

$$\begin{aligned} F_{\text{ol}}(s) &= -\frac{(\tilde{i}_r - \tilde{i})(s)}{\tilde{e}_{i_\beta}(s)} \\ &= \left[(1 - R_d H_m)\, T_\alpha |Y(j\omega_g)| + T_\beta H_m\right] G_{\text{PR}_a}. \end{aligned} \tag{32}$$

This model is employed in Section IV to verify the system closed-loop stability, given the parameters used for the implementation.

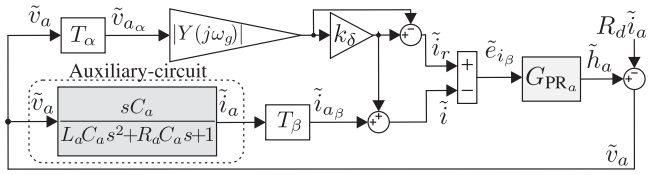


Fig. 3. Equivalent small-signal model for the auxiliary-circuit control.

TABLE I
System and Controller Parameters

Symbol	Value	Symbol	Value
V_{dc}	350 V	S_n	1 kVA
V_{g_n}	162 V_{rms}	I_{g_n}	6.17 A_{rms}
$\omega_g/(2\pi)$	50 Hz	t_D	1 μs
L_g; R_g	4.3 mH; 639 mΩ	L_a; R_a	3.8 mH; 447 mΩ
C_{dc}; C_a	470 μF; 120 μF	f_s; f_{pwm}	10 kHz; 10 kHz
K_{p_m}; T_{r_m}	22.73 Ω; 1.9 ms	K_{p_a}; T_{r_a}	15 Ω; 2 ms
k_δ; ϵ	1/4; 1 V^2	k_s; R_d	$\sqrt{2}$; 7.41 Ω
R_s	10 mΩ	L_s	6 μH

IV. Simulation Results

This section presents simulation results that demonstrate the performance of the proposed control strategy. Table I lists the parameters used in the simulation. S_n is the nominal apparent power of the converter, while V_{g_n} and I_{g_n} are the nominal rms values of v_g and i_g, respectively. The value of C_a was selected so that this capacitor operates with a rms voltage equal to V_{g_n} when its rms current is equal to I_{g_n}, i.e., $C_a = I_{g_n}/(\omega_g V_{g_n})$. In this way, the current and voltage stress of the system can be minimized [27]. The maximum current stress of the switches S_3 and S_4 [current $(i_g + i_a)$ in Fig. 1] is approximately $\sqrt{2}I_{g_n}$ for zero leading power factor. L_g and L_a were selected such that maximum peak-to-peak high-frequency current ripples $\Delta i_{g_{\text{HF}_{\max}}} \approx V_{\text{dc}}/(8L_g f_{\text{pwm}}) = 1$ A and $\Delta i_{a_{\text{HF}_{\max}}} \approx$

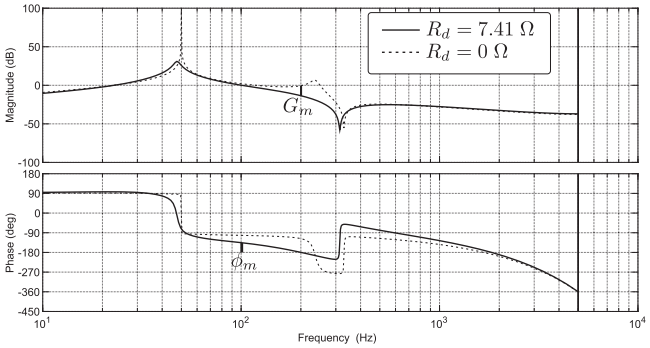


Fig. 4. Open-loop Bode plot of the equivalent small-signal model for $R_d = 0\ \Omega$ and $R_d = 7.41\ \Omega$.

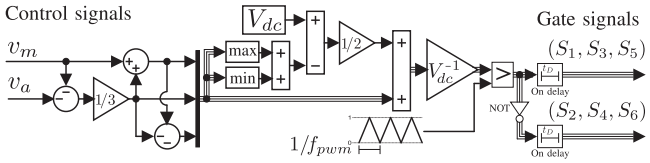


Fig. 5. Generation of converter gate signals from control signals v_m and v_a.

$V_{\rm dc}/(8L_a f_{\rm pwm}) = 1.15$ A [22], [25] are obtained for the main circuit and the auxiliary circuit, respectively. The dc-bus low-pass filter transfer function is given by $i_{\rm bus}(s)/i_{\rm inv}(s) = 1/[L_s C_s s^2 + R_s C_{\rm dc} s + 1]$. Since $R_s \approx 0$, the cutoff frequency f_c (bandwidth) of this transfer function can be approximated as $f_c \approx [\sqrt{(1+\sqrt{2})/(L_s C_{ds})}\,]/(2\pi)$[38]. In order to guarantee a low-pass filtering of $i_{\rm bus}$ with $f_c < 5$ kHz, $C_{\rm dc} > (1+\sqrt{2})/[L_s(2\pi f_c)^2] = 407\ \mu$F is required. Thus, the commercial capacitance value $C_{\rm dc} = 470\ \mu$F is used for the implementation. $k_s = \sqrt{2}$ was selected in (3), a value that is usually used to obtain a good performance of the SOGI-QSG [5]. Thus, the poles of (3) result in $(-1/\sqrt{2} \pm j1/\sqrt{2})\omega_g$, with which a 5% settling time $t_{s_{5\%}} \approx 3\sqrt{2}/\omega_g = 13.5$ ms is obtained [5]. In Table I, f_s is the sample frequency used to simulate the digital implementation of the control strategy, which corresponds to the one used for the practical implementation presented in Section V. For the digital implementation (with sampling period $T_s = 1/f_s$), the transfer functions (2), (3), (8), and (15) were discretized using the zero-order-hold method [39]. For the discrete modeling, a one sample delay z^{-1} cascaded with the PR regulators was considered, which takes into account the digital processing delay [34]. The virtual resistance R_d was selected to obtain a damping factor $\zeta = 0.7$ for the poles of (8). Fig. 4 shows the open-loop Bode plot obtained from the discretization of (32), for the case in which the selected value for R_d is used, and for the case in which $R_d = 0$ is used. Note that if $R_d = 0$, the system is unstable since its gain is greater than 0 dB when the phase crosses $-180°$, this is the reason why the active damping is implemented in Section II-B. With the selected values for K_{p_a} and T_{r_a} in (15), a stable system with phase margin $\phi_m \approx 45°$ and gain margin $G_m \approx 14$ dB is obtained. Fig. 5 shows the block diagram used for generating the converter PWM gate signals to synthesize the control action signals v_m and v_a (see Fig. 2). This block diagram implements a carrier-based modulation equivalent to SVM [22], [40].

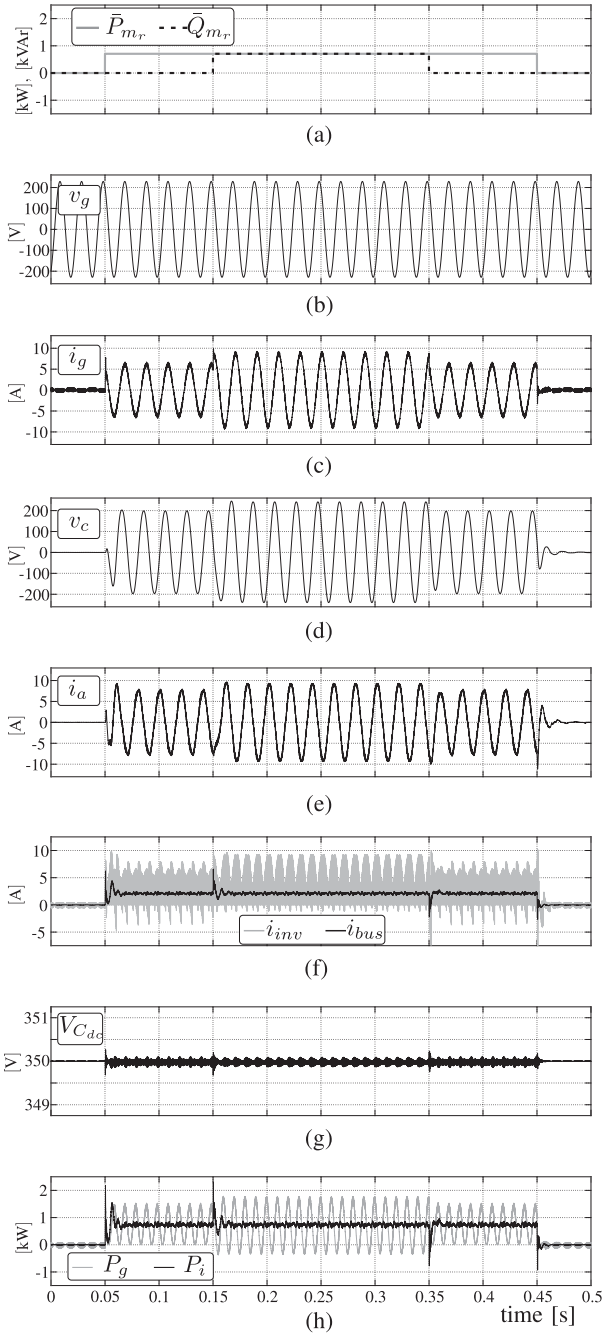


Fig. 6. Simulation results. (a) $\bar{P}_{m_r}$, $\bar{Q}_{m_r}$. (b) v_g. (c) i_g. (d) v_c. (e) i_a. (f) $i_{\rm inv}$, $i_{\rm bus}$. (g) $V_{C_{\rm dc}}$. (h) P_i, P_g.

In order to evaluate the performance of the control strategy under different conditions of power injected to the grid, the simulation results shown in Fig. 6 were obtained. Fig. 6(a) shows the references $\bar{P}_{m_r}$ and $\bar{Q}_{m_r}$ for $\bar{P}_m$ and $\bar{Q}_m$ defined in (4), respectively. Initially, $\bar{P}_{m_r} = \bar{Q}_{m_r} = 0$. At the instant $t = 0.05$ s, the active power reference is increased to $\bar{P}_{m_r} = S_n/\sqrt{2}$ holding $\bar{Q}_{m_r} = 0$. At $t = 0.15$ s, the reactive power reference is increased so that $\bar{P}_{m_r} = \bar{Q}_{m_r} = S_n/\sqrt{2}$. At $t = 0.35$ s, the reactive power reference is reduced again to $\bar{Q}_{m_r} = 0$, and at $t = 0.45$ s, the active power reference is reduced to $\bar{P}_{m_r} = 0$. Fig. 6(b) shows the grid voltage v_g. Fig. 6(c) shows the current

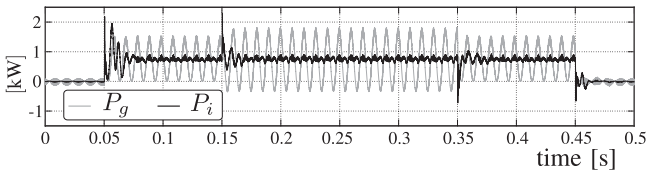


Fig. 7. Simulation results. P_i and P_g for a 50% increase in L_a and C_a.

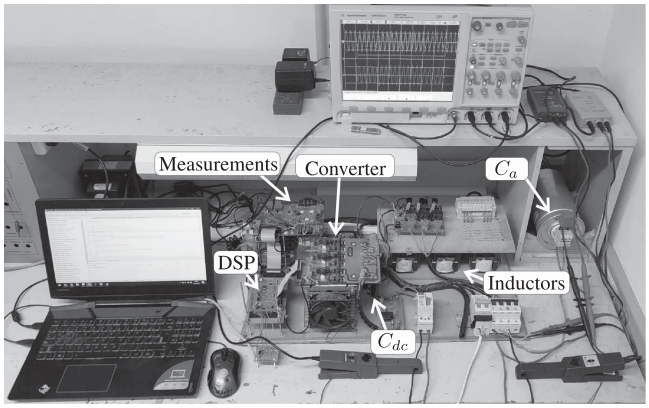


Fig. 8. Experimental setup.

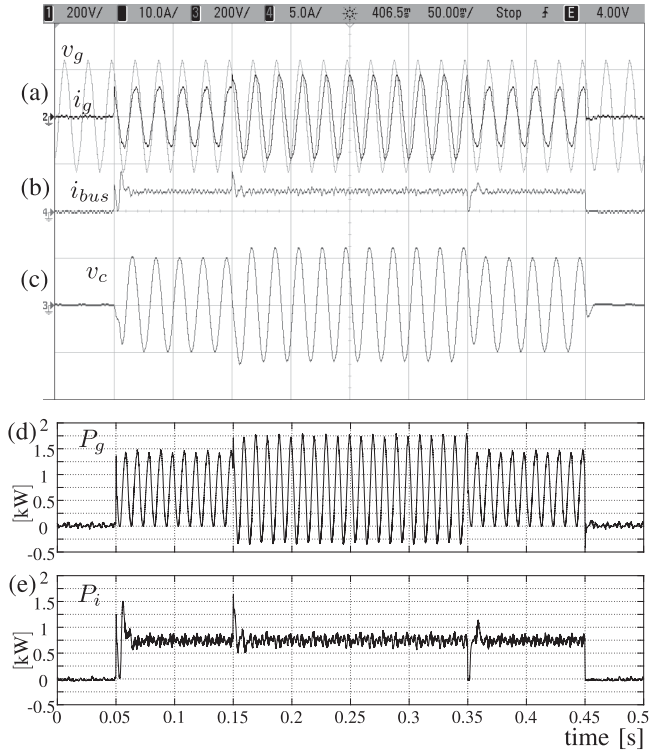


Fig. 9. Experimental results. (a) v_g [200 V/div], i_g [10 A/div]. (b)$i_{\rm bus}$ [5 A/div]. (c) v_c [200 V/div]. (d) P_g. (e) P_i. Time scale: 50 ms/div.

i_g injected to the grid. Fig. 6(d) shows the auxiliary circuit capacitor voltage v_c. Fig. 6(e) shows the auxiliary circuit current i_a. Fig. 6(f) shows the dc-source current $i_{\rm bus}$ and the converter dc-side current $i_{\rm inv}$ (ver Fig. 1). Fig. 6(g) shows the dc-bus capacitor voltage $V_{C_{\rm dc}}$. Fig. 6(h) shows instantaneous power $P_i = V_{\rm dc} i_{\rm bus}$ supplied by the dc-bus, and the instantaneous power $P_g = v_g i_g$ transferred to the grid. Note that the large second harmonic power ripple observed in P_g is the ripple that should be present in P_i if the APD were not implemented. However, the proposed control strategy successfully eliminates the presence of such a ripple from P_i. It can be seen that after each variation in the power injected to the grid, the proposed control strategy eliminates the second harmonic power ripple from P_i in less than one grid cycle. Fig. 7 shows dc-bus instantaneous power $P_i = V_{\rm dc} i_{\rm bus}$, and the power $P_g = v_g i_g$ injected to the grid, for the case in which the experience of Fig. 6 is repeated for a 50% increase in L_a and C_a. Note that although the transient response is degraded, the control strategy demonstrates its effectiveness in eliminating the second harmonic power oscillations on the dc-bus even against large parameteric variations.

V. Experimental Results

This section presents experimental results to verify the simulation results obtained in Section IV. A photograph of the experimental setup is shown in Fig. 8. The results were obtained using a three-leg converter prototype implemented with insulated-gate bipolar transistor devices IRG4PH50UD. $V_{\rm dc}$ was implemented using a unidirectional dc voltage source Sorensen SGI 600-25. A diode STTH6004 W was added in series with the source to protect it from negative current flow. The control strategy was implemented in a floating point digital signal processor TMS320F28335. An oscilloscope Agilent MSO7104B of four analog channels was used for the measurements. A generic electrolytic capacitor LGW2W471MELC45 was used for $C_{\rm dc}$. Available film capacitors B25667B5237A375 (77μF + $77/2\mu$F) in parallel with B32674D6505 K (5μF) were used for C_a. The parameters of the experimental system are listed in Table I. In Table I, $f_{\rm pwm}$ is the switching frequency and t_D is the turn-ON dead time of the converter switches. The same variations in the references $\bar{P}_{m_r}$ and $\bar{Q}_{m_r}$ shown in Fig. 6(a) were implemented in practice. The obtained experimental results can be seen in Fig. 9. Fig. 9(a) shows the grid voltage v_g and the current i_g injected to the grid. Note that this current is contaminated with high-frequency ripple produced by the converter modulation. Fig. 9(b) shows the measurement of the current $i_{\rm bus}$ supplied by $V_{\rm dc}$ (see Fig. 1). Fig. 9(c) shows the auxiliary-circuit capacitor voltage v_c. Note that this voltage is similar to the one obtained by simulation in Fig. 6(d). Fig. 9(d) shows the instantaneous power $P_g = v_g i_g$ injected to the grid, calculated with the data corresponding to i_g and v_g, acquired by using the oscilloscope internal memory. In the same way, Fig. 9(e) shows the instantaneous power $P_i = V_{\rm dc} i_{\rm bus}$ on the dc-bus, calculated with the data acquired from the measurements of $i_{\rm bus}$ and $V_{\rm dc}$. This last figure experimentally verifies that after each variation in the power injected to the grid, the proposed control strategy eliminates the presence of second harmonic ripple from P_i, in less than one grid cycle. At steady state, P_i only shows the presence of high-frequency ripple generated by the converter switching, the nonlinear harmonic distortion introduced by the dead time of the switching devices, and the grid harmonic distortion.

TABLE II
AC-SIDE APD USED IN THIS WORK AND DC-SIDE BUCK-TYPE APD: CHARACTERISTICS OF BOTH TOPOLOGIES AND DIFFERENT CONTROL STRATEGIES

Topology characteristics	DC-side buck-type	AC-side in this work
Max. efficiency [%]	93.2 [10], [15]; > 98 [18]	98 [22]; > 97 [26]
Power density [W/in^3]	22.56 [15]; 240 [18][a]	55.8 [22]
Min. dec. capacitor C_a [F]	$2V_{g_n}I_{g_n}/(\omega_g V_{dc}^2)$ [15][b]	$2V_{g_n}I_{g_n}/(\omega_g V_{dc}^2)$ [27][b]
Auxiliary inductor L_a [H]	$V_{dc}/(4\Delta i_{HF} f_{pwm})$ [22]	$V_{dc}/(8\Delta i_{HF} f_{pwm})$ [22]

Control strategy	Topology	Grid current response [c]	Bus power decoupling response [c]	Tracking dependent on circuit parameters	Closed-loop control of bus voltage/current
This work	AC-side	$< T_g/10$	$\sim T_g$	No	No
[22]	AC-side	$< T_g/10$	$> 2T_g$	Yes[e]	No
[25]	AC-side	$> T_g$	$> 10T_g$	Yes[e]	Yes
[28]	AC-side	$< T_g$	$> 20T_g$	No	Yes
[17]	buck-type	$> 2T_g$	$< T_g/10$	Yes (on L_g)	Yes
[29]	buck-type	$< T_g/10$	No data	Yes[d]	No

[a] Using high capacitance density ceramic capacitors. [b] Considering maximum capacitor voltage (V_{dc}). [c] $T_g = 2\pi/\omega_g$.
[d] Model-based predictive control. [e] Model-based estimate of v_c is required.

VI. CONCLUSION

A control strategy to implement the APD and, thus, eliminate the second harmonic ripple from the dc-bus in a bidirectional dc-ac single-phase converter was proposed. A three-leg topology with ac-side auxiliary circuit was used for the implementation. Making use of the instantaneous power theory for three-phase systems applied to single-phase systems, the proposal implements the control of the power oscillations on the ac side of the converter. The calculation of a reference for the auxiliary-circuit capacitor voltage based on the circuit parameters is not required. This allows to eliminate the second harmonic power oscillations on the dc-bus, even in the presence of parameteric variations. Both experimental and simulation results are presented to demonstrate the validity and effectiveness of the proposal. For the ac-side APD used in this work and the dc-side buck-type APD, the main characteristics of both topologies and different control strategies are listed in Table II.

REFERENCES

[1] F. Blaabjerg, Y. Yang, D. Yang, and X. Wang, "Distributed power-generation systems and protection," *Proc. IEEE*, vol. 105, no. 7, pp. 1311–1331, Jul. 2017.

[2] S. Xu, L. Chang, and R. Shao, "Evolution of single-phase power converter topologies underlining power decoupling," *Chin. J. Elect. Eng.*, vol. 2, no. 1, pp. 24–39, 2016.

[3] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, May 2013.

[4] S. Li, S.-C. Tan, C. K. Lee, E. Waffenschmidt, S. Y. Hui, and C. K. Tse, "A survey, classification, and critical review of light-emitting diode drivers," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1503–1516, Feb. 2016.

[5] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid Converters for Photovoltaic and Wind Power Systems*. Hoboken, NJ, USA:Wiley, Feb. 2011.

[6] S. Neira, J. Pereda, and F. Rojas, "Three-port full-bridge bidirectional converter for hybrid DC/DC/AC systems," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13077–13084, Dec. 2020.

[7] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.

[8] G. Fontes, C. Turpin, S. Astier, and T. A. Meynard, "Interactions between fuel cells and power converters: Influence of current harmonics on a fuel cell stack," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 670–678, Mar. 2007.

[9] H. Wang, C. Li, G. Zhu, Y. Liu, and H. Wang, "Model-based design and optimization of hybrid DC-link capacitor banks," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8910–8925, Sep. 2020.

[10] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778–4794, Jul. 2016.

[11] M. A. Vitorino, L. F. S. Alves, R. Wang, and M. B. de Rossiter Corrêa, "Low-frequency power decoupling in single-phase applications: A comprehensive overview," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2892–2912, Apr. 2017.

[12] A. R. Gautam, D. M. Fulwani, R. R. Makineni, A. K. Rathore, and D. Singh, "Control strategies and power decoupling topologies to mitigate 2ω-ripple in single-phase inverters: A review and open challenges," *IEEE Access*, vol. 8, pp. 147533–147559, 2020.

[13] Y. Liu, W. Zhang, Y. Sun, M. Su, G. Xu, and H. Dan, "Review and comparison of control strategies in active power decoupling," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 14436–14455, Dec. 2021.

[14] Z. Qin, Y. Tang, P. C. Loh, and F. Blaabjerg, "Benchmark of AC and DC active power decoupling circuits for second-order harmonic mitigation in kilowatt-scale single-phase inverters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 15–25, Mar. 2016.

[15] R. Wang et al., "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430–1443, May 2011.

[16] X. Cao, Q.-C. Zhong, and W.-L. Ming, "Ripple eliminator to smooth DC-bus voltage and reduce the total capacitance required," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2224–2235, Apr. 2015.

[17] H. Yuan, S. Li, W. Qi, S.-C. Tan, and S.-Y. Hui, "On nonlinear control of single-phase converters with active power decoupling function," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5903–5915, Jun. 2019.

[18] D. Neumayr, D. Bortis, and J. W. Kolar, "Ultra-compact power pulsation buffer for single-phase DC/AC converter systems," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, 2016, pp. 2732–2741.

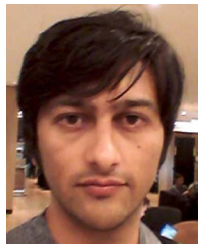
[19] Y. Tang and F. Blaabjerg, "A component-minimized single-phase active power decoupling circuit with reduced current stress to semiconductor switches," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2905–2910, Jun. 2015.

[20] Y. Tang, Z. Qin, F. Blaabjerg, and P. C. Loh, "A dual voltage control strategy for single-phase PWM converters with power decoupling function," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7060–7071, Dec. 2015.

[21] S. Bhowmick and L. Umanand, "A high-performance dynamic controller for an active power decoupler with AC-side storage element," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 2041–2056, Sep. 2019.

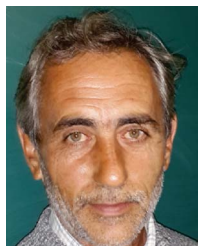
[22] A. S. Morsy and P. N. Enjeti, "Comparison of active power decoupling methods for high-power-density single-phase inverters using wide-bandgap FETs for Google little box challenge," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 790–798, Sep. 2016.

[23] H. Wu, S.-C. Wong, C. K. Tse, and Q. Chen, "Control and modulation of bidirectional single-phase AC-DC three-phase-leg SPWM converters with active power decoupling and minimal storage capacitance," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4226–4240, Jun. 2016.
[24] I. Serban, "Power decoupling method for single-phase H-bridge inverters with no additional power electronics," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4805–4813, Aug. 2015.
[25] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1308–1319, Mar. 2013.
[26] J. Xu, T. B. Soeiro, F. Gao, H. Tang, and P. Bauer, "Minimum switching losses discontinuous PWM strategy for bidirectional single-phase ac-dc converter with active power decoupling circuit," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 6118–6132, May 2021.
[27] R. Chen, Y. Liu, and F. Z. Peng, "DC capacitor-less inverter for single-phase power conversion with minimum voltage and current stress," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5499–5507, Oct. 2015.
[28] C. C. D. Viana, T. Soong, and P. W. Lehn, "Single-input space vector based control system for ripple mitigation on single-phase converters1," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3765–3774, Apr. 2019.
[29] B. Ge et al., "Direct instantaneous ripple power predictive control for active ripple decoupling of single-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3165–3175, Apr. 2018.
[30] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," *IEEE Trans. Ind. Appl.*, vol. IA-20, no. 3, pp. 625–630, May 1984.
[31] S. Caniggia and F. Maradei, *Signal Integrity and Radiated Emission of High-Speed Digital Systems. Appendix A: Formulae for Partial Inductance Calculation*. Hoboken, NJ, USA:Wiley, 2008.
[32] B. A. Francis and W. M. Wonham, "The internal model principle of control theory," *Automatica*, vol. 12, no. 5, pp. 457–465, Sep. 1976.
[33] D. G. Holmes, T. A. Lipo, B. P. McGrath, and W. Y. Kong, "Optimized design of stationary frame three phase AC current regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2417–2426, Nov. 2009.
[34] R. A. Fantino, C. A. Busada, and J. A. Solsona, "Optimum PR control applied to LCL filters with low resonance frequency," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 793–801, Jan. 2018.
[35] M. Monfared, M. Sanatkar, and S. Golestan, "Direct active and reactive power control of single-phase grid-tie converters," *IET Power Electron.*, vol. 5, no. 8, pp. 1544–1550, 2012.
[36] L. Ahlfors and K. M. R. Collection, *Complex Analysis: An Introduction to the Theory of Analytic Functions of One Complex Variable, Ser. International Series in Pure and Applied Mathematics*. New York, NY, USA: McGraw-Hill, 1979.
[37] H. K. Khalil, *Nonlinear Systems*, 3rd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2002.
[38] N. Nise, *Control Systems Engineering*, 7th ed. Hoboken, NJ, USA: Wiley, 2015.
[39] G. Goodwin, S. Graebe, and M. E. Salgado, *Control System Design*. Englewood Cliffs, NJ, USA: Prentice Hall, 2001.
[40] K. Zhou and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis [three-phase inverters]," *IEEE Trans. Ind. Electron.*, vol. 49, no. 1, pp. 186–196, Feb. 2002.



Roberto A. Fantino (Member, IEEE) received the B.Sc. degree in electronics engineering, the M.S. degree in electrical engineering, and the Ph.D. degree in control systems from the Universidad Nacional del Sur, Bahía Blanca, Argentina, in 2011, 2015, and 2018, respectively.

He is currently a Researcher and Teaching Assistant with CONICET and with the Departamento Ingeniería Eléctrica y de Computadoras, Instituto de Investigaciones en Ingeniería Eléctrica "Alfredo C. Desages," Universidad Nacional del Sur. His research interests include power electronics, grid power control, renewable energy resources, automotive applications, and distributed power generation.



Claudio A. Busada was born in Bahía Blanca, Argentina, on 13 March, 1962. He received the B.Sc. degree in electrical engineering and the Ph.D. degree in control systems from the Universidad Nacional del Sur, Bahía Blanca, in 1989 and 2004, respectively.

From 1988 to 2004, he was with Mechanic and Electrical Department, Bahía Blanca. Since 1989, he has been with the Departamento de Ingeniería Eléctrica y de Computadoras (DIEC), Universidad Nacional del Sur, where he is currently a Professor. He is also a Researcher with the Instituto de Investigaciones en Ingeniería Eléctrica "Alfredo C. Desages" (UNS-CONICET). His research interests include power electronics, rotating machinery, active filters, automatic control, and the integration of distributed energy systems.

Jorge A. Solsona (Senior Member, IEEE) received the B.Sc. degree in electronics engineering and the Ph.D. degree in electrical engineering from the Universidad Nacional de La Plata, La Plata, Argentina, in 1986 and 1995, respectively.

He is currently with the Departamento de Ingeniería Eléctrica y de Computadoras, Instituto de Investigaciones en Ingeniería Eléctrica "Alfredo C. Desages" (IIIE), Universidad Nacional del Sur, Bahía Blanca, Argentina, where he is currently a Professor, and with CONICET. He is involved in teaching. His research focuses on control theory and its applications to electromechanical systems.