A Modulation Scheme to Reduce Leakage Current of Split-Capacitor Four-Wire Current Source Inverter

Xin Li, Yao Sun, *Member, IEEE*, Li Jiang, Shiming Xie, Yonglu Liu, *Member, IEEE*, and Mei Su, *Member, IEEE*

***Abstract*—The transformer-less split-capacitor four-wire current source inverter is effective to reduce leakage current, but its effect is closely related to the impedance of the neutral wire and common mode voltage. The leakage current can be almost eliminated when the impedance of the neutral wire is zero, but the zero impedance condition does not hold in practice. To further suppress the leakage current, a new carrier-based modulation scheme with reduced common mode (CM) voltage is proposed in this article. The resulting CM voltage (peak-to-peak) is half that of the conventional modulation scheme. Moreover, the conducted interference is also effectively reduced. The experimental results validate the effectiveness of the proposed modulation scheme.**

***Index Terms*—Common mode (CM) voltage, current source inverter (CSI), leakage current, modulation scheme.**

I. Introduction

LEAKAGE current is one of the major concerns for photovoltaic (PV) inverters due to its potential safety issues [1], [2], [3]. PV inverters are mainly categorized into voltage source inverters (VSIs) and current source inverters (CSIs) [4]. Because reverse-voltage-blocking (RB) switch with higher conduction loss has to be used in CSIs, VSIs are typically more efficient than CSIs [5], which results in VSIs are the main solution in the PV inverter market [6], [7]. However, electrolytic capacitors in VSIs limit their reliability due to electrolyte evaporation [8], [9] and the potential risk of overcurrent due to the bridge leg shoot-through may lead to system failure. In contrast, CSIs avoid using bulky electrolytic capacitors and allow bridge leg shoot-through [10]. Moreover, the continuous dc-link current in the CSI benefits the maximum power point tracking (MPPT), and the inherent boost capability allows the CSI to interface low-voltage PV panels with the grid in a single stage to eliminate the need for a front-stage dc–dc converter [11]. Thus, CSIs have the potential to replace the VSIs in PV applications and may experience a revival in the near future [12]. However, like VSIs, leakage current is also a challenging problem in CSIs [13], [14].

Solutions to leakage current reduction mainly include modifying circuit topologies and modulation schemes. In [15], a space vector modulation (SVM) with reduced common mode (CM) voltage in the current source converter is proposed, where the vector sequence is arranged according to the selected zero vector. The methods for adding auxiliary switches are proposed in [10] and [16] for CH7 and CSI7 topologies, respectively. Instead of the conventional zero vector by the conduction of the auxiliary switch, which effectively reduces the CM voltage and the leakage current. A four-leg CSI with a new SVM is proposed in [17], which significantly reduces the CM voltage by the improved topology and modulation scheme. Besides, Sahan et al. [18] improved the SVM and topology with two X2-type capacitors and neutral wire, and this topology is referred to as split-capacitor four-wire CSI. However, as the X2-type capacitor is very small, there is a limited effect in reducing the leakage current. A similar topology is also presented for three-phase buck rectifier to suppress the high-frequency distortion of input currents [19]. However, a low-frequency current in the neutral wire can be observed, which is not conducive to reducing leakage current. Furthermore, a four-leg CSI with split-capacitors is proposed in [20]. However, the balance of the capacitor midpoint voltage is ignored, and the added fourth leg increases cost and implementation complexity. A CSI7 topology with internal current return path is presented in [21] to address the leakage current issue and reduce the neutral wire current. In fact, the neutral wire current in the split-capacitor four-wire CSI can be addressed by designing proper controllers and modulation schemes. Finally, a modulation scheme with zero average CM voltage is proposed for the split-capacitor four-wire CSI in [22], which ensures approximate zero neutral wire current, and reduces the leakage current obviously. Similar concept has also been used in the four-wire VSI to reduce leakage current [23]. However, compared to the conventional topologies, both of them have reduced the utilization of dc-links (current or voltage) [24]. For clarity, the state-of-the-arts of leakage current suppression techniques for CSI are summarized in Table I.

The leakage current of the split-capacitor four-wire CSI in [22] is mainly related to the impedance of the neutral wire and

Manuscript received 17 October 2022; revised 4 March 2023 and 20 May 2023; accepted 10 July 2023. Date of publication 18 July 2023; date of current version 1 September 2023. This work was supported in part by the National Natural Science Foundation of China under Grant 62125308, in part by the Science and Technology Innovation Program of Hunan Province under Grant 2020RC4002, in part by the Changsha City Science and Technology Plan Project under Grant kq2206013 and Grant kq2208278, and in part by the Central South University Innovation-Driven Research Programme under Grant 2023CXQD020. Recommended for publication by Associate Editor C. Rim. *(Corresponding author: Li Jiang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3296694.

Digital Object Identifier 10.1109/TPEL.2023.3296694

TABLE I
PERFORMANCE COMPARISONS FOR VARIOUS LEAKAGE CURRENT SUPPRESSION TECHNIQUES

	[10]	[15]	[16]	[17]	[18]	[19]	[20]	[21]	[22]
Modulation type	SVM	SVM	SVM	SVM	SVM	SVM	SVM	SVM	Carrier
Number of additional devices	1	0	1	2	0	0	2	1	0
CM voltage magnitude	Small	High	Small	Small	Small	High	High	Low	Low
Neutral wire current	–	High	–	–	High	High	High	Low	Low
Leakage current	Small	Large	Small	Small	Small	High	High	Low	Low

its CM voltage. If the impedance of the neutral wire is zero, the leakage current can be perfectly mitigated. However, it is impossible to realize zero impedance in practice. Recently, the leakage current limit has been reduced to 100 mA or 30 mA in some countries [25], [26]. To follow the stricter regulations, the leakage current is required to be further reduced. Therefore, it is necessary to reduce the CM voltage to further reduce the leakage current. In this article, a carrier-based modulation scheme with reduced CM voltage is proposed. The main contributions include the following.

1) The CM equivalent circuit model of the four-wire CSI for leakage current is developed. Based on the model, the importance of the low impedance design of neutral wire to suppress the leakage current is revealed.
2) An improved modulation scheme is proposed to further reduce the CM voltage of the four-wire CSI. The resulting CM voltage (peak-to-peak) is half that of the conventional modulation. Moreover, the conducted interference is effectively reduced.

The rest of this article is organized as follows. In Section II, CM voltage analysis for PV CSI is introduced. In Section III, the way to arrange the switching sequence is introduced and a modulation scheme with reduced CM voltage is derived. In Section IV, experiments are implemented to validate the proposed modulation scheme. Finally, Section V concludes this article.

II. COMMON MODE CIRCUIT ANALYSIS OF SPLIT-CAPACITOR FOUR-WIRE CSI

A. Topology of Split-Capacitor Four-Wire CSI

The topology of the grid-tied three-phase split-capacitor four-wire CSI investigated in this article is shown in Fig. 1. The CSI is implemented using the developed reverse blocking insulated gate bipolar translators (RB-IGBTs). On the dc side, the PV panels fed a stable current to the inverter through a dc filter composed of the split capacitors ($C_{\rm dc1}$ and $C_{\rm dc2}$) and inductors ($L_{\rm dc1}$ and $L_{\rm dc2}$). On the ac side, the inverter is connected to the grid through a filter composed of ac capacitors (C_f) and inductors (L_f). Different from the conventional CSI, a neutral wire is added to connect the midpoint of the dc link (O') and the neutral point of the ac filter capacitors (O), and Z_N denotes the impedance of the neutral wire. C_{pv1} and C_{pv2} represent the parasitic capacitors between the PV panels and ground, which are 50–150 nF/kWp for glass-faced modules and 1 μF/kWp for thin-film modules [3].

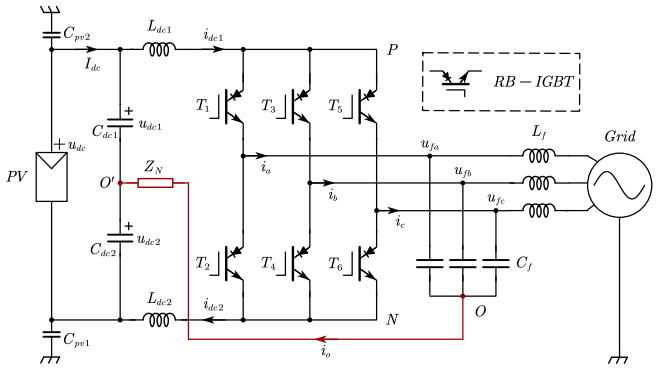

Fig. 1. Topology of PV CSI with reduced leakage current.

B. CM Equivalent Circuit Model

The equivalent circuit of the PV CSI is shown in Fig. 2(a). Z_N represents the parasitic impendence of the added neutral wire connecting the points O and O'. The voltages v_{PO} and v_{NO} are expressed as

$$v_{PO} = \begin{bmatrix} d_1 & d_3 & d_5 \end{bmatrix} \begin{bmatrix} u_{fa} & u_{fb} & u_{fc} \end{bmatrix}^T \tag{1}$$

$$v_{NO} = \begin{bmatrix} d_2 & d_4 & d_6 \end{bmatrix} \begin{bmatrix} u_{fa} & u_{fb} & u_{fc} \end{bmatrix}^T \tag{2}$$

where d_1–d_6 are the duty cycle of the switches T_1–T_6, respectively.

As the common equivalent circuit is concerned, the equivalent circuit is reduced to that shown in Fig. 2(b). Furthermore, since the impedance of bulk capacitors ($C_{\rm dc1}$, $C_{\rm dc2}$, and C_f) is very small at high frequencies, they are usually considered as short circuited in CM circuits, as illustrated in Fig. 2(c). According to Thevenin theorem, the circuit in Fig. 2(c) can be further simplified, as shown in Fig. 2(d), where the equivalent voltage v_{eq}, leakage current $i_{\rm leakage}$ are expressed as

$$v_{eq} = \frac{Z_N \left[Z\left(L_{\rm dc2}\right) v_{PO} + Z\left(L_{\rm dc1}\right) v_{NO} \right]}{Z\left(L_{\rm dc1}\right) Z\left(L_{\rm dc2}\right) + Z_N \left[Z\left(L_{\rm dc1}\right) + Z\left(L_{\rm dc2}\right) \right]} \tag{3}$$

$$i_{\rm leakage} = \frac{v_{eq}}{Z_1 + Z_2 + Z\left(C_{pv}\right)} \tag{4}$$

where $Z_1 = Z(L_{\rm dc1})//Z(L_{\rm dc2})//Z_N$, $Z_2 = Z(L_f)/3$, and $Z(L_{\rm dc1})$, $Z(L_{\rm dc2})$, $Z(L_f)$, and $Z(C_{pv})$ represent the impedance of $L_{\rm dc1}$,

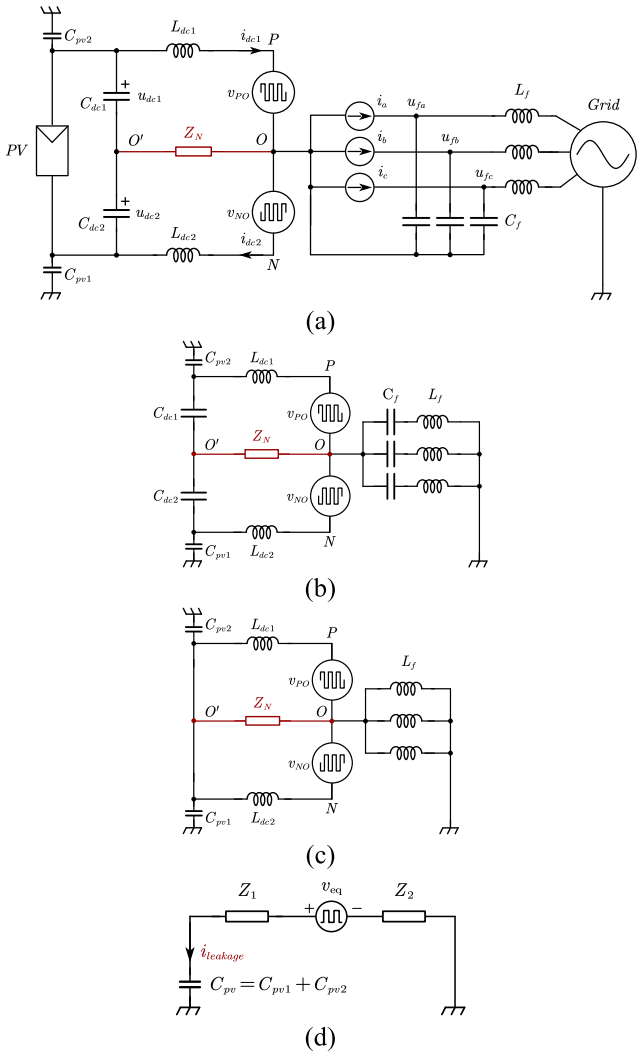

Fig. 2. CSI CM equivalent circuit model. (a) Equivalent model. (b) Reduced CM equivalent circuit. (c) CM Equivalent circuit at high frequency. (d) Simplified CM equivalent circuit.

L_{dc2}, L_f, and C_{pv}, respectively. Rewrite (3), we have

$$v_{eq} = \frac{Z_N\left\{\left[Z\left(L_{dc1}\right)+Z\left(L_{dc2}\right)\right]v_{cm}+\left[Z\left(L_{dc2}\right)-Z\left(L_{dc1}\right)\right]v_{dm}\right\}}{Z\left(L_{dc1}\right)Z\left(L_{dc2}\right)+Z_N\left[Z\left(L_{dc1}\right)+Z\left(L_{dc2}\right)\right]} \tag{5}$$

where $v_{cm} = (v_{PO} + v_{NO})/2$, which is often referred to as CM voltage, and $v_{dm} = (v_{PO} - v_{NO})/2$, which is different-mode (DM) voltage. Combining (4) and (5), it can be deduced that besides the CM voltage, the DM voltage also contributes to the leakage current when $Z(L_{dc1}) \neq Z(L_{dc1})$. Therefore, in order to reduce the leakage current, the circuit parameters in Fig. 2(c) are designed symmetrically, that is $L_{dc1} = L_{dc2} = L_{dc}$. Assuming that $Z(L_{dc1}) = Z(L_{dc2}) = Z(L_{dc})$, (5) can be simplified to

$$v_{eq} = \frac{Z_N}{Z\left(L_{dc}\right)/2+Z_N}v_{cm} = k\left(Z_N\right)v_{cm}. \tag{6}$$

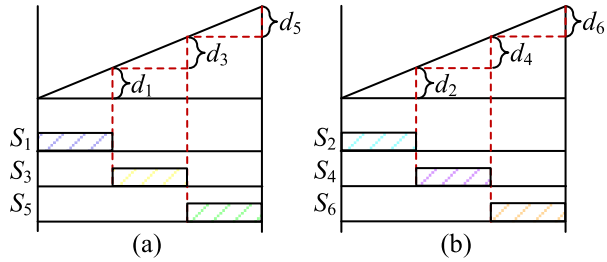

Fig. 3. Conventional switching pattern for CSI. (a) Upper switching pattern. (b) Lower switching pattern.

Clearly, the leakage current depends both on $k(Z_N)$ and v_{cm}. In [10], [16], and [17], the investigated topologies have no neutral wires, which is equivalent to $Z_N \to \infty$, i.e., $k(Z_N) = 1$. Hence, the leakage current can only be suppressed by reducing v_{cm}. While in this article, Z_N can be very small, such that $k(Z_N) << 1$. If Z_N is zero, the leakage current can be theoretically eliminated for any v_{cm}. However, it is not easy to let $Z_N = 0$ in practice. Therefore, optimizing the CM voltage is an important measure to reduce the leakage current further when the hardware configuration of the CSI has been determined.

C. Conventional Modulation and CM Voltage Analysis

The conventional modulation scheme of the PV CSI have been detailed in [22]. Considering the neutral wire current constraint $i_O = 0$, the duty cycles of T_1–T_6 were designed as

$$\begin{cases} d_1 = 1/3 + m_1 u_a^*,\ d_2 = 1/3 - m_2 u_a^* \\ d_3 = 1/3 + m_1 u_b^*,\ d_4 = 1/3 - m_2 u_b^* \\ d_5 = 1/3 + m_1 u_c^*,\ d_6 = 1/3 - m_2 u_c^* \end{cases} \tag{7}$$

where m_1 and m_2 are the modulation indexes for the upper and lower switches and they are less than 1/3; $u_a{}^* = \cos(\theta + \psi)$, $u_b{}^* = \cos(\theta - 2\pi/3 + \psi)$, and $u_c{}^* = \cos(\theta + 2\pi/3 + \psi)$, where θ is the phase information of the grid voltage, ψ is an angle, which depends on specific application requirements.

According to (7), it can be verified that the average values over per switching period of v_{PO} and v_{NO} are constant when m_1 and m_2 are constant. Thus, the volt-second balance of L_{dc1}, L_{dc2} can be satisfied and the neutral wire current can be controlled. In the past modulation methods [18], [19], since the volt-second balance is not guaranteed, a significant neutral wire current is found.

For ease of implementation, carrier modulation is adopted in conventional modulation, as shown in Fig. 3. Fig. 3(a) and (b) shows the switching state of the upper bridge arm switches and lower ones. And the switching patterns are always kept the same. For simplicity, the switching pattern of the conventional modulation is denoted as (1-3-5, 2-4-6).

According to Fig. 1, the CM voltage of the CSI is expressed with switching states

$$v_{cm} = \frac{v_{PO}+v_{NO}}{2} = \frac{[S_1+S_2\ S_3+S_4\ S_5+S_6]}{2}\begin{bmatrix} u_{fa} \\ u_{fb} \\ u_{fc} \end{bmatrix}. \tag{8}$$

TABLE II
CM VOLTAGE CORRESPONDING TO THE SWITCHING STATES

Switching states		On-state switches	CM voltages	Switching states		On-state switches	CM voltages
Active states	a	T_1 , T_4	$-u_{fc}/2$	Zero states	g	T_1 , T_2	u_{fa}
	b	T_1 , T_6	$-u_{fb}/2$		h	T_3 , T_4	u_{fb}
	c	T_3 , T_6	$-u_{fa}/2$		i	T_5 , T_6	u_{fc}
	d	T_2 , T_3	$-u_{fc}/2$				
	e	T_2 , T_5	$-u_{fb}/2$				
	f	T_4 , T_5	$-u_{fa}/2$				

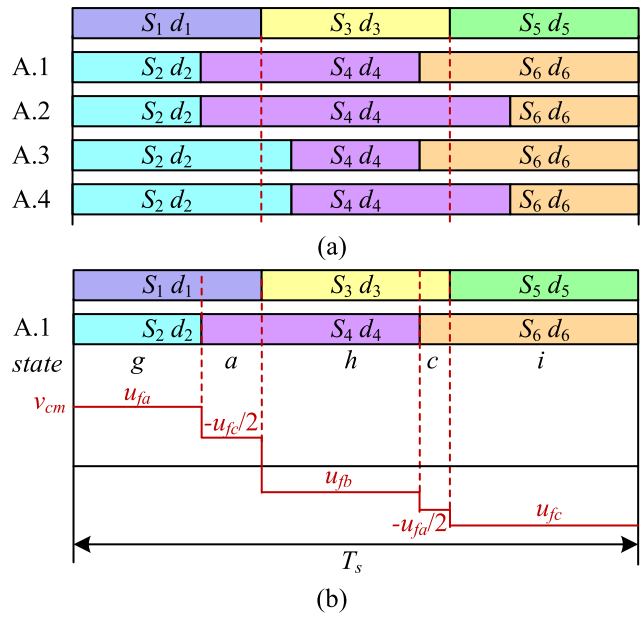

Fig. 4. Conventional switching sequence arrangement of the CSI. (a) Possible case of conventional switching pattern. (b) Switching states and CM voltage of switching sequence (A.1).

Since one and only one switch conducts in each of the upper and lower bridge arms at any time, there are nine different switch states altogether. And the CM voltages corresponding to each switching state are listed in Table II. It can be seen that the CM voltages of zero states are twice as large as those of active states.

According to the values of the duty cycles, there are four possible cases, as shown in Fig. 4(a). Taking the case (A.1) in Fig. 4(a) as an example, there are five switching states in one switching period, as shown in Fig. 4(b). The sequence of the switching states is ***g***-*a*-***h***-*c*-***i***. As seen that all the zero states are adopted in this case, which also means that the peak value and the rate of change of the CM voltage are large.

Because there is no degree of freedom in the duty cycles of the CSI shown in (7), changing the switching sequence (switching pattern) is the only solution to shaping the waveform of CM voltage. Fig. 5 shows the switching pattern after the switching sequence is changed and the switching pattern is denoted as (1-3-5, 4-6-2). It can be observed that the zero state ***g*** is avoided in this case. Therefore, it can be concluded that the CM voltage of the CSI can be changed by arranging the switching sequence.

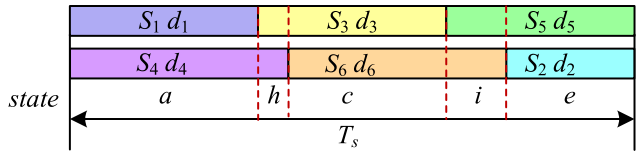

Fig. 5. Switching sequence of (1-3-5, 4-6-2).

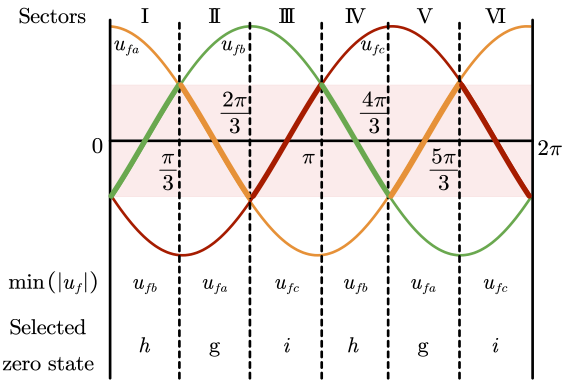

Fig. 6. Voltage sectors and zero state selection.

III. PROPOSED MODULATION SCHEME FOR CM VOLTAGE REDUCTION

Though CM voltage can be changed by arranging the switching sequence, how to arrange the switching sequence to get the desired CM voltage remains unknown. In this section, the way to arrange the switching sequence will be introduced and a modulation scheme with reduced CM voltage will be presented.

A. Selection of Switching Patterns

According to Table I, the CM voltages of zero states are equal to the phase voltages. If only the zero state with the minimum CM voltage (smallest voltage absolute value) appears in switching states, the resulting CM voltage will be reduced greatly. A fundamental frequency cycle can be divided into six sectors, as shown in Fig. 6. To reduce the CM voltage, zero states *h*, *g*, and *i* should be used in sectors I, II, and III, respectively.

Looking at the switching patterns (1-3-5, 6-4-2) and (5-3-1, 2-4-6), which are shown in Fig. 7, it is easy to find that only the zero state "***h***" appears in these cases. The reason for only one zero state can be explained as follows. Because the following inequalities $d_4 + d_6 = 2/3 + m_2 u_a^* > 1/3 + m_1 u_a^* = d_1$, and $d_4 + d_2 = 2/3 + m_2 u_c^* > 1/3 + m_1 u_c^* = d_5$ hold always, the zero states "***g***" and "***i***" cannot appear in those switching patterns. According to the feature of the switching patterns above, it is not difficult to deduce the other useful switching patterns where only one desired zero state appears. And the switching patterns are listed in Table II. For example, in sector II or V, in order to reduce CM voltage, the switching patterns (3-1-5, 6-2-4) or (5-1-3, 4-2-6) should be adopted. And then the CM voltage of the zero state is equal to u_{fa}.

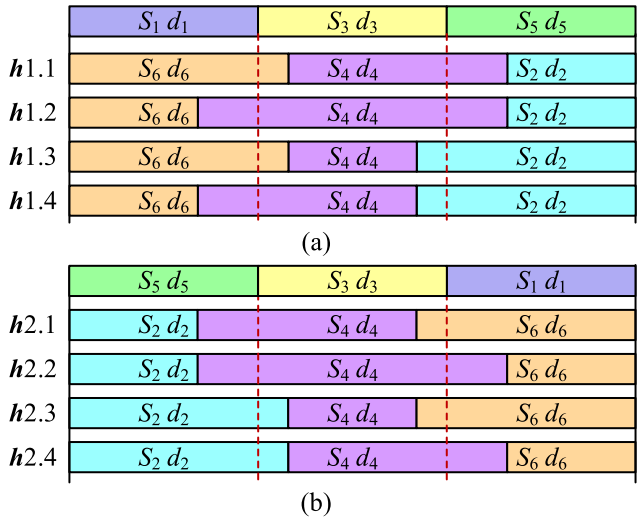

Fig. 7. Optimized switching patterns in sector I. (a) Switching pattern of (1-3-5, 6-4-2). (b) Switching pattern of (5-3-1, 2-4-6).

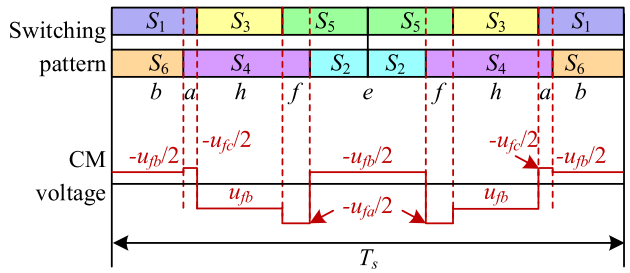

Fig. 8. Symmetrically arranged switching and CM voltage in the sector I.

TABLE III
CM VOLTAGE CORRESPONDING TO THE SPACE VECTORS

Sectors	I and IV		II and V		III and VI	
Zero state	h		g		i	
Switching patterns	(1-3-5, 6-4-2)	$bc\boldsymbol{h}fe$ $bc\boldsymbol{h}de$ $ba\boldsymbol{h}fe$ $ba\boldsymbol{h}de$	(3-1-5, 6-2-4)	$cb\boldsymbol{g}ef$ $cb\boldsymbol{g}af$ $cd\boldsymbol{g}ef$ $cd\boldsymbol{g}af$	(1-5-3, 4-6-2)	$af\boldsymbol{i}cd$ $af\boldsymbol{i}ed$ $ab\boldsymbol{i}cd$ $ab\boldsymbol{i}ed$
	(5-3-1, 2-4-6)	$ed\boldsymbol{h}ab$ $ed\boldsymbol{h}cb$ $ef\boldsymbol{h}ab$ $ef\boldsymbol{h}cb$	(5-1-3, 4-2-6)	$fa\boldsymbol{g}dc$ $fa\boldsymbol{g}bc$ $fe\boldsymbol{g}dc$ $fe\boldsymbol{g}bc$	(3-5-1, 2-6-4)	$de\boldsymbol{i}ba$ $de\boldsymbol{i}fa$ $dc\boldsymbol{i}ba$ $dc\boldsymbol{i}fa$

B. Switching Sequence Arrangement

Furthermore, in order to reduce the current ripple, the switching sequence is arranged symmetrically. As an example, the rearranged switching sequence in the sector I is shown in Fig. 8, which is also called as switching pattern (1-3-5-3-1, 6-4-2-4-6). The switching pattern is the combination of the two switching patterns: (1-3-5, 6-4-2) and (5-3-1, 2-4-6) in Table III.. Obviously, only the zero state $\boldsymbol{h}$ exists, and its corresponding CM voltage is only half of the grid voltage amplitude at maximum according to Fig. 6. This means that with the proposed switching pattern, the peak value of the CM voltage is half that of the conventional modulation scheme.

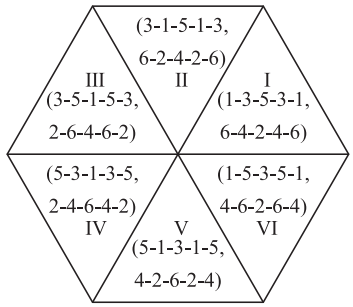

Fig. 9. Switching patterns of the proposed modulation scheme.

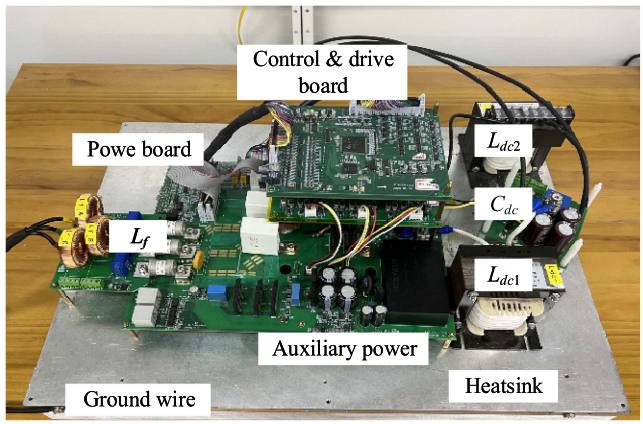

Fig. 10. Experimental prototype of the CSI system.

In addition, in order to reduce the number of switching operations during sector switching, the overall switching patterns of the proposed modulation scheme are shown in Fig. 9. It should be noted that the sector number in Fig. 9 is only used to determine the appropriate switching pattern rather than the vector synthesis in SVM. It is obvious that a minimal number of commutations can be achieved under such a switching pattern arrangement.

IV. EXPERIMENTAL RESULTS

A. Experimental Prototype and Setup

In order to verify the effectiveness of the proposed modulation scheme, the experimental tests are carried out on a laboratory prototype, which is shown in Fig. 10. Main parameters are listed in Table IV. The design methods of passive components refer to [27], which is no longer detailed due to page limits. The PV array is simulated by an ITECH IT6018C photovoltaic simulator. Compared with the real PV systems, the parasitic capacitance of the PV simulator is negligibly small. Thus, to match the reality, extra capacitors are connected between earth and the dc buses of CSI intentionally. In this setup, two 22 nF film capacitors are used. The main circuit is implemented by a subset of the Fuji 18MBI100W power module, where the RB-IGBT technology is employed.

Fig. 11 shows the control block diagram of the PV CSI system. The phase-lock loop (PLL) is applied to obtain the phase information of the grid voltage. The proportional controller

TABLE IV
SYSTEM PARAMETERS FOR CSI

Symbol	Descriptions	Value
C_{dc1}, C_{dc2}	Dc-link capacitance	160 μF
L_{dc1}, L_{dc2}	Dc inductance	5 mH
C_f	Ac filter capacitance	20 μF
L_f	Ac filter inductance	3 mH
u_g	Grid line voltage, rms	380 V
ψ	Phase angle	0
f_{sw}	Switching frequency (same to sampling frequency)	20 kHz
t_d	Overlap time	1.5 μs
k	Voltage balance controller parameter	50
k_{p1}	Proportion of PI (1) controller	0.08
k_{i1}	Integration of PI (1) controller	16.19
k_{p2}	Proportion of PI (2) controller	45.24
k_{i2}	Integration of PI (2) controller	6.3×10^4
P	Rated power	2500 W
u_{dc}	PV panels MPP voltage, $u_{dc}=u_{dc1}+u_{dc2}$	250 V
C_{pv}	PV panels parasitic capacitance, $C_{pv}=C_{pv1}+C_{pv2}$	44 nF

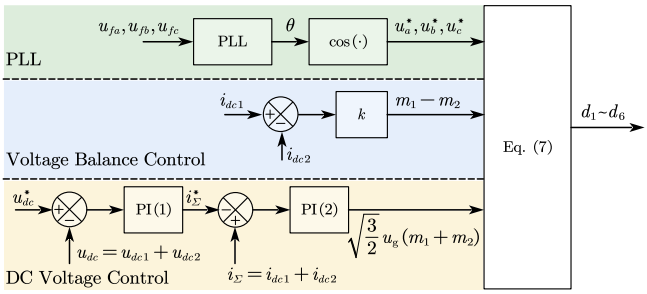

Fig. 11. Block diagram of the PV CSI control system.

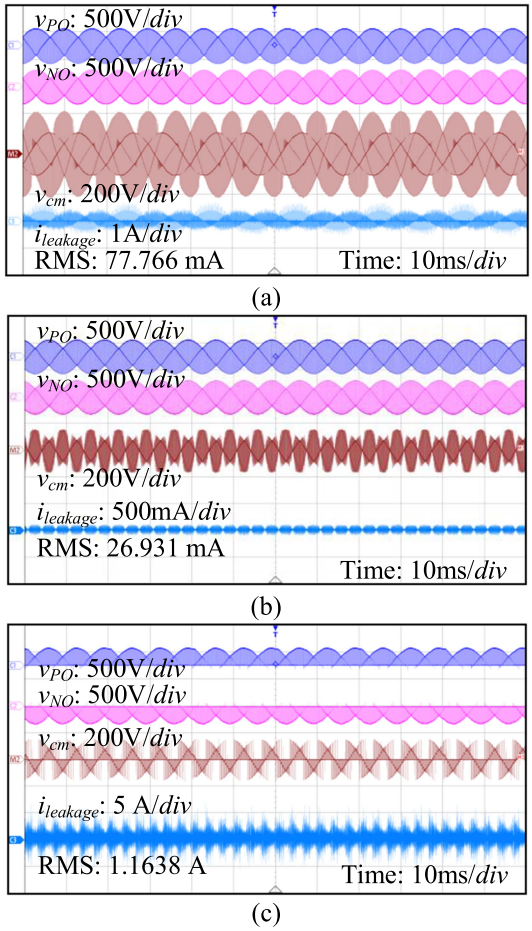

Fig. 12. CM voltage and leakage current waveforms. (a) Conventional modulation scheme of the four-wire CSI. (b) Proposed modulation scheme of the four-wire CSI. (c) Proposed modulation scheme in [17] of the four-leg CSI.

is used in the voltage balance control loop. The neutral-point voltage balance is realized by making $i_{\rm dc1}$ and $i_{\rm dc2}$ equal. The control mechanism is referred to [22]. In PV application, the dc-link voltage reference comes from MPPT algorithms. The dual close-loop control is employed to regulate the dc-link voltage and current. The parameters of the proportional integral (PI) controllers are listed in Table IV, and the frequency domain analysis method is applied for their tuning [28]. To satisfy the time-scale separation criterion and MPPT requirements, the bandwidths of controller's inner and outer loop are set to 4.5 kHz and 500 Hz, respectively.

B. *Effectiveness of the Proposed Modulation Scheme*

Fig. 12 illustrates the measured waveforms under the conventional modulation scheme and the proposed one. Fig. 12(a) shows the measured waveforms of CM voltages and leakage currents under the conventional modulation scheme. Fig. 12(b) shows the corresponding measured results under the proposed one. It is easy to find that the CM voltage (peak-to-peak) under the conventional modulation scheme is almost twice as large as that under the proposed one, which coincides with the theoretical result. The leakage current under the conventional modulation scheme and the proposed one are 77.76 mA and 26.93 mA (rms), respectively. It is evident that the proposed modulation method effectively reduces the leakage current. Fig. 12(c) shows the CM voltage and leakage current of a four-leg CSI proposed in [17] with the same circuit parameters. Since the four-leg CSI cannot eliminate the leakage current, its measured leakage current reaches 1.16 A. It demonstrates that the four-wire CSI has a much lower leakage current level.

Fig. 13(a) shows the output current of CSI before CL filter under the proposed modulation scheme, where the CSI outputs bipolar current with a reduced CM voltage. Fig. 13(b) shows gating voltage during one switching period in sector I.

Fig. 14(a) and (b) shows the CM voltage spectra. It can be observed that the proposed modulation scheme effectively reduces the CM voltage level at the switching frequency and its multiples.

In addition, Fig. 15 shows the spectrum of the CM current measured by a high frequency current probe R&S EZ-17 and an EMI test receiver R&S ESR7. The results of the CM current spectrum show that the CM current at the switching frequency and its multiples of the proposed modulation are also reduced. Clearly, the proposed modulation is conducive to reducing the conducted interference.

Fig. 16 shows the experimental waveforms of the CSI system in normal operation under the proposed modulation scheme.

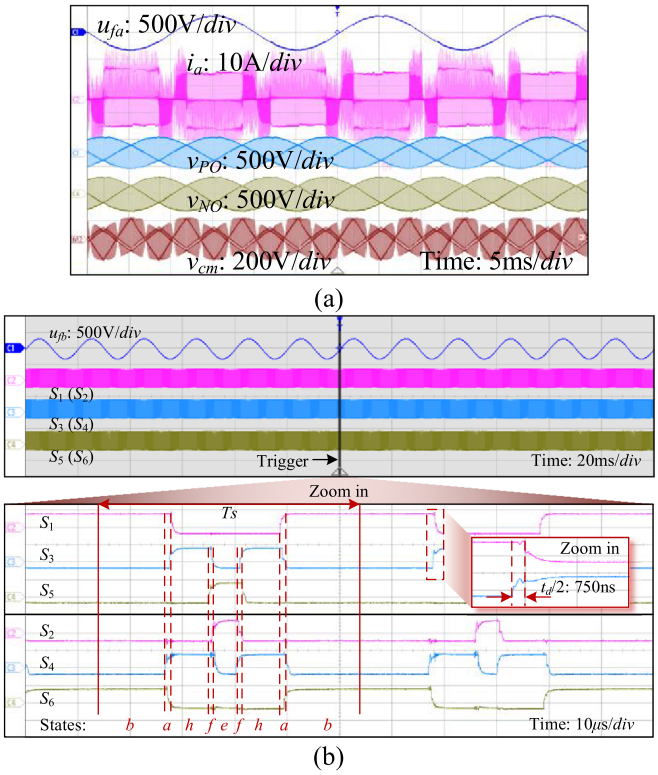

Fig. 13. CSI output current and switching pattern. (a) Output current of the CSI before the CL filter. (b) Gating voltage within one switching period.

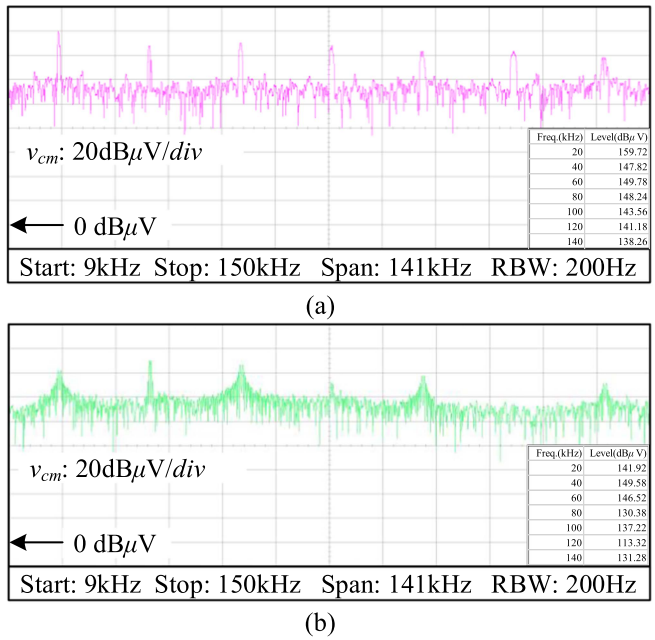

Fig. 14. CM voltage spectrum of CSI with (a) conventional modulation scheme; and (b) proposed modulation scheme.

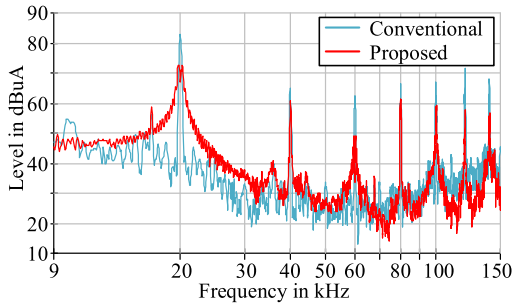

Fig. 15. Spectrum of CM current.

Fig. 16(a) shows the three-phase grid current waveforms. The results show that three-phase balanced, and sinusoidal currents are achieved. Fig. 16(b) presents the i_{dc1}, i_{dc2}, i_o, and u_{dc} of the CSI system. It can be observed that the two dc currents through positive and negative busbars are equal and constant. Meanwhile, the neutral wire current is almost zero. By contrast, the neutral wire current is large and fluctuant under the past modulation and control schemes [18], [19].

Fig. 17 presents the experimental waveforms when the PV panels operating at different irradiances (different voltages and currents). Fig. 17(a) illustrates the MPP of the PV panel operating at 230 V and 7 A under a low irradiance. In this case, the CM voltage and leakage current of the conventional modulation scheme and the proposed one are shown in Fig. 17(b) and (c), respectively, and the corresponding leakage current is 76.867 mA and 30.143 mA. Compared to the leakage current in the rated condition, it is evident that the different MPP voltages and currents of the PV panel have negligible effect on the CM voltage and leakage current.

Fig. 18 presents the experimental results under dynamic operation. Fig. 18(a) illustrates the operation from null to full load. At instant t_1, the dc current steps from 0 to rated 10 A, with a rise time about 10 ms. Fig. 18(b) shows that irradiance and temperature changes begin at t_2. As the irradiance decreases and temperature increases, the PV MPP voltage decreases slightly, and the MPP current decreases from 10 A to 7 A. Since these changes are relatively slow, the regulation time of CSI is about 0.11 s, with about 99.1% dynamic MPPT efficiency. The abovementioned experimental results show that the CSI has good dynamic performance.

C. Comparison of Efficiency

According to the operating principle of CSI, the conduction losses of conventional modulation scheme and the proposed one are equal [17]. Thus, the differences in efficiency under different modulation schemes depend on switching losses. The switching losses of the CSI under the proposed modulation increase due to more commutations compared with that under the conventional modulation. On the other hand, because the current ripple is smaller with the proposed modulation when the same modulation period is used, a longer modulation period can be selected (lower switching frequency).

Fig. 19 shows the measured efficiency under different power ratios with the conventional and proposed modulation schemes. Moreover, the efficiency curve of the CSI under proposed modulation with a reduced switching frequency is also included in Fig. 19. And the switching frequency is selected based on the

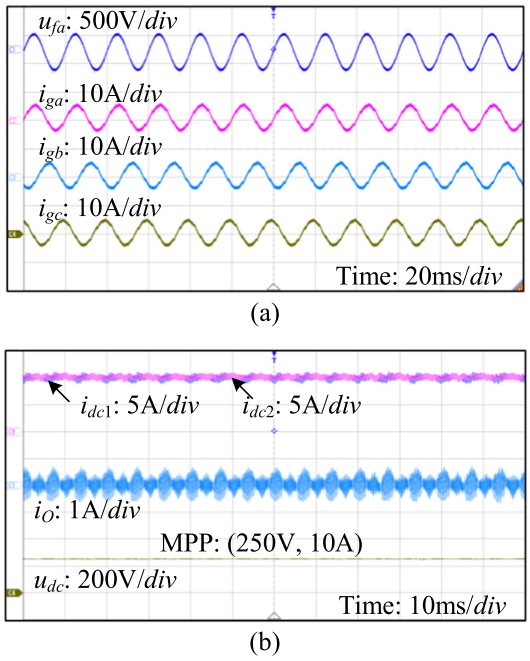

Fig. 16. Experimental waveforms of the CSI system in operation (MPP: 250 V, 10 A). (a) u_{fa}, i_{ga}, i_{gb}, and i_{gc}. (b) i_{dc1}, i_{dc2}, i_o, and u_{dc}.

principle that current ripples are equal. According to the results shown in Fig. 17, the calculated California (CAL) efficiencies are: 77.27% under the conventional scheme, 76.20% under the proposed one with the same switching frequency, and 78.22% with the reduced switching frequency.

It should be noted that the measured efficiency is not high. The reasons are twofold. First, the power losses of the used power switches are relatively large. Second, the main purpose of the prototype is to demonstrate the effectiveness of the proposed scheme, and it is not specially designed for improving efficiency. Indeed, due to the reverse-voltage-blocking (RB) switches, the efficiency of CSI is lower. Fortunately, the development of WBG-based bidirectional switches with RB capability and significantly lower conduction loss opens the possibility of building higher efficiency CSIs [29], [30].

D. Effect of Neutral Wire Impedance on Leakage Current

To evaluate the effect of the neutral wire impedance on leakage current, a 39 μH inductor is connected in series with the neutral wire. Fig. 20 illustrates the measured results. Fig. 20(a) shows the measured waveforms of CM voltages and leakage currents under the conventional modulation scheme. Fig. 20(b) shows the corresponding measured results under the proposed one. As seen, the leakage current increases from 77.766 mA to 282.837 mA under the conventional scheme with a large neutral wire impedance. By comparison, the leakage current only increases from 26.931 mA to 71.019 mA under the proposed one in the same case. The results highlight the importance of the proposed modulation scheme, when it is difficult to control the neutral wire impedance.

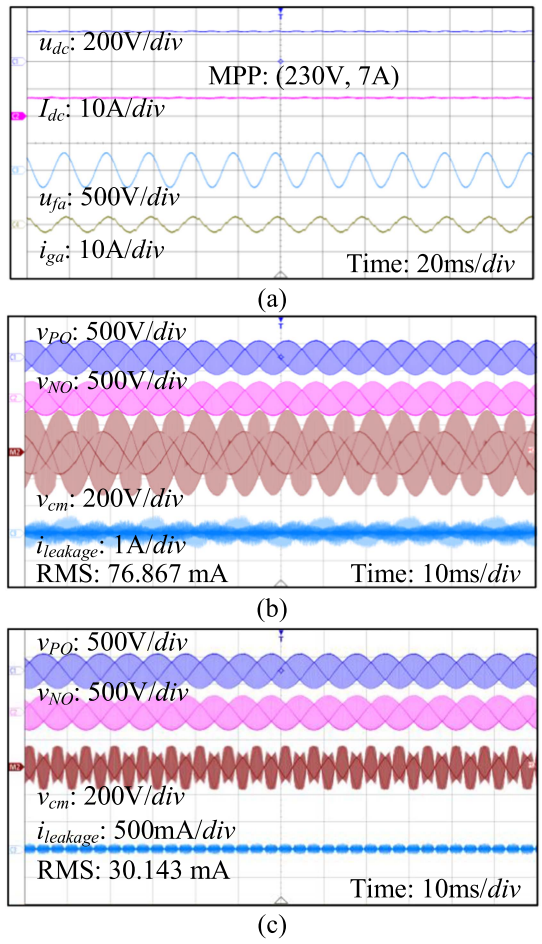

Fig. 17. CM voltage and leakage current with a lower irradiance (MPP: 230 V, 7 A). (a) u_{dc}, I_{dc}, u_{fa}, and i_{ga}. (b) Conventional modulation scheme. (c) Proposed modulation scheme.

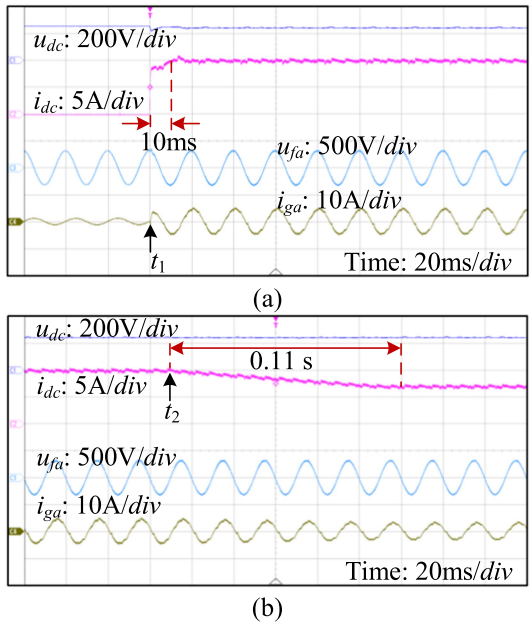

Fig. 18. Experimental waveforms under dynamic operation. (a) Null to full load operation. (b) Irradiation and temperature changes.

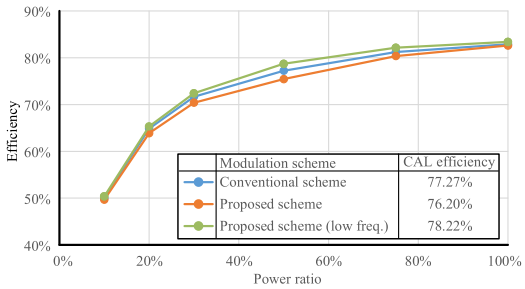

Fig. 19. Measured efficiency of the prototype.

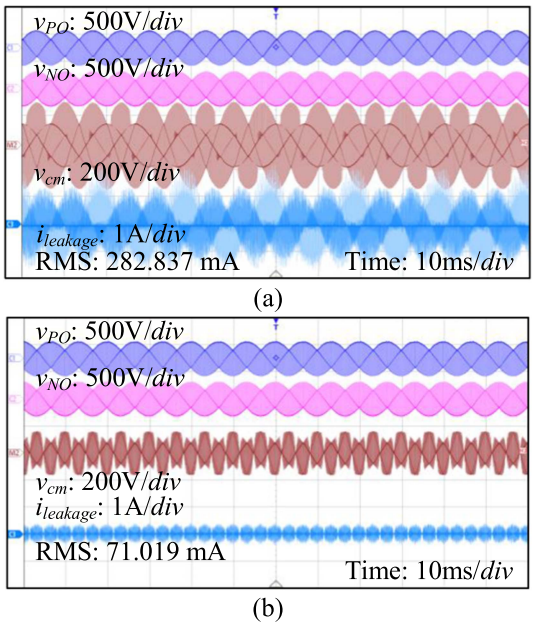

Fig. 20. CM voltage and leakage current with extra neutral wire inductance. (a) Conventional modulation scheme. (b) Proposed modulation scheme.

V. Conclusion

This article has presented a carrier-based modulation scheme to reduce the leakage current of the three-phase split-capacitor four-wire CSI. The switching sequence is rearranged to minimize the CM voltage. Compared to the conventional modulation, the proposed one reduces the CM voltage by half. In addition, conducted disturbances are also reduced. The proposed modulation scheme is verified by experimental results.

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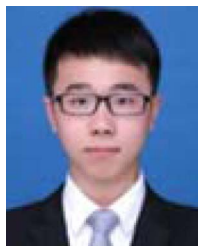

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