A High Step-Down Partial Power Processing Switched-Capacitor Converter for Wide Input Voltage Range Medium Voltage DC Applications

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***Abstract*—This article proposed a partial power processing switched-capacitor converter (P^3SCC) for medium voltage dc applications, where a high-frequency switched-capacitor converter (HFSCC) operating in a series resonant state is used to transmit most of the power, and the remaining small power is regulated by a partial power processing phase-shift full bridge (P^4SFB). Different from the conventional switched capacitors that use a dc bus to transfer energy from the highest voltage capacitor to the lowest voltage capacitor step by step, the P^3SCC transfers power directly from each input capacitor to the load synchronously via the HFSCC, with uniform distribution of voltage and current stress, so the proposed one is more suitable for medium voltage high power conversion. Moreover, the P^4SFB controls the HFSCC voltage amplitude by phase-shifting with the main power HFSCC, eventually regulating the output voltage, the main power is transmitted through only one resonant converter and soft switching of the main power MOSFETs is achieved. The P^3SCC has higher efficiency in medium voltage wide input range voltage regulation applications, since the P^4SFB process half the current of the conventional partial power converter. A 1–1.6-kV dc input with 100-V dc/1 kW output prototype is built to verify the feasibility of the proposed topology.**

***Index Terms*—High step-down ratio, medium voltage dc converter, partial power processing, switched-capacitor, wide range voltage regulation.**

I. Introduction

HIGH step-down ratio dc converters linking medium-voltage dc (MVdc) and low-voltage dc (LVdc) systems are widely used in MVDC power grids (5–10 kV dc to 400 Vdc), dc shipboard power systems (6.6–11 kV dc to 480 or 690 Vdc), photovoltaic battery energy storage system, electric vehicle power distribution unit, and so on [1], [2], [3], [4], [5], [6], [7]. In these applications with high voltage step-down ratio and a wide range of input voltage variations, switched-capacitor converters have become a hot topic of research because of the large voltage step-down ratio, the low voltage stress on the device and expandability to higher voltage levels [8], [9], [10], [11].

The energy transfer path of typical switched-capacitor converters is to transfer the energy of capacitors with different potentials to the lowest potential capacitor step by step by changing the switching state, featuring a large number of scalable modules, multiple level combinations, and flexible regulation, but the switching transient current inrush is large, causing high current stress in the power device and difficult to achieve soft switching [12], [13], [14], [15]. Hybrid switched-capacitor converters using series inductors or resonant switched-capacitor can suppress current shocks and achieve soft switching for a certain load range [15], [16]. However, the current and voltage stress balancing of multiple switches requires additional control, increasing the control complexity of power balancing [17]. In order to solve the voltage stress imbalance problem of the submodules, a parallel switched-capacitor branch is proposed in [18] for phase shifting control to achieve voltage balancing of individual submodules, but the number of power switches and capacitors is increased. A method to control capacitor voltage balancing by adjusting the inductor current valley (or minimum) to the same level for each switching state was proposed in [19], automatically capacitor voltage balancing was also achieved, however, additional current detection hardware and the complex control algorithm are still required.

The wide input voltage range is another challenge for MVdc high-power conversion, due to the large range of input voltage variations influenced by line resistance or source voltage fluctuations [20], [21]. Since the switch frequency was limited by power loss and magnetic components, the voltage regulation range of resonant switched-capacitor topology is quite narrow [22]. To expand the voltage regulation ability, a method combining frequency conversion, phase shifting and dead time control for voltage regulation was proposed in [23], but a large amount of arithmetic was required. The combination of multiple active switching units in [24] extends the voltage regulation range, but the connection of capacitors of different voltages causes current surges that need to be buffered by large inductors, which cause electromagnetic interference and increase the size of the

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converter. Using the multistage converter structure shown in [25], switched-capacitor topologies are employed as fixed-ratio dc transformers and a series PWM converter for voltage regulation in the second stage can achieve a wide range of voltage regulation, but the two-stage conversion reduces the overall system efficiency. The partial power handling converter achieves a wide range of voltage regulation and the regulated converter processes only part of the power, reducing losses, which is used in battery charger and PV grid-tied systems [26], [27], but efficiency improvement was limited in applications with high output currents because the partial power converter current at the output is not reduced and needs to be optimized in high step-down applications [28], [29].

To overcome the above-mentioned problems, this article proposes a partial power processing switched-capacitor converter (P^3SCC) for MVdc applications, where the high-frequency switched-capacitor converter (HFSCC) operating in the series resonant state is used to transmit most of the power, and the remaining small power is regulated by a partial power processing phase-shift full bridge (P^4SFB). The P^3SCC transfers power directly from each input capacitor to the load synchronously via the HFSCC, with uniform distribution of voltage and current stress, so the proposed one is more suitable for medium voltage high power conversion. Moreover, the P^4SFB controls the HFSCC voltage amplitude by phase-shifting with the main power HFSCC, eventually regulating the output voltage over a wide input voltage, the main power is transmitted through only one resonance stage and soft switching of the main power MOSFETs over the full voltage range is achieved.

The rest of this article is organized as follows. Section II describes the operating principle of the proposed P^3SCC topology, the output regulation principle and the distribution of power are analyzed in detail and the waveforms of each operating mode are plotted. In Section III, the design basis for key parameters such as the main power transformer of the P^3SCC, resonance parameters, transformer for the P^4SFB, and the selection of inductors and capacitors. The control strategy for output voltage regulation over a wide input range is also analyzed in detail. In Section IV, the output voltage regulation results, the submodules input voltage stress and the MOSFETs current stress of the proposed converter, and the soft-switching results are experimentally verified on a 1–1.6 kV input and 100 V/1 kW output converter prototype with the proposed control strategy. Finally, Section V concludes this article.

II. Principles of Operation and Regulation

The topology of the proposed converter consists of 2 m half bridge modules SM#N ($N = 1 \ldots 2$ m) and partial power processing phase shifted full bridge (P^4SFB) converter, where SM#1-SM#2 m are connected in series to block the input medium voltage, operating as a high-frequency switched-capacitor series resonant converter to transmit most of the power with high efficiency, and the power flow direction is shown in the red area in Fig. 1. The partial power output voltage regulation is achieved by adjusting the phase difference between the v_{CD} and the v_{EF} port as shown in Fig. 1 (the reasons for choosing v_{EF} as the port for phase shifting are explained in detail in Section II-B). C_{1N}-C_{2N} are the input dc capacitors and L_{sN} is the inductor to assist in realizing soft switching. L_{sN} is necessary because the medium voltage converter is difficult to realize soft switching due to the high input voltage and the large number of switches. L_{bN} and the balancing capacitor C_{bN} form the HFSCC circuit to realize multiple power units SM#N with different electrical potentials supplying power to the load synchronously to achieve power balancing. Besides, L_{bN} and L_{Lk} is part of series resonant inductor. D_u and D_d are diodes to select the ac input circuit.

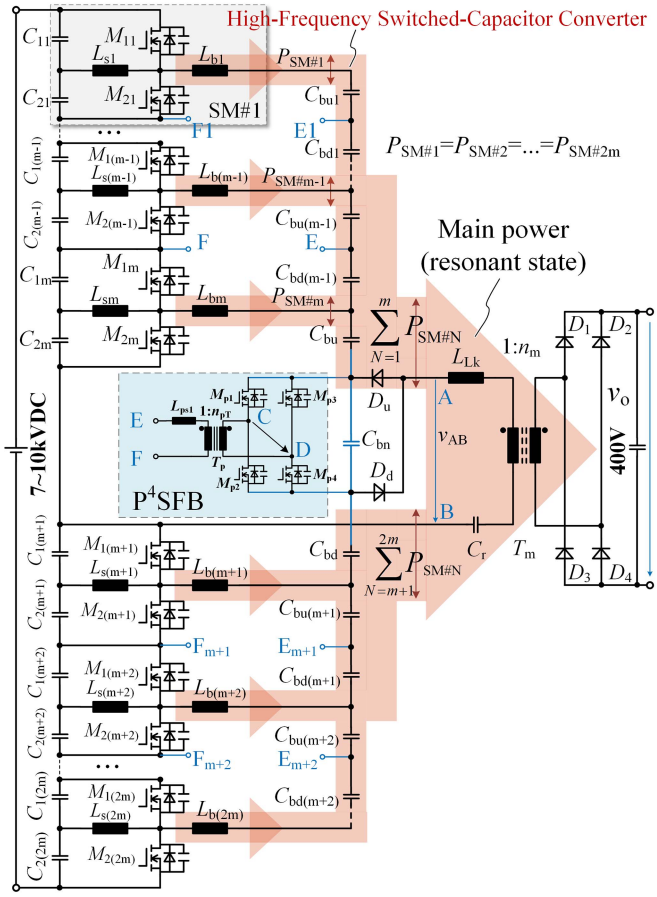

Fig. 1. Composition and power flow of the proposed high step-down ratio converter P^3SCC.

A. Operation Principles

The operation of the proposed converter can be divided into two parts, most of the power is transmitted through the HFSCC and a small portion of the power is transmitted through the P^4SFB converter. As the input voltage rises, the power of P^4SFB increases, as shown in Fig. 2. To simplify the analysis, the output voltage v_{cbn} of P^4SFB is equivalent to a controlled voltage source. The voltage of the resonant tank is divided into two stages, 0–T_s/2 and T_s/2–T_s, and the switching states and power flow directions of the two stages are shown in Fig. 3(a) and (b).

In the 0–T_s/2 stage, M_{1N} turned ON, M_{2N} turned OFF, and the resonant tank input voltage $v_{AB} > 0$, the power flow is shown

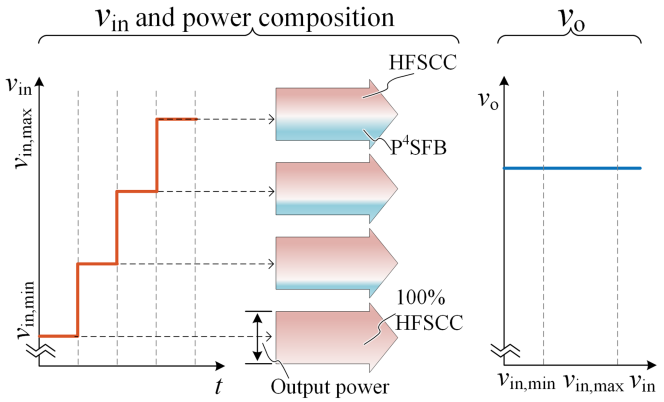

Fig. 2. Power distribution of the P³SCC in the HFSCC (operating in series resonant state) and P⁴SFB with varying input voltage.

in Fig. 3(a). The composition of v_{AB} is

$$v_{AB} = \begin{bmatrix} v_{11} - Z_{M11}\left(i_{M11} - i_{Ls1}\right) \\ v_{12} - Z_{M12}\left(i_{M12} - i_{Ls2}\right) \\ v_{13} - Z_{M13}\left(i_{M13} - i_{Ls3}\right) \\ v_{14} - Z_{M14}\left(i_{M14} - i_{Ls4}\right) \end{bmatrix}. \quad (1)$$

v_{11}–v_{14} are equivalent voltage sources with the following composition:

$$\begin{bmatrix} v_{11} \\ v_{12} \\ v_{13} \\ v_{14} \end{bmatrix} = \begin{bmatrix} v_{SM1} + v_{SM2} - v_{Cbu1} - v_{Cbd1} - v_{Cbu} - v_{Cbn} \\ v_{SM2} - v_{Cbu} - v_{Cbn} \\ v_{Cbd} \\ v_{Cbd} + v_{Cb3} - v_{SM3} \end{bmatrix}. \quad (2)$$

Z_{11}–Z_{14} is the equivalent internal impedance of the power supply, composed of (3) shown at the bottom of the next page.

In the $T_s/2$–T_s stage, M_{1N} turned OFF, M_{2N} turned ON, and the resonant tank input voltage $v_{AB} < 0$, the power flow is shown in Fig. 3(b). The calculation of the voltage and current is similar to the 0–$T_s/2$ stage.

The balance of the dc link capacitor voltages v_{SM1} to v_{SM4}, v_{Cbu} and v_{Cbd} is analyzed as follows: taking SM#1 and SM#2 as an example for simplified analysis. Fig. 4(a) shows the switching states in the period 0–$T_s/2$. The power transfer path of multiple submodules supplying energy to the load via C_{buN} and C_{bdN} is shown in Fig. 4(b). For the power circuit of SM#1, the circuit consisting of C_{11}, C_{21}, L_{s1}, L_{b1}, C_{bu1}, and C_{bd1} contains two components: the current i_{Ls1} for L_{s1} and the current i_{M11} to the loads Z_{AB} and Z_{EF}, as shown in Fig. 4(b). i_{Ls1} is mainly used to assist in the implementation of soft switching, and the L_{s1} branch can be ignored when considering multiple supplies to power the loads. The load power supply circuit is simplified in Fig. 4(c). The input voltage v_{SMN} of each module and the balanced capacitor voltage v_{cbuN} and v_{cbdN} are

$$\begin{bmatrix} v_{SM1} \\ v_{SM2} \end{bmatrix} = \begin{bmatrix} v_{c11} + v_{c21} \\ v_{c12} + v_{c22} \end{bmatrix}$$

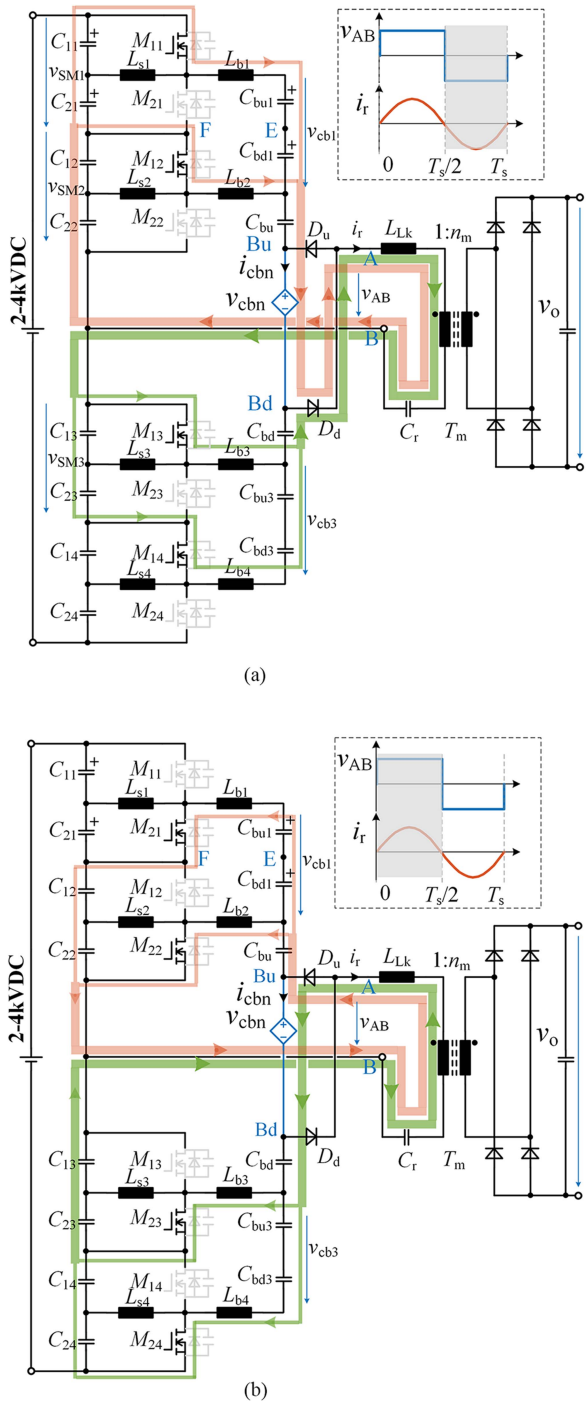

Fig. 3. Two main operating stages of the proposed converter. (a) In the 0–$T_s/2$ stage, M_{1N} is turned ON, M_{2N} is turned OFF and the resonant current i_r is positive. (b) In the $T_s/2$–T_s stage, M_{1N} is turned OFF and M_{2N} is turned ON, with a negative resonant current i_r.

$$= \begin{bmatrix} L_{b1}\frac{di_{Lb1}}{dt} - L_{b2}\frac{di_{Lb2}}{dt} + v_{cbu1} + v_{cbd1} \\ L_{b2}\frac{di_{Lb2}}{dt} - L_{b3}\frac{di_{Lb3}}{dt} + v_{cbu2} + v_{cbd2} \end{bmatrix}. \quad (4)$$

i_{Lb1} and i_{Lb2} can be decomposed into two parts according to their function: the "common mode" currents i_{Lb1C} and i_{Lb2C} that constitute the load Z_{AB} and Z_{EF} currents, and the charge and discharge "balance" currents i_{Lb12B} that are equivalently

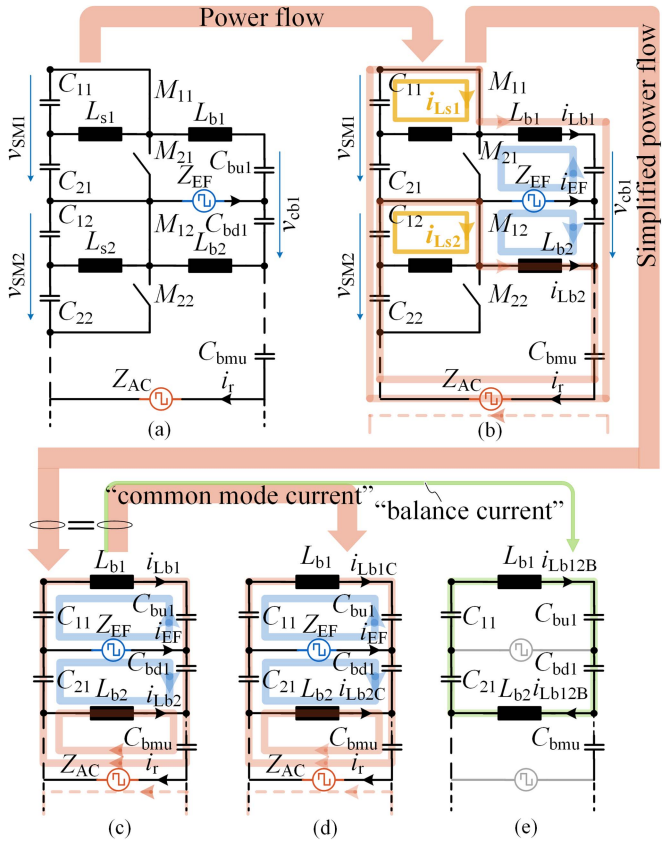

Fig. 4. Equivalent circuit of DC link capacitor self-balancing in the 0–T_s/2 cycle. (a) Switching status of SM#1 and SM#2. (b) Power flow of SM#1 and SM#2. (c) Power flow from SM#1 and SM#2 to the load. (d) "Common mode current" equivalent circuit of SM#1 and SM#2 to the load Z_{EF} and Z_{AB}. (e) "Balance current" circuit between SM#1 and SM#2.

connected in parallel with the adjacent capacitors, as shown in Fig. 4(d) and (e)

$$\begin{bmatrix} i_{Lb1} \\ i_{Lb2} \end{bmatrix} = \begin{bmatrix} i_{Lb1C} + i_{Lb12B} \\ i_{Lb2C} - i_{Lb12B} \end{bmatrix}. \tag{5}$$

The relationship between i_{Lb1C} and i_{Lb2C} is

$$L_{b1}\frac{di_{Lb1C}}{dt} - \Delta v_{SM1} + \Delta v_{cbu1} + \Delta v_{cbd1} = L_{b2}\frac{di_{Lb2C}}{dt}. \tag{6}$$

The voltage fluctuations of L_{b1} and L_{b2} are much larger than Δv_{SM1}, Δv_{cbu1}, and Δv_{cbd1} at the switching frequency, due to the large value of the dc link capacitance, that is

$$L_{b1}\frac{di_{Lb1C}}{dt} - L_{b2}\frac{di_{Lb2C}}{dt} = 0. \tag{7}$$

According to Fig. 4(c)–(e), the balance current is

$$i_{Lb12B} = i_{Lb2C} - i_{Lb1C}. \tag{8}$$

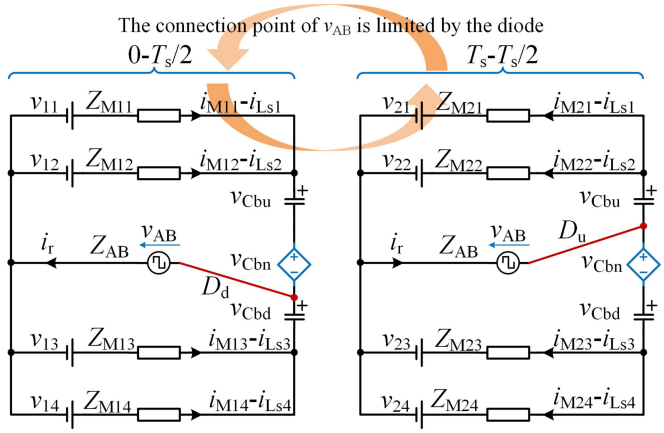

Fig. 5. Composition of the HFSCC power circuit in the 0–T_s/2 and T_s/2–T_s cycles.

In the design, $L_{b1} = L_{b2} = L_{bN} = L_b$, the balance current $i_{Lb12B} = 0$, then $v_{c11}+v_{c12} = v_{cbu1}+v_{cbd1}$, the voltage balance of other modules is the same as the above-mentioned analysis, and the same analysis is T_s/2–T_s, then

$$\begin{bmatrix} v_{SMN} \\ v_{SM(N+1)} \end{bmatrix} = \begin{bmatrix} v_{cbuN} + v_{cbdN} \\ v_{cbu(N+1)} + v_{cbd(N+1)} \end{bmatrix} = \begin{bmatrix} v_{SM(N+1)} \\ v_{SM(N+2)} \end{bmatrix}. \tag{9}$$

According to the above-mentioned analysis, the input voltage of each submodule is automatically balanced. The above-mentioned analysis of the voltage self-balance is independent of the value of the dc link capacitors, therefore the value of the dc link capacitor does not affect the voltage self-balance between the modules. The deviations of the inductors L_{bN-1} and L_{bN} also have no effect on the voltage balance, as the voltage drop across L_b is very small. Based on the above-mentioned operating principle analysis, the output regulation process during the 0–T_s/2 and T_s/2–T_s cycles can be simplified to the voltage source and impedance shown in Fig. 5.

B. Output Regulation Principle

According to (1)–(3) and Fig. 5, v_{AB} depends on v_{in}, v_{cbu}, v_{cbn}, and v_{cbd}. v_{cbn} is related to v_{cbu} and v_{cbd} as

$$\frac{v_{in}}{2m} = v_{cbu} + v_{cbn} + v_{cbd} \tag{10}$$

where $v_{cbu} = v_{cbd}$, due to the current of the series resonant state is symmetrical in the 0–T_s/2 and T_s/2–T_s periods. Therefore, adjusting v_{cbn} can control v_{AB} and eventually achieve output voltage regulation, as shown in Fig. 5.

The method of regulating v_{cbn} is to transfer the energy from v_{cbn} to HFSCC, using a P^{4}SFB that forms a phase shift ac source with HFSCC, where there are many ac ports available for HFSCC, such as v_{E1F1}, v_{EF}, $v_{Em+1Fm+1}$, $v_{Em+2Fm+2}$ … shown

$$\begin{bmatrix} Z_{11} \\ Z_{12} \\ Z_{13} \\ Z_{14} \end{bmatrix} = \begin{bmatrix} \frac{-1}{j\omega C_{11}} - \frac{1}{j\omega C_{21}} - \frac{1}{j\omega C_{12}} - \frac{1}{j\omega C_{22}} - \frac{1}{j\omega C_{bu1}} - \frac{1}{j\omega C_{bd1}} + j\omega L_{b1} \\ \frac{-1}{j\omega C_{12}} - \frac{1}{j\omega C_{22}} + j\omega L_{b2} \\ j\omega L_{b3} \\ \frac{-1}{j\omega C_{13}} - \frac{1}{j\omega C_{23}} - \frac{1}{j\omega C_{b3}} + j\omega L_{b4} \end{bmatrix}. \tag{3}$$

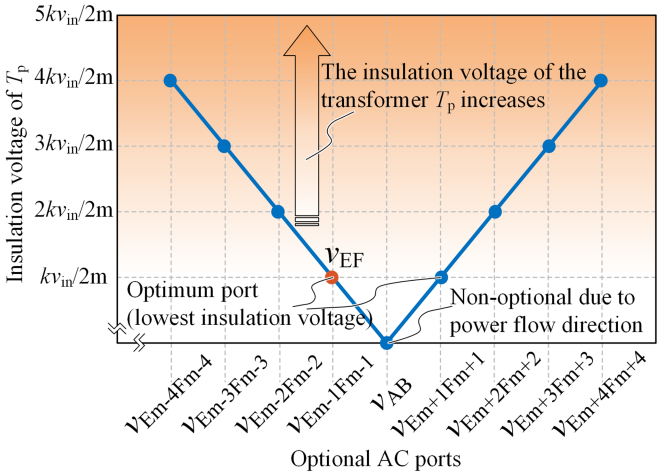

Fig. 6. Relationship between the position of the optional AC port and the insulation voltage of the transformer T_p of the P⁴SFB.

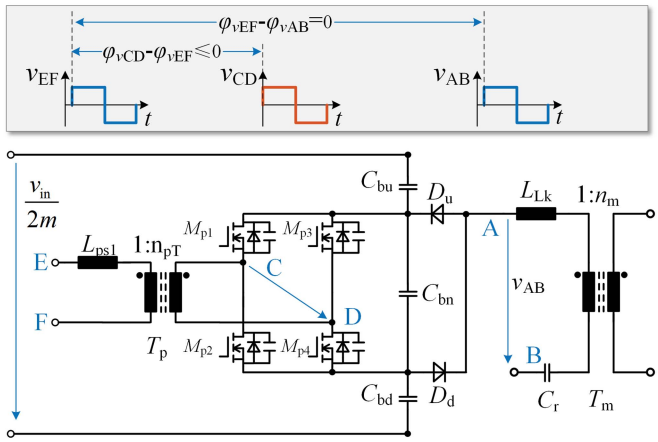

Fig. 7. Composition of P⁴SFB and the phase of the voltage, the phase of v_{CD} is always ahead of v_{EF} and the phase of v_{EF} to v_{AB} is always the same.

in Fig. 1. Due to the consistency of the ac port voltages of the HFSCC, the phase and voltage of these ac ports are identical, the main difference is that the insulation level with v_{cbn} is different. Different choices of the referenced phase-shifted ac port result in different isolation voltage levels for the transformer T_p of P⁴SFB are

$$\begin{bmatrix} v_{iso1} \\ \cdots \\ v_{iso} \\ v_{iso(m+1)} \\ v_{iso(m+2)} \\ \cdots \end{bmatrix} = \begin{bmatrix} mk_{iso}v_{in}/(2m) \\ \cdots \\ k_{iso}v_{in}/(2m) \\ k_{iso}v_{in}/(2m) \\ 2k_{iso}v_{in}/(2m) \\ \cdots \end{bmatrix} \tag{11}$$

where v_{iso1}, v_{iso}, $v_{iso(m+1)}$, and $v_{iso(m+2)}$ are the T_p isolation voltages for the different HFSCC ports selected, k_{iso} is the isolation voltage margin considered in the engineering design, generally k_{iso} = 2–3. The insulation voltage levels required for T_p with the different ac ports selected for HFSCC are shown in Fig. 6, and it can be seen that the lowest isolation voltages are obtained by selecting the v_{EF} or $v_{Em+1Fm+1}$ case. So that v_{EF} or $v_{Em+1Fm+1}$ can be chosen in the design as the v_{CD} phase-shifted secondary ac voltage, and in the subsequent analysis, v_{EF} is chosen as the reference for phase shifting, the port for energy interaction with v_{cbn}.

P⁴SFB is redrawn in Fig. 7, v_{EF} is one of the ac ports for the main power HFSCC, and M_{p1}–M_{p4} are the switches for the additional P⁴SFB converter. By adjusting the phase difference between v_{CD} and v_{EF}, the interaction between the energy of C_{bn} and the energy of the main power HFSCC can be achieved, regulating v_{cbn} and v_o.

In the case of input voltage rise, the regulation principle of the output voltage is shown in Fig. 8. There are three stages, $t = t_0$-t_1, $t = t_1$-t_2, and $t > t_2$, and the working principle of each stage is as follows.

1) In the t_0–t_1 stage, v_{in} is lower, a larger phase shift angle φ_{vCD}–φ_{vAB} is needed to transfer energy from v_{cbn} to the v_{EF} port, lowering v_{cbn} and ensuring constant v_{cbu} and v_{cbd}, which means that v_{AB} is constant, thus achieving regulation of the output voltage v_o. At this stage, the v_{cbn} voltage is low, the power of P⁴SFB is very small, and the main power is processed by HFSCC, achieve high efficiency.
2) In the t_1–t_2 stage, v_{in} rises, the phase shift angle φ_{vCD}–φ_{vAB} needs to be reduced to control the energy transferred from v_{cbn} to the v_{EF} port, it is equivalent to rising v_{cbn}, offsetting the rise in v_{cbu} and v_{cbd} caused by the rise in v_{in}, ensuring that v_{cbu} and v_{cbd} are constant, resulting in v_{AB} is constant, thus achieving the regulation of the output

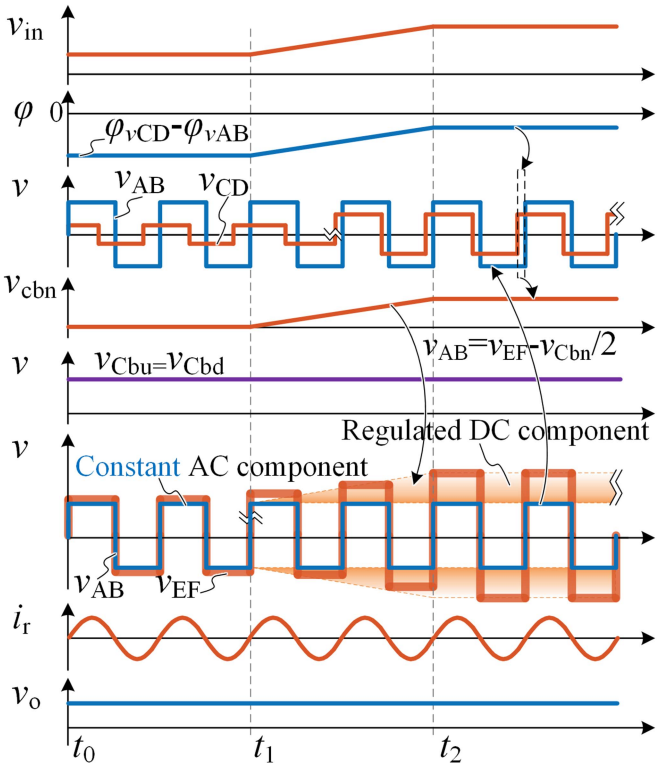

Fig. 8. Principle diagram for output voltage regulation with a wide range of input voltage variations. The v_{AB} and v_o are regulated by changing v_{Cbn} by phase shifting to offset the variation in v_{EF}.

voltage v_o. The v_{cbn} voltage rises at this stage and the power of the P^{4}SFB rises, but the main power is processed by the HFSCC, which still has a high efficiency.

3) In the $t > t_2$ stage, v_{in} is higher, keeping a smaller phase shift angle φ_{vCD}–φ_{vAB}, controlling the energy transferred from v_{cbn} to the v_{EF} port. The v_{cbn} voltage rises at this stage and the power of the P^{4}SFB increases, but the main power is processed by the HFSCC, which still has a high efficiency.

C. Power Distribution and System Efficiency

Based on the above-mentioned analysis, it is clear that the power processed by the P^{4}SFB depends on the input voltage, expressed as

$$P_{P^4SFB} = v_{Cbn} i_{P^4SFB,avg}. \tag{12}$$

v_{cbn} can be obtained from the self-balancing characteristic of the submodules

$$v_{Cbn} = \frac{v_{in}}{2m} - \frac{2v_o}{1/n_m}. \tag{13}$$

According to the operating modes within the 0–T_s/2 period and T_s/2–T_s in Fig. 3, the average value of the load current of P^{4}SFB is

$$i_{P^4SFB,avg} = \frac{2\sqrt{2}}{2\pi} i_{r,rms} \tag{14}$$

where $i_{r,rms}$ is the resonant current, $i_{r,rms}$ can be expressed as

$$i_{r,rms} = \frac{v_o \sqrt{8\pi^2 L_m^2 f_r^2 + 2(1/n_m)^4 R_L^2}}{8(1/n_m) R_L L_m f_r}. \tag{15}$$

L_m is the magnetizing inductor, R_L is the load resistance, and f_r is the resonant frequency, which can be expressed as

$$f_r = \frac{1}{2\pi\sqrt{(L_b/2m) + L_{Lk}}}. \tag{16}$$

L_b is the impedance balance inductor, L_{Lk} is the series inductor, these inductors form the resonant inductor.

Considering $m = 2$, v_{in} = 1–1.6 kV variation, output voltage of 100 V and power of 1 kW, the curve of power variation with turns ratio of HFSCC transformer T_m and input voltage for P^{4}SFB processing is shown in Fig. 9. According to (12)–(16)

1) For a certain output power and input voltage, the power processed by the P^{4}SFB increases with the increase of the transformer turns ratio 1:n_m between the primary and secondary sides. Thus, when considering the variation ratio of the primary circuit, choosing $n_m \leq 1$ enables the P^{4}SFB to process less power.
2) For a certain output power and transformer turns ratio, the P^{4}SFB processing power is close to 0 at the lowest voltage input conditions and the main converter operates at high efficiency; as the v_{in} rises, the power processed by P^{4}SFB is increased. Therefore, it is needed to determine the processing power of the P^{4}SFB according to the variation range of the input voltage.

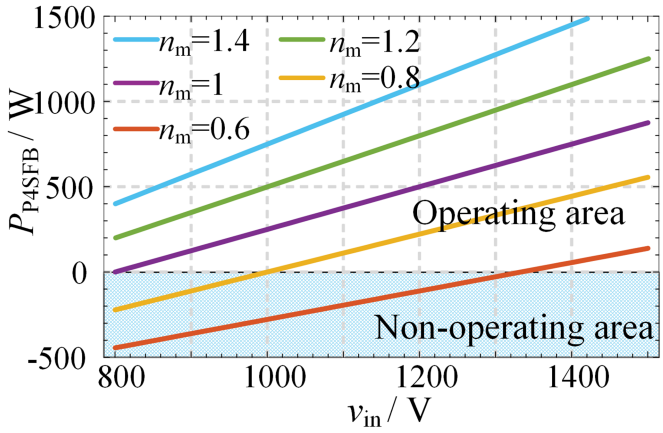

Fig. 9. Power distribution of the P^{4}SFB of the proposed converter versus the input voltage for the different transformer ratios of the HFSCC.

III. Design of Hardware and Control System

A. Design of Hardware

1) Turns Ratio of Main Power Transformer T_m*:* Considering 1–1.6 kV input and 100 V/1 kW output, it is known from the above analysis that the power processed by P^{4}SFB decreases as the primary to secondary ratio of the main power transformer T_m decreases by 1:n_m when the input voltage is certain, and n_m should be chosen smaller for higher efficiency. $n_{m,min}$ should satisfy

$$\frac{v_{in,min}}{4m} > \frac{v_o}{n_{m,min}}. \tag{17}$$

In order to avoid the resonant element parameter deviations resulting in resonant tank gain less than 1, the turns ratio should take a certain margin, and this design takes $n_m = 1$.

The insulation design of the transformer of the MV converter has two difficulties: the design of the parameters and the insulation design, while the soft switching result and gain adjustment of the proposed converter does not depend on the magnetizing inductance of the transformer, the leakage inductance and parasitic capacitance of the transformer and other parameters have less influence on the P^{3}SCC. The main focus is on the insulation design of medium voltage transformers. The transformer is a planar structure, using the PCB for the windings, which facilitates the realization of high-voltage insulation, as shown in Fig. 10. The insulation design has three main aspects:

Distribution of electrical potential points: the primary winding is a suspended high-voltage potential point and the secondary winding is a low-potential point, therefore connecting the secondary winding and the core together avoids the core potential point being uncertain and being struck by high voltage.

Insulation of the primary and secondary windings: the 10 kVdc insulation of the primary and secondary windings is achieved using FR4 insulation boards (dielectric strength >30 kV/mm), with the edges and the core central column hole sections reinforced with polyimide film tape (dielectric strength >60 kV/mm). The insulation of the lead wire of the primary winding and the secondary winding (magnetic core) is achieved

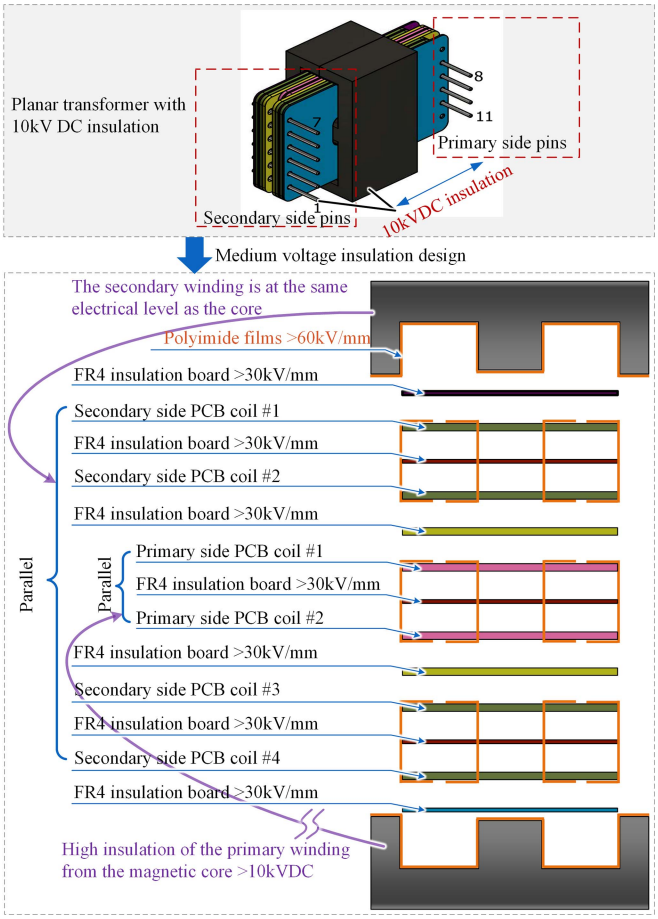

Fig. 10. Insulation design for 10 kV insulated planar transformers.

by the air insulation spacing (dielectric strength >0.5 kV/mm), which is 3 cm in the case of 10 kVdc insulation.

Insulation of the primary and magnetic core: the core is insulated with polyimide film tape on the inner surface and the PCB winding adjacent to the core is also insulated with a polyimide film tape, the insulation structure is shown in Fig. 10. The insulation of the transformer is tested by applying a voltage of 10 kVdc to the primary and secondary sides for one minute and testing the leakage current <4 μA, with no insulation breakdown.

2) Turns Ratio of P⁴SFB Transformer T_p*:* T_p is selected based on the current stress and voltage stress on the primary and secondary sides of the P⁴SFB are similar, which facilitates device selection and circuit design. The range of the secondary voltage v_{cbn} of P⁴SFB is

$$\frac{v_{in,min}}{2m} - 2v_{cbu} < v_{cbn} < \frac{v_{in,max}}{2m} - 2v_{cbu} \tag{18}$$

$$v_{cbu} = v_{cbd} > v_o/n_m. \tag{19}$$

The range of the primary side voltage v_{EF} of P⁴SFB is

$$\frac{v_{in,min}}{4m} < v_{EF} < \frac{v_{in,max}}{4m}. \tag{20}$$

In the case where v_{in} changes from $v_{in,min}$ to $v_{in,max}$, the turns ratio should satisfy $1{:}n_{pT} \approx v_{EF}{:}v_{cbn}$, so that the primary and secondary currents and voltage of P⁴SFB are close to each other and the current and voltage stress is reduced, respectively. Therefore, $1{:}n_{pT} = 1{:}1$.

3) Input Capacitor C_{1N}*,* C_{2N}*, and the Balance Capacitor* C_b*:* C_{1N}, C_{2N}, and C_b are all dc bus capacitors. The capacitance value is not sensitive to the converter design and the same capacitance value can be chosen, 50 μF was chosen for the experimental prototype.

4) Resonant Components L_b*,* L_{rs}*, and* C_r*:* First, determine L_b, according to (3), the value of L_b should satisfy $Z_{11} = Z_{12} = Z_{13} = Z_{14}$, L_b range is

$$j\omega_s L_b > 10\left(\frac{m}{j\omega_s C_{1N}} + \frac{1+m/2}{j\omega_s C_b}\right). \tag{21}$$

Calculating and considering the margin, the inductance value of L_b can be taken as 3 μH or larger due to the small impedance of the dc bus capacitor $1/\omega C_{1N}$, $1/\omega C_{2N}$, and $1/\omega C_b$. Then, according to (16) and transformer leakage inductance L_{rs}, C_r can be calculated as 32 nF.

5) Auxiliary Soft Switching Inductor L_s*:* The soft-switching result of the proposed converter is independent of the magnetizing inductance of transformer. To facilitate transformer design and reduce transformer losses, the magnetizing inductance is much larger than the leakage inductance in the design, and thus the soft-switching charging and discharging current is mainly provided by L_s. The complete charging and discharging of all MOSFET junction capacitors C_{oss} within the dead time should satisfy

$$\begin{aligned} &2mC_{oss}\Delta v_{Coss} + C_{eq}\Delta v_{Ceq} \\ &\le \int_0^{t_d} 2mi_{Coss}(t)dt + \int_0^{t_d} i_{Ceq}(t)dt \end{aligned} \tag{22}$$

C_{eq} is the equivalent capacitance of the main power transformer and the secondary diode. t_d is the dead time, i_{Coss} and i_{Ceq} is the current to charge C_{oss1N} (junction capacitor of M_{1N}), C_{oss2N} (junction capacitor of M_{2N}), and C_{eq}, respectively

$$2mi_{Coss}(t) + i_{Ceq}(t) = \sum_{N=1}^{m} i_{LsN}(t) + i_{Lm}(t). \tag{23}$$

i_{Lm} is small and can be ignored, as the main power operates in the series resonant state, the value of L_m is large. i_{Ls} is equal to a current source during the dead time, (22) can be expressed as

$$mi_{Ls,max}t_d \ge 2C_{oss}v_{in} + C_{eq}v_{in}/m \tag{24}$$

$$i_{Ls,max} = \frac{v_{in}(T_s/2 - t_d)}{4mL_s}. \tag{25}$$

According to the above calculation, $L_s = 200$ μH is selected.

B. Design of Control System

The control system of the proposed converter is shown in Fig. 11. The sampled output voltage v_{o_sam} is feedback to the control system after high voltage isolation and is subtracted from the reference value of the output voltage v_{o_ref}. The voltage difference is processed by proportional integration (PI) to calculate the phase difference between the P⁴SFB and HFSCC,

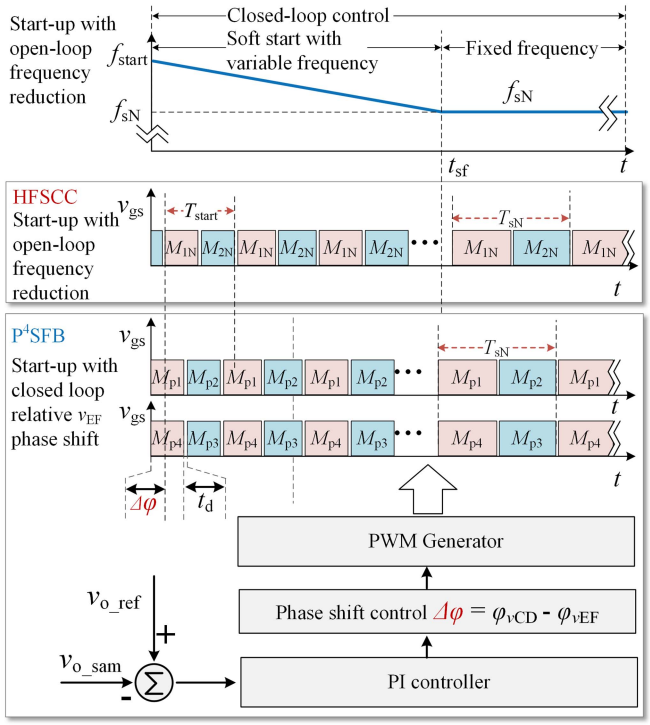

Fig. 11. Block diagram of the phase shift control strategy and gate driver logic of the proposed converter.

TABLE I
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Symbol	Parameter	Values
v_{in}	Input voltage	1–1.6 kV dc
m	Number of SM	4
v_o	Output voltage	100 V dc
P_o	Output power	1 kW
f_{sw}	Switching frequency	200 kHz
C_{1N}	Input capacitance	50 μF
C_b	Balance capacitance	50 μF
L_s	Auxiliary inductors for soft-switch	200 μH
L_b	Impedance matching inductance	3 μH
L_{Lk}	Leakage inductance of transformer	18 μH
C_r	Capacitance for series resonance	32 nF
1:n_m	Turns ratio of HFSCC transformer	1:1
1:n_{pT}	Turns ratio of P^{4}SFB transformer	1:1

$\Delta\varphi = \varphi_{vCD} - \varphi_{vAB}$. Using the gate driver of the HFSCC as the reference value, the P^{4}SFB is phase-shifted to achieve output voltage regulation. The derivation of the transfer function and the design of the PI parameters refer to the literature [31], [32], [33]. During the start-up stage, with the high input voltage v_{in} already established, direct start-up can cause huge current surges, requiring a high switching frequency ($2f_s$) at first start-up and a gradual reduction of the switching frequency to the rated design operating frequency f_s, as shown in Fig. 11.

IV. EXPERIMENTAL RESULTS AND COMPARISON

A prototype converter with a variable input of 1–1.6 kV and an output of 100 V/1 kW was built to verify the feasibility of the proposed converter topology and control method, as shown in Fig. 12. The detailed parameters are listed in Table I.

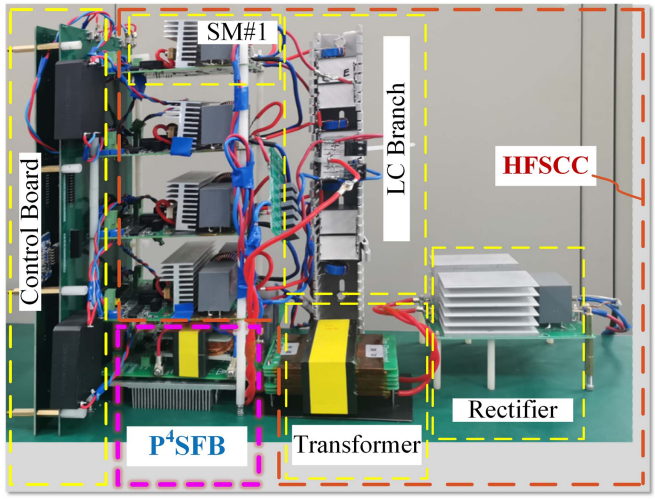

Fig. 12. Experimental prototype and components of the proposed converter with 1.6 kV input.

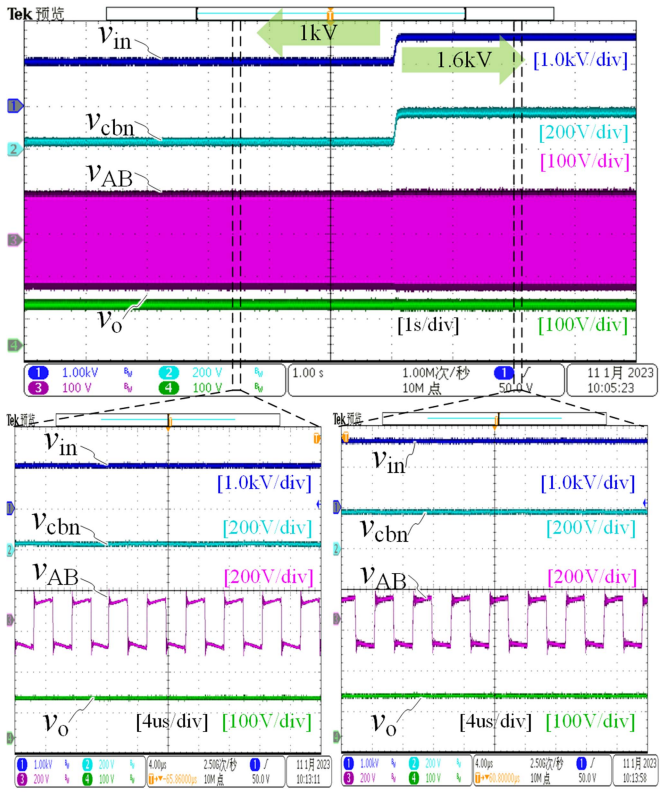

Fig. 13. Experimental waveforms of the output voltage v_o, the excitation square wave voltage v_{AB} of the series resonant tank and the DC bus voltage v_{cbn} of the P^{4}SFB (v_{cbn} characterizes the power processed by the P^{4}SFB) with the input voltage v_{in} rising from 1 to 1.6 kV, respectively.

A. Wide Input Range Voltage Regulation Experiments

As shown in Fig. 13, at the input voltage of 1 kV, v_{cbn} close to 0. With a rise in v_{in} to 1.6 kV, v_{cbn} is controlled by the P^{4}SFB to rise, offsetting the effects of the v_{in} rise, v_{AB} remains unchanged and the output voltage v_o remains unchanged, indicating that the proposed converter achieves output voltage regulation over

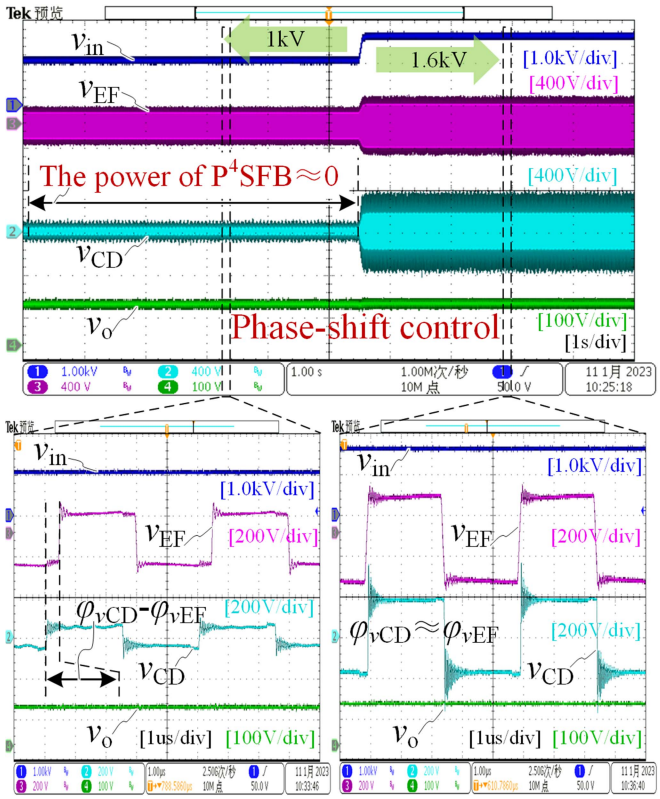

Fig. 14. Experimental waveforms of v_o, the voltage amplitude and phase of one of the HFSCC v_{EF} of the main power, the phase shifted voltage v_{CD} of the P⁴SFB (showing the phase difference between v_{CD} and v_{EF}), respectively, with the input voltage v_{in} rising from 1 to 1.6 kV.

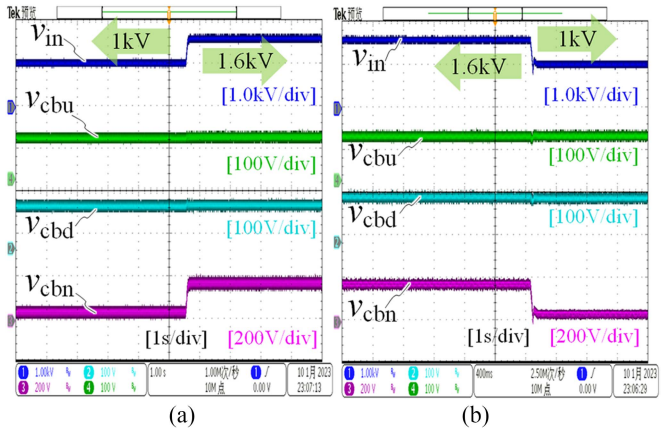

Fig. 15. Experimental waveforms of the DC bus voltage v_{cbn} of the P⁴SFB and the voltages v_{cbu} and v_{cbn} of the capacitors C_{bu} and C_{bn}, respectively. (a) In the case of the input voltage v_{in} rising from 1 to 1.6 kV. v_{cbu} and v_{cbn} represent the amplitudes of the positive and negative half-cycles of the series resonant tank input voltage. (b) With v_{in} dropping from 1.6 to 1 kV.

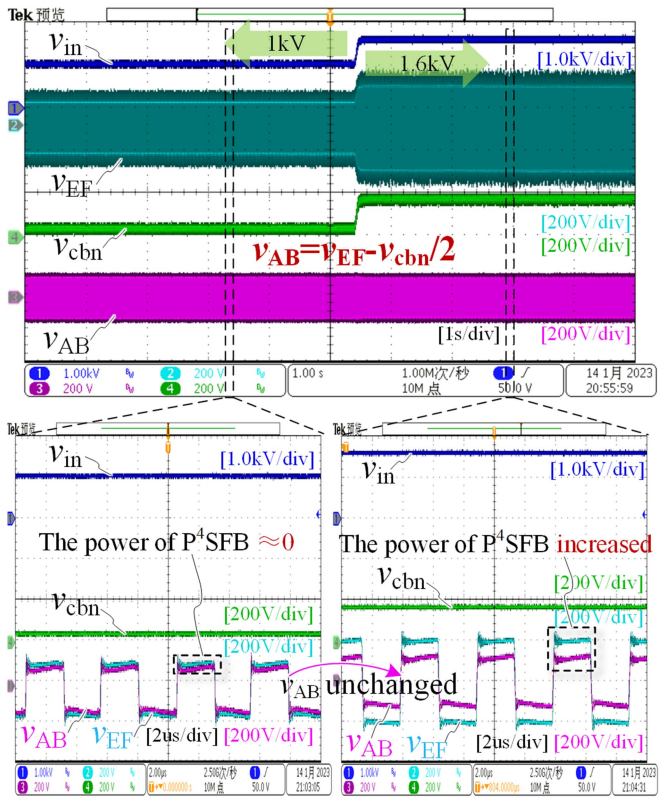

Fig. 16. Experimental waveforms of the DC bus voltage v_{cbn} of the P⁴SFB and the voltages v_{AB} and v_{EF} of the two AC bus ports of the main power HFSCC, respectively, with v_{in} rising from 1 to 1.6 kV. The voltage difference between v_{AB} and v_{EF} indicates the part of the power being regulated by P⁴SFB.

a wide input voltage range. The phase adjustment of v_{CD} and v_{AB} is shown in Fig. 14. v_{in} = 1 kV, φ_{vCD} is more ahead of φ_{vEF}, and v_{in} = 1.6 kV, φ_{vCD} is less ahead of φ_{vAB}, and both are close to each other in phase. v_{in} = 1 kV, v_{CD} amplitude is close to 0, and the power of P⁴SFB is close to 0. v_{in} = 1.6 kV, v_{CD} amplitude rises, and the power of P⁴SFB increases.

Fig. 15 shows the waveforms of v_{cbu}, v_{cbn}, and v_{cbd} varying with the input voltage v_{in}. v_{cbn} is controlled to rise as v_{in} rises, keeping v_{cbu} and v_{cbd} constant. v_{AB} and v_{EF} characterize the power processed by the P⁴SFB, as shown in Fig. 16. v_{EF} is the uncontrolled ac port voltage and v_{AB} is the controlled ac port voltage. v_{AB} = v_{EF}-v_{cbn}/2, it can be seen that v_{AB} is controlled to a constant value, achieving a constant controlled output voltage v_o. The waveforms of v_o, v_{AB}, and i_o are shown in Fig. 17, indicating that the proposed converter has good voltage regulation under dynamic changes in load. The overshoot of the output voltage v_o is less than 3% as the load power dynamically changes from 50% load to 100% load and from 100% load to 50% load.

The input voltage v_{in} rises from 1 to 1.6 kV, the input voltage stresses for each module are shown in Fig. 18. v_{SM1}, v_{SM2}, v_{SM3}, and v_{SM4} completely overlap during the steady-state and transient processes, indicating that the proposed converter has good self-balancing results and low stress for each module input voltage. The current waveforms of each MOSFET of the main power are shown in Fig. 19. i_{M11}, i_{M12}, i_{M13}, and i_{M14} completely overlap in the steady-state and transient processes, it is shown that good current self-balancing results and low current stress are achieved for each MOSFET of the proposed converter.

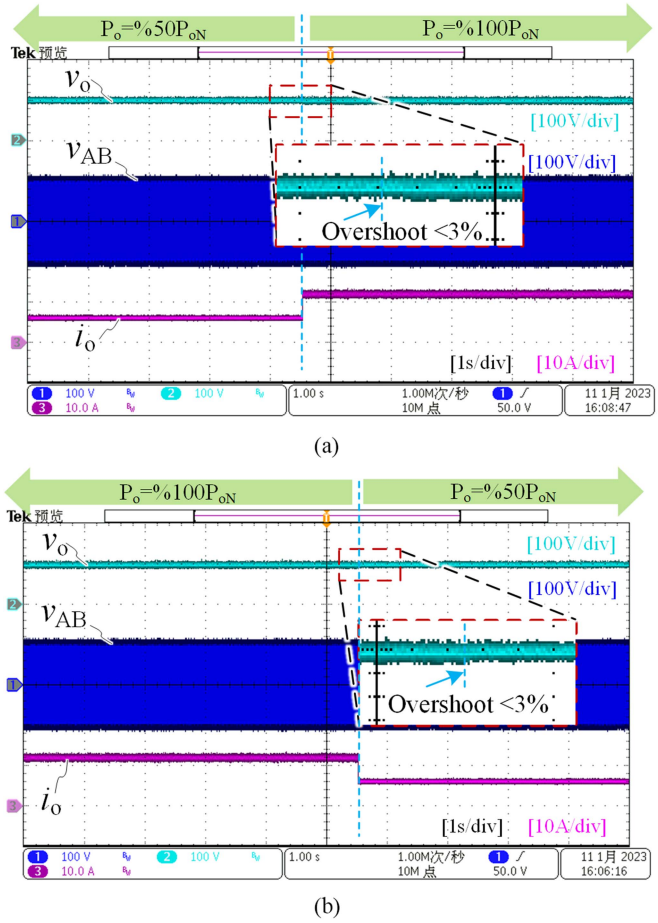

Fig. 17. Waveforms of the regulated output voltage v_o and output current i_o for (a) a load changing from 50% to 100% load power and (b) a load changing from 100% to 50% load power, respectively.

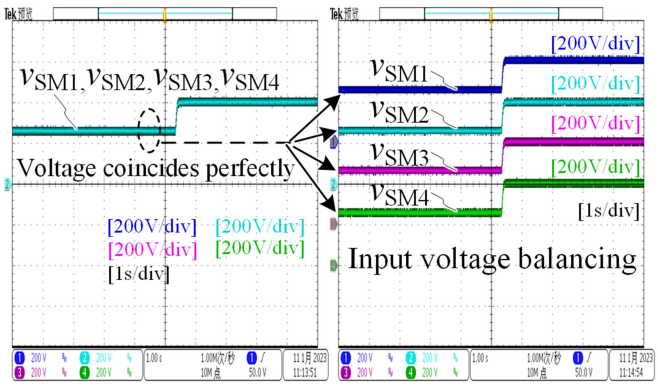

Fig. 18. Voltage self-balancing waveforms of the proposed converter submodules under sudden change of v_{in} from 1 to 1.6 kV.

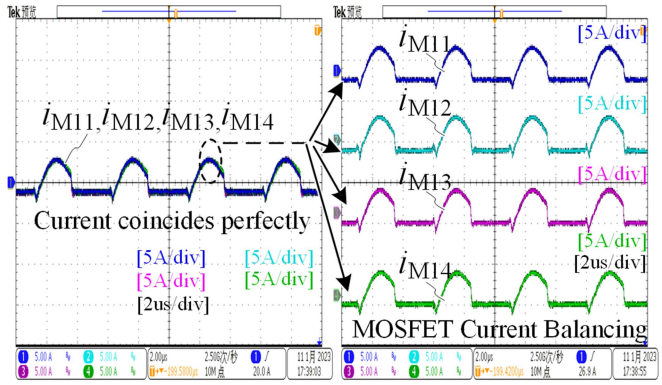

Fig. 19. Current self-balancing waveforms of the main power MOSFETs M_{11}, M_{12}, M_{13}, and M_{14} of the proposed converter.

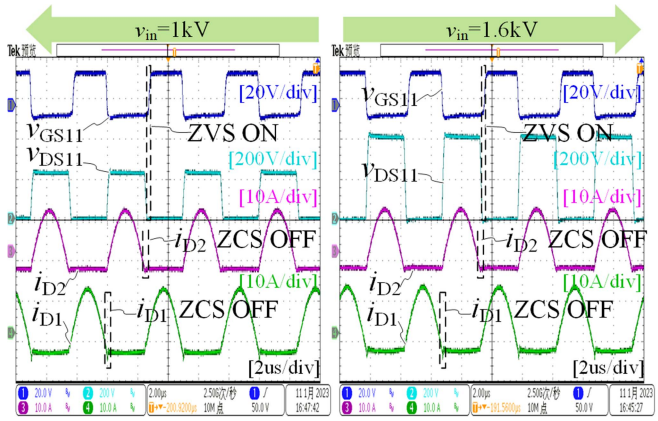

Fig. 20. Main power MOSFETs ZVS turn-ON and diodes ZCS turn-OFF soft-switching waveforms of the proposed converter.

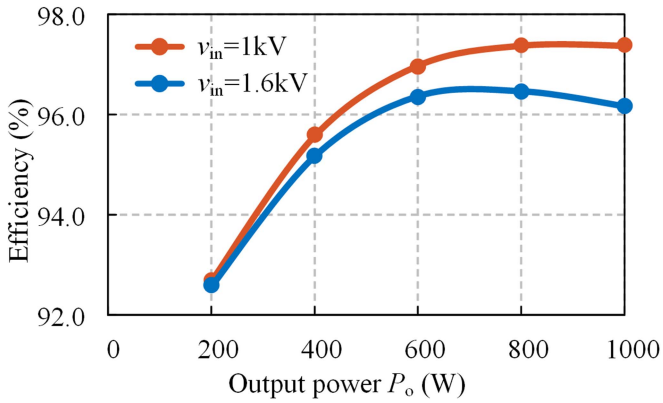

Fig. 21. Efficiency curves of the proposed converters at 1 kV and 1.6 kV respectively.

B. MOSFET and Diode Soft Switching Experiments

The gate driver signal v_{GS} of the main power MOSFETs, the drain-source voltage v_{DS} and the current waveforms i_{D1} and i_{D2} of the secondary rectifier diode are shown in Fig. 20, at v_{in} is 1 kV and 1.6 kV, respectively. It shows that the proposed converter P^{3}SCC main power MOSFETs and diodes achieve soft switching in a wide input voltage range. The efficiency curves for the proposed converter at 1 kV and 1.6 kV are shown in Fig. 21 with a peak efficiency of 97.3%. The histogram of the loss distribution for different input voltages is shown in Fig. 22.

The volume of the converter is about 400 in^3 and the power density is about 2.5 W/in^3 (on the one hand the experimental prototype is a high voltage converter, the insulation distance occupies part of the volume; on the other hand the power density

TABLE II
COMPARISON WITH CONVENTIONAL WIDE INPUT VOLTAGE RANGE HIGH STEP-DOWN CONVERTER

Topologies	[14]	[18]	[30]	[34]	[35]	[36]	Proposed
Number of MOSFETs	5m	9m	2m-2	2m	2m	2m	2m+4
Number of diodes	3m	No	2	4	2m	2m	6
Number of inductors	2m	m	m-1	7	2m	2m	2m
Number of capacitors	3m	m	2m-1	2m+4 (high voltage)	2m	4m	3m+3
Number of transformers	No	m	No	1	No	No	2
Output isolation	No	Yes	No	Yes	No	No	Yes★
Input voltage auto-balancing	/	Controlled	No	No	/	Yes	Yes★
MOSFET current auto-balancing	No	No	No	No	No	No	Yes★
Soft switching	No	Yes	Yes	Yes	No	No	Yes★
Input voltage	300 V	343 V	85–120 V	480–720 V	200–400 V	700 V–1 kV	1–1.6 kV★
Input voltage regulation range	medium	wide	medium	medium	wide	medium	wide★
Energy transfer paths	Indirect	Direct	Indirect	Direct	Direct	Indirect	Direct★
Power level	100 W	800 W	140 W	1 kW	2 kW	100 W	1 kW
Peak efficiency	93.4%	95.8%	94.6%	94%	96.9%	>92%	97.3%★

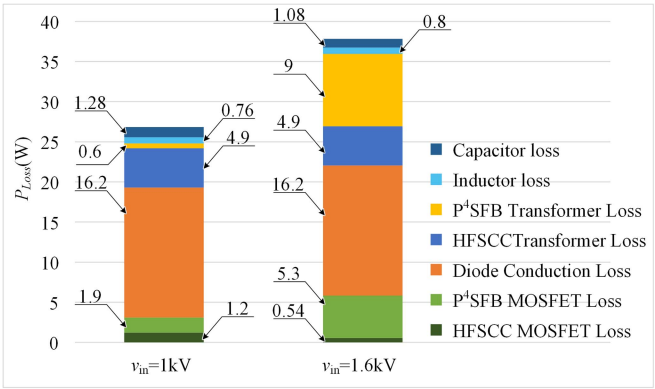

Fig. 22. Loss distribution at $v_{\text{in}} = 1$ kV and $v_{\text{in}} = 1.6$ kV.

TABLE III
FAULT TYPES AND RELIABILITY

Fault types	Operating status
MOSFETs short-circuit (permanently)	√ Operating normally but with rising voltage stress
Inconsistent gate drive of MOSFETs	√ Operating normally
MOSFETs open circuit (milliseconds)	√ Output normally but transient voltage imbalance
MOSFETs open circuit (permanently)	× Cannot operate (voltage divergence of the module)

can be further increased, most of the components of the current experimental prototype are external verification functions).

C. Comparison With Conventional High Step-Down Switched-Capacitor Converters

Table II shows the comparison of the proposed topology with conventional high step-down switched-capacitor converters such as the valley-fill switched capacitor structure in [14], which utilizes a multistage interleaved topology to achieve a high step-down ratio and a wide range of regulation using varying duty cycles, but requires more switching devices, does not achieve soft switching and has a lower efficiency for wide range regulation, the proposed P³SCC has a wide voltage regulation range, and a smaller number of devices, soft switching over the full power range and is easier expansion to multiple modules. Compared to the dc transformer based on switched capacitor proposed in [18], the proposed converter has a similar regulation range but with a simpler hardware circuit structure, less sampling, and a simpler control strategy. The multilevel step-down resonant switched-capacitor converters proposed in [30] use multilevel combinations to achieve a wide range of voltage regulation, but with large differences in the current stress of MOSFETs at different levels, and has a high voltage capacitor-inductor branch, an increase in capacitor-inductor insulation volume as the input voltage rises, and requires separate sampling and control. The MMDC in [34] can process higher dc input voltages, has a scalable soft-switching range and improves the efficiency of the MV converter. However, the input voltage of each module needs to be detected and controlled, which increases the hardware cost in MV dc systems and the reliability needs to be improved. The asymmetric PWM series capacitor high conversion ratio dc–dc converter in [35] can be regulated over a wide input voltage range by adjusting the duty cycle, but the limited input voltage makes it difficult to extend to medium voltage dc applications. The article by Zhu et al. [36] uses the basic principle of switched capacitors and the voltage regulation characteristics of the buck-boost converter, which features a wide voltage regulation range, independent operation of each sub-module, and voltage balancing without communication and synchronization. However, the energy is transferred from the highest potential converter to the lowest potential point through 2m steps, which increases the losses, and it is difficult to achieve isolation and is usually used in low-power applications.

In contrast, the proposed converter achieves a wide range of voltage regulation with low and balanced voltage and current stress. The input side can be directly connected in series with several modules without additional design, which makes it easier to modularize the design for MVdc applications.

In addition, the proposed converter has the advantage of high reliability, as shown in Table III.

1) If one or two MOSFETs have a permanent short-circuit fault, the converter continues to operate, the voltage of the faulty module becomes zero and the voltage of the other modules

rises. However, too many MOSFETs are short-circuited, resulting in overvoltage in the normal module.

2) Even if the MOSFET gate drives of the modules are not fully synchronized (the time difference less than the dead time), there is no effect on the normal operation of the converter and the voltage self-balance.
3) If an open circuit fault in one of the MOSFETs can be recovered within a few tens of milliseconds, the output of the converter is normal and the voltage balance is quickly restored; if the MOSFET is open for a longer time or has a permanent open circuit fault, the voltage of each module of the converter is severely dissipated, resulting in overvoltage damage to the converter and failure to operate normally.

V. Conclusion

A partial power processing switched-capacitor converter for medium voltage applications is proposed in this article, the feasibility of the proposed converter and the correctness of the analysis are verified by an experimental prototype with 1–1.6 kV input and 100 V/1 kW output. The experimental results showed that the proposed converter achieves output voltage regulation over a wide input voltage range, with most of the power processed by the high-efficiency HFSCC operating in a series resonant state and a small portion of the power processed by the P^4SFB, realizing higher efficiency. Furthermore, analysis and experiments show that the proposed converter has the features of low voltage and current stress with automatic input voltage balancing and MOSFET current balancing, and the number of submodules is expandable easily, so it is more suitable for high-efficiency conversion of medium voltage and high power with wide input voltage range.

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