A Bidirectional Modular Multilevel Resonant DC–DC Converter for Wide Voltage Range Medium-Voltage Power Conversion

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***Abstract*—The arm inductor is found to cause the loss of soft switching in modular multilevel resonant dc–dc converters, so a full-range soft switching converter with wide voltage gain is proposed in this article. The modular multilevel structure and the *CLLC* resonant tank are utilized in the converter for isolated and bidirectional power conversion in medium-voltage applications with high efficiency. Wide and continuous voltage gain regulation can be achieved with the proposed coordinated gain control method. The submodule voltages are balanced by voltage sampling and individual gate signal controls. The requirements for full-range soft switching are explained. Finally, a laboratory prototype is constructed and the experimental results verify the theoretical analysis.**

***Index Terms*—Bidirectional, dc–dc, medium voltage (MV), modular multilevel converter (MMC), resonant, soft switching, wide voltage range.**

I. Introduction

DC DISTRIBUTION systems offer several advantages over conventional ac systems, including higher efficiency, improved current carrying capacity, and faster dynamic response [1]. Additionally, they provide a more natural interface with various energy storage systems (ESSs) [2] and renewable energy systems. In any dc system, the dc–dc converter plays a crucial role as it enables voltage matching, power control, and galvanic isolation.

The dc–dc converter interconnecting the medium-voltage dc (MVDC) with the low-voltage dc (LVDC) may require wide voltage regulation capability due to the significant voltage variations that can occur on both sides of the converter. For instance, when connecting an LV battery ESS or dc microgrid to the MVDC grid, the battery terminal voltage can vary widely depending on its state of charge, often reaching half of its nominal voltage [3], [4], [5]. Similarly, an LVDC microgrid may experience voltage variations of up to 10% for droop control [6], [7]. Moreover, the MVDC voltage itself can exhibit a wide range of variability [8]. For instance, in certain applications, such as undersea observatories, the conversion of an MVDC voltage ranging from 9–15 kV to 750 V LVDC is required [9].

The feasible solutions for MVDC power conversion are the input-series–output-parallel (ISOP) structure and the modular multilevel dc–dc converter (MMDC).

In ISOP configuration, multiple isolated converter modules are connected in series on the high-voltage side and in parallel on the low-voltage side [10], [11], [12]. With simple system architecture, high modularity, and good reliability, ISOP is popular and widely employed in the industry [13]. To achieve wide voltage range operation, various topologies and control methods in low voltage levels can be migrated to ISOP architecture, such as employing a two-stage topology, toggling between full-bridge and half-bridge, and dynamically reforming the rectifying structure [14], [15].

However, the power transformer in each module has to sustain the galvanic voltage up to tens of kilovolts, which results in a bulky transformer volume and limits the power density of the system [16]. Besides, the additional control degrees of freedom introduced by modularization are not thoroughly exploited for wide voltage operation.

The MMDC combines the advantages of the widely adopted modular multilevel converter (MMC) [17] with conventional dc–dc topologies, such as the dual active bridge (DAB) converter [18], [19] and resonant converters [20], which can dramatically reduce the transformer isolation requirement and is attractive in these applications.

The modular multilevel DAB (MMDAB) is proposed and investigated in [21], [22], [23], [24], [25], [26], and [27]. When the voltage gain deviates from the unit gain, DAB efficiency is severely reduced [19]. To solve this problem, one effective approach is to leverage the control freedom provided by the

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modular structure to maintain DAB in an optimal operation state when the system voltage varies widely. Investigated control freedom includes the quantity of inserted submodules (SMs), phase shift between SMs, and the SM duty cycle [23], [24], [25], [26], [27].

MMDC combining MMC and resonant converters was proposed in [9], [28], [29], [30], [31], and [32]. By means of modular structure control, the resonant converter can effectively operate within a limited frequency range while achieving a wide range of voltage gain. One example is the modular multilevel resonant (MMR) converter proposed in [9]. By constantly inserting a certain number of SMs into the arm according to the input voltage, MMR can operate near its resonant frequency, irrespective of a wide input voltage range.

Similar to MMC, the above MMDC [9], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32] has an inherent dc circulating current. Although this circulating current is typically not a problem in conventional MMC, it will deteriorate the soft switching characteristics of MMDC. The current through the MV side power devices has a dc bias and the converter may lose zero voltage switching-ON (ZVS-ON) under most of the load conditions, which reduces the benefits offered by DAB or resonant converters. Besides, the bidirectional operation of resonant MMDC is not investigated.

This article reveals that the circulating current is introduced by the arm inductor, and full-range soft switching can be achieved by removing the arm inductor. Based on this, a soft switching bidirectional MMR (BMMR) converter without an arm inductor is proposed. Moreover, a coordinated gain control method for wide and continuous voltage gain control is proposed. Furthermore, this article also analyzes the active control method of the modular structure in rectifying state for wide voltage range operation.

The rest of this article is organized as follows. Section II analyzes the effect of the arm inductors. Section III introduces the coordinated voltage gain control method for wide voltage regulation. Section IV gives the gate signals generation method for SM voltage balancing. Section V analyzes the soft switching requirements under different operation conditions. Section VI validates the theoretical analysis through experiments. Finally, Section VII concludes this article.

II. Analysis of the Effect of the Arm Inductor

The arm inductor introduces a circulating current into the modular arm, which will deteriorate the soft switching performance. By removing the arm inductor, full-range soft switching can be achieved.

The arm configuration, the typical arm currents i_{a1} and i_{a2}, and the SM switch waveforms are illustrated in Fig. 1(a), where ZVS-ON of SM lower switch Q_1 is lost [9]. An equivalent circuit is illustrated in Fig. 2(a). The input voltage and the dc-link capacitors are replaced with voltage sources V_1 and V_2, where $V_1 = V_2 = V_{\text{MV}}/2$. The multiple series SMs in each arm are merged into one. The other circuit, including the resonant tank, the transformer, and the LV side, is approximated as a sinusoidal

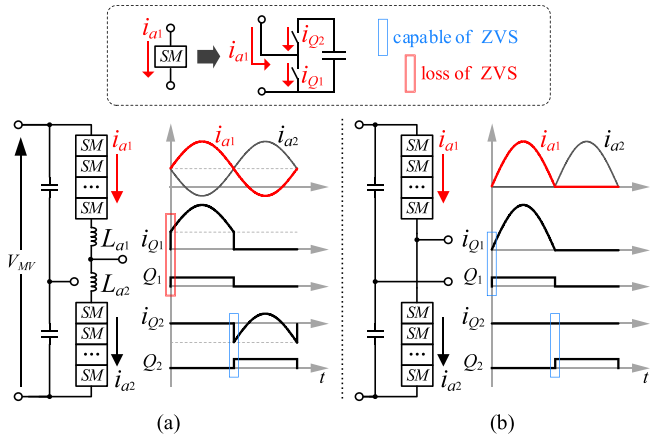

Fig. 1. Arm configuration and arm currents in the modular multilevel resonant converter (a) with arm inductor utilized and (b) without arm inductor.

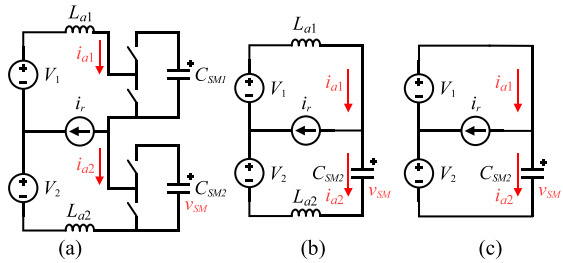

Fig. 2. Equivalent circuits. (a) Circuit in resonance. (b) Circuit with arm inductor in $[0, T_s/2)$. (c) Circuit without arm inductor in $[0, T_s/2)$.

current source i_r when considering the situation in resonance and ignoring the magnetizing current.

Taking one half-switching cycle $[0, T_s/2)$ as an example, the circuit is shown in Fig. 2(b) and can be described by a set of equations as

$$\begin{cases} L_a \frac{di_{a1}(t)}{dt} + v_{SM}(t) + L_a \frac{di_{a2}(t)}{dt} = V_1 + V_2 \\ i_{a2}(t) = i_{a1}(t) - I_r \sin \omega t \\ i_{a2}(t) = C_{\text{SM2}} \frac{dv_c(t)}{dt} \\ i_{a1}(0) = i_{a1}(T_s/2) \\ i_{a2}(0) = i_{a2}(T_s/2) \\ v_{\text{SM}}(0) = v_{\text{SM}}(T_s/2) \end{cases} \tag{1}$$

where $\omega = 2\pi/T_s$ is the switching frequency in radians, I_r is the amplitude of the resonant current, and $L_a = L_{a1} = L_{a2}$. v_{SM} is the capacitor voltage in an arm, which is approximately equal to V_{MV}. The following are the solutions for arm currents:

$$\begin{cases} i_{a1}(t) = a_1 \sin \omega t + b_1 \cos(ct + d) \\ i_{a2}(t) = a_2 \sin \omega t + b_2 \cos(ct) - k \sin(ct) \end{cases} \tag{2}$$

where a_1, a_2, b_1, b_2, c, d, and k are complicated coefficients related to ω, C_a, L_a, and I_r (cf., Appendix).

According to (2), when the arm inductance L_a is greater than tens of μH in a medium frequency converter (about 10 kHz), the arm currents can be approximated as

$$\begin{cases} i_{a1}(t) \approx \frac{I_r}{\pi} + \frac{I_r}{2} \sin \omega t \\ i_{a2}(t) \approx \frac{I_r}{\pi} - \frac{I_r}{2} \sin \omega t \end{cases}, \quad t \in [0, T_s/2). \tag{3}$$

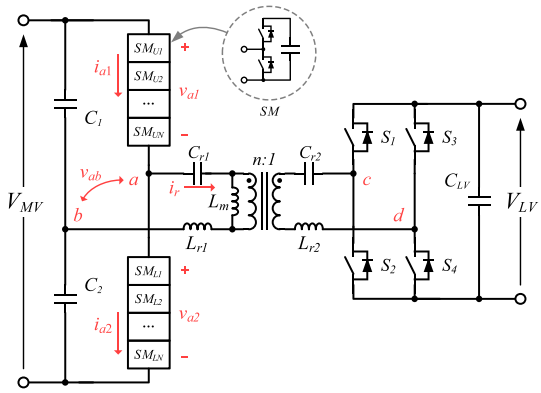

Fig. 3. Proposed bidirectional modular multilevel resonant converter.

This suggests that a dc-like circulating current of I_r/π exists in both arms and leads to the loss of ZVS-ON, as shown in Fig. 1(a).

When the arm inductor is removed, the equivalent circuit can be simplified to Fig. 2(c), and the arm current becomes

$$\begin{cases} i_{a1}(t) = I_r \sin \omega t \\ i_{a2}(t) = 0 \end{cases}, \quad t \in [0, T_s/2). \tag{4}$$

Similar analysis can be performed on the other half cycle and it also suggests that the resonant current is only conducted in one arm [cf., Fig. 1(b)], and ZVS-ON can be easily achieved, just like the situation in normal resonant converters.

Although the arm inductor is typically required in conventional MMC for ac or dc fault tolerance, it is unnecessary in some MMDC converters: the dc faults can be mitigated by installing inductors in the dc bus lines; the ac lines of MMDC are positioned inside the converter cabin, as opposed to conventional MMCs, whose ac lines typically extend outside the converter and are connected to transmission lines, so it is predicted that ac faults will be less common in MMDC. Besides, the arm inductor in MMC is necessary for suppressing the currents due to instantaneous voltage differences between the arms and the dc bus [33]. In MMC, the SM capacitor voltage has a 10%–15% ripple at the line frequency. Since the switching frequency is much higher than the line frequency, the dc voltage of each phase (excludes the arm inductors) is different at each switching cycle, and the arm inductors are therefore required. In MMDC, however, the SM capacitor voltage ripple frequency is the same as the switching frequency, and the dc-side voltage of each phase is almost the same at each switching instant. It is feasible to let MMDC operate like a two-level or quasi-two-level converter.

Based on the above analysis, a BMMR converter shown in Fig. 3 is proposed, where the arm inductor is eliminated to avoid the dc circulating current. BMMR can thus achieve soft switching in full load and gain range. A *CLLC* resonant tank, which consists of the resonant capacitors C_{r1} and C_{r2}, the resonant inductors L_{r1} and L_{r2}, and the magnetizing inductor L_m, is employed for bidirectional operation. The modular structure consists of two arms, and each arm has N cascaded SMs. As listed in Table I and illustrated in Fig. 4, each SM may have three states according to the Q_1 and Q_2 gate signals. For brevity,

TABLE I
OPERATION STATES OF SUBMODULE

SM state	SM signal (g)	Q_1	Q_2	C_{SM} state
Conducted	Positive	On	Off	Bypassed
Freewheeling	Zero	Off	Off	Bypassed or inserted
Inserted	Negative	Off	On	Inserted

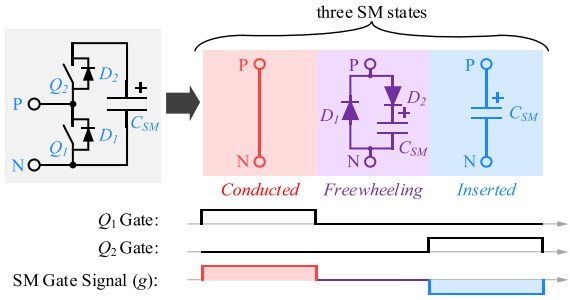

Fig. 4. Equivalent circuits and gate signals of three submodule states.

the SM state is represented by a virtual three-level compound control signal g, which is the combination of the Q_1 and Q_2 gate signals. The corresponding equivalent circuits in each state are also shown. Note that the state of the SM capacitor C_{SM} is distinct from the SM state.

III. Modulation and Control for Wide Voltage Range Regulation

By modulating the modular structure and changing the switching frequency coordinately, BMMR can achieve a much wider voltage regulation range when compared with normal resonant converters. Special modulation and control are required for the proposed BMMR.

A. Voltage Gain of BMMR

The voltage gain G of the BMMR converter is the product of the modular structure voltage gain G_a and the resonant tank voltage gain G_r, which can be written as

$$G = \frac{V_{\text{MV}}}{n \cdot V_{\text{LV}}} = \frac{V_{\text{MV}}}{n \cdot V_{cd}} = \frac{V_{\text{MV}}}{V_{ab}} \cdot \frac{V_{ab}}{n \cdot V_{cd}} = G_a \cdot G_r \tag{5}$$

where V_{ab} is the amplitude of the resonant tank MV-side voltage v_{ab}, whereas V_{cd} is for the LV side. The turn ratio of the transformer is denoted as n.

G_r varies with the switching frequency, whereas G_a varies with the gate signals for SMs. The control method in forward mode is explained first, where energy is transferred from the MV side to the LV side.

$G_a = 2$ if the SMs in each arm are assigned the same gate signal, as illustrated in Fig. 5(a). g_u and g_l are the gate signals for the upper arm and the lower arm SMs. S_1–S_4 are in OFF state. T_s is the switching period of the power devices and deadtime is currently not considered for simplicity.

G_a can be regulated with special control of the modular structure, where the gate signal for each SM is individually

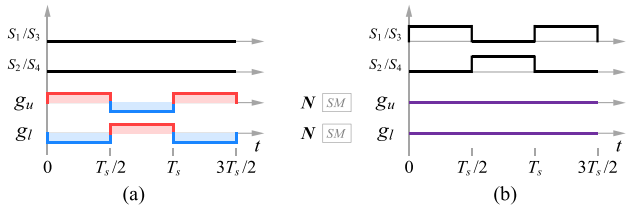

Fig. 5. Gate signals when $G_a = 2\,(M = 0)$. (a) Forward mode. (b) Backward mode.

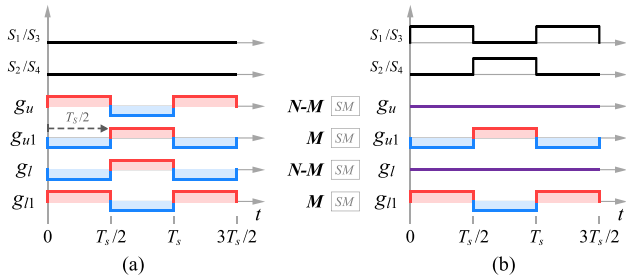

Fig. 6. Gate signals when $M > 0$. (a) Forward mode. (b) Backward mode.

TABLE II
RELATED NOMENCLATURE

Symbols	Meaning
G	BMMR voltage gain
G_a	Modular structure voltage gain
G_r	Resonant tank voltage gain
N	Number of SMs in each arm
M	Control factor of modular structure voltage regulation
N_{i1}	Number of *inserted* SMs in the first half cycle in one arm
N_{i2}	Number of *inserted* SMs in the second half cycle in one arm

controlled. Due to the removal of the arm inductors, the proposed BMMR does not permit dynamically changing the total number of inserted SMs in the modular structure [9], as there will be a significant spike current in the arm. However, the inserted SM number in each arm can be changed to regulate G_a. As illustrated in Fig. 6(a), by choosing M SMs in each arm and applying a phase shift of π to their gate signals, the inserted number is changed. M is the control factor of modular structure voltage regulation. The shifted signals are denoted by g_{u1} and g_{l1}. The related nomenclature is given in Table II. As shown in Fig. 7, when BMMR is in steady state, the number of inserted SMs in the first half cycle $[0,\ T_s/2)$ in the lower arm is

$$N_{i1} = N - M. \tag{6}$$

The inserted number in the second half cycle $[T_s/2,\ T_s)$ is

$$N_{i2} = M. \tag{7}$$

Considering that V_{MV} is equally shared by all the inserted SMs in the arms, which is ensured by the balancing method to be discussed in the following section, the average voltage V_c of

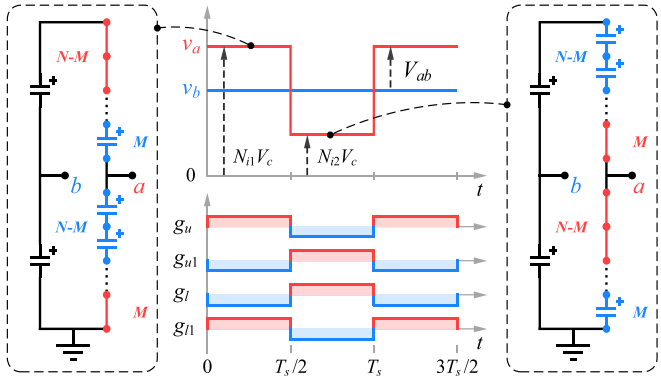

Fig. 7. Gate signals, waveforms, and equivalent circuits in forward mode.

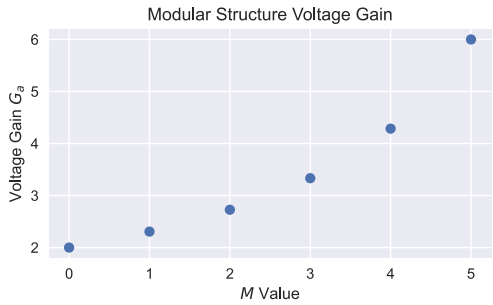

Fig. 8. Modular structure voltage gain versus M when $N = 15$.

the SM capacitor C_{sm} is

$$V_c = V_{\mathrm{MV}}/N. \tag{8}$$

The amplitude of v_{ab} is derived as

$$V_{ab} = \frac{N_{i1}V_c - N_{i2}V_c}{2} = \frac{(N-2M)\,V_{\mathrm{MV}}}{2N}. \tag{9}$$

Hence, the voltage gain of the modular structure is

$$G_a = \frac{V_{\mathrm{MV}}}{V_{ab}} = \frac{2N}{N-2M}. \tag{10}$$

M is limited to integers, thus G_a has discrete values, as shown in Fig. 8, where an arm with 15 SMs is taken as an example.

B. Coordinated Gain Control Method

Coordinated gain control is proposed to coordinate the adjustment of M and the switching frequency f_s, achieving a wide and continuous regulation of voltage gain G. Moreover, the BMMR resonant tank can work near resonance, making it easier to design optimal resonant parameters and achieve higher overall efficiency.

The gain G versus frequency curves of the resonant tank with different M are illustrated in Fig. 9. The x-axis stands for the normalized switching frequency $f_n = f_s\,/f_0$, where f_0 is the resonant frequency. On each curve, G varies within a small range as f_n changes. However, changing M allows the gain to step between the curves, greatly extending the gain range within a given frequency range $[f_{\min}, f_{\max}]$.

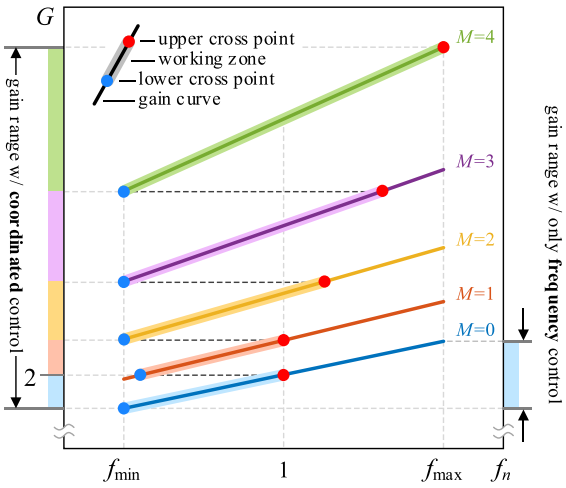

Fig. 9. Voltage gain with coordination control of M and f_n.

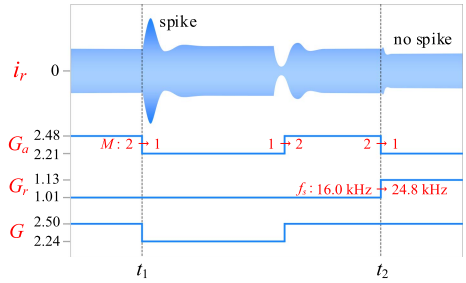

Fig. 10. Resonant current with a step of M and the switching frequency.

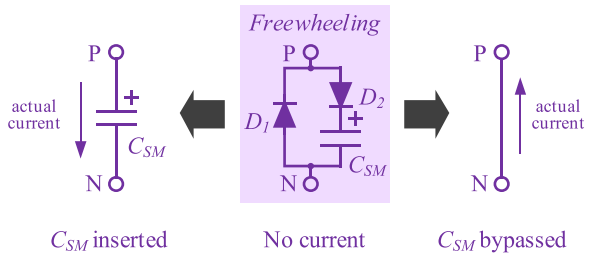

Fig. 11. Capacitor state in the freewheeling submodule is subject to the PN current direction.

However, merely changing M leads to the abrupt change of G, which will cause a voltage mismatch across the resonant tank and an unexpected spike in resonant current. As a result, when changing M, f_n is changed simultaneously to keep G constant. Fig. 10 shows a simulation in PLECS that supports the concept. A spike occurs in the resonant current i_r when M changes alone at t_1, whereas there is no spike when f_s is changed simultaneously at t_2.

The cross points between different gain curves, i.e., dots in Fig. 9, should be chosen properly, and the frequency of the cross point is called the cross point frequency. Before introducing the principles to choose the cross points, an example demonstrating the coordination of f_n and M is given: when f_n increases and reaches the upper cross point on the $M = 1$ curve in Fig. 9, if a larger G is needed, M will change to 2 and f_n will change to the lower cross point frequency on the $M = 2$ curve. The points between the lower and the upper cross points on the curves constitute the working zone of BMMR.

There are several principles to find out the cross points. The adjacent cross points on two adjacent curves should have the same G. Besides, BMMR prefers to work at or below resonance to achieve soft switching of the rectifying side power devices, thus the working zone on each curve is preferred to be lower, yet contain 1. Denote the gain of the combination (M, f_n) as $G(M, f_n)$, and the design method is given as follows.

1) The lower cross point on the $M = 0$ curve is $(0, f_{\min})$ and the upper cross point on the $M = M_{\max}$ curve is $(M_{\max}, f_{\max})$ for the widest gain range within the given frequency range $[f_{\min}, f_{\max}]$.
2) For the other cross points, if $G(M, 1) \geq G(M + 1, f_{\min})$, set the upper cross point on curve M as $(M, 1)$ and the lower cross point on curve $M + 1$ as $(M + 1, f_l)$, where $G(M + 1, f_l) = G(M, 1)$; otherwise, set (M, f_u) and $(M + 1, f_{\min})$ as cross points, where $G(M, f_u) = G(M + 1, f_{\min})$.

The voltage gain of the resonant tank is subject to load conditions thus the cross points may vary. The cross points can be designed by simulations based on the above method, and be stored in a look-up table (LUT). In field operation, the simulation-based LUT and interpolation method are employed to perform the coordinated gain control under different load conditions.

C. Voltage Gain Control in Backward Mode

The control of G_a and the coordinated gain control are also applied in backward mode, where energy is transferred from the LV side to the MV side.

The gate signals are illustrated in Fig. 5(b), where the LV side generates an exciting voltage v_{ef} on the resonant tank and the SMs are in a freewheeling state. If the forward voltage of D_2 is ignored, the average voltage V_c of the SM capacitor C_{sm} is also V_{MV}/N. This is because that the capacitor in a freewheeling SM is inserted into the arm when there is current from P to N (cf., Fig. 11), whereas it is bypassed from the arm when current flows from N to P. Besides, when there is no current in a freewheeling SM, the PN voltage is clamped to the capacitor voltage. In backward mode, the resonant current flows from N to P in one arm, consequently there are total N SM capacitors inserted and V_{MV} is clamped to the sum of the inserted SM capacitor voltages.

As illustrated in Fig. 6(b), assign M SMs in the upper arm to inserted state in the first half cycle and conducted in the second half cycle, and these signals are denoted by g_{u1}. Meanwhile, assign M SMs in the lower arm to conducted state in the first half cycle and inserted them in the second half cycle, and these signals are denoted by g_{l1}. The voltage gain of the modular structure is the same as (10).

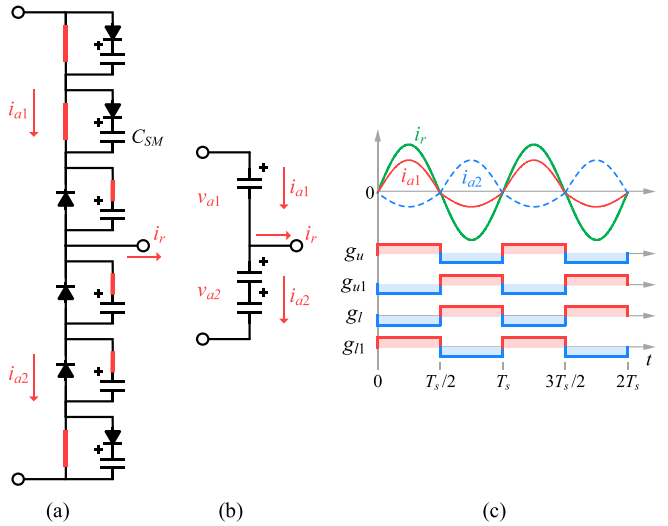

Fig. 12. Modular structure and the arm currents in forward mode with $M > 0$. (a) Modular structure. (b) Equivalent circuit. (c) Theoretical waveforms.

D. Currents in Voltage Gain Control

The theoretical arm currents in BMMR remain consistent with traditional LV dc–dc resonant converters when the voltage gain control is not applied ($M = 0$).

When $M > 0$, each arm contains M SMs with shifted gate signals. Taking $N = 3$ and $M = 1$ as an example, the equivalent circuit of the modular arm in the first half cycle $[0, T_s/2)$ is illustrated in Fig. 12(b). Assuming that the MV voltage remains constant and ignoring the parasitic parameters, the arm currents can be described as

$$\begin{cases} i_{a1}(t) = C_{a1}\frac{\mathrm{d}v_{a1}(t)}{\mathrm{d}t} \\ i_{a2}(t) = C_{a2}\frac{\mathrm{d}v_{a2}(t)}{\mathrm{d}t} \\ v_{a1}(t) + v_{a2}(t) = V_{\mathrm{MV}} \\ i_{a1}(t) - i_{a2}(t) = i_r(t) \end{cases}, \quad t \in [0, T_s/2) \tag{11}$$

where v_{a1} and v_{a2} are the arm voltages and C_{a1} and C_{a2} are the total inserted arm capacitance. It can be derived that the arm current is proportional to C_a. There are M SMs inserted in the upper arm and $N - M$ SMs inserted in the lower arm. Considering that C_a is inversely proportional to the number of inserted SMs, the arm current can be expressed as

$$\begin{cases} i_{a1}(t) = \frac{N-M}{N} i_r(t) \\ i_{a2}(t) = -\frac{M}{N} i_r(t) \end{cases}, \quad t \in [0, T_s/2). \tag{12}$$

As illustrated in Fig. 12(c), the resonant current is split between both arms according to the number of inserted SMs. Note that in the presence of voltage gain control, there can be a negative current in the upper arm, which is not consistent with the situation when the voltage gain control is not applied [as depicted in Fig. 1(b)]. However, there is no dc bias current introduced in the arm currents. This allows for the achievement of soft switching for SMs, as will be further discussed in the subsequent sections.

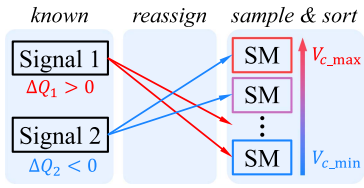

Fig. 13. Gate signal reassigning.

IV. Submodule (SM) Voltage Balancing

The balance of SM capacitor voltages is a critical consideration in modular converters for reliable operation to avoid potential overvoltage damage. In BMMR, SM voltage divergence in an arm can occur due to variations in component parameters or differences in gate signal delay, thus a proper method to restrict it within an acceptable range is necessary.

Because the ac resonant current changes direction every switching period, the traditional MMC SM balancing method is not suitable in BMMR. In this article, the SM gate signals are individually controlled to balance the voltages, as ΔQ of the different gate signals can be different. ΔQ of a gate signal refers to the net charge difference experienced by the capacitor C_{sm} within the SM throughout a switching cycle when that specific gate signal is assigned to it. When BMMR operates in steady state, the sum of the inserted SM voltages is equal to V_{MV} and remains the same, which derives that

$$\sum_{i=1}^{p} q_i \Delta Q_i = 0 \tag{13}$$

where there are p kinds of gate signals per arm and each is assigned to q_i SMs with a charge difference of ΔQ_i. This suggests that for a certain combination of gate signals which BMMR works stably with, ΔQ of some signals are positive and some negative, otherwise all ΔQ equal zero.

In practical implementation, the balancing of SM voltages is achieved through a repetitive process that involves sampling and sorting the capacitor voltages. Subsequently, reassign the gate signal with the largest positive ΔQ to the lowest voltage SMs and so is the opposite [31], [34], as is illustrated in Fig. 13.

To perform the balancing control, ΔQ of the BMMR gate signals in forward and backward modes are analyzed in detail. Notice that ΔQ is the integration of the current via the SM capacitor over a switching cycle, which is subject to both the SM state and the arm current. The inserted SMs will be charged or discharged, and the freewheeling SMs with an arm current from P to N will be charged. In other cases, the SM voltage remains the same.

A. Voltage Balancing When $M > 0$

There are two kinds of gate signals in each arm when BMMR operates with $M > 0$, for example, g_u and g_{u1} in the upper arm. In forward mode, the typical upper arm current waveform is illustrated in Fig. 14(a) as an example. According to the current direction, it can be derived that $\Delta Q_u < 0$ and $\Delta Q_{u1} > 0$ over a whole switching cycle. A similar analysis can be performed

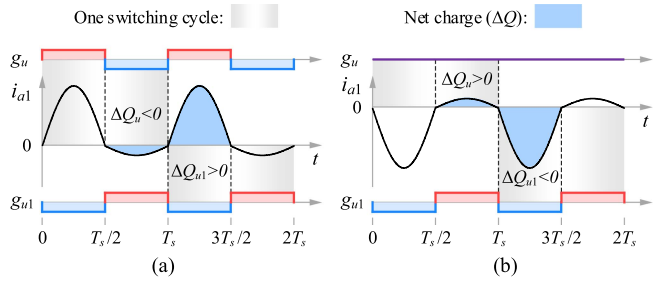

Fig. 14. ΔQ of the BMMR gate signals when $M > 0$. (a) Forward mode. (b) Backward mode.

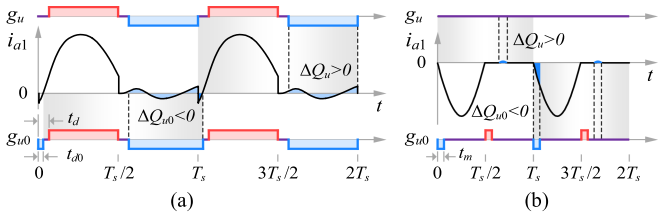

Fig. 15. ΔQ of the BMMR gate signals when $M = 0$. (a) Forward mode. (b) Backward mode.

on the lower arm and it suggests that $\Delta Q_l < 0$ and $\Delta Q_{l1} > 0$. Situation in backward mode is illustrated in Fig. 14(b) and it can be derived that $\Delta Q_u,\ \Delta Q_l > 0$ and $\Delta Q_{u1}, \Delta Q_{l1} < 0$.

B. Voltage Balancing When $M = 0$

To balance the SM voltages, a certain variation on the original gate signal is required to achieve a different ΔQ, otherwise, there is only one kind of gate signal in each arm. To construct a gate signal with different ΔQ, it is suitable to differ the SM state in deadtime, where the arm current is not zero and the voltage increment of SMs in different states may be different.

One possible design in forward mode is illustrated in Fig. 15(a), where the derived gate signal is denoted by g_{u0}. Taking the upper arm for example, in deadtime $[0,\ t_d)$, the SMs assigned g_u enter freewheeling state, whereas the SMs assigned g_{u0} enter inserted state for t_{d0} before entering freewheeling state. The signals in the rest time are the same so all the capacitors in the arm share a common current. By contrast, $\Delta Q_{u0} < \Delta Q_u$. From (13), it is derived that $\Delta Q_{u0} < 0$ and $\Delta Q_u > 0$. Situation is similar in the lower arm, where C_{sm} in the SM assigned g_{l0} is discharged for t_{d0} in deadtime $[T_s,\ T_s + t_d)$, thus $\Delta Q_{l0} < 0$ and $\Delta Q_l > 0$.

In backward mode, all the SMs are in freewheeling state, thus the capacitors' voltage cannot be discharged, which may lead to an overvoltage fault. To solve this problem, the SMs with higher voltages should be inserted into the arm when the current is negative. As shown in Fig. 15(b), an SM is inserted into the arm at the beginning of the first half cycle $[0, t_m)$, and is in conducted state at the beginning of the second half cycle $[T_s/2, T_s/2 + t_m)$ to let the sum of the inserted SMs equal N. This special signal is denoted by g_{u0} in the upper arm and g_{l0} in the lower arm. t_m is typically smaller than $0.05T_s$, and the voltage gain of the modular structure is approximately the same. The discharging signal g_{u0} and g_{l0} ($\Delta Q_{u0}, \Delta Q_{l0} < 0$) will be assigned to the SM with a higher voltage.

With the proposed voltage balance control, each SM voltage is regulated to V_{MV}/N in various operating conditions. This implies that the SM voltages are closely tracking the MV-side voltage, leading to the natural balancing of energies in the arms. As a result, there is no need for individual arm inductors to serve as buffers when the MV voltage varies.

Additionally, in contrast to traditional MMCs, the charging or discharging of each SM capacitor occurs during every switching cycle, resulting in a significantly reduced voltage ripple, typically smaller than 0.5% when $M = 0$. When $M > 0$, there are M SMs inserted in the current path and the ripple becomes larger. Nevertheless, the voltage balance control ensures that higher voltage SMs are inserted in one arm while lower voltage SMs are inserted in the other arm at each switching instant. As a result of this effective control, the instantaneous voltage levels across the inserted capacitors between the MV lines are very close to the MV voltage. The mismatch between the voltages is so low that the presence of parasitic impedance in the system eliminates the need for individual arm inductors.

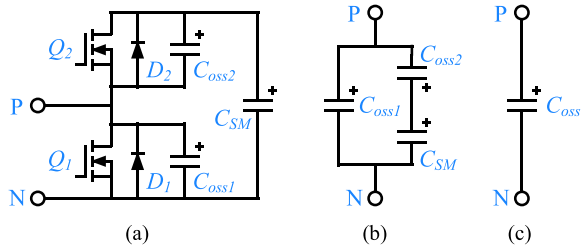

Fig. 16. Detailed and simplified submodule circuits. (a) Detailed model. (b) Simplified model in freewheeling state. (c) Equivalent output capacitor.

V. Soft Switching Analysis

Soft switching is one of the main advantages of resonant converters, which results in minimal switching loss and high efficiency. Without dc bias caused by arm inductors, the BMMR arm current is similar to that of conventional resonant converters and BMMR can achieve full-range soft switching when the gain of the modular structure is not regulated.

A. Soft Switching Analysis When $M = 0$

Like in conventional resonant converters, the soft switching commutation occurs in deadtime and is driven by the magnetizing current i_m.

A more detailed SM circuit configuration is given in Fig. 16(a), in which C_{oss1} and C_{oss2} are the output capacitance of Q_1 and Q_2. When the SM is in freewheeling state, both power devices are OFF and the SM circuit is further simplified to Fig. 16(b), where only the situation before D_1 or D_2 begins to conduct is considered. C_{oss2} (pF level) is much smaller than SM capacitor C_{SM} (μF level), thus the equivalent capacitance of the series connection of C_{oss2} and C_{SM} is equal to C_{oss2}. Besides,

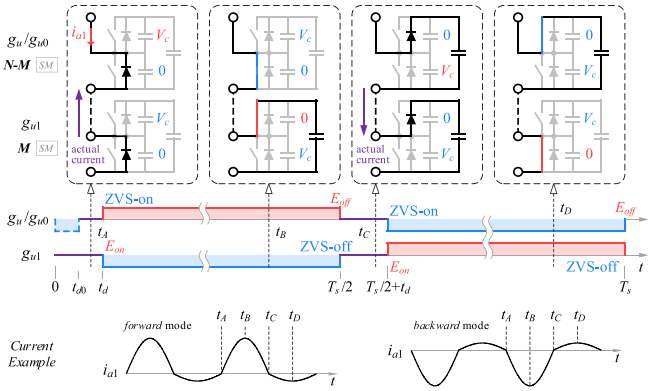

Fig. 17. Current path and gate signals in the upper arm in forward mode.

there is

$$V_{\text{oss1}} + V_{\text{oss2}} = V_c \tag{14}$$

which suggests that the charging or discharging of C_{oss1} and C_{oss2} occurs at the same time as V_c is relatively stable during deadtime. Therefore, the equivalent capacitance of one SM can be written as

$$C_{\text{oss}} = C_{\text{oss1}} + C_{\text{oss2}}. \tag{15}$$

Fig. 17 illustrates the current path in the upper arm at several instants during a forward mode switching cycle. Two SMs in the upper arm are illustrated. One represents the SMs assigned signal g_u or g_{u0}, which include all the SMs in nonregulated operation ($M = 0$). To achieve ZVS-ON of most SMs in the arm, i.e., the SMs assigned signal g_u or g_{u0}, the actual arm current i_{a1} is supposed to be negative at t_d. Notice the C_{oss} voltage of each power device indicated in the illustration, and it suggests that from t_A to t_B, the lower device Q_1 of the g_u/g_{u0} SM turns ON with ZVS, and Q_2 also achieves ZVS-ON from t_C to t_D.

For the converter in backward mode and $M = 0$, ZVS-ON of the LV side devices is achieved as the converter operates in the inductive region, and there is no switching loss on the MV side as no switching occurs.

In conclusion, all the power devices of BMMR can achieve full-range ZVS-ON when $M = 0$ (nonregulated operation), regardless of the voltage gain or the load condition.

B. Soft Switching Analysis When $M > 0$

M can be larger than zero for voltage regulation or SM voltage balancing in backward mode, where some switching loss may be introduced. There are M g_{u1} SMs in the upper arm in Fig. 17, and they turn on with loss while achieving ZVS-off. And in backward mode, as illustrated in Fig. 18, the g_{u1} or g_{u0} SM turns ON with loss and achieves ZVS-OFF ($f_n \leq 1$).

As a comprehensive summary, Table III elaborates the soft switching characteristics in various operating conditions.

It is necessary to point out that M is much smaller than N in practice ($M_{\text{max}} = 4$ when $N = 15$ in the experimental prototype), thus it is reasonable to place particular emphasis

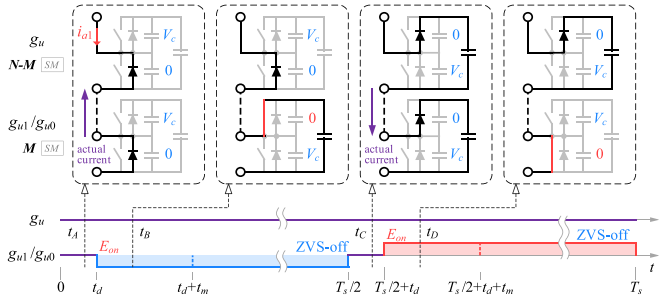

Fig. 18. Current path and gate signals in the upper arm in backward mode.

TABLE III
SOFT SWITCHING IN DIFFERENT CONDITIONS

Mode	M value	$N-M$ SMs	M SMs	LV side
Forward	$M = 0$	ZVS-on	/	ZCS ($f_n \leq 1$)
	$M > 0$		Lossy turn-on	
Backward	$M = 0$	ZCS ($f_n \leq 1$)	/	ZVS-on
	$M > 0$		Lossy turn-on	

on the switching analysis and design considerations pertaining to the $N - M$ SMs and the LV devices, which play a crucial role in achieving the desired performance and efficiency of the converter.

C. Soft Switching Requirements

The requirement to achieve ZVS-ON in forward mode is that C_{oss} of the power device to turn ON is discharged to zero voltage within the deadtime. Considering that the resonant current in deadtime is equal to the magnetizing current i_m and it drives the charging or discharging of C_{oss}, the critical soft switching equation is written as

$$2V_c\,(N - M) \cdot \frac{C_{\text{oss}}}{N - M} = I_m t_d \tag{16}$$

where total $N - M$ SMs are to be charged/discharged per arm and t_d is the duration of the deadtime. i_m in deadtime is approximately equal to its amplitude I_m, which is derived as

$$I_m = \frac{V_{ab}}{2L_m} = \frac{V_{MV}}{2L_m G_a}. \tag{17}$$

Equation (16) can be rewritten as

$$t_d = \frac{8L_m\,(C_{\text{oss1}} + C_{\text{oss2}})}{N - 2M} \tag{18}$$

which gives the minimum deadtime for soft switching.

The minimum deadtime for soft switching is extended by t_{d0} when $M = 0$, as the g_{u1}/g_{l1} SMs stay in the inserted state in deadtime for a time of t_{d0}, and during this interval, no C_{oss} is charged or discharged. The soft switching requirements in backward mode is the same as for conventional resonant converters.

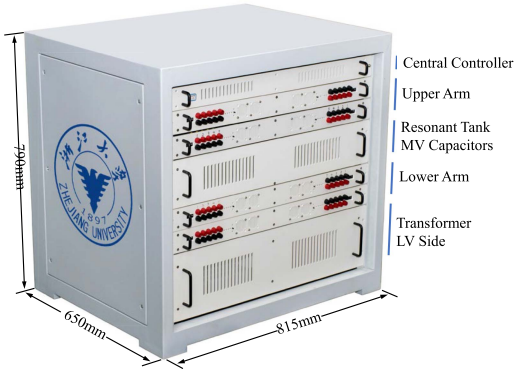

Fig. 19. Photograph of the experimental prototype.

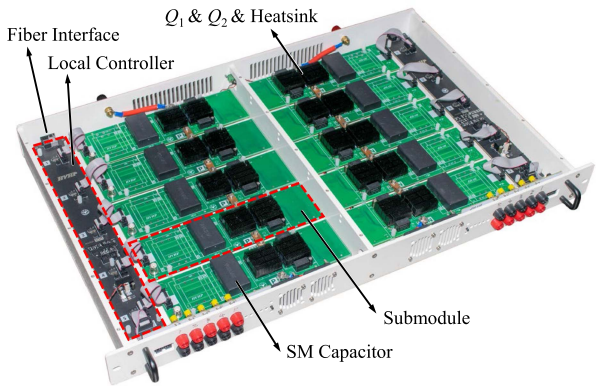

Fig. 20. Photograph of submodules and the local controllers.

TABLE IV
PARAMETERS OF THE PROTOTYPE

Parameters	Symbols	Values
MV rated voltage	V_{MV}	1000V
LV rated voltage	V_{LV}	300V
Rated power	P_o	3.8kW
Number of SMs per arm	N	15
MV resonant inductance	L_{r1}	400μH
MV resonant capacitance	C_{r1}	600nF
LV resonant inductance	L_{r2}	120μH
LV resonant capacitance	C_{r2}	2μF
Magnetizing inductance	L_m	3mH
Transformer turn ratio	n	5/3
MV DC-link capacitance	C_1, C_2	320μF
LV DC-link capacitance	C_{LV}	360μF
Switching frequency	f_s	~7.8kHz
Submodule capacitance	C_{sm}	10μF
Q_1 output capacitance	C_{oss1}	180pF@1000V
Q_2 output capacitance	C_{oss2}	58pF@1000V
S_1~S_4 output capacitance	C_{ossLV}	1.1nF@800V

VI. EXPERIMENTAL VERIFICATION

A downscaled prototype to verify the aforementioned analysis is designed and built, and the experimental results are analyzed in detail.

A. Design of the Prototype

A picture of the prototype is shown in Fig. 19 and the parameters of the experimental setup are listed in Table IV.

With a large number of SMs to control, a two-level control architecture is employed. As shown in Fig. 20, each local controller based on a field-programmable gate array (FPGA) is responsible for the control of five SMs and it communicates with the FPGA and digital signal processor–based central controller. The central controller runs the control logic, sorting the SM voltages, and assigning gate signals for every SM and the LV side device. The control instructions are transmitted to each local controller with an optical fiber connection. The local controller generates gate signals for switches, samples every SM voltage, and sends it to the central controller.

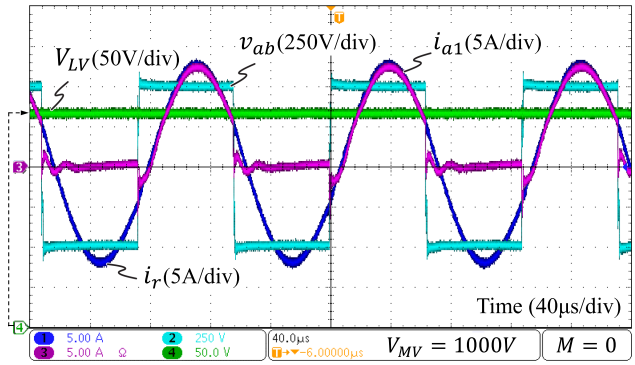

Fig. 21. Experimental waveforms in forward mode steady state when $M = 0$.

The lower and the upper switch in SM are CREE C3M0021120K and C3M0075120K SiC MOSFETs, and the LV side switch is CREE CAS120M12BM2 Half-Bridge Module.

B. Experimental Results

1) Steady-State Waveforms: Fig. 21 shows the waveforms of the prototype in forward mode steady state with $M = 0$ and medium voltage $V_{\rm MV}$= 1000 V, where the resonant current i_r, the upper arm current i_{a1}, and the LV side output voltage $V_{\rm LV}$ are displayed. These waveforms resemble that of a regular *CLLC* converter. v_{ab} is a square wave with an amplitude of 500 V, as same as $V_{\rm MV}/2$ and the modular structure gain is 2. i_{a1} is equal to i_r in a half switching cycle and becomes zero in the other. This suggests that the resonant current totally flows through one arm per half cycle, which is consistent with (4).

When $M > 0$, the resonant current flows via both arms as shown in Fig. 22 where $M = 2$. i_{a1} is smaller than i_r in a half switching cycle and is not zero in the other half cycle. This is because there are two SMs inserted in each arm and they are charged, so the sum voltage of the SMs will be larger than $V_{\rm MV}$. As a result, there will be a discharging current in the arm and thus the resonant current is no longer flowing in one arm alone.

Figs. 23 and 24 show the waveforms in backward mode when M equals 0 and 2, respectively. Due to the symmetry of the topology, the waveforms are like that in forward mode.

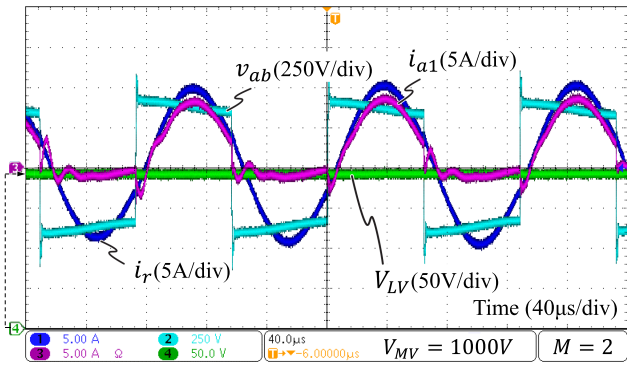

Fig. 22. Experimental waveforms in forward mode steady state when $M = 2$.

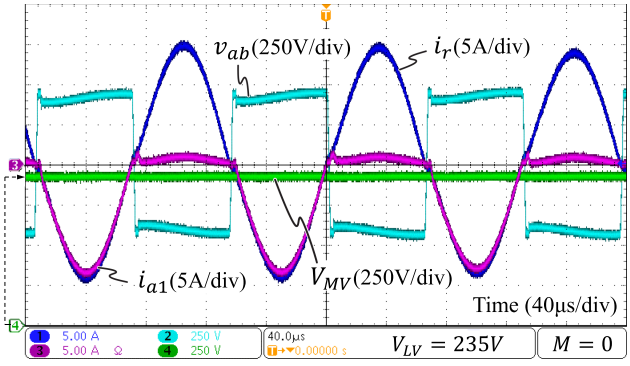

Fig. 23. Experimental waveforms in backward mode steady state when $M = 0$.

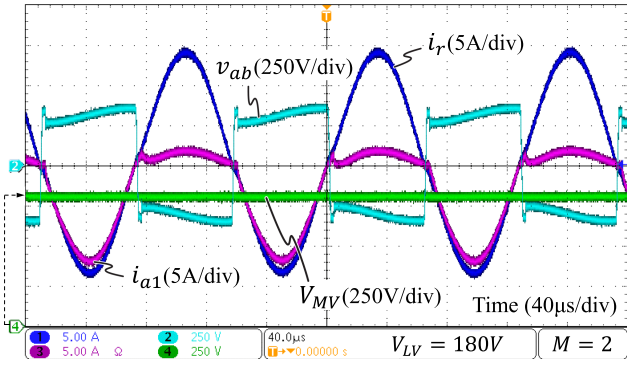

Fig. 24. Experimental waveforms in backward mode steady state when $M = 2$.

2) Soft Switching Verification: The gate voltage v_{gs}, the drain-source voltage v_{ds}, and the drain current i_d of the lower power device in an upper arm SM is probed and the results are shown in Fig. 25.

In forward mode and $M = 0$, two kinds of gate signals, namely g_u and g_{u0}, can be assigned to an SM, and ZVS-ON of the power devices can be achieved with both. Fig. 25(a) is the waveforms of a lower device when the SM is assigned g_u and Fig. 25(b) is that when g_{u0} is assigned. They both show that ZVS-ON is achieved. Fig. 25(c) shows the waveforms of a lower device when $M = 1$ and the SM is assigned g_{u1}, and it suggests that the device experiences hard switching ON.

TABLE V
OUTPUT VOLTAGE IN FORWARD MODE

M	0	1	2	3	4	5
V_{LV}(V)	78.7	68.9	58.8	48.3	37.6	26.6

TABLE VI
OUTPUT VOLTAGE IN BACKWARD MODE

M	0	1	2	3	4	5
V_{MV}(V)	185	211	246	295	367	480

In backward mode, most power devices in SMs are in OFF state. Fig. 25(d) shows the gate signal and drain–source voltage of a lower device when $M = 0$ and the SM is assigned g_{u0}, in which the gate signal is a short pulse of about 0.8 μs. The waveforms suggest that ZVS-ON is not achieved, which is consistent with the analysis aforementioned.

3) SM Voltage Balancing: Figs. 26 and 27 show several SM capacitor voltages v_{c1}–v_{c4} in arm. The proposed feedback balancing method and an open-loop rotating balancing method [35] are tested. As shown in Fig. 26, the voltage divergence is significant in the rotating balancing method, whereas it reduces to a reasonable level when the proposed balancing method is applied. The probed v_c increased as they were lower than the mean voltage.

The SM voltage in forward mode with $V_{\mathrm{MV}} = 1000V$ and $M = 0$ and $M = 2$ is shown in Fig. 27(a) and (b), respectively. The SM voltage in backward mode with $V_{\mathrm{MV}} = 1000$ V and $M = 0$ and $M = 2$ is shown in Fig. 27(c) and (d) , respectively. The SM voltages are well-balanced, and their mean voltage equals V_{MV}/N.

4) Coordinated Voltage Control: Fig. 28 shows the transition of M from 2 to 1 with f_s unchanged, where BMMR works in forward mode and $V_{\mathrm{MV}} = 300$ V. The LV-side voltage V_{LV}, the resonant current i_r, the capacitor voltage v_c, and the modular structure voltage v_{ab} are shown in Fig. 28. A current spike occurs during the transition, where the peak value is about 180% of the normal value. V_{LV} increases from 57 to 67 V. The mean SM capacitor voltage remains the same, although the fluctuation becomes larger. They have an average value of V_{MV}/N, as analyzed before.

Test the circuit with various M, and the output voltages are recorded in Table V and VI. The input voltage in forward mode and backward mode is $V_{\mathrm{MV}} = 300$ V and $V_{\mathrm{LV}} = 60$ V, respectively. Considering that the voltage gain of the resonant tank may not be the unity gain and that there are some inevitable voltage drops on power devices and power lines, a fixed correction factor is multiplied by the voltages to make sure that $G_a = 2$ when $M = 0$. The calculated and scaled G_a is illustrated in Fig. 29. The result in forward mode fits well with the theoretical result. However, the result in the backward mode diverges from the theoretical one. This is because the forward voltage V_f of the diode D_1 is not taken into consideration in (10) for simplicity. A more realistic gain expression

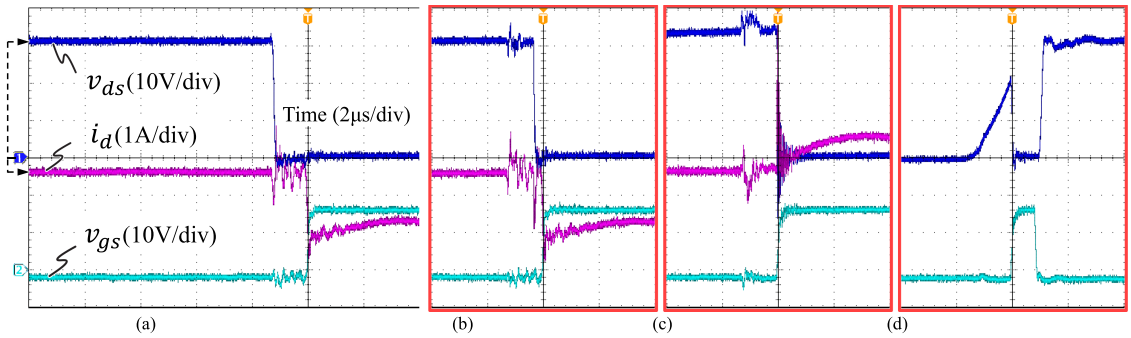

Fig. 25. Experimental waveforms of a submodule lower device in forward mode [(a), (b), and (c) with $V_{\mathrm{MV}} = 450$ V] and in backward mode [(d) with $V_{\mathrm{LV}} = 140$ V]. (a) ZVS-ON and $M = 0$. (b) ZVS-ON and $M = 0$. (c) Hard switching ON and $M = 1$. (d) Hard switching ON and $M = 0$.

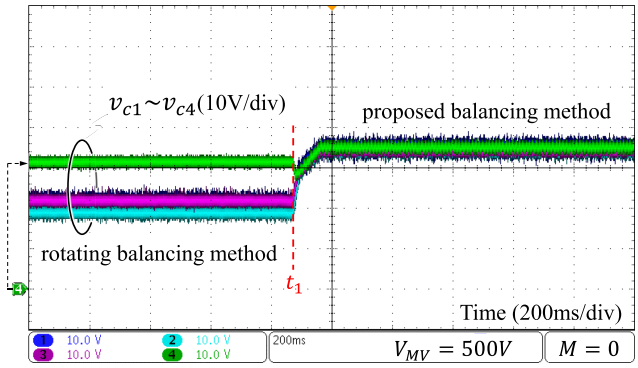

Fig. 26. Experimental waveforms of the submodule voltages in forward mode when switching to the proposed balancing method.

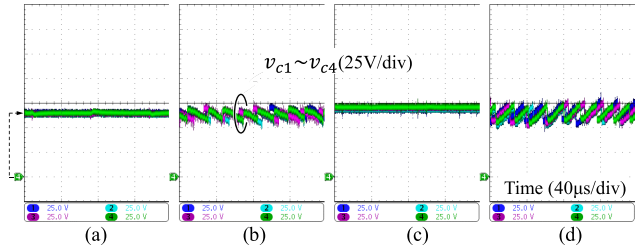

Fig. 27. Experimental waveforms of the submodule voltages in forward mode [(a) and (b)] and backward mode [(c) and (d)]. (a) $M = 0$. (b) $M = 2$. (c) $M = 0$. (d) $M = 2$.

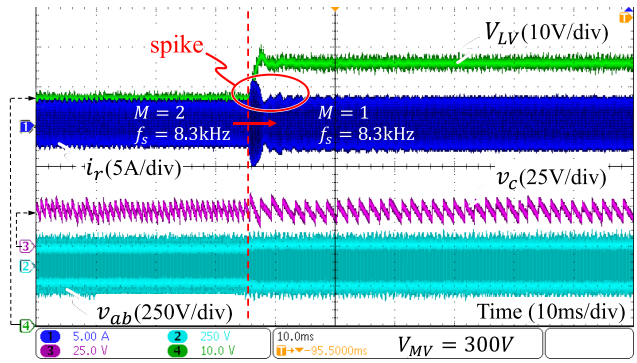

Fig. 28. Experimental waveforms in forward mode when M changes without frequency change.

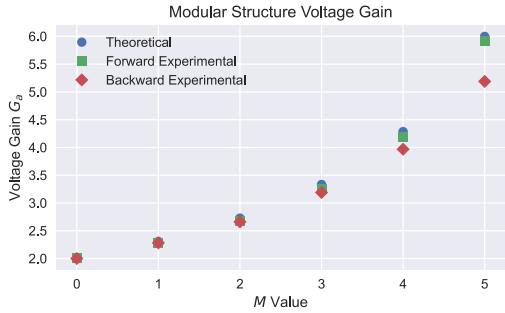

Fig. 29. Modular structure voltage gain versus M by experimental results.

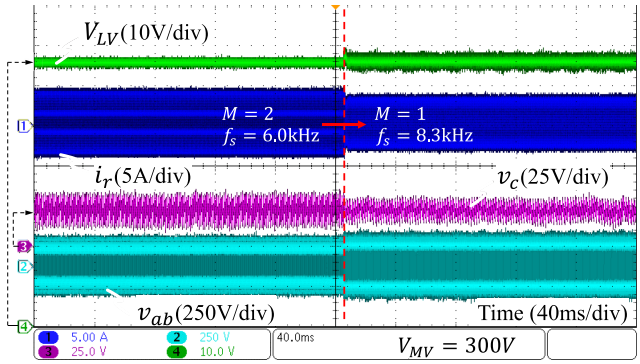

Fig. 30. Experimental waveforms in forward mode when M changes with frequency change, i.e., with coordinated gain control.

involving V_f will be

$$G_a = \frac{2N}{N - 2M} \cdot \frac{V_{ab} - NV_f}{V_{ab}}. \tag{19}$$

In coordinated voltage control shown in Fig. 30, simultaneously change M and f_s and no spike occurs. V_{LV} remains the same during the transition. The experimental waveforms in Fig. 31 verified the analysis in backward mode.

A continuous voltage gain range is achieved in Fig. 32, where the coordinated gain control is employed. The frequency is decreasing at a certain speed and steps to an upper cross point

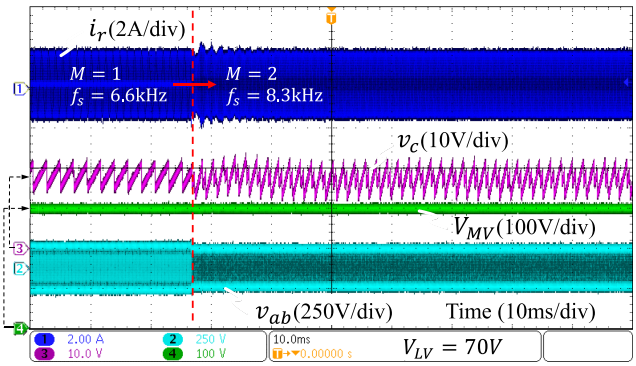

Fig. 31. Experimental waveforms in backward mode when M changes with frequency change, i.e., with coordinated gain control.

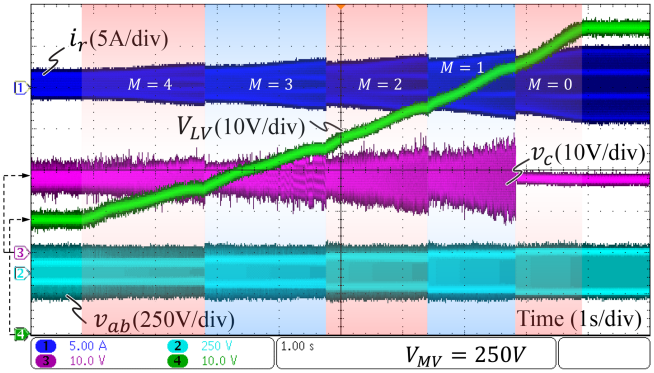

Fig. 32. Experimental waveforms in forward mode when the voltage gain continuously changes by coordinated gain control.

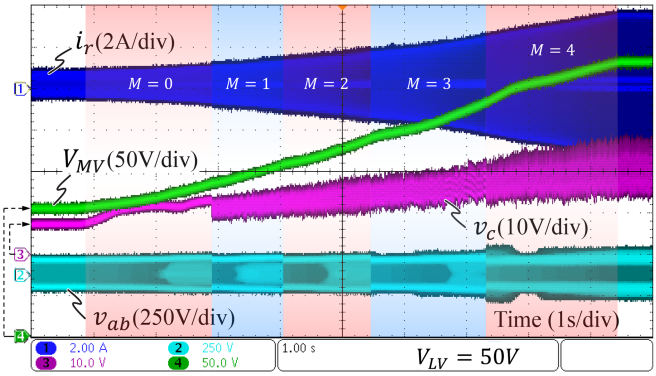

Fig. 33. Experimental waveforms in backward mode when the voltage gain continuously changes by coordinated gain control.

when it meets the lower cross point. Notice that the transition is smooth as there is no resonant current spike or overshot in the LV output voltage. A similar test is performed in backward mode and the results are similar, as shown in Fig. 33. Notice that in the backward experiment, the LV-side voltage is fixed and the voltage gain is changed, thus the MV voltage changes. As a result, the capacitor voltage also changes as it is proportional to the MV-side voltage.

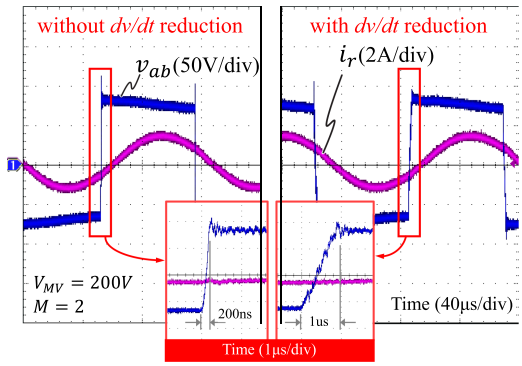

Fig. 34. Comparison of experimental waveforms with and without dv/dt reduction control in forward mode.

For dv/dt-sensitive applications, the BMMR modulation method can be slightly modified to let the converter operate in quasi-two-level mode, with little impact on voltage balancing and soft switching. By grouping the SMs into several groups and applying various small delays to their gate signals, the dv/dt can be significantly reduced. As shown in Fig. 34, the switching transience duration is changed from 200 ns to 1 μs, and the dv/dt is decreased to one-fifth of its original value.

VII. Conclusion

A BMMR dc–dc converter with a wide voltage range for medium-voltage power conversion applications is proposed in this article. Compared with ISOP structures, BMMR uses only one high-power transformer, which can greatly reduce the total volume of power transformer(s) and leads to a low system footprint. Compared with other MMDCs, the proposed arm-inductor-less converter operates with soft switching in full voltage and load range, due to the elimination of the dc circulating current that is typically present in the modular structure. Analysis of operation principles and voltage gain control of the converter in steady state are presented. The coordinated voltage gain control that combines the modulation control of SMs and the control of switching frequency is proposed, by which the converter achieves a wide and continuous voltage gain range within a relatively narrow frequency range. The SM voltage balancing method by sorting the SM voltages and reassigning the gate signals is implemented in different working conditions. The soft switching requirements are analyzed in detail. Finally, experimental results on a BMMR prototype are given to demonstrate the feasibility. These results suggest that BMMR is a promising candidate for MVDC applications requiring bidirectional power conversion over a wide voltage range.

Appendix

The arm current expressions are given as

$$\begin{cases} i_{a1}(t) = a_1 \sin \omega t + b_1 \cos(ct + d) \\ i_{a2}(t) = a_2 \sin \omega t + b_2 \cos(ct) - k \sin(ct) \end{cases}, \quad t \in [0, T_s/2)$$

where

$$\begin{cases} a_1 = \frac{I_r\left(C_{\mathrm{SM2}}L_a\omega^2-1\right)}{2C_{\mathrm{SM2}}L_a\omega^2-1}\ ,\ a_2 = \frac{-I_rC_{\mathrm{SM2}}L_a\omega^2}{2C_{\mathrm{SM2}}L_a\omega^2-1} \\ b_1 = \frac{I_r\omega\sqrt{2C_{\mathrm{SM2}}L_a}\csc\left(\frac{\pi}{2\omega\sqrt{2C_{\mathrm{SM2}}L_a}}\right)}{4C_{\mathrm{SM2}}L_a\omega^2-2} \\ b_2 = \frac{I_r\omega\sqrt{2C_{\mathrm{SM2}}L_a}\cot\left(\frac{\pi}{2\omega\sqrt{2C_{\mathrm{SM2}}L_a}}\right)}{4C_{\mathrm{SM2}}L_a\omega^2-2} \\ c = -\frac{1}{\sqrt{2C_{\mathrm{SM2}}L_a}},\ d = \frac{\pi}{2\omega\sqrt{2C_{\mathrm{SM2}}L_a}}\ ,\ k = \frac{I_r\omega\sqrt{2C_{SM2}L_a}}{4C_{\mathrm{SM2}}L_a\omega^2-2} \end{cases}.$$

As L_a approaches infinity, the limits of the expressions are as follows:

$$\begin{cases} i_{a1}(t) = \frac{I_r}{\pi} + \frac{I_r}{2}\sin\omega t \\ i_{a2}(t) = \frac{I_r}{\pi} - \frac{I_r}{2}\sin\omega t \end{cases},\quad t \in [0, T_s/2).$$

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