Thermal–Electrical Modeling and Co-Optimization of a Half-Bridge Power Module With Silver-Sintered Molybdenum Packaging

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***Abstract*—This article proposes a methodology of analytical modeling and optimization of power modules, especially compatible with modules with silver-sintered molybdenum (SSM) packaging or other insulated metal substrate types of packaging schemes. First, a decoupled Fourier-based thermal model is presented, which considers the barrier effect between substrate segments. Compared with the original Fourier-based model, it reduces the average error from 93.8% to 10.9%, when estimating the difference of junction temperatures (T_j) for power modules with asymmetric substrates. Then, a stray inductance (L_s) model is developed based on the partial inductance method and the actual current distribution, whose error is less than 12.1% when tested with example half-bridge SSM modules. Next, analytical models are combined with the particle swarm optimization algorithm to design a half-bridge power module with SSM packaging. Numerical simulations prove that the analytical estimations of T_j and L_s of the optimized module are accurate, with errors of 4.6% and 8.3%, respectively. The fabrication process of the designed SSM module is then elaborated. Finally, the accuracy of L_s estimation is validated by the double-pulse test, where the error is 0.4%. The junction-to-case thermal resistance is characterized by the structural function analysis, in which the error is 3.4%**

***Index Terms*—Modeling, optimization methods, power electronics, semiconductor device packaging.**

I. Introduction

POWER modules are the main building blocks in power electronic systems. The optimal design of power modules is essential for achieving satisfactory efficiency, reliability, and power density. When bare semiconductor dies are packaged into a power module, multiphysics challenges exist. Proper thermal management is necessary to deal with the heat losses generated by dies. Meanwhile, parasitic elements of the internal conductors affect the switching behavior of devices. Specifically, there are two major parameters to consider. One is the junction temperature (T_j) of semiconductor dies, which should be limited to a safety threshold. The other is the stray inductance of the main switching loop (L_s), which should be minimized to reduce the switching loss and the overvoltage during switching. There exist several methods to evaluate T_j and L_s of power modules. Numerical methods, such as finite-element analysis (FEA), are accurate but time-consuming and are mostly used in simulating a fixed structure. Instead, analytical models are more suitable for rapid calculations during optimization.

Generally, there are two types of analytical thermal models: lumped thermal network model and physical-based model. The thermal network varies from 1-D structures [1], [2] to 3-D structures [3], [4]. However, since the network parameters need to be extracted from numerical simulations, this method can only be used for a fixed geometry, making it unpractical for optimizing geometric variables. Some studies reported physical-based thermal networks. However, they are only verified to be accurate with 1-D simplified geometries [2]. Masana [5] introduced a simplified physical-based thermal resistance model, the constant spreading angle model. However, this model is only verified to be accurate with a single-layer geometry. Bouguezzi et al. [1] integrated the constant spreading model with a 1-D thermal network. However, the thermal coupling between different heat sources still requires FEA calibration. Fourier-based models are another type of analytical model. They directly solve the heat transfer equations, such as Laplace's equation for the steady-state conduction, in the form of finite Fourier series [6], [7], [8], [9]. The challenge is to determine the Fourier constants using boundary conditions. Thus, the geometry needs to be simplified. The authors in [8] and [9] proposed Fourier-based solutions for printed circuit boards (PCBs) with embedded heat sources. The authors in [6] and [7] derived the temperature field of conventional power modules based on this method and obtained a good accuracy of 96.5%. Generally, the Fourier-based models exhibit improved

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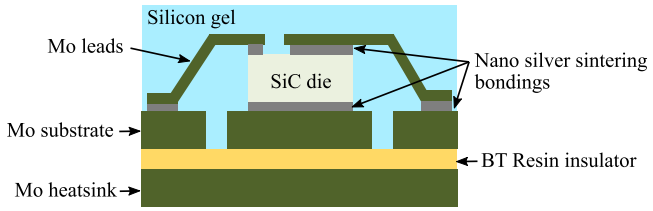


Fig. 1. SSM packaging scheme.

accuracy than other analytical models and are suitable for optimization.

Similarly, conductors' L_s can be estimated by both the numerical methods and the analytical models. Numerical tools, such as ANSYS Q3D, are now convenient and accurate but, again, computationally expensive. The analytical expression for L_s has been studied for decades. There are extensively proven equations for simple conductors, such as wires and coils, which have been summarized by Grover [10] and Leferink [11]. However, power modules have complicated internal conductors, which are similar to busbars. Wada et al. [12] introduced a partial inductance model for rectangular busbars, which is also suitable for power modules.

When designing power modules, there is always a tradeoff between the thermal performance, power density, and L_s. Generally, a larger footprint could reduce T_j but also reduce the power density and increase L_s. Therefore, co-optimization is needed to ensure balanced performances. Evolutionary algorithms have been widely applied in this field. Ji et al. [13] introduced an optimization process using the nondominated-sorting-genetic algorithm II for power module design, which shows promising performance in dealing with multiobjective optimizations. The same algorithm has been used in the development of the PowerSyth Software [14] for the co-optimization of conventional planar power modules. Another practical and effective algorithm is the particle swarm optimization (PSO) algorithm. Alavi et al. [15] used PSO in optimizing the thermal design of a power module. Similarly, Alizadeh et al. [16] applied this algorithm in designing silicon carbide (SiC) converters. In fact, thermal-electrical co-optimization methods for power modules with various algorithms have been widely studied in the literature.

Although the conventional planar packaging with the direct bond copper (DBC) substrate is still the mainstream, new packaging technologies have been proposed in the past two decades in response to the growing need for performance, reliability, and cost [17]. Different packaging technologies usually require special design methodologies. This article focuses on a novel packaging technology, named silver-sintered molybdenum (SSM) packaging, proposed in our previous work [18]. It features with high-temperature durability and long lifetime. SSM packaging falls into the category of insulated metal substrate (IMS) type of packaging, which has a simplified layer stack-up compared to the DBC-based modules. Therefore, directly applying the design methods for the DBC module would be inadequate. The SSM packaging scheme is shown in Fig. 1. The molybdenum (Mo) substrate is integrated on a direct-cooled Mo heatsink

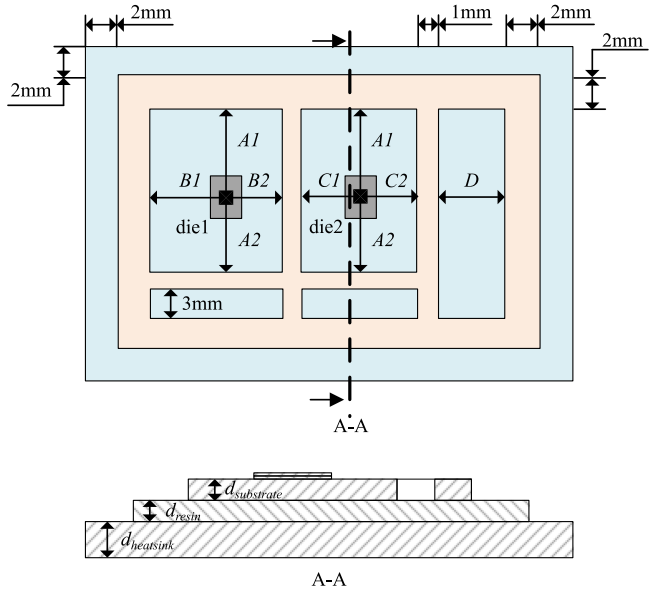


Fig. 2. Geometrical layout of the half-bridge SSM module.

using bismaleimide triazine (BT) resin bonding, which forms an IMS-type structure. The SiC die is sintered on the substrate, and the interconnections are constructed by planar leads.

In this article, a half-bridge module containing two dies is studied. The layout of this module is shown in Fig. 2, where several geometric parameters are defined and will be considered as variables in the optimization.

The rest of this article is organized as follows. First, an analytical thermal model, named decoupled Fourier model, is introduced in Section II. Then, an L_s model based on the partial inductance method is presented in Section III. Next, Section IV introduces the thermal–electrical co-optimization using the PSO algorithm, as well as the simulation validation of the optimized module. Finally, the designed module is fabricated and characterized experimentally in Section V. Finally, Section VI concludes this article.

The main contribution of this study is that thermal–electrical modeling methods and a co-optimization procedure are proposed for SSM power modules. Compared with most of the existing thermal–electrical models that are designed for power modules with the conventional packaging, models proposed in this article are especially designed for the SSM packaging and similar packaging structures. Therefore, they exhibit greatly improved accuracies when applied on concerned structures. Meanwhile, as analytical models, they require no calibrations using numerical simulations, which enable much faster calculations than methods involving simulations. Mathematical processes of analytical models are also explained thoroughly to provide readers with complete know-how and flexibility for different applications. Second, the proposed co-optimization method provides a working procedure for the optimal design of half-bridge SSM power modules, which has also not been reported in the literature. Finally, the accuracies of the proposed methods are validated through both numerical simulations and experiments.

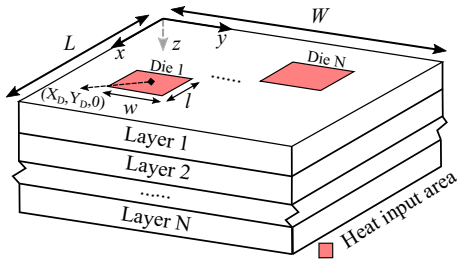


Fig. 3. Simplified power module with cuboid layers.

II. Thermal Model

Thermal management is essential in power module design. The temperature distribution, especially T_j at dies, affects the reliability and lifetime of the device. Typically, it is required to keep T_j within a safe range. In this article, the threshold is 200 °C for the considered SSM packaging [18]. It is also important to ensure that the difference of T_j between different dies is limited.

A. Fourier-Based Model for a Three-Layer Simplified Geometry

The internal structure of power modules is similar to a stack of cuboid layers with a unified section area. On the top of the first layer, several rectangular areas receive the heat flux, representing the corresponding areas on the substrate, and are equal to the die area. The simplified geometry is illustrated in Fig. 3. If multiple heat sources exist, the total temperature field is the summation of all the temperature fields when considering each heat source individually due to the linearity of this heat transfer problem.

The governing equation for the steady-state 3-D heat transfer is as follows:

$$\frac{\partial^2\theta}{\partial x^2}+\frac{\partial^2\theta}{\partial y^2}+\frac{\partial^2\theta}{\partial z^2}=0. \tag{1}$$

The boundary conditions for the geometry in Fig. 1 are summarized in (2)–(4). Specifically, in the SSM packaged module, there are only three layers to be considered: the substrate layer, the resin layer, and the heatsink layer.

On the top of layer 1, we have

$$\begin{cases}\frac{\partial\theta}{\partial z}|_{z=0}=-\frac{P}{k_1 lw}\ \text{(Inside die areas)}\\ \frac{\partial\theta}{\partial z}|_{z=0}=0\ \text{(Outside of die areas)}\end{cases}. \tag{2}$$

At interfaces between layers, we have

$$\begin{cases}k_i\frac{\partial\theta_i}{\partial z}|_{z=z_i}=k_{i+1}\frac{\partial\theta_{i+1}}{\partial z}|_{z=z_i}\\ \theta_i(x,y,z_i)=\theta_{i+1}(x,y,z_i)\end{cases}. \tag{3}$$

At the bottom of layer 3, we have

$$k_3\frac{\partial\theta_3}{\partial z}|_{z=z_3}=-h\cdot\theta_3|_{z=z_3} \tag{4}$$

where θ refers to the temperature rise, which is the temperature difference between the specific location and the coolant. k_i denotes the thermal conductivity of the ith layer. z_i refers to the bottom of the ith layer, which equals $\sum_{j=1}^{i} d_j$, where d_i is the thickness of the ith layer. P is the heat flow at each heat input area. h is the equivalent convection coefficient at the bottom. The geometrical variables, including X_D, Y_D, l, w, L, and W, can be found in Fig. 3.

This problem can be solved by the Separation of the Variable method. The general solution is as follows:

$$\begin{aligned}\theta(x,y,z)=A_{i0}+B_{i0}z+\sum_{m=1}^{\infty}\cos(a_m x)[A_{im}\cosh(a_m z)\\ +B_{im}\sinh(a_m z)]\\ +\sum_{n=1}^{\infty}\cos(b_n y)[A_{in}\cosh(b_n z)\\ +B_{in}\sinh(b_n z)]\\ +\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\cos(a_m x)\cos(b_n y)[A_{imn}\cosh(c_{mn}z)\\ +B_{imn}\sinh(c_{mn}z)]\end{aligned} \tag{5}$$

where $a_m=\frac{m\pi}{L}$, $b_n=\frac{n\pi}{W}$, $c_{mn}=\sqrt{a_m+b}$. A_{i0}, B_{i0}, A_{im}, B_{im}, A_{in}, B_{in}, A_{imn}, and B_{imn} are parameters to be determined by integral and differential operations of boundary conditions. Choudhury and Rogers [7] proposed an iterative method to derive those parameters.

The SSM power packaging has a three-layer configuration. And only the temperature distribution of the first layer is needed to calculate the junction temperature. The required parameters are solved and elaborated in (6)–(18). With those parameters, the temperature field can be easily expressed using (5) and (19)

$$B_{10}=-\frac{P}{k_1 LW} \tag{6}$$

$$A_{10}=\frac{P}{LW}\left[\frac{d_1}{k_1}+\frac{d_2}{k_2}+\frac{d_3}{k_3}+\frac{1}{h}\right] \tag{7}$$

$$B_{1m}=\frac{-4P\cos(a_m X_D)\sin(a_m l/2)}{LWlk_1 a_m^2} \tag{8}$$

$$B_{1n}=\frac{-4P\cos(b_n Y_D)\sin(b_n w/2)}{LWlk_1 b_n^2} \tag{9}$$

$$B_{1mn}=\frac{B_{1m}B_{1n}a_m b_n LWk_1}{c_{mn}} \tag{10}$$

$$A_{1m}=-\frac{B_{1m}}{V_{1m}} \tag{11}$$

$$A_{1n}=-\frac{B_{1n}}{V_{1n}} \tag{12}$$

$$A_{1mn}=-\frac{B_{1mn}}{V_{1mn}}. \tag{13}$$

Intermediate parameters needed for (11)–(13) are defined as follows:

$$\begin{aligned}&V_{1p}(p=m,n,mn)\\ &=\frac{\left(\frac{V_{3p}U_{2p}-I_{2p}}{V_{3p}I_{2p}-O_{2p}}\right)U_{1p}-I_{1p}}{\left(\frac{V_{3p}U_{2p}-I_{2p}}{V_{3p}I_{2p}-O_{2p}}\right)I_{1p}-O_{1p}}\end{aligned} \tag{14}$$

$$V_{3p} = \frac{\delta \sinh(\delta z_3) + \frac{h\cosh(\delta z_3)}{k_3}}{\delta \cosh(\delta z_3) + \frac{h\sinh(\delta z_3)}{k_3}} \tag{15}$$

$$U_{ip} = \cosh^2\left(\delta \sum_{j=1}^{i} d_j\right) - \frac{k_i}{k_{i+1}} \sinh^2\left(\delta \sum_{j=1}^{i} d_j\right) \tag{16}$$

$$I_{ip} = \sinh\left(\delta \sum_{j=1}^{i} d_j\right) \cosh\left(\delta \sum_{j=1}^{i} d_j\right) \left(1 - \frac{k_i}{k_{i+1}}\right) \tag{17}$$

$$O_{ip} = \sinh^2\left(\delta \sum_{j=1}^{i} d_j\right) - \frac{k_i}{k_{i+1}} \cosh^2\left(\delta \sum_{j=1}^{i} d_j\right) \tag{18}$$

(if $p = m$, $\delta = a_m$; if $p = n$, $\delta = b_n$; and if $p = mn$, $\delta = c_{mn}$).

Finally, T_j needs to include the coolant temperature (T_{coolant}) and the temperature rise at the die bonding layer and the die layer, as shown in the following equation:

$$T_j = \theta(X_D, Y_D, 0) + \frac{Pd_{Ag}}{lwk_{Ag}} + \frac{Pd_{\text{die}}}{lwk_{\text{die}}} + T_{\text{coolant}}. \tag{19}$$

A brief introduction of the solving process of Fourier parameters is given in the following paragraphs, which is based on the iterative process proposed by Choudhury and Rogers [7].

Step 1: Obtain B_{1m}, B_{1n}, B_{1mn}, and B_{10}.

Substitute (5) into (2) and solve it. Then, (6) and (8)–(10) are obtained.

Step 2: Obtain A_{10}.

Assume a two-layer structure. Use the bottom surface boundary condition [see (4)] and (5); then, (20) can be obtained. Similarly, use the interface boundary conditions [see (3)] and (5); then, (21) and (22) can be obtained. Next, (23) can be obtained by combining (6) and (21). In addition, use (20), (22), and (23); A_{10} for the assumed two-layer structure can be obtained, as shown in (24). Therefore, A_{10} for a three-layer structure (SSM packaging) can be written in the same pattern as shown in (7)

$$-(h/k_2)A_{20} = B_{20}\left(1 + \frac{h(d_1 + d_2)}{k_2}\right) \tag{20}$$

$$k_1 B_{10} = k_2 B_{20} \tag{21}$$

$$A_{10} + B_{10}d_1 = A_{20} + B_{20}d_1 \tag{22}$$

$$B_{20} = -\frac{P}{k_2 LW} \tag{23}$$

$$A_{10} = \frac{P}{LW}\left(\frac{d_1}{k_1} + \frac{d_2}{k_2} + \frac{1}{h}\right). \tag{24}$$

Step 3: Obtain A_{1m}, A_{1n}, and A_{1mn}.

Substitute (5) into (4) and solve it. Then, (15) is obtained. Combining it with (3), the following equation can be obtained:

$$V_{1p}(p = n, m, mn) = -\frac{B_{1m}}{A_{1m}} = \frac{V_{2p}U_{1p} - I_{1p}}{V_{2p}I_{1p} - O_{1p}} \tag{25}$$

$$V_{2p}(p = n, m, mn) = -\frac{B_{2m}}{A_{2m}} = \frac{V_{3p}U_{2p} - I_{2p}}{V_{3p}I_{2p} - O_{2p}}. \tag{26}$$

Substitute (14) into (25) and (26); then, A_{1m} can be solved. A_{1n} and A_{1mn} can be obtained in the same fashion.

B. Decoupled Fourier-Based Model for IMS-Type Power Modules

The aforementioned original Fourier-based method has two major limitations. First, areas of all the layers are assumed equal, which is unrealistic. For example, the heatsink layer is usually larger than the substrate layers. Thus, there should be an equivalent area assigned for all the layers. Defining the equivalent area is essential to achieve accurate estimation using Fourier-based thermal models. In practice, the equivalent area should be defined based on the thermal coupling and heat spreading. In other words, the equivalent area should represent where the main heat flux pass through horizontally. Second and more importantly, all the layers are assumed to be a single and united body. However, in power modules, some layers are separated into segments, such as the top tracing layer of the substrate. This assumption does not have a noticeable effect on conventional power modules, because their tracing layer is very thin and has little impact on the heat spreading. However, this could lead to significant errors when applied in IMS-type modules.

IMS-type packaging is featured with a sandwich structure. Unlike the conventional packaging, where the baseplate is the main heat spreader, the heat spreading in IMS-type modules mostly occurs at the thick substrate layer. In addition, because of the extremely low k of the resin layer, the thermal coupling between different substrate segments is very minimum. The horizontal heat flux commuting between different segments is extremely low and neglectable. Therefore, each segment should be considered individually.

To capture the unique heat transfer characteristics of IMS-type modules, a decoupling method is proposed. The decoupling of a half-bridge module with two dies is given in Fig. 4 as an example. There are two substrate segments that are receiving the heat flux. The volume under each segment is considered as an individual heat transfer unit, which is utilized to calculate T_j of the corresponding die using the Fourier-based method. The equivalent area for each individual calculation equals the area of the corresponding Mo substrate due to the aforementioned reasons.

C. Simulation Evaluation

To evaluate the accuracy of the decoupled Fourier-based method for IMS-type power modules, six cases are simulated using the original coupled model, the decoupled model, and FEA (conducted in ANSYS Mechanical). The geometrical topology follows the schematic shown in Fig. 2, and their dimensions are summarized in Table I. Other dimensions remain constants, specifically, $A1 = A2 = 10$ mm, $D = 5$ mm, $d_{\text{substrate}} = 1$ mm, and $d_{\text{resin}} = 0.2$ mm. These cases covered symmetric and asymmetric designs with different footprints. In simulations, h is 5000 W/m^2·°C at 105 °C coolant temperature. P_{loss} is 41 W for each die. T_j values from FEA simulations are measured at the center of dies' top surface, which agrees with the T_j definition in the analytical thermal model.

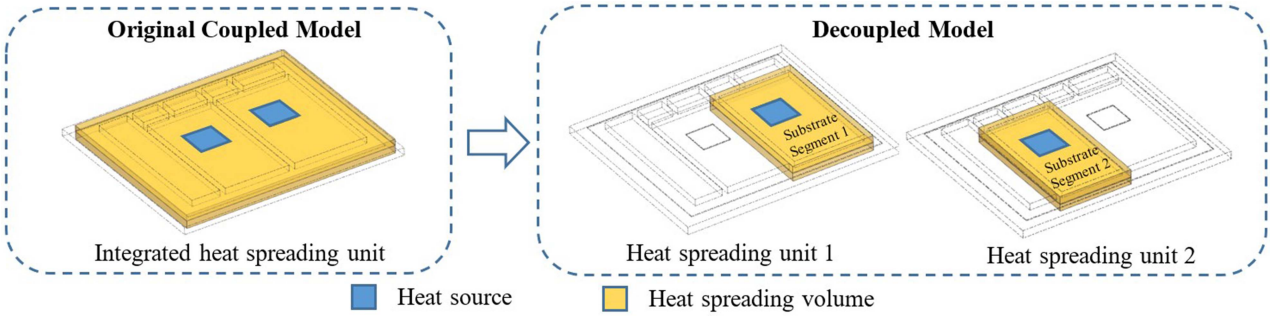


Fig. 4. Decoupling of heat spreading in a half-bridge IMS-type module.

TABLE I
DIMENSION OF CASES FOR THERMAL MODEL EVALUATION

Dimensions	Case A	Case B	Case C	Case D	Case E	Case F
B1 (mm)	10	10	10	15	10	15
B2 (mm)	10	10	10	15	10	15
C1 (mm)	5	10	15	10	5	5
C2 (mm)	15	10	5	10	5	5

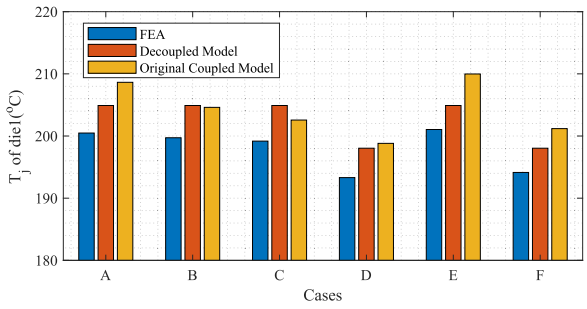


Fig. 5. T_j of die 1.

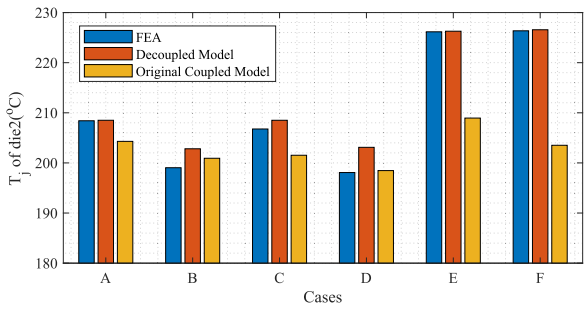


Fig. 6. T_j of die 2.

T_j of die 1 (located on substrate segment 1) is illustrated in Fig. 5. FEA results of cases A–C show that T_j of die 1 is not affected by the area of segment 2, which is also found in results from the decoupled model. However, the original coupled model fails to capture this trend. Fig. 6 shows T_j of die 2. The original coupled model shows significantly larger errors in cases E and F, where segment 1 is several times larger than segment 2. Overall, when estimating the temperature rise

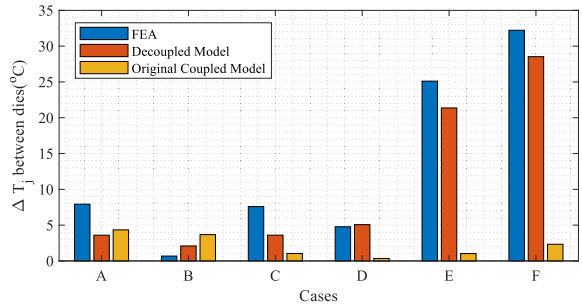


Fig. 7. ΔT_j between dies.

$(T_j - T_{\text{coolant}})$ for symmetric layouts, average errors are 3.7% and 4.7% for the decoupled model and the original coupled model, respectively, while for asymmetric layouts, they are 3.2% and 9.5%, respectively.

More importantly, as can be seen in Fig. 7, when using the original coupled model, the estimations of ΔT_j between dies are very inaccurate for asymmetric cases (D–F). Only in case A does the original coupled model show a slightly smaller error. This is because die 2 is located closer to die 1 instead of at the center of segment 2 in case A, which strengthens the coupling effect between the two segments. Overall, the decoupled model reduced the average error of ΔT_j estimation from 93.8% to 10.9% for asymmetric layouts. As expected, the proposed decoupled model exhibits significant benefits for IMS-type modules by considering the barrier effect between the substrate segments and the low thermal spreading at the resin layer. Therefore, it will guarantee accurate calculations during the design optimization.

III. STRAY INDUCTANCE MODEL

Stray inductance leads to overvoltage and contributes to the switching loss of power modules. Therefore, it needs to be minimized. Power modules have busbar-like internal conductors. Therefore, a method called the partial inductance model is adopted in this article, which was initially developed for estimating L_s of laminated busbars.

The total inductance of the power modules' main commutation loop (L_s) is of the greatest concern because it contributes to the drain–source overvoltage during switching. Therefore, minimizing L_s is desired when designing power modules. As

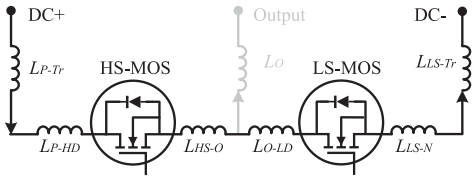


Fig. 8. Main commutation loop in a half-bridge module.

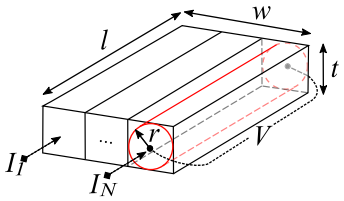


Fig. 9. Partial inductance scheme of a rectangular inductor.

highlighted in Fig. 8, L_s is a combination of several inductance segments. Since there is no overlap between these corresponding conductors, mutual inductance can be ignored. Therefore, the total L_s is the summation of self-inductances of all the conductor segments, as given in the following equation:

$$L_s = L_{P-Tr} + L_{P-HD} + L_{HS-O} + L_{O-LD} + L_{LS-N} + L_{N-Tr}. \tag{27}$$

A. Partial Inductance Model for Rectangular Conductors

The partial inductance model for rectangular conductors is introduced by Wada et al. [12]. In this theory, a wide conductor can be separated into N sets of thin conductors in parallel with a square cross section, as shown in Fig. 9. Furthermore, thin rectangular conductors can be simplified as circular wires whose radius (r) equals half of the thickness (t). The self-inductance of a single wire (L_w) is obtained in (28). The mutual inductance between the ith and jth wires (M_{w-ij}) is expressed in (29)

$$L_w = \frac{\mu_0\, l}{8\pi} + \frac{\mu_0}{2\pi}\left(l \ln \frac{\sqrt{r^2+l^2}+l}{r} - \sqrt{r^2+l^2} + r\right) \tag{28}$$

$$M_{w-ij} = \frac{\mu_0}{2\pi}\left(l \ln \frac{\sqrt{(d_{ij}+2r)^2+l^2}+l}{d_{ij}+2r} - \sqrt{(d_{ij}+2r)^2+l^2} + (d_{ij}+2r)\right) \tag{29}$$

where μ_0 (free space permeability) is $4\pi \times 10^{-7}$ H/m, l is the length of the wire, and d_{ij} is the center-to-center distance between the ith and jth wires.

L_s of the wide conductor can be obtained by the combination of the partial inductances of those paralleled wires. The voltage and current of those conductors are described in (30). The matrix is inversed in (31). The total current is the summation of all wires' current, as written in (32). Therefore, the total inductance

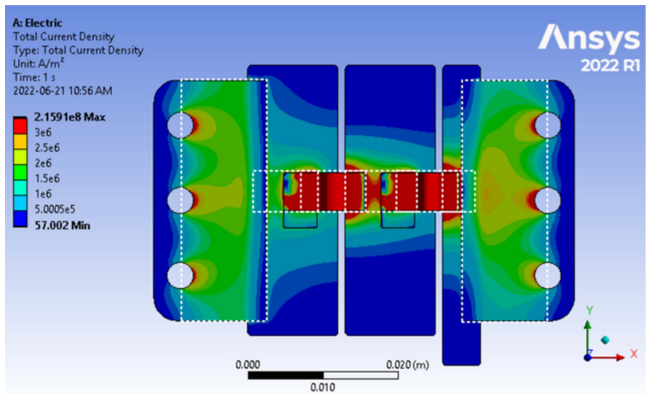


Fig. 10. Current density distribution for the L_s model.

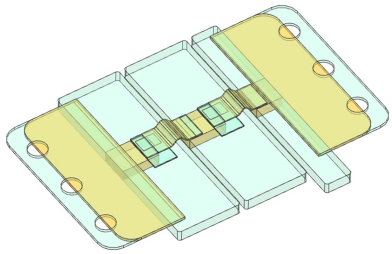


Fig. 11. Conductor layout for stray inductance calculation.

L_s is given in (33)

$$\begin{bmatrix} V \\ \dots \\ V \end{bmatrix} = jw \begin{bmatrix} L_w \dots M_{w-1n} \\ \dots \ \dots \ \dots \\ M_{w-n1} \ \dots L_w \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ \dots \\ I_n \end{bmatrix} \tag{30}$$

$$\begin{bmatrix} I_1 \\ \dots \\ I_n \end{bmatrix} = \frac{1}{jw} \begin{bmatrix} L_w \ \dots M_{w-1n} \\ \dots \ \dots \ \dots \\ M_{w-n1} \ \dots L_w \end{bmatrix}^T \cdot \begin{bmatrix} V \\ \dots \\ V \end{bmatrix} \tag{31}$$

$$I = I_1 + \cdots + I_n = \frac{1}{jw} \times \text{sum}\left(\begin{bmatrix} L_w \ \dots M_{w-1n} \\ \dots \ \dots \ \dots \\ M_{w-n1} \ \dots L_w \end{bmatrix}^T\right) \times V \tag{32}$$

$$L_s = \left(\text{sum}\left(\begin{bmatrix} L_w \ \dots M_{w-1n} \\ \dots \ \dots \ \dots \\ M_{w-n1} \ \dots L_w \end{bmatrix}^T\right)\right)^{-1}. \tag{33}$$

A half-bridge module consists of several conductor bodies, including terminals, substrates, and leads. A profile of the current density of an SSM module is shown in Fig. 10, which illustrates an uneven distribution. Therefore, only the main portions of conductors are considered in the calculation of L_s, which are the highlighted parts in Fig. 11.

B. Simulation Evaluation

Numerical simulations in ANSYS Q3D parasitic extractor are performed to evaluate the accuracy of the analytical model.

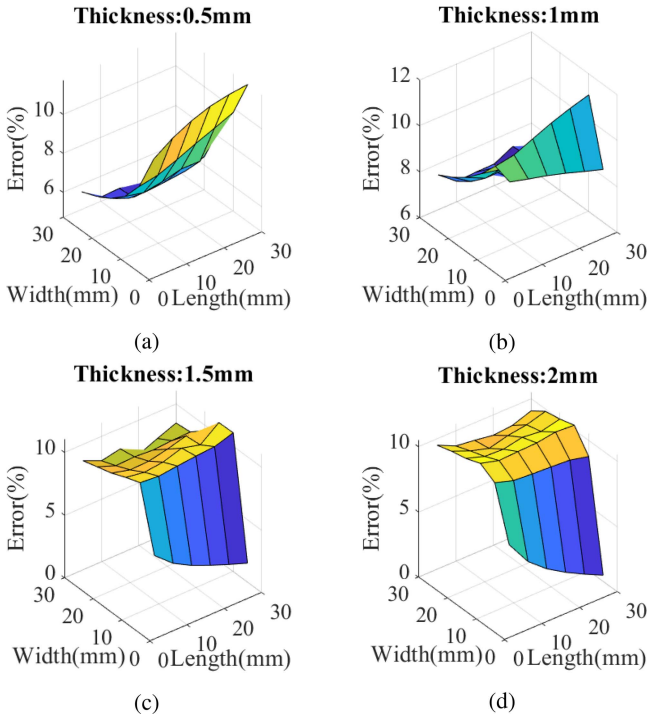


Fig. 12. (a)–(d) Parametric evaluation on error of the partial inductance model on rectangular conductors with various dimensions.

TABLE II
DIMENSION OF CASES FOR STRAY INDUCTANCE MODEL EVALUATION

Dimensions	Case A	Case B	Case C	Case D	Case E
$A1$ (mm)	10	15	15	20	20
$A2$ (mm)	10	15	15	20	20
$B1$ (mm)	10	10	10	10	10
$B2$ (mm)	10	10	5	10	5

Single rectangular conductors with various l, w, and t are simulated using both Q3D and the analytical model. The frequency is 60 MHz in all the simulations, which refers to the common switching speed of SiC MOSFETs. Results of the parametric comparisons are shown in Fig. 12, which shows that the maximum error of the partial inductance model is less than 11%.

In order to evaluate the accuracy of the model when applied in half-bridge SSM power modules, numerical simulations are again conducted on five example cases, as shown in Table II. Here, $d_{\text{substrate}}$ is 2 mm, d_{lead} is 0.1 mm, D is 5 mm, $C1$ equals $B1$, and $C2$ equals $B2$. These five cases cover half-bridge SSM modules with different footprints and conditions of symmetry. Results from the analytical model and numerical simulations are compared in Table III. It can be seen that the maximum error of simulated cases is 12.1%, which indicates that the proposed model has a good accuracy.

TABLE III
COMPARISON BETWEEN THE ANALYTICAL STRAY INDUCTANCE MODEL AND NUMERICAL SIMULATIONS

Results	Case A	Case B	Case C	Case D	Case E
L_s−FEA (nH)	28.3	25.2	18.8	23.2	17.2
L_s− Model (nH)	26.2	24.9	16.6	24.2	15.8
Error	7.4%	1.2%	12.1%	4.3%	8.1%

IV. OPTIMIZATION

A. Problem Statement

The target is to design a half-bridge module based on the SSM packaging scheme. Dimensional variables should be optimized to ensure that the module meets certain thermal and stray inductance expectations.

In this problem, there are two constraints to consider: 1) T_j of two dies should be lower than 200 °C, under 41-W power loss per die, 5000 W/m^2·°C convection cooling, and 105 °C coolant temperature; and 2) ΔT_j between two dies should be less than 5 °C under the same thermal boundary conditions.

The minimization targets include L_s and the volume (V_e) of the module. They are combined using artificially defined weight factors (po_1 and po_2) to simplify the problem into a single-objective problem. Furthermore, to scale those two criteria, reference values based on a survey of similar power modules are used. Specifically, $L_{s-\text{ref}}$ equals 10 nH, and $V_{e-\text{ref}}$ equals 1.9×10^{-5} m^3. Constraints and the cost function are shown in (34)–(36). In this problem, F is to be minimized. po_1 and po_2 are set to be 0.3 and 0.7, respectively

$$\text{Constraints-1} : \max(T_{j1}, T_{j2}) < 200^{\circ}\text{C} \tag{34}$$

$$\text{Constraints-2} : |T_{j1} - T_{j2}| < 5^{\circ}\text{C} \tag{35}$$

$$\text{Cost function} : F = po_1 \times \frac{V_e}{V_{e-\text{ref}}} + po_2 \times \frac{L_s}{L_{s-\text{ref}}}. \tag{36}$$

B. PSO Algorithm

The PSO algorithm is a well-known evolutionary algorithm. First introduced in 1995 by Kennedy and Eberhart [19], it has been applied in seeking the global optimal of multivariable problems, such as the thermal design of power electronics [15], [16]. The PSO algorithm is constructed by simulating social interaction. A swarm of particles is searching for the optimal position in the defined search space. The update of particle velocity considers the self-inertia of particle, the influence from the historical best position of the particle, and the influence from the current global best position, as shown in (37). $v_i(it)$ means the velocity of the ith particle at the itth iteration. $x_{i\text{best}}$ (it) is the historical best position of this particle. x_{global} (it) is the global best position. we is the inertia weight factor. c_1 is the self-learning factor. c_2 is the global-learning factor. The position update is obtained in (38)

$$v_i(it+1) = we \times v_i(it) + c_1 r_1 (x_{i\text{best}}(it) - x_i(it))$$

TABLE IV
PSO PARAMETERS

we	c_1	c_2	$v_{i-\max}$	N
0.7298	1.4962	1.4962	$0.02 \times (x_{\max} - x_{\min})$	30

TABLE V
SPECIFICATIONS OF CPM3-1200-0013A [22]

Parameter	Information
Semiconductor type	*N*-Channel Enhancement SiC MOSFET
Maximum V_{DS}	1200 V
Maximum I_{DS} at T_C=25°C	149 A
$R_{DS(on)}$ at T_j=175 °C	21 mΩ
Die dimensions (L × W)	4.36×7.26 mm
Die thickness	180 μm ($\pm$10%)

TABLE VI
OPTIMIZATION VARIABLES

Variables	$A1/A2$(mm)	$B1/C1$(mm)	$B2/C2$(mm)	$d_{\text{substrate}}$ (mm)
Upper Limit	20	10	10	2
Lower Limit	15	7	5	0.2
Optimized	18	7	5	2

$$+ c_2 r_2 (x_{g\text{best}}(it) - x_i(it)) \tag{37}$$

$$x_i(t+1) = x_i(t) + v_i(t+1). \tag{38}$$

The selection of the aforementioned parameters is critical for ensuring stabilized results and a proper convergence. Based on literature reviews [20], [21] and parametric studies, the selected parameters in this article are shown in Table IV. $v_{i-\max}$ is the maximum allowed velocity of particles, and $x_{\max}$ and $x_{\min}$ are the boundaries of the searching space. N is the swarm population.

C. Optimized Design

The analytical models are combined with the PSO algorithm to form a complete design methodology. A half-bridge module with the SSM packaging scheme is designed using this method. There are two SiC MOSFET dies in the module, forming the half-bridge circuit. The die is CPM3-1200-0013A from Wolfspeed [22], whose major parameters are listed in Table V.

The overall layout of the half-bridge module is shown in Fig. 2. In this optimization, the layout is symmetric for simplification, where $A1 = A2$, $B1 = C1$, and $B2 = C2$. In addition, several dimensions are fixed due to fabrication considerations. Specifically, $D = 5$ mm, $d_{\text{lead}} = 0.1$ mm, $d_{\text{resin}} = 0.2$ mm, and $d_{\text{heatsink}} = 2$ mm. The length of dc terminals is 15 mm. Their width equals the width of the contacted substrate with a margin of 2 mm from both the sides, which is $(A1 + A2 - 4)$ mm.

These variables are optimized using the PSO algorithm introduced above. The searching space and optimized results are summarized in Table VI. The analytical model outputs T_j of around 183 °C, for both the dies and L_s of 17.3 nH for the optimized design. It is worth noting that off-the-shelf devices could have a lower inductance due to die paralleling. However, the target of this study is mainly the validation of the proposed methodologies. Thus, die paralleling is avoided to simplify the fabrication process.

The half-bridge module with the optimized dimensional variables is shown in Fig. 13. Its thermal–electrical performances will be evaluated by numerical simulations.

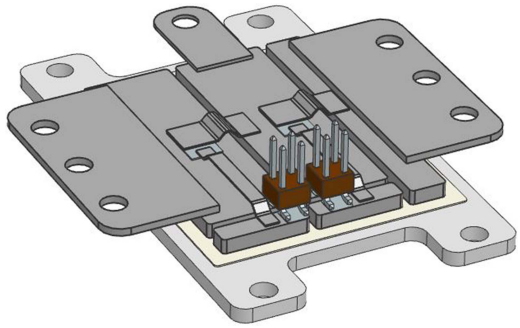


Fig. 13. CAD model of the optimized SSM half-bridge module.

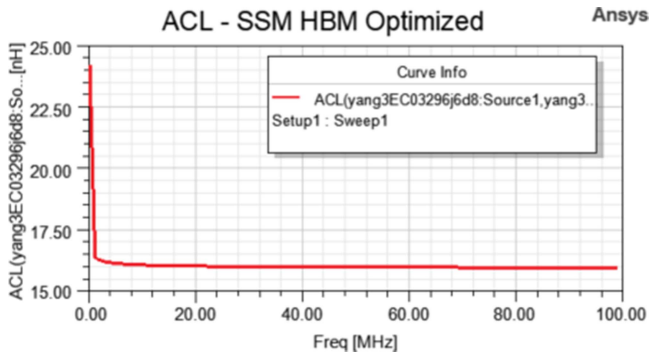


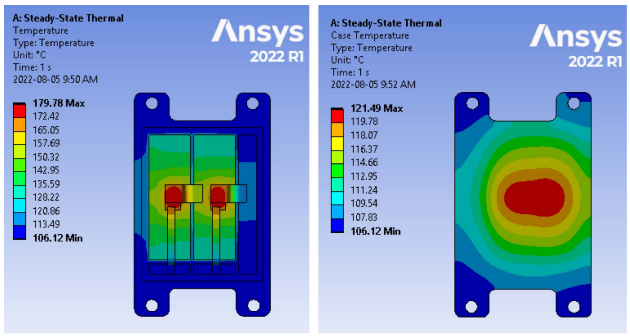
Fig. 14. Frequency sweep of L_s of the designed module.

D. Simulation Evaluation

Numerical simulations are conducted to evaluate the performances of the optimized module. In the stray inductance simulation using ANSYS Q3D, the designed module results in L_s of 16.0 nH at 60 MHz, as shown in Fig. 14. The inductance value decreases with the frequency due to the skin effect. However, it is stabilized after reaching the megahertz range.

The steady-state temperature profile obtained in ANSYS Mechanical is shown in Fig. 15. The influence of terminals and leads on heat transfer is considered negligible since they are not in the main heat transfer path. The definition of T_j remains the same in these simulations, which is the temperature at the center of dies' top surface.

The comparison between analytical estimations and numerical simulations is summarized in Table VII. The analytical models exhibit good accuracy with errors less than 4.6% and 8.3% for dT_j and L_s estimations, respectively.



(a) (b)

Fig. 15. Thermal profile of the optimized half-bridge module. (a) Top. (b) Bottom.

TABLE VII
COMPARISON BETWEEN THE ANALYTICAL MODEL AND THE NUMERICAL SIMULATIONS FOR THE OPTIMIZED MODULE ($dT_j = T_j - T_{\text{coolant}}$)

Results	dT_j (°C) of the left die	dT_j (°C) of the right die	L_s (nH) at 60 MHz
Analytical model	77.8	77.8	17.3
Numerical simulation	74.8	74.5	16.0
Error (%)	4.1	4.6	8.3

V. PROTOTYPING AND EXPERIMENT

A. Prototyping

The fabrication process of the optimized prototype module is illustrated in Fig. 16, where four main steps are introduced.

In step 1, SiC dies are remetalized to be compatible with double-side sintering. The original metallization of the gate and source pads on the top of the SiC die (CPM3-1200-0013 A) is aluminum (Al), which is designed for Al wire bonding. In the SSM packaging, top interconnections are Mo leads, which are sintered on dies. Thus, top pads need to be coated with metal layers suitable for nanosilver sintering, where Ni (0.05 μm)/Au (0.1 μm) are selected. Meanwhile, the insulation distance between the gate and source pads needs to be enlarged. First, a 0.25-μm SiO_2 layer is deposited uniformly on the top of the original dies by plasma-enhanced chemical vapor deposition to form a new insulation layer between gate and source. Then, small windows are opened on areas above the original gate and source pads by means of photolithography and chemical etching. Finally, new Ni/Au pads are metalized on these windows by ultrahigh vacuum (UHV) electron-beam evaporation, with larger areas and a wider gap distance between gate and source.

In step 2, substrate segments are bonded to the heatsink through vacuum curing of the BT resin layer. Alignment jigs are applied to ensure the accuracy of assembly. The curing profile is shown in Fig. 17, which is recommended by the supplier.

In step 3, SiC dies are bonded to the substrate by nanosilver sintering. The nanosilver paste is nanoTach-X from NBE [23]. The paste is applied by screen printing. The pressureless sintering process is shown in Fig. 18, which resulted in excellent sintering quality in our previous work [24]. A similar approach is implemented in step 4, where leads and terminals are assembled. It is worth noting that Mo parts were also coated with Ni (0.8 μm)/Au (0.1 μm).

TABLE VIII
COMPARISON OF DOUBLE-PULSE TEST/SIMULATION RESULTS

Results	f_o (MHz)	$L_{s-\text{loop}}$ (nH)
Experiment	55.1	21.8 (Calculated)
Simulation	54.8	21.9 (Q3D)
Error (%)	0.5	0.4

B. Double-Pulse Test

The double-pulse test characterizes the switching behavior of a device, which can reflect the loop parasitic parameters, including L_s. The schematic of the double-pulse test with the low-side MOSFET switching is shown in Fig. 19. In this circuit, the high-side MOSFET is kept OFF. When the low-side MOSFET switches OFF, I_2 decreases, and I_1 increases to maintain I_{Load}. Therefore, a commuting loop is formed. V_{DS-LS} will be measured. It is worth mentioning that the measured voltage includes the back electromotive force of the LS-L_s. The corresponding experimental setup is shown in Fig. 20.

In this article, an indirect validation method is applied to evaluate the accuracy of the proposed inductance model. The turn-OFF transient of MOSFETs can indicate the stray inductance of the switching loop. Therefore, turn-OFF waveforms are measured during the double-pulse test. The double-pulse test circuit is also simulated in the PSIM software. In these simulations, capacitor's equivalent series resistance (ESR) and equivalent series inductance are cited from its datasheet, which are 0.85 mΩ and 2.5 nH, respectively. The PCB-L_s is obtained in ANSYS Q3D simulations, which is 7.15 nH. HS-L_s and LS-L_s equal to half of the total L_s of the power modules, which are calculated using the proposed analytical model. Meanwhile, the mutual inductance (also obtained in Q3D) between conductors is also considered and subtracted from the self-inductance. Assume that inductance values obtained from Q3D simulations and the datasheet are trust worthy; then, the accuracy of the power module's inductance can be evaluated by comparing waveforms from both PSIM simulations and experiments, which could then prove the accuracy of the analytical inductance model proposed in this study.

The experiment and simulation are conducted at a dc voltage of 300 V and I_{Load} of 60 A. Waveforms of V_{DS-LS} during low-side turning-OFF are shown in Fig. 21. The oscillation frequency (f_o) is determined by the output capacitance of the low-side MOSFET (C_{oss}) and the total stray inductance of the commuting loop ($L_{s-\text{loop}}$), as explained in (39), which is commonly used to verify the estimation of $L_{s-\text{loop}}$. According to the datasheet, C_{oss} of the MOSFET is 383 pF at 300 V

$$f_o = \frac{1}{2 \times \pi \times \sqrt{C_{oss} \times L_{s-\text{loop}}}}. \tag{39}$$

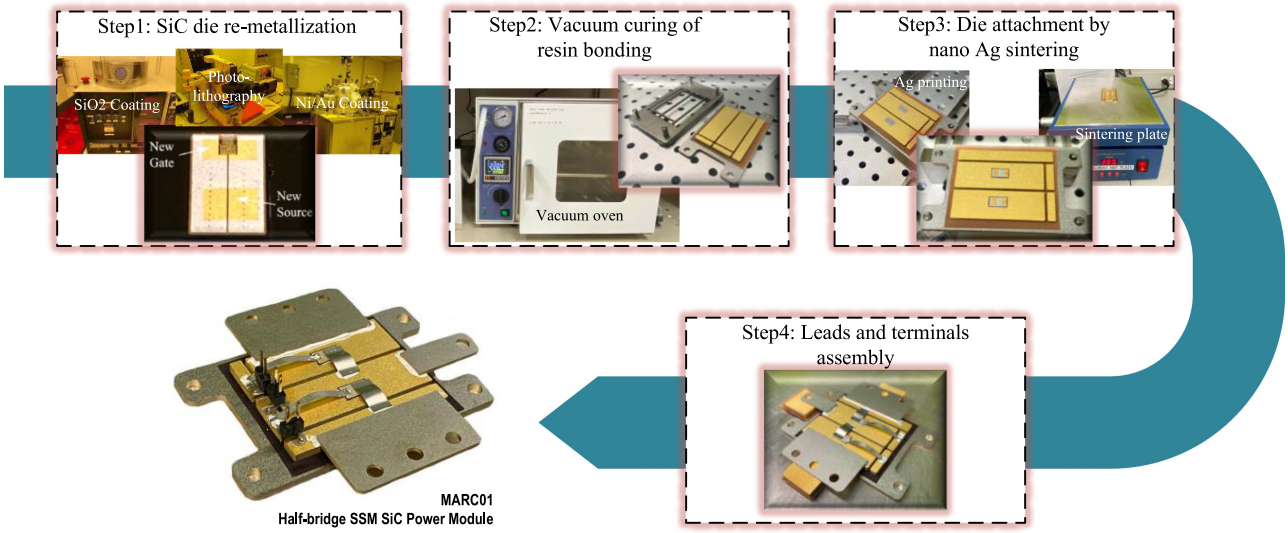


Fig. 16. Fabrication process of the prototype module.

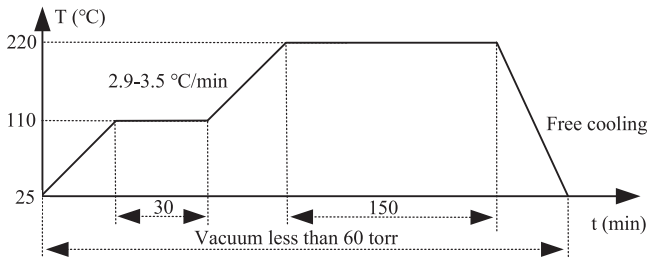


Fig. 17. Curing profile of BT resin.

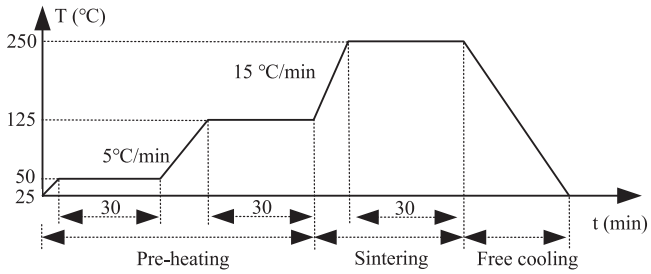


Fig. 18. Nanosilver sintering profile.

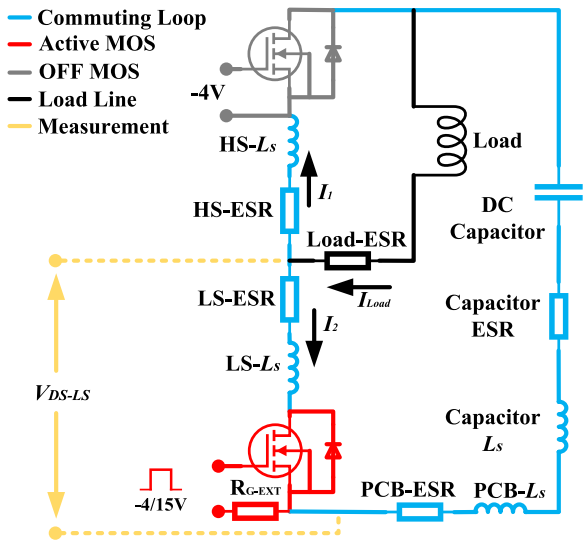


Fig. 19. Double-pulse test schematic of switching the low-side MOSFET.

It can be seen in Table VIII and Fig. 21 that the Q3D simulation matches with the experiment well. In previous sections, the analytical L_s model has been proven as accurate compared with the Q3D simulation. Thus, it is credible to conclude that the analytical L_s model is highly accurate.

C. Thermal Impedance Characterization

Junction-to-case thermal resistance ($R_{\text{th}(j-c)}$) is the most important parameter to evaluate the heat transfer performance of power modules, which is calculated using (40). In the SSM packaging, the case temperature (T_b) refers to the temperature at the point that is located directly below the center of the die at the bottom surface of the heatsink. The SIEMENS Power T3ster (PWT-1500A) is used to characterize the $R_{\text{th}(j-c)}$ of the prototype module, which can also validate the accuracy of the analytical thermal model. The characterization method is named structural function analysis, which has been introduced in several studies [25], [26]. Since directly measuring T_j is difficult and not accurate, the structural function analysis method uses thermal sensitive parameters (TSPs) to correlate the virtual T_j. In this study, the voltage drop across the body diode (V_D) during reverse conduction is selected as the TSP. Its relationship with T_j is obtained by thermal-static calibrations, as shown in (41)

$$R_{\text{th}(j-c)} = \frac{T_j - T_b}{P_{\text{die}}} \tag{40}$$

$$T_j = -348.2042 \times V_D + 974.1909. \tag{41}$$

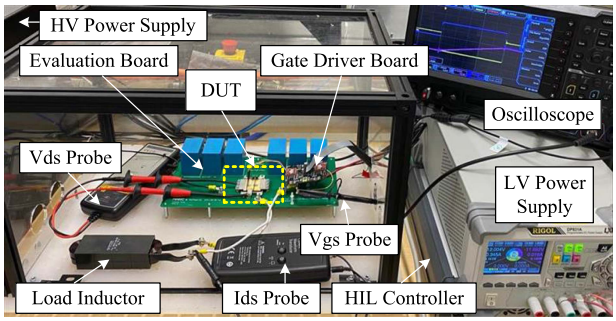


Fig. 20. Double-pulse test setup.

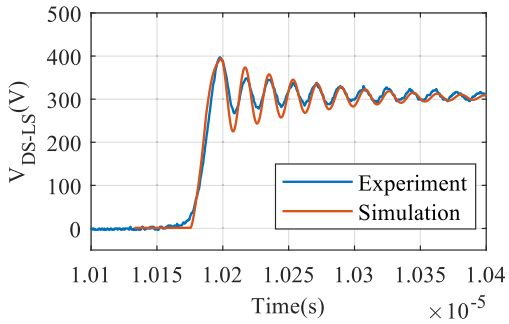


Fig. 21. Double-pulse test result: V_{DS-LS} during low-side turning-OFF at 300 V/60 A.

(a) (b)

Fig. 22. Thermal characterization setup. (a) Device under test. (b) SIEMENS Power T3ster.

The power module is characterized under two conditions: 1) the module is mounted on the cold plate without a thermal pad (TIM) and 2) the module is mounted on the cold plate with a thermal pad. Fig. 22(a) is the magnified view of the device under test, and Fig. 22(b) is the SIEMENS Power T3ster.

Two structural function curves are combined in Fig. 23, which describes the accumulation of thermal impedance from the die junction to the external environment. The intersection point refers to the impedance values between the junction to case, in which $R_{\text{th}(j-c)} = 1.46$ K/W. It can be seen in Table IX that both the analytical thermal model and the ANSYS simulation exhibit a very good accuracy. It is worth noting that off-the-shelf devices could have a lower $R_{\text{th}(j-c)}$ due to die paralleling. However, the target of this article is mainly validating the proposed methodologies.

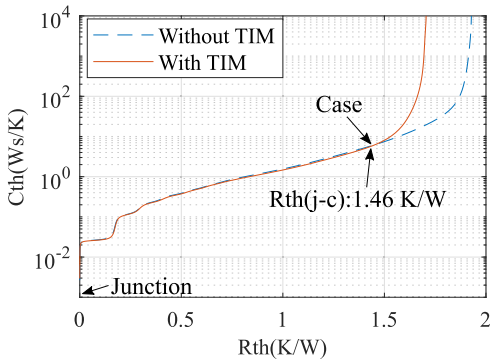


Fig. 23. $R_{\text{th}(j-c)}$ characterization by the structural function.

TABLE IX
COMPARISON OF $R_{\text{th}(j-c)}$

Results	Experiment	ANSYS simulation	Analytical thermal model
$R_{\text{th}(j-c)}$(K/W)	1.46	1.42	1.51
Error (%)	–	2.7	3.4

VI. CONCLUSION

This article presented a complete work of the modeling, optimization, manufacturing, and characterization of a half-bridge power module based on the SSM package. The main contributions of this study include the proposal and validation of analytical thermal and stray inductance models and the co-optimization method.

A decoupled Fourier-based thermal model was developed in Section II, which is suitable for IMS-type modules in particular. Compared with the original Fourier-based model, the proposed decoupled model reduced the average error of T_j estimation from 9.5% to 3.2% for asymmetric layouts. More importantly, it reduced the average error of ΔT_j by 82.9% for asymmetric layouts. In Section III, an analytical stray inductance model for half-bridge SSM modules was proposed based on the partial inductance modeling method and the actual current distribution. Simulations validated that the maximum error is 12.1% when estimating L_s of example half-bridge SSM modules. In Section IV, analytical models were combined with the PSO algorithm to form a design optimization method, with which a half-bridge power module was designed. The analytical estimations of T_j and L_s of the optimized module matched with the numerical simulations with errors less than 4.6% and 8.3%, respectively.

The process to prototype an SSM packaged power module was elaborated in Section V. Then, the prototype module was characterized experimentally. The V_{DS-LS} curve during the turning-OFF of the low-side MOSFET was obtained in the double-pulse test, which exhibited a good match with the corresponding simulation result. By comparing the voltage oscillation frequency, the accuracy of L_s estimation by the analytical model was validated. The thermal performance of the prototype module was characterized using structural function analysis methods.

The measured $R_{\text{th}(j-c)}$ was 1.46 K/W, while the estimated values by the analytical model and the numerical simulation were 1.51 and 1.42 K/W, respectively. Therefore, the accuracy of the analytical thermal model was also validated.

Overall, the accuracy of analytical models was verified. The prototyping process of the SSM packaged module was validated. In future work, the proposed methods can be applied in designing more complicated power modules. It is also meaningful to compare performances of different optimization algorithms. Meanwhile, definitions of the optimizations' searching space can be further studied. The outcome of this article provides a working methodology for power module designers and proves the feasibility of the SSM packaging.

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