Single-Phase Virtual-Ground Transformerless Buck–Boost Inverters

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***Abstract*—This article presents a new family of transformerless buck–boost voltage-source inverter topologies for photovoltaic systems. Due to variations in irradiance, temperature, and shading effects, the terminal voltages of photovoltaic panels can vary, making the use of buck–boost inverters crucial. The proposed topologies have a virtual-ground feature that effectively mitigates the common-mode voltage issue and results in low leakage current. The simple inductor-based proposed inverter can achieve a wide gain range. Also, other counterparts obtained from extending the underlying concept of the simple inductor-based proposed inverter, such as the switched inductor, three-winding coupled inductor, and series capacitor converters, are capable of achieving high boost voltage gain with lower duty ratios. Comprehensive circuit analyses are provided, along with simulation results, to confirm the operation of each proposed topology. Additionally, experiment findings for a 500-W prototype built on the simple inductor topology are presented to support the theoretical analysis and effectiveness of the proposed designs.**

***Index Terms*—Photovoltaic systems, power semiconductor devices, pulse width modulation, voltage source inverters.**

I. Introduction

PHOTOVOLTAIC (PV) panels have become increasingly popular as a source of clean energy. However, their terminal voltages are often variable, making it necessary to use isolated or nonisolated buck–boost inverters (BBIs) to connect them to the grid or load. Transformerless BBIs are more commonly used due to their low cost, high efficiency, and compact size. However, because transformerless inverters lack galvanic isolation, they must address the issue of ground leakage current, which is caused by parasitic capacitances ($C_{\rm pv1}$ and $C_{\rm pv2}$) of the PV panel due to the high-frequency (HF) common-mode voltage ($v_{\rm cm}$) fluctuations, as presented in Fig. 1. To avoid negative impacts from the leakage current, the leakage current should not exceed 300 mA [1].

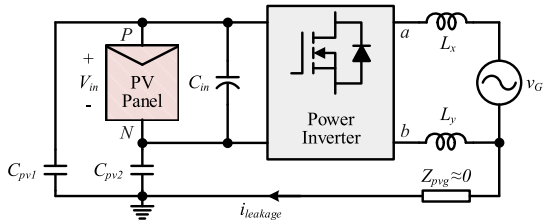

Fig. 1. Generic block diagram of a grid-tied inverter.

Well-known examples of transformerless topologies include full-bridge voltage-source inverters and current-source inverters. However, voltage-source inverters can only step down the input voltage, whereas current-source inverters can only step it up. A typical approach for achieving step up/down function is to cascade a conventional boost converter [2], [3] to a voltage-source inverter or a buck converter with a current source inverter. This two-stage inverter is effective but reduces overall efficiency due to the HF switching stages. Several single-stage inverters, such as impedance-source inverters, integrated inverters, and combined inverters, have been developed to reduce power processing stages. Impedance-source inverters [4] overcome the limitations of voltage-source inverters and current-source inverters, but the passive components decrease power density. Moreover, simultaneous switching and voltage spikes across all switches degrade system efficiency [5].

Another approach to realizing buck–boost dc–ac conversion is integrating different converters. In [6] and [7], a boost dc–dc converter, whereas in [8], a buck–boost dc–dc converter is integrated into a full-bridge voltage-source inverter. These inverters have a low switch count, but they have low dc-link voltage utilization and simultaneous HF operation of the switching devices. An active BBI (ABBI) can be obtained by integrating a full-bridge voltage-source inverter and an ac–ac boost structure [9]. ABBI requires only one inductor and eight active switches. However, it has high conduction losses and high leakage current. In contrast, two novel BBIs that use ac–ac buck–boost structures have been proposed in [10] and [11] using ac–ac buck–boost

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structures. These inverters can overcome the leakage current problem but require either two PV sources or two electrolytic dc-link capacitors. Additionally, they are susceptible to short-circuit and open-circuit problems due to the employment of ac switches. The inverters in [12], [13], [14], and [15] have small leakage currents and need one PV source, but they require many semiconductor devices.

Another promising category for dc–ac conversion is combined inverter topologies. Combined inverters are originated from the combination of different converters like a buck, boost, and buck–boost converters. In [16], a doubly grounded transformerless inverter is developed by combining buck and buck–boost converters. This inverter has no current shoot-through and leakage current problem, but it can perform only the step-down function. The inverter in [17] can perform the buck–boost function and is developed from the combination of two buck–boost converters. It clamps the common mode voltage, but its input current is pulsating and requires more passive components. Differential-boost inverter (DBI) consists of two bidirectional boost converters [18] and can perform the buck–boost function with low common-mode voltage, which is a vital property for PV applications. However, all the switching devices of DBI [18] work at high or medium frequency, and in consequence, the switching loss is high. Furthermore, the core and copper loss are increased because of the circulating current in the step-up inductors. Tang et al. [19] used a half-cycle modulation strategy to address these issues and proposed an improved DBI. This inverter can achieve high efficiency because only two switches operate simultaneously at a high frequency, and there is no circulating current through the inductors. Despite improvements, the combined inverters have a downside of employing several inductors. To decrease the size of magnetics, Manitoba BBI [20] and virtual-ground BBI [21] are recently proposed. Manitoba inverter needs only two inductors used for buck–boost operations and removing the HF component of the grid current. Moreover, it resolves the common-mode voltage problem by employing the active-virtual-ground (AVG) concept [22], [23], [24]. The typical configurations of inverters with AVG circuit are presented in Fig. 2. The two terminals of the AVG circuit are connected to the line and neutral of the grid, whereas the third terminal is connected to either the positive or negative terminal of the dc link as displayed in Fig. 2(a) and (b), respectively. The bidirectional switching devices (S^+ and S^-) in the AVG circuit operate alternatively at line frequency during the AVG capacitor C_{AVG} clamps the voltage between the grid and dc bus to mitigate the issue of the common-mode voltage. Moreover, the circuit is given the name AVG because of the impedance of voltage sources and the capacitor C_{AVG} are negligible at HF signals point of view, and the dc link always seems connecting to the network ground. The downside of Manitoba BBI is that it needs eight power switches. Both inductors still need to be designed with saturation current equal to the summation of input and output current. In contrast, virtual-ground BBI [21] has low common-mode voltage and needs two inductors in which one is dedicated for buck–boost operation while the other is dedicated for filtering the output grid current only. However, it is unidirectional

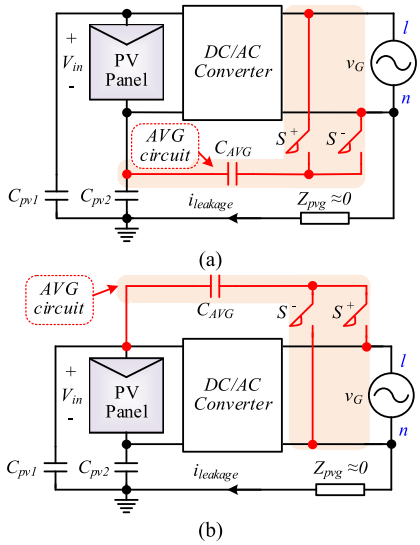

Fig. 2. Configurations of inverters with AVG circuit. (a) Type I. (b) Type II.

and requires seven semiconductor devices and two output filter capacitors.

It is noteworthy that all the above-mentioned BBIs [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21] have practically limited voltage step-up gain due to the parasitic resistances of the components at a high duty ratio. Various research efforts are therefore dedicated to developing power inverters with high voltage gain capabilities in [25], [26], [27]. However, these topologies suffer from the severe ground leakage current problem. Switched-capacitor inverters [28], [29] and differential Y-source inverters [30] have low ground leakage current with high voltage step-up capabilities. Still, many active and passive components are the downside of these topologies.

This article proposes new topologies of single-phase transformerless BBI for PV systems to overcome the aforementioned challenges. The general configuration of the proposed inverters consists of a boost cell, input capacitor C_{in}, output capacitor C_o, and four line-frequency (LF) switches S_a–S_d as presented in Fig. 3(a). Type I inverter, which is presented in Fig. 3(b), uses a simple inductor structure, whereas Types II, III, and IV inverters, as presented in Fig. 3(c) and (d), use switched-inductor [31], three-winding coupled inductor [30], and series-capacitor high conversion ratio [32] structures in place of boost cell, respectively. The working principle of all the proposed inverters is similar; that is, the step-up cell is responsible for generating a rectified sinusoidal voltage with dc offset equivalent to the input voltage across the capacitor C_o, which is later on removed with the help of line frequency switches to obtain pure sinusoidal voltage. Type I inverter needs one inductor only to provide a wide range of buck–boost operation, whereas the other three types can achieve high boost gain at small duty ratios. The proposed inverters also have low common-mode voltage and leakage current due to virtual-ground characteristics and can achieve high power conversion efficiency because there are only two HF switches in Type I, II, and III inverters while four HF switches in Type IV

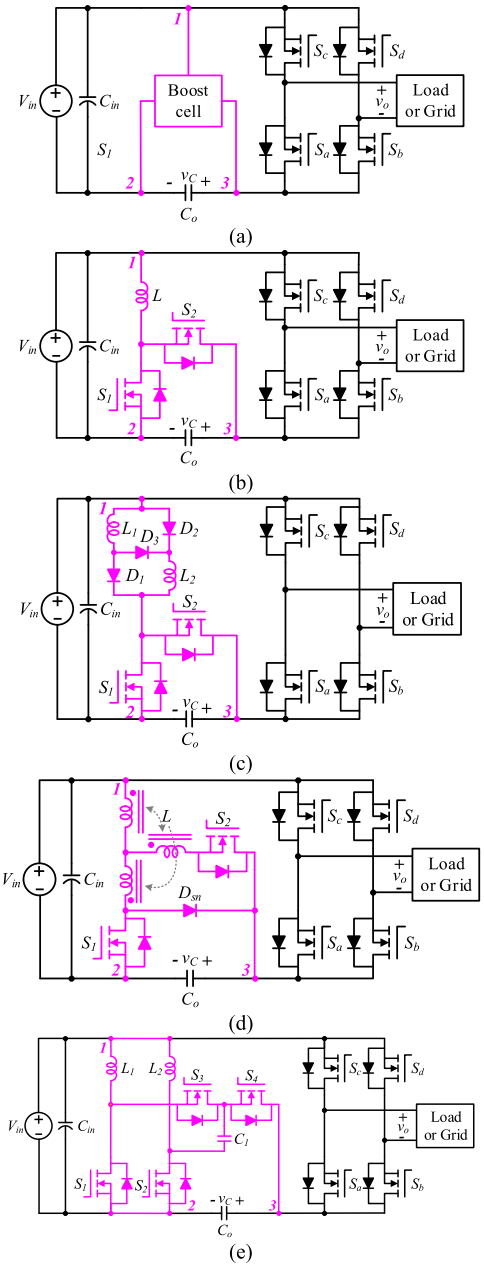

Fig. 3. Proposed virtual-ground BBI. (a) General configuration. (b) Type I. (c) Type II. (d) Type III. (e) Type IV.

Inverter. The LF switches have low voltage and current stresses which further allow selecting MOSFETs with low drain–source ON resistances irrespective of taking into consideration their switching losses. The HF switches in this article refer to the switching devices that operate at the switching frequency which is 50 kHz, whereas the LF switches are the switching devices that operate at 50 Hz.

The rest of this article is organized as follows. Section II describes the modulation strategy and operating modes of the proposed Type I inverter, followed by its leakage current consideration and design guidelines in Section III, and its experiment verification in Section IV. The switching strategies, design guidelines, and simulation results of the proposed extended

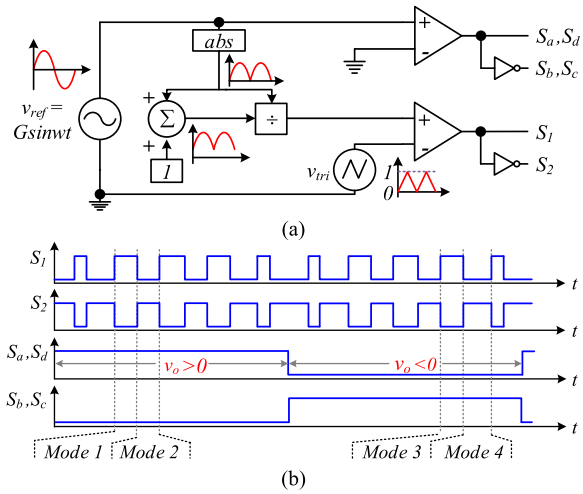

Fig. 4. (a) Block diagram for gate signals generation of the proposed Type I inverter. (b) Gate signals and operational modes.

high-gain topologies (Types II, III, and IV) are included in Section V. Finally, Section VI concludes this article.

II. Modulation Strategy and Circuit Operation of the Proposed Type I Inverter

In proposed inverters (Type I to Type IV), the switching devices S_a and S_d are ON for only the positive half of the output voltage, whereas the switching devices S_b and S_c are ON for only the negative half of the output voltage. The output voltage v_o can thus be represented by the following equation:

$$v_o = V_o \sin wt = \begin{cases} v_C - V_{\text{in}}, & \text{for } v_o > 0 \\ V_{\text{in}} - v_C, & \text{for } v_o < 0 \end{cases} \tag{1}$$

where V_o is the peak value of output voltage, v_C is the voltage of capacitor C_o, and V_{in} is the input voltage. From (1), the voltage on capacitor v_C can be written as

$$v_C = V_{\text{in}} + |v_o| = V_{\text{in}} + |V_o \sin wt| . \tag{2}$$

To generate $v_C = V_{\text{in}} + |V_o \sin wt|$ from the proposed Type I inverter, the complementary switches S_1 and S_2 are operated at HF through a proper modulation scheme such that

$$v_c = V_{\text{in}} + |V_o \sin \omega t| = \frac{V_{\text{in}}}{1 - d_1} \tag{3}$$

where d_1 is the duty ratio of the switching device S_1. Rearranging (3), d_1 is calculated as follows:

$$d_1 = \frac{|V_o \sin \omega t|}{V_{\text{in}} + |V_o \sin \omega t|} . \tag{4}$$

The duty ratio d_1 can be written in respect of the voltage gain $G = \frac{V_o}{V_{\text{in}}}$ as

$$d_1 = \frac{|G \sin \omega t|}{1 + |G \sin \omega t|} . \tag{5}$$

Fig. 4(a) depicts the block diagram for generating the proposed Type I inverter's gate signals. It can be observed that the gate signals for the switching device S_1 is acquired from (5), which indicates that the reference $v_{\text{ref}} = G \sin \omega t$ is

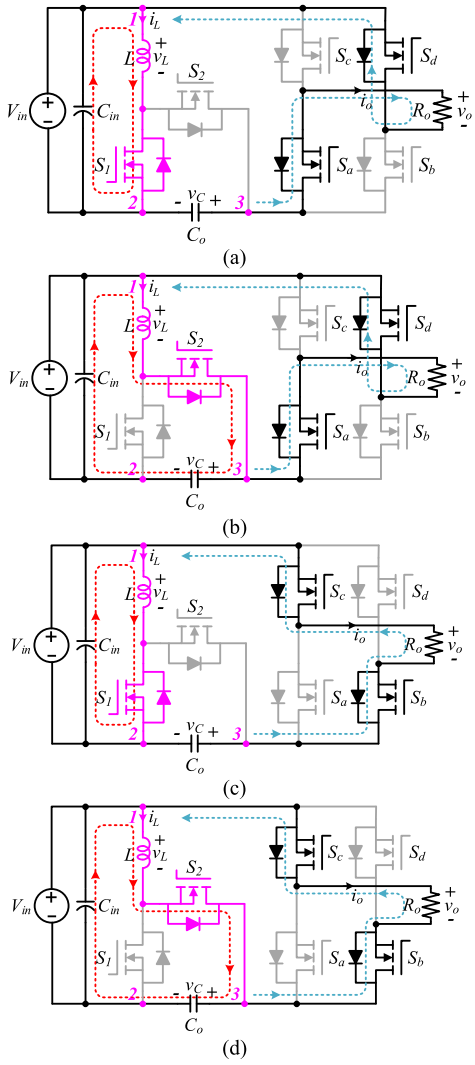

Fig. 5. Modes of operation. (a) Mode-1. (b) Mode-2. (c) Mode-3. (d) Mode 4.

created. Then, its absolute value ($|G \sin \omega t|$) is divided by ($1 + |G \sin \omega t|$). The quotient is then compared with the triangular carrier v_{tri} to obtain gate signals for S_1. The complementary signals of S_1 are then applied to S_2. The gate signals and operational modes of the proposed Type I inverter in the complete line cycle of the output voltage are presented in Fig. 4(b). Modes 1 and 2 appear for $v_o > 0$, whereas modes 3 and 4 occur for $v_o < 0$. The current paths during each mode of operation are presented in Fig. 5.

1) *Mode 1:* In this mode, the switching devices S_1, S_a, and S_d are ON. The inductor L stores energy, whereas the capacitor C_o supplies energy to the load. The current paths are presented in Fig. 5(a) and the inductor current ripple Δi_L is given by

$$\Delta i_L = \frac{V_{\text{in}} d_1 T_s}{L} \tag{6}$$

where T_s is the switching time period.

2) *Mode 2:* In this mode, the switching devices S_2, S_a, and S_d are ON. The inductor L provides energy to both capacitor C_o and the load. The current directions are presented in Fig. 5(b), whereas Δi_L is given by

$$\Delta i_L = -\frac{v_o (1 - d_1) T_s}{L}. \tag{7}$$

3) *Mode 3:* In this mode, the switching devices S_1, S_b, and S_c are ON. The inductor L stores energy, and the output capacitor C_o delivers energy to the load. The current directions are presented in Fig. 5(c) and Δi_L is similar to that in mode 1.

4) *Mode 4:* In this mode, the switching devices S_2, S_b, and S_c are ON. The inductor L provides energy to both the output capacitor C_o and the load. The current directions are presented in Fig. 5(d), whereas Δi_L is given by

$$\Delta i_L = \frac{v_o (1 - d_1) T_s}{L}. \tag{8}$$

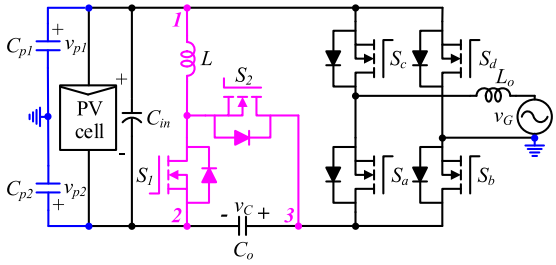

Fig. 6. Grid-tied mode of the proposed Type I inverter.

III. Leakage Current and Design Guidelines of the Proposed Inverter (Type I)

This section explains the performance of the proposed inverter (Type I) in terms of leakage current and also provides guidelines for the components selection.

A. Leakage Current Consideration

PV installations are mostly grid-tied, so leakage current is an important design parameter. In a grid-tied transformerless PV system, leakage current can flow through the parasitic capacitances of PV panels. Large leakage currents are produced by substantial HF voltage variations within the parasitic capacitances, whereas LF variations produce small leakage currents. On the other hand, the leakage current becomes zero if there are no variations across the parasitic capacitances' voltages.

The typical grid-connected configuration of the proposed Type I inverter is presented in Fig. 6. The parasitic capacitances of PV panel are denoted by C_{p1} and C_{p2}, whereas their voltages are represented by v_{p1} and v_{p2}. The inductor L_o filters the HF harmonics and is also required for conventional grid-tied inverters. Voltages across the parasitic capacitances in positive and negative half-cycles of the output voltage can be obtained from the simplified circuits presented in Fig. 7(a) and (b). The simplified circuits are obtained by replacing always ON and OFF switches with short-circuit and open-circuit, respectively. Voltages appearing across the parasitic capacitances are included in Table I. Throughout the output voltage's positive half-cycle, the leakage current is zero because the ac ground is directly connected to the dc bus and the parasitic capacitance's voltages

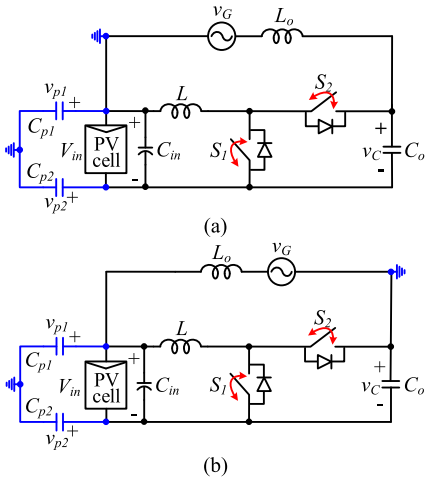

Fig. 7. Simplified circuits of grid-tied Type I inverter. (a) $v_o > 0$. (b) $v_o < 0$.

TABLE I
VOLTAGES FOR THE PARASITIC CAPACITANCES

Parasitic capacitance voltage	Output voltage +ve half-cycle	Output voltage -ve half-cycle
v_{p1}	0	$V_{in} - v_C$
v_{p2}	$-V_{in}$	$-v_C$

$(v_{p1},\ v_{p2})$ are constant. On the other hand, v_{p1} and v_{p2} change according to both capacitor voltage v_c and input voltage in the negative half-cycle. Input voltage is constant and according to (3), and v_c varies sinusoidally with line frequency. This implies that there are no substantial HF variations across the parasitic capacitances and the leakage current will be low. From the standpoint of HF signals, the capacitor C_o offers a low-impedance route that virtually links the ground of the grid to the common terminal of the PV panel making the virtual grounded circuit.

B. Voltage Gain

The maximum duty ratio $D_{1\_\max}$ of switch S_1 can be obtained from (4) and is given by

$$D_{1\_\max} = \frac{V_o}{V_{in} + V_o}. \tag{9}$$

Using (9), the voltage gain G can be expressed in terms of $D_{1\_\max}$ as follows:

$$G = \frac{V_o}{V_{in}} = \frac{D_{1\_\max}}{1 - D_{1\_\max}}. \tag{10}$$

The graph of G versus $D_{1\_\max}$ is presented in Fig. 8. The proposed Type I inverter will perform the buck function if $D_{1\_\max} < 0.5$ and boost function if $D_{1\_\max} > 0.5$.

C. Switch Selection

The voltage and current ratings are used to choose the switching devices. The maximum drain-to-source voltages appearing across the proposed Type I inverter's switches are given by

$$V_{ds-1} = V_{ds-2} = V_{in} + V_o \tag{11}$$

$$V_{ds-a} = V_{ds-b} = V_{ds-c} = V_{ds-d} = V_o \tag{12}$$

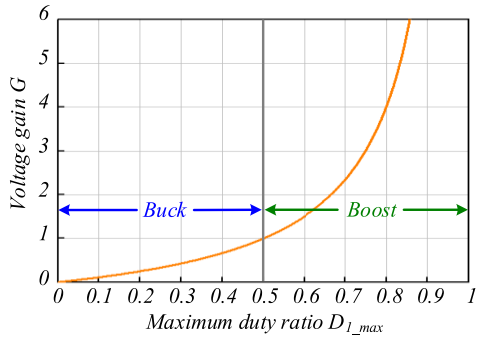

Fig. 8. Graph of voltage gain and the maximum duty ratio of Type I inverter.

where (V_{ds-1}, V_{ds-2}) and $(V_{ds-a} - V_{ds-d})$ represent the maximum drain-to-source voltages of the switching devices (S_1, S_2) and $(S_a - S_d)$, respectively. The voltage stresses of the switching devices can be normalized to the peak output voltage V_o and represented in terms of voltage gain G as follows:

$$\frac{V_{ds-1}}{V_o} = \frac{V_{ds-2}}{V_o} = \frac{1+G}{G} \tag{13}$$

$$\frac{V_{ds-a}}{V_o} = \frac{V_{ds-b}}{V_o} = \frac{V_{ds-c}}{V_o} = \frac{V_{ds-d}}{V_o} = 1. \tag{14}$$

Similarly, the maximum current and rms current flowing through the switching devices are normalized to the output current's maximum value I_o and are calculated as follows:

$$\frac{I_{S1rms}}{I_o} = \sqrt{\frac{1}{\pi}\int_0^{\pi} \left[G\sin^3\omega t\,(1 + G\sin\omega t)\right] d\,(\omega t)} \tag{15}$$

$$\frac{I_{S2rms}}{I_o} = \sqrt{\frac{1}{\pi}\int_0^{\pi} \left[\sin^2\omega t\,(1 + G\sin\omega t)\right] d\,(\omega t)} \tag{16}$$

$$\frac{I_{Sarms}}{I_o}, \frac{I_{Sbrms}}{I_o}, \frac{I_{Scrms}}{I_o}, \frac{I_{Sdrms}}{I_o} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} \sin^2\omega t d\,(\omega t)} \tag{17}$$

$$\frac{I_{S1}}{I_o} = \frac{I_{S2}}{I_o} = 1 + G \tag{18}$$

$$\frac{I_{Sa}}{I_o} = \frac{I_{Sb}}{I_o} = \frac{I_{Sc}}{I_o} = \frac{I_{Sd}}{I_o} = 1 \tag{19}$$

where (I_{S1rms}, I_{S2rms}) and $(I_{Sarms} - I_{Sdrms})$ represent the rms current and (I_{S1}, I_{S2}) and $(I_{Sa} - I_{Sd})$ represent the maximum current flowing through the switching devices (S_1, S_2) and $(S_a - S_d)$, respectively.

The graphs of normalized voltage stresses, rms current, and current stresses of the switching devices are presented in Fig. 9. It can be observed that the voltage stresses of the switching devices S_1 and S_2 decrease, whereas the current stresses increase with the voltage gain G. This implies that the voltage ratings of these switches should be selected based on the minimum required

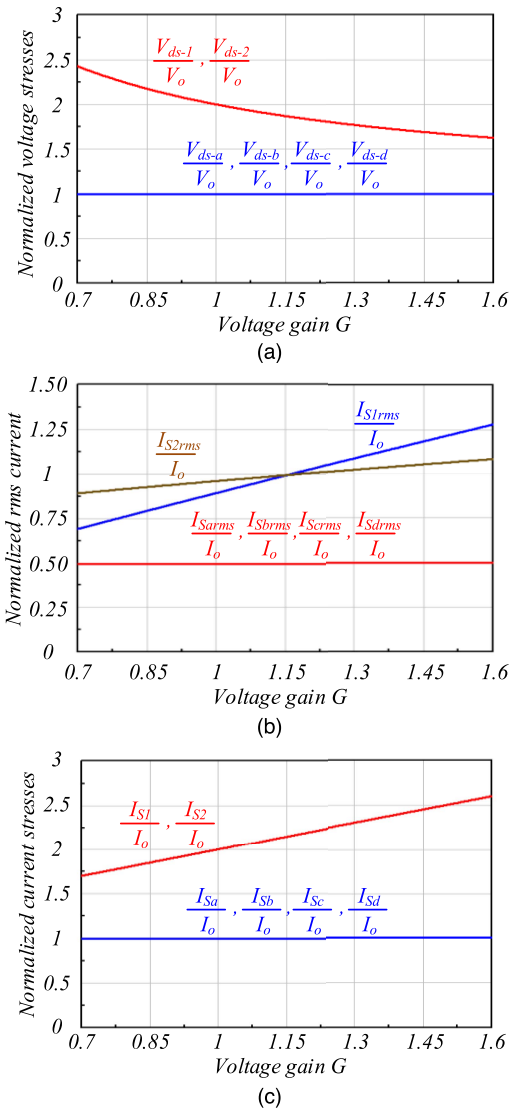

Fig. 9. (a) Normalized voltage stresses with respect to voltage gain. (b) Normalized rms current with respect to voltage gain. (c) Normalized current stresses with respect to voltage gain.

value of G, whereas the current ratings should be selected based on the maximum value of G.

D. Input Capacitor Selection

Similar to conventional inverters, the proposed Type I inverter also requires an input capacitor for power decoupling. The value of the input capacitor can be calculated as follows:

$$C_{\text{in}} = \frac{P_{\text{in}}}{2\pi f_o V_{\text{in}} \Delta V_{\text{in}}} \tag{20}$$

where P_{in} is the input power, f_o is the output or grid frequency, and ΔV_{in} is the allowable input voltage ripple. A common approach is to select ΔV_{in} equal to $(5-10)\%$ of V_{in}.

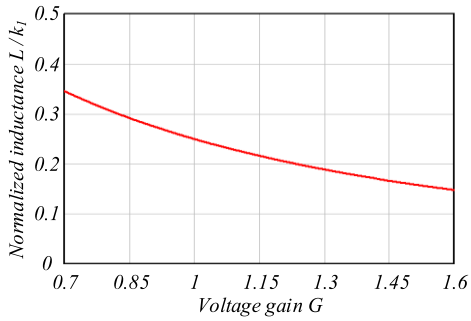

Fig. 10. Normalized inductance versus voltage gain.

E. Inductor Design

The maximum inductor current ripple $\Delta i_{L\max}$ calculated from (6), (9), and (10) is given by

$$\Delta\, i_{L\max} = \frac{V_{\text{in}} T_s G}{L\,(1+G)} \tag{21}$$

where $\Delta i_{L\max} = yI_L$, $y = 10\%$ to 50%, and the maximum inductor current $I_L = (1+G)I_o$. Putting these values in (21), the formula for inductance L is calculated as follows:

$$L = \frac{V_{\text{in}} T_s G}{y(1+G)^2 I_o} = \frac{V_o T_s}{y(1+G)^2 I_o}. \tag{22}$$

Replacing $V_o T_s / yI_o$ in (22) by constant k_1, the normalized inductance L/k_1 is plotted in Fig. 10. The graph implies that the value of inductance L should be chosen at the minimum voltage gain G because the inductance is maximum at this point.

F. Filter Capacitor Selection

The function of the filter capacitor C_o is to limit the output voltage ripple and the leakage current. The general formula for calculating the value of the filter capacitor is given by

$$C_o = \frac{i_c \Delta t}{\Delta v} \tag{23}$$

where i_c is the current flowing through the capacitor during Δt, and Δv is the voltage ripple of the output or capacitor voltage. $\Delta v = zV_o$ and z is typically selected in the range of 5% to 10%. As explained in mode analysis, the output current i_o flows through the capacitor C_o for duty ratio d_1. This implies that the required value of capacitance can be calculated from (23) using the maximum duty ratio and is given by

$$C_o \geq \frac{I_o D_{1\_\max} T_s}{zV_o} = \frac{I_o G T_s}{zV_o\,(1+G)}. \tag{24}$$

Replacing $I_o T_s / zV_o$ in (24) by constant k_2, the normalized capacitance C_o/k_2 is drawn in Fig. 11. The diagram implies that the value of the capacitance C_o should be selected at maximum voltage gain because the required capacitance increases with the voltage gain G. The increase in capacitance is actually due to an increase in the voltage ripple as well as the increase in the voltage gain.

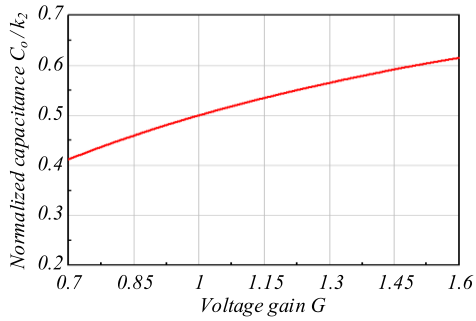

Fig. 11. Normalized capacitance versus voltage gain.

TABLE II
ELECTRICAL SPECIFICATIONS

Output power	500 W
Input voltage V_{in}	100 − 200 V_{dc}
Output voltage	155 V_{peak}
Switching frequency	50 kHz
Switches (S_1, S_2)	UF3C065040K3S
Switches (S_3, S_4, S_5, S_6)	IRF250P224
Inductor L	500 μH
Capacitor C	6.8 μF
Parasitic capacitances C_{p1}, C_{p2}	50 nF

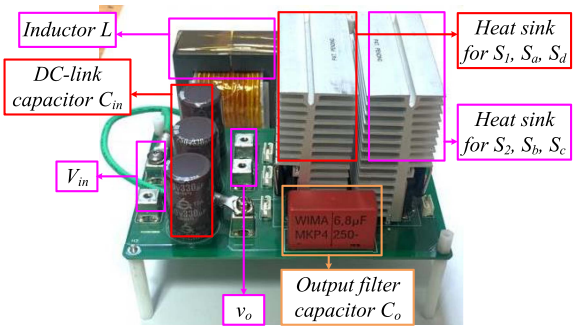

Fig. 12. Prototype photograph of the proposed Type I inverter.

IV. EXPERIMENT RESULTS

To verify the performance of the proposed Type I inverter, experiments are conducted in both the step-down and the step-up modes of operation. The electrical specifications for the experiment setup are included in Table II and the hardware prototype picture is shown in Fig. 12. Figs. 13–15 show the waveforms in the step-up mode with a 100 V input voltage. Gate signals for the switching devices $(S_1,\ S_2)$ and $(S_a - S_d)$ are presented in Fig. 13(a), whereas the input voltage V_{in}, output voltage v_o, output current i_o, and inductor current i_L are presented in Fig. 13(b). The voltage across the capacitor v_C and drain–source voltages of HF switches v_{ds-1}, v_{ds-2} are presented in Fig. 14(a). The drain–source voltages of LF switches $v_{ds-a} - v_{ds-d}$ are presented in Fig. 14(b). Waveforms of voltages across the parasitic capacitances and the corresponding leakage currents are presented in Fig. 15.

Similarly, Figs. 16 and 17 display the experiment results in the step-down mode with an input voltage of 200 V. Input voltage, output voltage, output current, and inductor current are presented in Fig. 16(a), whereas the voltage across the capacitor v_C and

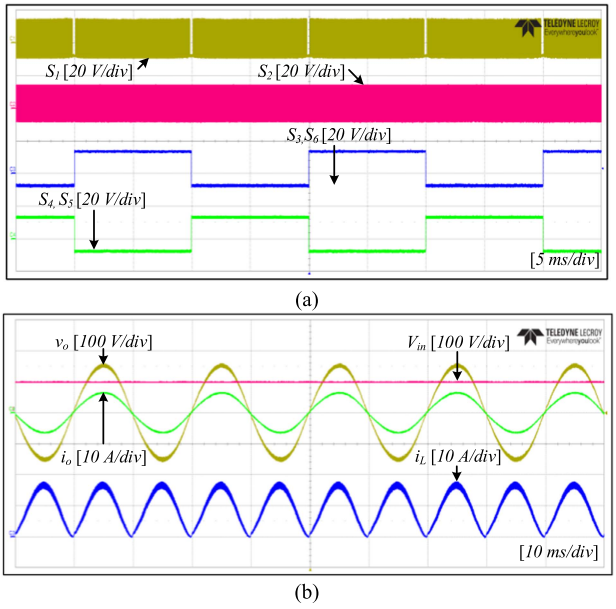

Fig. 13. Experiment waveforms in the step-up mode. (a) Gate signals. (b) Input voltage V_{in}, output voltage v_o, output current i_o, and inductor current i_L.

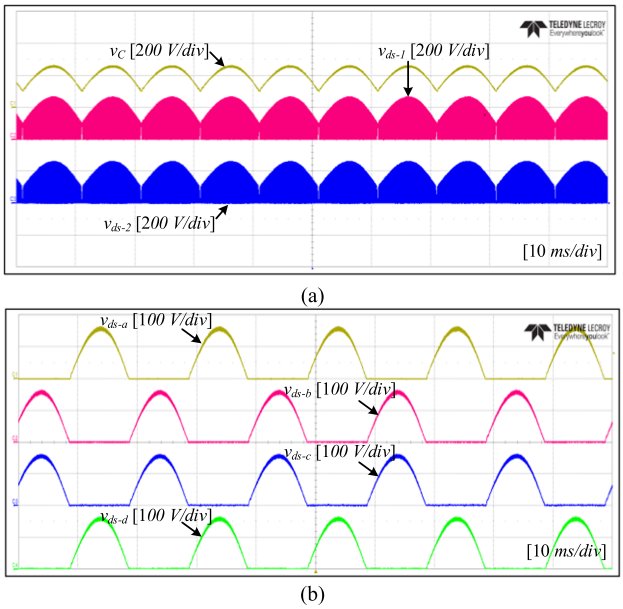

Fig. 14. Experiment waveforms in the step-up mode. (a) Voltage across the filter capacitor v_C and drain–source voltages of switches S_1 and S_2. (b) Drain–source voltages of switches S_a, S_b, S_c, and S_d.

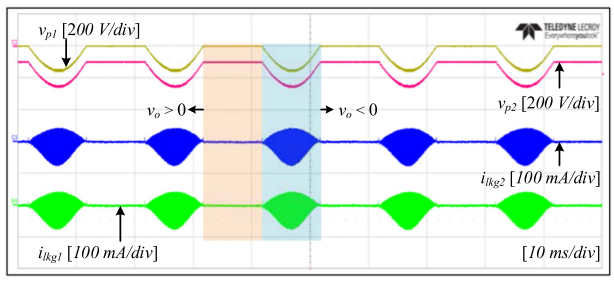

Fig. 15. Voltages across the parasitic capacitances v_{p1} and v_{p2} and their leakage currents i_{lkg1} and i_{lkg2} in the step-up mode.

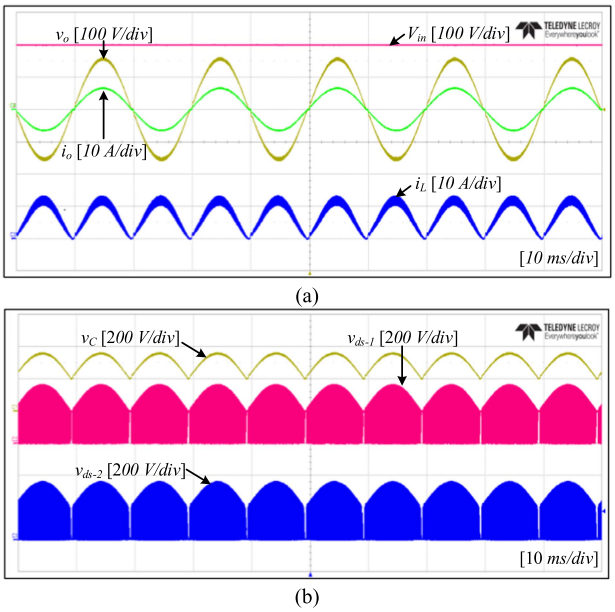

Fig. 16. Experiment waveforms in the step-down mode. (a) V_{in}, v_o, i_L, and i_o. (b) Voltage v_C and drain–source voltages of switches S_1 and S_2.

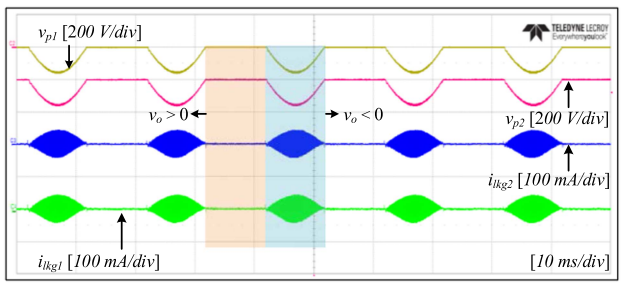

Fig. 17. Voltages across the parasitic capacitances v_{p1} and v_{p2} and their leakage currents i_{lkg1} and i_{lkg2} in the step-down mode.

drain–source voltages of HF switches are presented in Fig. 16(b). The drain–source voltages of LF switches are similar to those of the step-up mode; thus, they are not presented again. Voltages across the parasitic capacitances and the leakage currents are presented in Fig. 17.

The experiment results confirm that only HF switches S_1 and S_2 have voltage stresses equal to $V_{\text{in}} + V_o$. The voltage stresses of LF switches are low and equal to the peak output voltage V_o. Similarly, it can be observed that voltages across the parasitic capacitances are similar, as listed in Table I. During $v_o > 0$, the leakage currents are almost zero because both v_{p1} and v_{p2} are clamped to dc values. On the other hand, during $v_o < 0$, v_{p1} and v_{p2} vary with line frequency, and their HF ripples are significantly attenuated by the filter capacitor C_o. Therefore, small leakage currents exist during the negative portion of output voltage, but they are well below the industrial standards of 300 mA. The maximum leakage currents measured during the step-up and the step-down modes are about 75 mA and 45 mA, respectively.

The efficiency and total harmonic distortions (THD) of the output voltage are measured at 500 W for various input voltages, and the results are plotted in Fig. 18(a). The measured THD is

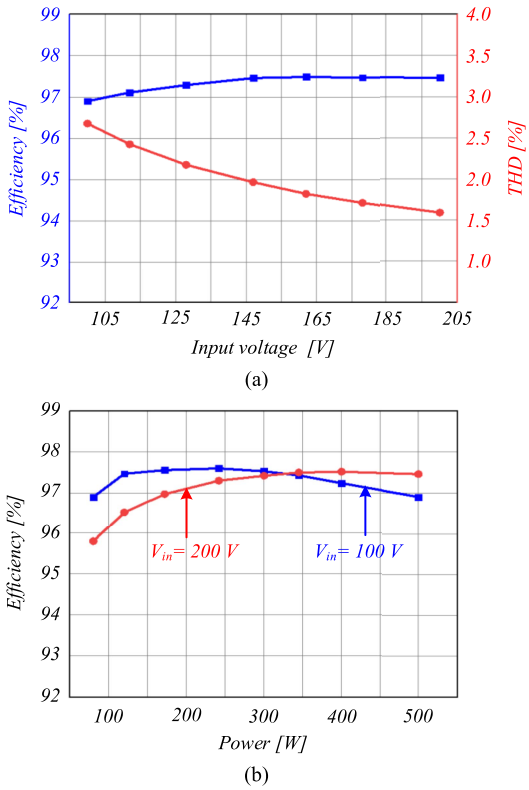

Fig. 18. (a) Efficiency and THD versus input voltage. (b) Efficiency versus power at different input voltages.

much below the IEEE-519 limits throughout the voltage range, and a peak efficiency of 97.5% is achieved at $V_{\text{in}} = 160$ V. Similarly, efficiency is measured under different output power with constant output voltage and changing the load resistor. The graph of efficiency versus output power for two different input voltages is plotted in Fig. 18(b). While keeping output voltage constant, switching losses are more dominant than conduction losses at low power. However, the conduction losses increase with increasing power and eventually become dominant. Due to this reason, as presented in Fig. 18(b), the efficiency in the step-up mode is higher than the step-down mode in the low-power region. However, the efficiency in the step-down mode becomes better than the step-up mode in the high-power region.

Finally, a detailed comparison of the proposed inverter with the well-known conventional buck–boost inveters, which are good in terms of leakage current, are included in Table III. It can be observed that apart from the proposed and virtual-ground BBI [21], all the other inverters require two inductors for the buck–boost function with the same peak current ratings. However, the inverter in [21] still needs two filter capacitors and hence it can be concluded that the proposed inverter has the fewest number of passive components (inductors and capacitors), which makes it good in terms of power density. The proposed inverter has six semiconductor devices and only DBI [18] is good in terms of semiconductor count. However, all of the switches in [18] operate at HF and has high voltage and current stresses. In the proposed inverter, only two switches with the same voltage and current stresses like in [18] operate at HF. The other four switches

TABLE III
COMPARISON OF THE PROPOSED TYPE I AND CONVENTIONAL BUCK–BOOST INVERTERS

Topology	H6 buck-boost inverter [15]	Buck boost inverter [17]	Differential boost inverter [18]	Improved differential boost inverter [19]	Manitoba inverter [20]	Virtual ground buck boost inverter [21]	Proposed type I inverter
Voltage gain (G)	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{1-D}$
Switches	6 ($S_1 - S_6$)	4 ($S_1 - S_4$)	4 ($S_1 - S_4$)	6 ($S_1 - S_6$)	8 ($S_1 - S_8$)	5 ($S_1 - S_5$)	6 ($S_1, S_2, S_a, S_b, S_c, S_d$)
Diodes	2 (D_1, D_2)	2 (D_1, D_2)	0	0	0	2 (D_1, D_2)	0
Voltage stresses of switches ($V_{ds\_(n)}$)* and diodes ($V_{D\_(n)}$)*	$V_{ds\_(1,3,5,6)} = \frac{V_o(1+G)}{G}$ $V_{ds\_(2,4)} = \frac{V_o}{G}$	$V_{ds\_(1,2)} = V_{D\_(1,2)} = \frac{V_o(1+G)}{G}$ $V_{ds\_(3,4)} = \frac{V_o}{G}$	$V_{ds\_(1-4)} = \frac{V_o(1+G)}{G}$	$V_{ds\_(1-4)} = \frac{V_o(1+G)}{G}$ $V_{ds\_(5,6)} = V_o$	$V_{ds\_(1-4)} = \frac{V_o(1+G)}{G}$ $V_{ds\_(5-8)} = V_o$	$V_{ds\_(1-3)} = \frac{V_o(1+G)}{G}$ $V_{ds\_(4,5)} = V_o$	$V_{ds\_(1,2)} = \frac{V_o(1+G)}{G}$ $V_{ds\_(a-d)} = V_o$
Current stresses of switches ($I_{S\_(n)}$)* and diodes ($I_{D\_(n)}$)*	$I_{S\_(1-6)} = I_o(1+G)$ $I_{D\_(1,2)} = I_o(1+G)$	$I_{S\_(1,2)} = I_{D\_(1,2)} = I_o(1+G)$ $I_{S\_(3,4)} = I_oG$	$I_{S\_(1-4)} = I_o(1+G)$	$I_{S\_(1-4)} = I_o(1+G)$ $I_{S\_(5,6)} = I_o$	$I_{S\_(1-4)} = I_o(1+G)$ $I_{S\_(5-8)} = I_oG$	$I_{S\_(1-3)} = I_{D\_(1,2)} = I_o(1+G)$ $I_{S\_(4,5)} = I_o$	$I_{S\_(1,2)} = I_o(1+G)$ $I_{S\_(a-d)} = I_o$
Line-frequency switches	4	2	0	0	4	4	4
High-frequency switches/diodes	2	2	4	2	1	2	2
Inductors	2	2	2	2	2	1	1
Inductors peak current	L_o: I_o L_1: $I_o(1+G)$	$I_o(1+G)$	$I_o(1+G)$	$I_o(1+G)$	$I_o(1+G)$	$I_o(1+G)$	$I_o(1+G)$
Input DC capacitors	1	1	1	1	1	1	1
Filter capacitors	2	1	2	2	1	2	1
Leakage current	small	small	small	small	small	small	small
Peak reported efficiency (%)	96.8 at 800 W and 40 kHz	87 at 300 W and 10 kHz	86.3 at 300 W and 20 kHz	92.6 at 300 W and 20 kHz	93.7 at 800 W 95.7 at 160 W	97 at 500 W and 50 kHz	97.5 at 500 W and 50 kHz

(*) 'n' in the subscript represent the switch/diode numbers.

in the proposed inverter operate at LF and have low voltage and current stresses. The lesser number of passive components and HF switches make the proposed inverter quite good in terms of efficiency as well which is evident from Table III.

V. MODULATION SCHEMES, DESIGN GUIDELINES, AND SIMULATION RESULTS OF THE PROPOSED INVERTERS (TYPES II–IV)

The proposed inverters (Types II–IV) have high voltage gain capabilities and can generate a high output voltage at small values of duty ratios. As mentioned earlier, the working principle of all the proposed inverters is similar; that is, the step-up cell is responsible for generating a full-wave rectified sinusoidal voltage with a dc offset equal to the input voltage across the output capacitor C_o. Furthermore, the switching devices S_a and S_d are ON for only the positive half of the output voltage, whereas the switching devices S_b and S_c are ON for only the negative half of the output voltage in all the proposed inverters. The output voltage v_o and the voltage v_C of capacitor C_o are represented by the equations presented in (1) and (2), respectively. To generate $v_C = V_{\text{in}} + |V_o \sin wt|$, the switching devices of the step-up cell of the proposed inverters (Types II–IV) are operated at HF through proper modulation schemes as follows.

A. Operation of the Step-Up Cell of Type II Inverter

The operating modes of Type II inverter are similar to those of Type I inverter, which are presented in Fig. 4(b). In modes 1 and 3, the switching device S_1 is ON, and the inductors L_1 and L_2 store energy from the input source V_{in} through the diodes D_1 and D_2, respectively, as presented in Fig. 19(a). In modes 2 and 4, the switching device S_1 is OFF and the inductors L_1 and L_2 appear in series and charge the output capacitor C_o by D_3 as demonstrated in Fig. 19(b). By applying the volt–second balance condition on inductors L_1 and L_2, the voltage on the capacitor C_o can be derived, which is given by

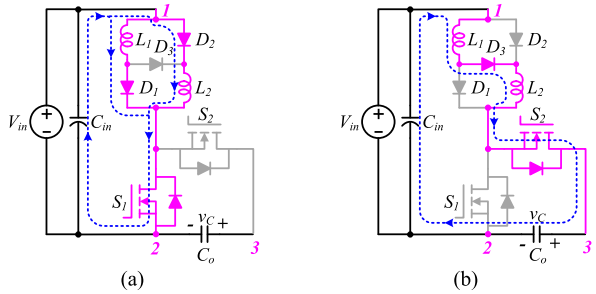

Fig. 19. Operation modes for the step-up cell of inverter Type II. (a) Modes 1 and 3. (b) Modes 2 and 4.

$$v_c = V_{\text{in}} + V_o\ |\sin \omega t| = \frac{V_{\text{in}}\,(1+d_1)}{1-d_1} \tag{25}$$

where d_1 is the duty ratio of the switching device S_1. Rearranging (25), d_1 can be written in terms of voltage gain $G = \frac{V_o}{V_{\text{in}}}$, and is given by

$$d_1 = \frac{G\,|(\sin \omega t))|}{2 + G\,|(\sin \omega t)|}\,. \tag{26}$$

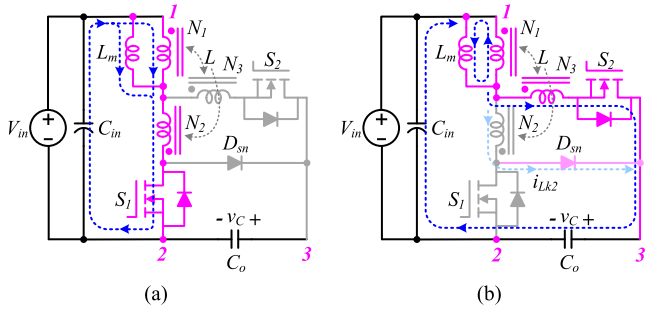

Fig. 20. Operation of the step-up cell of Type III inverter. (a) Modes 1 and 3. (b) Modes 2 and 4.

The maximum duty ratio D_{1_max} of switch S_1 can be obtained from (26) and is given by

$$D_{1\_max} = \frac{G}{2+G}. \tag{27}$$

Using (27), the voltage gain G can be expressed in terms of D_{1_max} as

$$G = \frac{V_o}{V_{in}} = \frac{2D_{1\_max}}{1-D_{1\_max}}. \tag{28}$$

B. Operation of the Step-Up Cell of Type III Inverter

The operating modes of Type III inverter are also similar to those of Type I inverter, which are presented in Fig. 4(b). In modes 1 and 3, the switching device S_1 is ON and the magnetizing inductor L_m is charged by the voltage contributed by the input source V_{in} and winding N_2 as presented in Fig. 20(a). In modes 2 and 4, the switching device S_1 is OFF and the switching device S_2 is ON. The windings N_1 and N_3 in series charge the capacitor C_o and the magnetizing inductor L_m is discharged through the winding N_1 directly and winding N_3 indirectly through coupling as presented in Fig. 20(b). It should be noted here that the lossless diode D_{sn} performs voltage clamping when the switching device S_1 is turned OFF by providing a path for the current of leakage inductance L_{lkg2} of winding N_2 to freewheel to the capacitor C_o. On the other hand, if both HF complementary switches S_1 and S_2 are OFF during the small dead-time interval, the current of leakage inductances L_{lkg1} and L_{lkg3} of windings N_1 and N_3 can flow through the body diode of S_2 to energize the capacitor C_o and do not require extra diodes or snubbers for voltage clamping. By applying voltage–second balance condition on magnetizing inductor L_m, the voltage on the capacitor C_o can be derived, which is given by

$$v_c = V_{in} + V_o\,|\sin\omega t| = \frac{V_{in}\left[1+\left(\frac{N_2+N_3}{N_1-N_2}\right)d_1\right]}{1-d_1} \tag{29}$$

where d_1 is the duty ratio of the switching device S_1. Rearranging (29), d_1 can be written in terms of voltage gain $G = \frac{V_o}{V_{in}}$, and is given by

$$d_1 = \frac{G\,|(\sin\omega t))|}{\left(\frac{N_1+N_3}{N_1-N_2}\right)+G\,|(\sin\omega t)|}. \tag{30}$$

The maximum duty ratio D_{1_max} of switch S_1 can be obtained from (30) and is given by

$$D_{1\_max} = \frac{G}{\left(\frac{N_1+N_3}{N_1-N_2}\right)+G}. \tag{31}$$

Using (31), the voltage gain G can be expressed in terms of D_{1_max} as

$$G = \frac{V_o}{V_{in}} = \frac{D_{1\_max}\left(\frac{N_1+N_3}{N_1-N_2}\right)}{1-D_{1\_max}}. \tag{32}$$

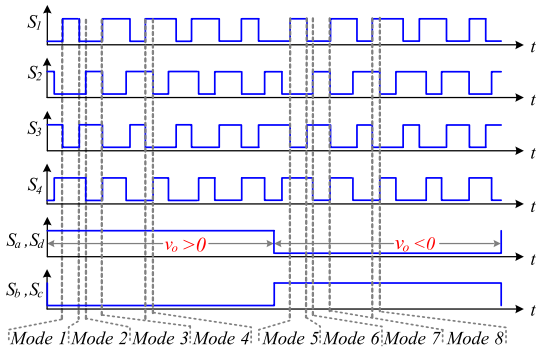

Fig. 21. Gate signals and operating modes of Type IV inverter.

C. Operation of the Step-Up Cell of Type IV Inverter

The gate signals and modes of operation of Type IV inverter are presented in Fig. 21. The switching devices S_1 and S_2 are operated at the same duty ratios; however, their gate signals are interleaved, which means a phase shift of 180^o is included in their carrier signals. The gate signals of the switching device S_3 is complementary to switch S_1, whereas the gate signals of the switching device S_4 is complementary to switch S_2. Modes $1-4$ appear in the positive half of the output voltage, whereas modes $5-8$ appear in the negative half of the output voltage. The operation of LF switches (S_a-S_d) are exactly similar to that of inverter Type I, whereas HF switches (S_1-S_4) of the step-up cell are operated through a proper modulation scheme to obtain $v_C = V_{in} + |V_o \sin wt|$.

In modes 1 and 5, the switching devices S_1 and S_4 are ON, whereas the switching devices S_2 and S_3 are OFF. The inductor L_1 stores energy from the input source V_{in}, whereas the inductor L_2 and capacitor C_1 supply energy to the output capacitor C_o as presented in Fig. 22(a). In modes 2 and 6, the switching devices S_3 and S_4 are ON, whereas the switching devices S_1 and S_2 are OFF. Both inductors $(L_1,\ L_2)$ and capacitor C_1 supply energy to the output capacitor C_o as presented in Fig. 22(b). In modes 3 and 7, the switching devices S_2 and S_3 are ON, whereas the switching devices S_1 and S_4 are OFF. The inductor L_2 stores energy from the input source V_{in}, whereas the capacitor C_1 is charged by the current flowing through the inductor L_1 as

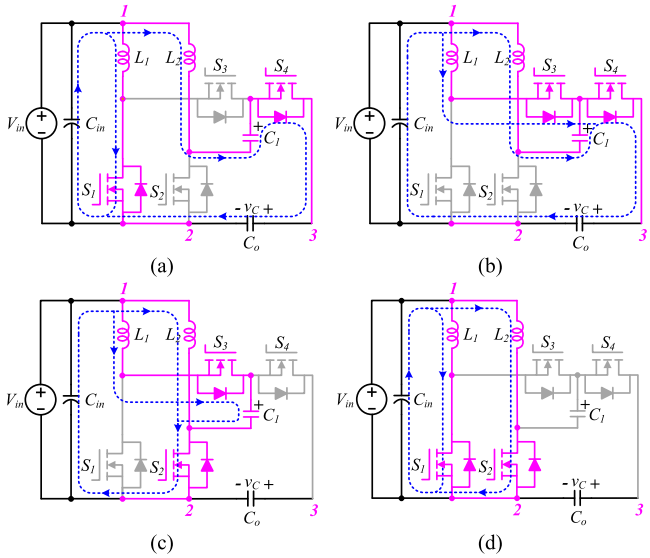

Fig. 22. Operation of the step-up cell of Type IV inverter. (a) Modes 1 and 5. (b) Modes 2 and 6. (c) Modes 3 and 7. (d) Modes 4 and 8.

presented in Fig. 22(c). The switching devices S_1 and S_2 are ON in modes 4 and 8, whereas the switching devices S_3 and S_4 are OFF. Both inductors L_1 and L_2 are charged by the input source V_{in}, whereas the capacitor C_1 is neither charged nor discharged, as presented in Fig. 22(d). It should be noted here that modes 4 and 8 appear only if the duty ratios of switches S_1 and S_2 are greater than 0.5. Similarly, modes 2 and 6 appear only if the duty ratios of switches S_1 and S_2 are smaller than 0.5. By applying voltage–second balance condition on inductors L_1 and L_2, the voltage on capacitor C_o can be derived as

$$v_c = V_{\text{in}} + V_o\ |\sin\omega t| = \begin{cases} \frac{V_{\text{in}}}{(1-d_1)^2} & \text{if } d_1 < 0.5 \\ \frac{2V_{\text{in}}}{1-d_1} & \text{if } d_1 \geq 0.5 \end{cases} \tag{33}$$

where d_1 is the duty ratio of the switching device S_1 and is equal to the duty-ratio d_2 of switch S_2 as explained earlier. Rearranging (33), d_1 can be expressed in terms of voltage gain

$$d_1 = \begin{cases} \frac{\sqrt{1+G|\sin\omega t|}-1}{\sqrt{1+G|\sin\omega t|}} & \text{if } d_1 < 0.5 \\ \frac{G|\sin\omega t|-1}{1+G|\sin\omega t|} & \text{if } d_1 \geq 0.5 \end{cases}. \tag{34}$$

The maximum duty ratio $D_{1\_\max}$ of switch S_1 can be obtained from (34) and is given by

$$D_{1\_\max} = \begin{cases} \frac{\sqrt{1+G}-1}{\sqrt{1+G}} & \text{if } D_{1\_\max} < 0.5 \\ \frac{G-1}{1+G} & \text{if } D_{1\_\max} \geq 0.5 \end{cases}. \tag{35}$$

Using (35), the voltage gain G can be expressed in terms of $D_{1\_\max}$ as

$$G = \frac{V_o}{V_{\text{in}}} = \begin{cases} \frac{D_{1\_\max}(2-D_{1\_\max})}{D_{1\_\max}^2-2D_{1\_\max}+1} & \text{if } D_{1\_\max} < 0.5 \\ \frac{1+D_{1\_\max}}{1-D_{1\_\max}} & \text{if } D_{1\_\max} \geq 0.5 \end{cases}. \tag{36}$$

D. Components Design Guidelines

The selection of input capacitor C_{in} and output capacitor C_o of the inverters (Type II–IV) are similar to that of Type I inverter and are represented by (20) and (24), respectively. The normalized maximum drain–source voltages and the normalized peak current flowing through the LF switches $(S_a - S_d)$ are also similar to Type I inverter and are given by (14) and (19), respectively. The normalized values for voltage stresses for Type II inverter's HF diodes and switches are presented as follows:

$$\begin{cases} \frac{V_{ds-1}}{V_o} = \frac{V_{ds-2}}{V_o} = \frac{1+G}{G} \\ \frac{V_{D1}}{V_o} = \frac{V_{D2}}{V_o} = \frac{1}{2} \\ \frac{V_{D3}}{V_o} = \frac{1}{G} \end{cases} \text{Type II} \tag{37}$$

where V_{ds-1} and V_{ds-2} represent the voltage stresses of the switching devices S_1 and S_2, whereas V_{D1}, V_{D2}, and V_{D3} represent the voltage stresses of the diodes D_1, D_2, and D_3.

Similarly, the maximum current flowing through the diodes and switches of Type II inverter are normalized to the peak output current I_o and are calculated as follows:

$$\begin{cases} \frac{I_{D1}}{I_o} = \frac{I_{D2}}{I_o} = \frac{I_{D3}}{I_o} = \frac{I_{S2}}{I_o} = \frac{2+G}{2} \\ \frac{I_{S1}}{I_o} = 2+G \end{cases} \text{Type II} \tag{38}$$

where I_{D1}, I_{D2}, I_{D3}, I_{S1}, and I_{S2} represent the maximum current flowing through the diodes D_1, D_2, D_3, and switches S_1 and S_2, respectively.

The current handling requirements $(I_{L1},\ I_{L2})$ of inductors L_1 and L_2 are given by

$$I_{L1} = I_{L2} = I_o\left(\frac{2+G}{2}\right) \quad \text{Type II.} \tag{39}$$

The maximum inductor current ripple $\Delta i_{L1\max}$ and $\Delta i_{L2\max}$ for Type II Inverter are given by

$$\Delta i_{L1\max} = \frac{V_{\text{in}} T_s G}{L_1\,(2+G)} \text{ and } \Delta i_{L2\max} = \frac{V_{\text{in}} T_s G}{L_2\,(2+G)} \quad \text{Type II} \tag{40}$$

where $\Delta\, i_{L1\max} = \Delta\, i_{L2\max} = y\, I_{L1} = y I_{L2}$, and $y = 10\%$ to 50%. Putting these values and (39) in (40), the formula for inductances L_1 and L_2 can be calculated as follows:

$$L_1 = L_2 = \frac{2V_{\text{in}} T_s G}{y(2+G)^2 I_o} = \frac{2V_o T_s}{y I_o (2+G)^2} \quad \text{Type II.} \tag{41}$$

The normalized voltage and current stresses of HF switches and diodes of Type III and IV inverters can be derived similarly and are as follows.

$$\begin{cases} \frac{V_{ds-1}}{V_o} = \frac{V_{Dsn}}{V_o} = \frac{1+G}{G} \\ \frac{V_{ds-2}}{V_o} = \left(1 + \frac{(N_1+N_3)}{G(N_1-N_2)}\right) \end{cases} \text{Type III} \tag{42}$$

$$\begin{cases} \frac{I_{S1}}{I_o} = \frac{I_{Dsn}}{I_o} = \frac{(N_1+N_3)}{(N_1-N_2)} + G \\ \frac{I_{S2}}{I_o} = 1 + \frac{G(N_1-N_2)}{(N_1+N_3)} \end{cases} \text{Type III} \tag{43}$$

$$\begin{cases} \frac{V_{ds-1}}{V_o} = \begin{cases} \frac{1+G}{G} & \text{if } G < 3 \\ \max\left(\frac{4}{G},\ \frac{1+G}{2G}\right) & \text{if } G \geq 3 \end{cases} \\ \frac{V_{ds-2}}{V_o} = \frac{V_{ds-4}}{V_o} = \begin{cases} \frac{\sqrt{1+G}}{G} & \text{if } G < 3 \\ \frac{1+G}{2G} & \text{if } G \geq 3 \end{cases} \\ \frac{V_{ds-3}}{V_o} = \frac{1+G}{G} \end{cases} \text{Type IV} \tag{44}$$

TABLE IV
COMPARISON OF THE PROPOSED TOPOLOGIES

Proposed inverter	Voltage gain	S(1)	D(2)	L(3)	C(4)	Voltage stresses of switches & diodes	Current stresses of switches & diodes	Inductor current	Inductance
Type I	$G=\frac{D_{1\_max}}{1-D_{1\_max}}$	6	0	1	2	$\frac{V_{ds-1}}{V_o},\frac{V_{ds-2}}{V_o}=\frac{1+G}{G}$	$\frac{I_{S1}}{I_o},\frac{I_{S2}}{I_o}=1+G$	$I_L=(1+G)I_o$	$L=\frac{V_oT_s}{y(1+G)^2I_o}$
Type II	$G=\frac{2D_{1\_max}}{1-D_{1\_max}}$	6	3	2	2	$\frac{V_{ds-1}}{V_o},\frac{V_{ds-2}}{V_o}=\frac{1+G}{G}$; $\frac{V_{D1}}{V_o},\frac{V_{D2}}{V_o}=\frac{1}{2}$; $\frac{V_{D3}}{V_o}=\frac{1}{G}$	$\frac{I_{D1}}{I_o},\frac{I_{D2}}{I_o},\frac{I_{D3}}{I_o},\frac{I_{S2}}{I_o}=\frac{2+G}{2}$; $\frac{I_{S1}}{I_o}=2+G$	$I_{L1},I_{L2}=I_o\left(\frac{2+G}{2}\right)$	$L_1,L_2=\frac{2V_oT_s}{yI_o(2+G)^2}$
Type III	$G=\frac{D_{1\_max}\left(\frac{N_1+N_3}{N_1-N_2}\right)}{1-D_{1\_max}}$	6	1	1 CL(5)	2	$\frac{V_{ds-1}}{V_o},\frac{V_{Dsn}}{V_o}=\frac{1+G}{G}$; $\frac{V_{ds-2}}{V_o}=\left[1+\frac{(N_1+N_3)}{G(N_1-N_2)}\right]$	$\frac{I_{S1}}{I_o},\frac{I_{Dsn}}{I_o}=\frac{(N_1+N_3)}{(N_1-N_2)}+G$; $\frac{I_{S2}}{I_o}=1+\frac{G(N_1-N_2)}{(N_1+N_3)}$	$I_{Lm}=I_o\left[1+\frac{G(N_1-N_2)}{N_1+N_3}\right]$	$L_m=\frac{V_oT_sN_1(N_1+N_3)}{yI_o[(N_1+N_3)+G(N_1-N_2)]^2}$
Type IV	*if* $D_{1\_max}<0.5$	8	0	2	3	*if* $G<3$	*if* $G<3$	*if* $G<3$	*if* $G<3$
	$G=\frac{D_{1\_max}(2-D_{1\_max})}{D_{1\_max}^2-2D_{1\_max}+}$					$\frac{V_{ds-1}}{V_o},\frac{V_{ds-3}}{V_o}=\frac{1+G}{G}$; $\frac{V_{ds-2}}{V_o},\frac{V_{ds-4}}{V_o}=\frac{\sqrt{1+G}}{G}$	$\frac{I_{S1}}{I_o},\frac{I_{S3}}{I_o}=\sqrt{1+G}$; $\frac{I_{S2}}{I_o},\frac{I_{S4}}{I_o}=1+G$	$I_{L1}=I_o(\sqrt{1+G})$; $I_{L2}=I_o(1+G-\sqrt{1+G})$	$L_1=\frac{V_oT_s(\sqrt{1+G}-1)}{yI_oG(1+G)}$; $L_2=\frac{V_oT_s(\sqrt{1+G}-1)}{yI_oG\sqrt{1+G}(1+G-\sqrt{1+G})}$
	if $D_{1\_max}\geq 0.5$					*if* $G\geq 3$	*if* $G\geq 3$	*if* $G\geq 3$	*if* $G\geq 3$
	$G=\frac{1+D_{1\_max}}{1-D_{1\_max}};$					$\frac{V_{ds-1}}{V_o}=max\left(\frac{4}{G},\frac{1+G}{2G}\right)$; $\frac{V_{ds-2}}{V_o},\frac{V_{ds-4}}{V_o}=\frac{1+G}{2G}$; $\frac{V_{ds-3}}{V_o}=\frac{1+G}{G}$	$\frac{I_{S1}}{I_o},\frac{I_{S3}}{I_o},\frac{I_{S4}}{I_o}=\frac{1+G}{2}$; $\frac{I_{S2}}{I_o}=1+G$	$I_{L1},I_{L2}=\frac{I_o(1+G)}{2}$	$L_1=\frac{2V_oT_s(G-1)}{yI_oG(1+G)^2}$; $L_2=\frac{2V_oT_s(G-1)}{yI_oG(1+G)^2}$

(1) S: Number of switches. (2) D: Number of diodes. (3) L: Number of inductors. (4) C: Number of capacitors. (5) CL: Coupled inductor.

$$\begin{cases} \frac{I_{S1}}{I_o}=\frac{I_{S3}}{I_o}=\sqrt{1+G} & \text{if } G<3 \\ \frac{I_{S1}}{I_o}=\frac{I_{S3}}{I_o}=\frac{1+G}{2} & \text{if } G\geq 3 \\ \frac{I_{S2}}{I_o}=1+G & \\ \frac{I_{S4}}{I_o}=1+G & \text{if } G<3 \\ \frac{I_{S4}}{I_o}=\frac{1+G}{2} & \text{if } G\geq 3 \end{cases} \quad \text{Type IV.} \tag{45}$$

The current handling requirements of the magnetizing inductor L_m of Type III inverter and the inductors L_1 and L_2 of Type IV inverter are given by

$$\begin{cases} I_{Lm}=I_o\left(1+\frac{G(N_1-N_2)}{N_1+N_3}\right) & \text{Type III} \\ I_{L1}=\begin{cases} I_o\left(\sqrt{1+G}\right) & \text{if } G<3 \\ \frac{I_o(1+G)}{2} & \text{if } G\geq 3 \end{cases} & \text{Type IV} \\ I_{L2}=\begin{cases} I_o\left(1+G-\sqrt{1+G}\right) & \text{if } G<3 \\ \frac{I_o(1+G)}{2} & \text{if } G\geq 3 \end{cases} & \text{Type IV} \end{cases}. \tag{46}$$

The values of magnetizing inductance L_m of Type III inverter and the inductors L_1 and L_2 of Type IV inverter are given by

$$\begin{cases} L_m=\frac{V_oT_sN_1(N_1+N_3)}{yI_o[(N_1+N_3)+G(N_1-N_2)]^2} & \text{Type III} \\ L_1=\begin{cases} \frac{V_oT_s\left(\sqrt{1+G}-1\right)}{yI_oG(1+G)} & \text{if } G<3 \\ \frac{2V_oT_s(G-1)}{yI_oG(1+G)^2} & \text{if } G\geq 3 \end{cases} & \text{Type IV} \\ L_2=\begin{cases} \frac{V_oT_s\left(\sqrt{1+G}-1\right)}{yI_oG\sqrt{1+G}\left(1+G-\sqrt{1+G}\right)};G<3 & \\ \frac{2V_oT_s(G-1)}{yI_oG(1+G)^2} & \text{if } G\geq 3 \end{cases} & \text{Type IV} \end{cases}. \tag{47}$$

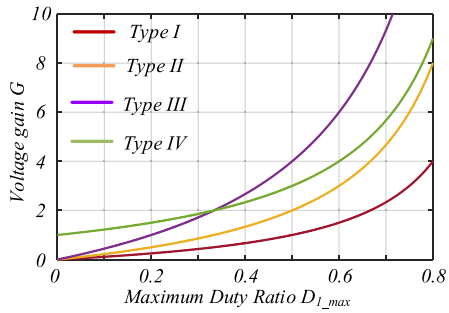

Fig. 23. Voltage gain versus maximum duty ratios of the proposed inverters.

Finally, the aforementioned results are summarized in Table IV to briefly compare all the proposed topologies. The equations for voltage and current stresses of LF switches, output capacitor, and input capacitor are similar for all the proposed inverters given by (14), (19), (20), and (24) and are not included in Table IV. The graph of voltage gain G versus maximum duty ratio $D_{1\_\max}$ for the proposed inverters is plotted in Fig. 23. For the graph of Type III inverter $N_1:N_2:N_3$ is kept $2:1:2$. Fig. 23 confirms that the proposed Type II, III, and IV inverters have high voltage gain capabilities with a Type III inverter having an additional degree of flexibility to achieve high voltage gain by adjusting the turns ratio of the coupled inductor. A Type I inverter is suitable for applications when the input voltage can be both greater and smaller than the output voltage [9], [10], [11], [12], [13], [14], [15], [17], [18], [19], [20], such as several

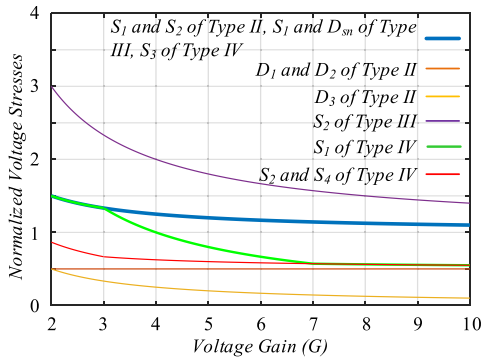

Fig. 24. Graph of the normalized voltage stresses versus voltage gain of the proposed inverters (Type II–IV).

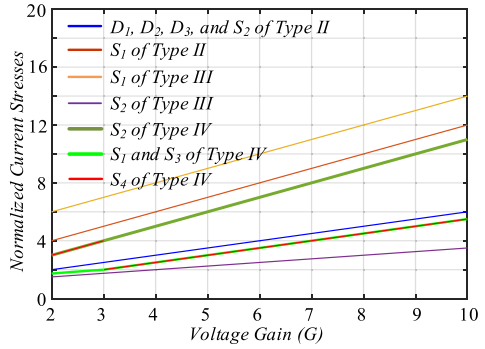

Fig. 25. Graph of normalized current stresses versus voltage gain of the proposed inverters (Type II–IV).

PV panels connected to the grid. On the other hand, Type II, III, and IV inverters are suitable for applications when the output voltage is substantially higher than the input voltage [25], [26], [27], [28], [29], [30] such as a single PV panel connected to the grid. The graphs of normalized voltage and current stresses of the switching devices and diode (see Table IV) of the Type I inverter are already shown in Fig. 9, whereas that of Type II, III, and IV inverters are presented in Figs. 24 and 25. It can be observed that the voltage stresses of the switching devices and diodes of the proposed inverters decrease while their current stresses increase with the voltage gain G. This implies that the voltage ratings for the diodes and switching devices should be based on the minimum required value of G, whereas the current ratings should be selected based on the maximum value of G. Similarly, replacing V_oT_s/yI_o in Table IV by constant k, the normalized inductances (L/k) of the Type II, III, and IV inverters are plotted in Fig. 26, whereas that of Type I inverter is already presented in Fig. 10 earlier. The graphs imply that the value of inductance L should be chosen at the minimum voltage gain G because the inductance value is maximum at this point.

E. Simulation Results and Comparative Analysis

To prove the working principle of the proposed inverters (Type II–IV), simulations are performed in PSIM software with the electrical specifications mentioned in Table V. The waveforms of input voltage V_{in}, output voltage v_o, output current i_o, the

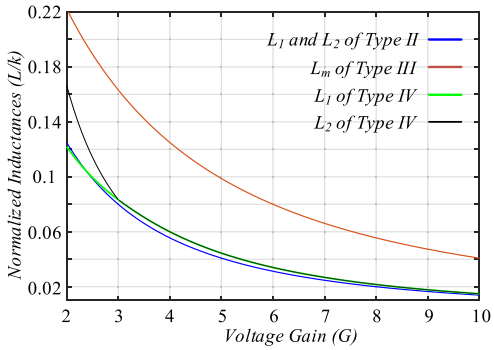

Fig. 26. Graph of normalized inductances versus voltage gain of the proposed inverters (Type II–IV).

TABLE V
ELECTRICAL SPECIFICATIONS OF TYPE II, III, AND IV INVERTERS

Output power	250 W
Input voltage V_{in}	30 V_{dc}
Output voltage v_o	155 V_{peak}
Inductors L_1, L_2 (Type II)	200 μH
Magnetizing inductor L_m (type III)	250 μH
Inductors L_1, L_2 (Type IV)	200 μH
Capacitor C_1 (Type IV)	5 μF
Capacitor C_o	5 μF
Parasitic capacitances C_{p1}, C_{p2}	50 nF

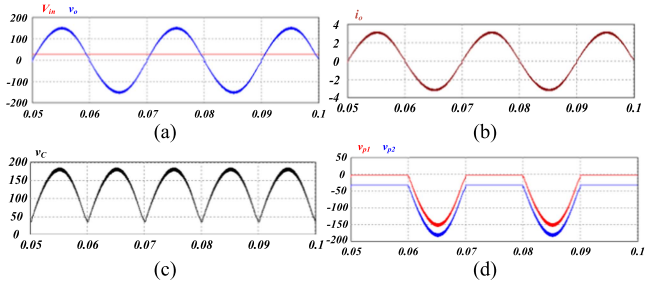

Fig. 27. Simulation waveforms of Type II inverter. (a) Input voltage V_{in} and output voltage v_o. (b) Output current i_o. (c) Voltage across output filter capacitor v_C. (d) Voltages across parasitic capacitances v_{p1} and v_{p2}.

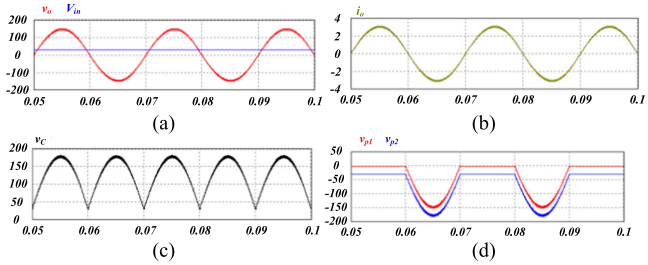

Fig. 28. Simulation waveforms of Type III inverter. (a) V_{in} and v_o. (b) Output current i_o. (c) Voltage v_C. (d) Voltages v_{p1} and v_{p2}.

voltage across the output filter capacitor v_C, and voltages across the parasitic capacitances v_{p1} and v_{p2} of the proposed Type II inverter are presented in Fig. 27. The simulation waveforms of Type III inverter are presented in Fig. 28, and the simulation waveforms of Type IV inverter are presented in Fig. 29. It can

TABLE VI
COMPARISON OF THE PROPOSED TYPE II, III, AND IV INVERTERS WITH CONVENTIONAL HIGH-GAIN INVERTERS

Topology	[25]	[26]	[29]	[30]	Proposed type II	Proposed type III	Proposed type IV
Voltage gain (G)*	$\frac{1}{1-\frac{2}{1-n}D}$	$\frac{(1+nD_{bst})D}{1-D_{bst}}$	$\frac{(k+1)(2D-1)}{D(1-D)}$	$\frac{D\left(\frac{N_1+N_3}{N_1-N_2}\right)}{1-D}$	$G=\frac{2D}{1-D}$	$\frac{D\left(\frac{N_1+N_3}{N_1-N_2}\right)}{1-D}$	$if\ D<0.5$ $G=\frac{D(2-D)}{D^2-2D+1}$ $if\ D\geq 0.5$ $G=\frac{1+D}{1-D}$;
Switches	5	4	8	4	6	6	8
Diodes	3	3	0	2	3	1	0
Inductors (L)/ Coupled inductors (CL)	2 (1 L and 1 CL)	2 (1 L and 1 CL)	2 L	2 CL	2 L	1 CL	2 L
Capacitors	3	3	6	3	2	2	3
Line-frequency switches	0	0	0	0	4	4	4
High-frequency switches	5	4	8	4	2	2	4
Leakage current	High	High	small	small	small	small	small

* "n" represents the turns ratio of the coupled inductor; "D" represents the peak of the value of duty ratio of sinusoidal pulsewidth modulatopm scheme; "D_{bst}" is constant and it represents the duty ratio of the integrated boost converter; "k" represents the number of multiplier cells.

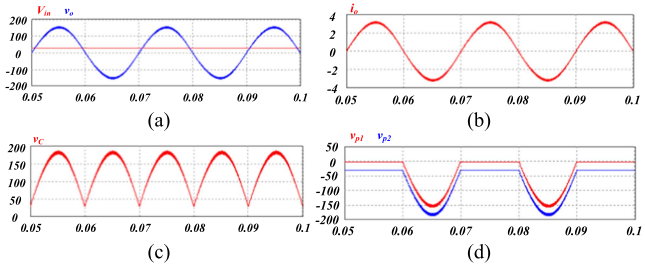

Fig. 29. Simulation waveforms of Type IV inverter. (a) V_{in} and v_o. (b) Output current i_o. (c) Voltage v_C. (d) Voltages v_{p1} and v_{p2}.

be observed that the voltages across the output filter capacitors of the inverters (Type II–IV) are rectified sinusoidal voltages with dc offset equal to the input voltage. Similarly, voltages across the parasitic capacitances are either constant or vary sinusoidally with no significant HF voltage variations, which agrees with the earlier theoretical analysis. A brief comparison of the proposed Type II, III, and IV inverters is also made with the conventional high-gain topologies in Table VI. It can be observed that all the inverters in Table VI are capable of achieving high voltage gain. The inverters in [25] and [26] are good in terms of switch count but the high leakage current makes it less effective. The inverter in [29] has small leakage current but the high number of active and passive components is the downside of this topology. The inverter in [30] is another promising topology with voltage gain exactly similar to that of the proposed Type III inverter but it has only 50% magnetic utilization. Furthermore, all the proposed inverters have low leakage current due to their virtual-ground characteristics and have the least number of switches operating at high frequency which is good for achieving high efficiency and makes it suitable for PV applications.

VI. CONCLUSION

In this article, a new family of single-phase transformerless BBIs is proposed. The family includes four types of inverters (Type I–IV). The proposed Type I Inverter has a wide gain range, whereas Type II, III, and IV are capable of achieving high voltage gain at small duty ratios. These inverters possess virtual-ground characteristics, which makes them efficient in terms of leakage current. Additionally, four of the switching devices in the proposed inverters operate at low frequencies and have low voltage and current stresses. This feature is beneficial in terms of efficiency, as it reduces switching losses. The performance of the proposed inverters is supported by detailed theoretical analysis, simulations, and experiment results, which demonstrate their effectiveness.

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