Sigma Converter Family With Common Ground for the 48 V Data Center

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***Abstract*—The 48 V bus architecture has become a standard in modern data centers, due to the increasing power demands of digital loads. This requires low-profile, high-density intermediate bus converters, able to efficiently step-down the input bus. Usually, this bus has a wide variation (40–60 V), and the voltage regulation module (VRM) must withstand the whole converted range, with a negative impact on efficiency due to design oversizing. A regulated intermediate bus converter can address this issue, enabling a fine-tuned VRM design. In this article, a novel regulated regulated hybrid switched capacitor (RHSC) sigma converter family is proposed, which enables regulation without sacrificing efficiency or power density. This is enabled by a new architecture featuring the *sigma* connection of a high-efficiency, unregulated converter with a low-power, regulated one sharing the same ground reference potential (GND) domain, i.e., without the need of functional isolation. With this approach, efficiency and regulation can coexist in a single converter. This work includes the full analysis and design tools for the new RHSC family, together with two demonstrators: a 1.2 kW, 48–12 V down-solution and a 750 W, 48–5.1 V eighth-brick module, both exceeding a power density of 1 kW/in^3.**

***Index Terms*—48 V, data center, hybrid switched capacitor (HSC), hyperscale, input-series output-parallel (ISOP), intermediate bus converter (IBC), regulated converter, sigma.**

I. Introduction

HYPERSCALE computing and artificial intelligence have become the backbone of the modern digital world [1], requiring increasing efficiency and power density from the power converters in the rack. The 48 V distribution bus is now widespread in modern data centers [2], [3], and it is mandatory to support nowadays' power demands, mainly due to the lowered distribution losses with respect to the old 12 V systems. The 48 V conversion chain is usually composed of one or more unregulated intermediate-bus converters (IBCs), which provide a middle-voltage rail [4], and a voltage regulation module (VRM) placed close to the digital load. The first stage is usually characterized by high efficiency and no regulation, while the VRM must regulate the application-specific integrated circuit (ASIC) core voltage.

The last decades have shown that ASIC/CPU voltage is constantly decreasing: in 2000 a high-performance CPU required 1.8 V on average, but now this value can be as low as 0.6 V, especially for accelerator modules [5]. This values are not scaling at constant power; on the contrary, ASIC power density is rapidly increasing with the massive use of high-performance chips and parallel computing [6]. This trend makes the VRM design critical: duty-cycle reduction encounters a limit in terms of control and efficiency, and therefore, the intermediate bus must decrease as well. One end, 48–12 V bus converters occupy the greater share of today's data centers server boards [7]; but recent research suggests [8] that when both the intermediate bus converter and the second-stage buck converters are considered, a lower intermediate bus voltage (e.g., 6 V) may offer superior overall efficiency. As a consequence, there is a strong interest in high-efficiency fixed-ratio conversion with ratios of 8–1 V and more. In this scenario, the IBC could play a fundamental role in the system improvement. When the input voltage has a wide variation range (40–60 V is the most common), the VRM must be designed to operate in these corner cases, as the IBC is performing a fixed conversion: a regulated IBC with high efficiency could relieve VRM design constraint and allow us to use lower voltage devices with a better performance. Numerous high-power density, very efficient fixed ratio solutions have been presented in the literature and implemented in industry [9], [10], [11], [12]. On the other hand, the new open compute project (OCP) specification will fix a narrow input voltage range of 49–51 V in the near future [13], paving the way for partial-power architectures exploiting the small input variation.

High step-down requirement, semiregulation with a wide input variation or full regulation with a narrow input variation are scenarios, which could benefit from a sigma IBC stage. Sigma [or input-series output-parallel (ISOP)] converters can achieve output regulation while maintaining a high efficiency and power density [14], [15], [16], [17]. This approach combines two converters, which share the same input current and the same output voltage, as shown in Fig. 1: input voltage is divided among the two inputs, and overall efficiency can be tailored to strongly depend on the high-efficiency block

$$\eta = \frac{V_{\text{in1}}}{V_{\text{in}}} \cdot \eta_1 + \frac{V_{\text{in2}}}{V_{\text{in}}} \cdot \eta_2 = \frac{KV_{\text{out}}}{V_{\text{in}}} \cdot \eta_1 + \frac{V_{\text{in}} - KV_{\text{out}}}{V_{\text{in}}} \cdot \eta_2. \tag{1}$$

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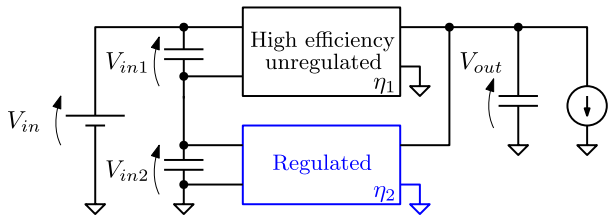

Fig. 1. Sigma connection (also called ISOP) between a high-efficiency converter and a regulated converter.

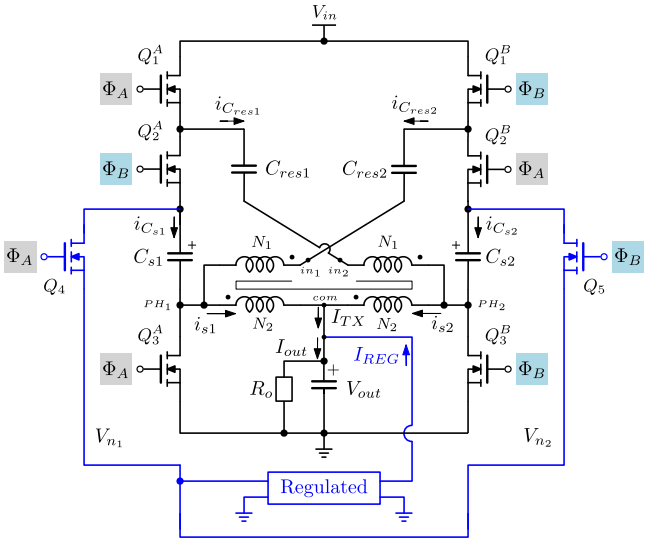

Fig. 2. Input-series, output-parallel (also called *sigma*) connection between a high-efficiency converter and a regulated converter.

This is possible because power must not be entirely processed through the regulated subconverter, which has an intrinsic lower efficiency. Following the (1), the design criterion of the ISOP system is to choose the conversion ratio of the unregulated converter K to minimize the converted power of the regulated on-demand to guarantee its operation in the whole range of V_{in}. As shown in [14], [15], [16], and [17], ISOP can be obtained by exploiting a converter functional isolation: this automatically enables the level shifting of one block to a certain voltage domain. For example, the first block on Fig. 1 could be an isolated *LLC*. This work expands the results of [18] by using a basic scheme as reported in Fig. 2, where the ISOP connection is performed without the requirement for isolation. The proposed solutions are based on an autotransformer, enabling a strong increase in power density: this is due to an electrical power transfer from input to output, which is prevented in isolated solutions. Also, a hybrid switched capacitor (HSC) converter can be built with ideal winding interleaving. These factors yield lower losses compared to an *LLC* [19]. The unregulated stage is based on an HSC converter with a conversion ratio that depends on an autotransformer turn ratio N_1/N_2. In general, N_1 can also be 0. As it will be discussed in the following sections, the input-series behavior is ensured by *sigma* capacitors $C_{s_{1,2}}$, which are alternatively placed in series to the unregulated resonant currents and then used as supply for the regulated converter. This enforces the same average input current between HSC and regulated block, as shown in Fig. 1. As the new converter family is the combination of an HSC and a regulated block, it is given the name of *regulated hybrid switched capacitor* (RHSC) converter. In this work, RHSC will be used to address any topology following the generalized circuit of Fig. 2.

This key difference can be summarized with the *common-ground* words, as the two blocks now exist in the same *GND domain*. This work proves this concept with two demonstrators: a 48–12 V down-solution and a 48–5.1 V eighth-brick module, both exceeding a power density of 1 kW/in^3.

This article presents and analyzes the two solutions, both based on the *sigma* (ISOP) common-ground concept, analyzing architecture, waveforms, and experimental results for both in the last section. In addition, an in-depth explanation of the planar magnetic of the 48–5 V eighth brick is shown, where the regulated-block inductor is embedded with the HSC autotransformer and the small-signal analysis. For the module solution, the autotransformer is embedded in the printed circuit board (PCB) to decrease termination loss and leakage inductance due to higher output currents; for the down- (or discrete-) solution, the autotransformer is implemented as and surface mounting device (SMD) block to yield an unexpensive and flexible example.

II. 48–12 V: Low Step-Down RHSC Version

The best ISOP configuration of Fig. 2 for a 48–12 V application is $N_1 = 0$ ($K = 4$) and a noninverting buck–boost as regulated block, as reported in Fig. 3. As Fig. 6 will show, the output can be regulated at 12 V for most of the input voltage range, and most importantly is never rising over 12 V. In a data center board, this can be useful for VRM supply and/or peripherals accepting this behavior; in particular, the VRM can be operated at a higher frequency: it must not support high input voltage operation anymore and the driving strength can be increased. With the proposed solution, semiregulation does not imply lower efficiency. The buck–boost is designed to operate as a pure boost converter, since DT signal duration is very short, as reported in Fig. 4. The presence of DT is to avoid interaction between the two subconverters during HSC dead-time and zero-voltage switching (ZVS). From here on, the regulated converter will be called only *boost*; nonetheless, the derived conversion ratio can be extended by the modulation of DT. The employment of capacitors to create the sigma connection allows for highly efficient regulation.

The hybrid switch capacitor subconverter, which consists of MOSFETs $Q_1^{A,B}$, to $Q_3^{A,B}$, operates in resonant mode and features ZVS+zero-current switching (ZCS) transitions on each component. The converter is driven by pulsewidth modulation (PWM) signals Φ_A and Φ_B at fixed frequency and fixed duty-cycle. While magnetizing current is utilized for soft switching, resonance occurs between the autotransformer's leakage inductance, which is made up of two windings with the same turn number, and resonant capacitors C_{res1} and C_{res2}. Sigma capacitors C_{s1} and C_{s2} act as decoupling capacitors and have negligible interaction with the resonance, supplying the boost subconverter when the respective synchronous rectifier Q_3^A or Q_3^B is active; for this reason are bigger in value than resonant

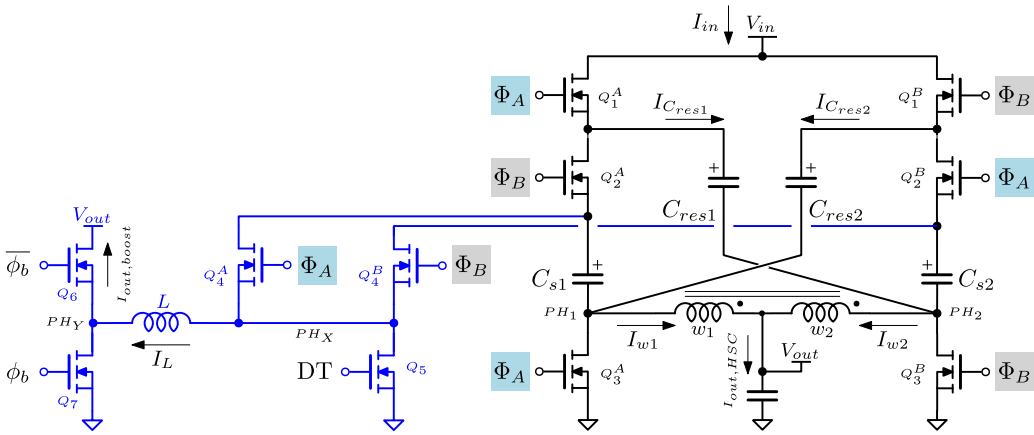

Fig. 3. Low step-down RHSC topology with PWM signals. HSC subconverter (black) is on the right. Boost subconverter (blue) is on the left. Pass-transistors $Q_4^{A,B}$ are used in combination with sigma-capacitors C_{s1} and C_{s2} to implement a sigma connection of the two blocks.

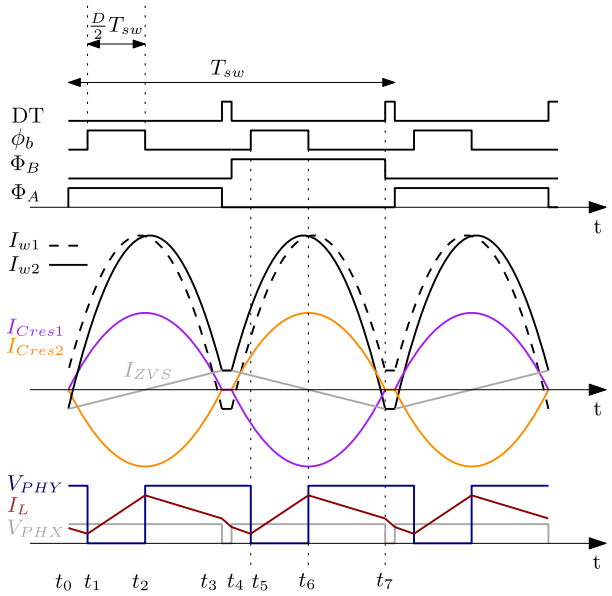

Fig. 4. Low step-down RHSC main waveforms.

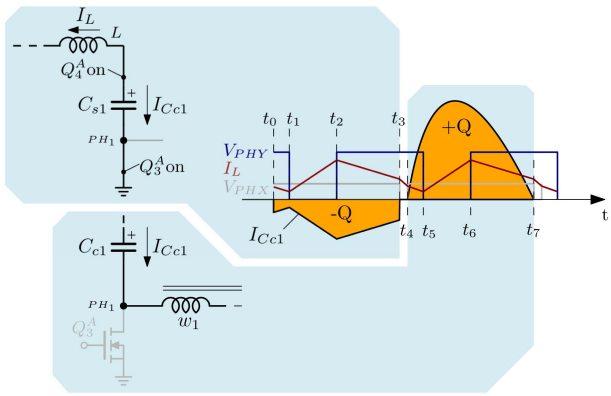

Fig. 5. Charge balance mechanism on *sigma capacitors* C_{sx}, ensuring the equivalent input-series connection between the HSC and the boost block.

capacitors. As *pass transistors*, Q_4^A and Q_4^B enable node PH_X to be connected to the proper supply voltage. Thus, neglecting the little dead time DT during which Q_5 is active, PH_X is usually always coupled to one of the two sigma capacitors C_{sx}. On the other hand, PH_Y is driven with a duty-cycle D as a conventional boost converter. In this converter architecture, the input voltage of the boost converter is the voltage of the sigma capacitors, while its output corresponds to the actual output voltage V_{out}. In steady state, I_L current is always flowing through one sigma capacitor C_{sx}, except during DT. In the next phase, C_{sx} is recharged by the autotransformer current, as reported in Fig. 5. Charge balance ensures that both the HSC and the boost converter's inputs have the same average current, as shown in Fig. 1. The possible conversion for pure boost operation, which is preferred to maximize efficiency, ranges from $V_{out} = V_{in}/4$ to $V_{in}/5$. In modern data centers V_{in} varies from 48 to 60 V, so a regulated 12 V output voltage can always be obtained.

With reference to Fig. 4, converter's operation phases are here described.

$t_0 \rightarrow t_3$: Q_1^A, Q_2^B, and Q_3^A are in ON state. C_{s1} is connected to ground and supplies the converter boost through Q_4^A. In this phase, Q_7 connects the terminal inductor PH_Y to ground at node during the interval $t_1 \rightarrow t_2$, while Q_6 connects the inductor to V_{out} in the remaining time. The regulated converter has a dead-time at each period, which is not shown in Fig. 4. Charge Q is removed from C_{s1} (this is shown in Fig. 5), while C_{s2} gets charged in the opposite direction. A resonant current, I_{Cres1}, flows from V_{in} through Q_1 and C_{res1}, resonates with the two-winding transformer's leakage inductance, flows into w_2, and charges V_{out} in the end. The resonance of C_{res2} with the leakage inductance induces another equal resonant current while Q_3^A is connecting PH_1 to ground. This current flows into C_{s2} adds up to I_{Cres1} at PH_2 node, also flowing into winding w_2 and ultimately to V_{out}, therefore

$$I_{w2} = 2 \cdot I_{Cres1} = 2 \cdot I_{in}. \tag{2}$$

The other winding w_1 is connected to ground. It magnetically delivers to the output I_{w1}, which is a copy of I_{w2} (supposing a

high coupling factor). HSC total output current is

$$I_{\text{out,HSC}} = I_{w1} + I_{w2} = 4 \cdot I_{\text{in}}. \tag{3}$$

This shows that the 2-windings HSC converter multiplies by four the input current, and alone would be a 4:1 unregulated converter. The sigma capacitors $C_{s1,2}$ allow us to offset this conversion ratio, as an additional current is delivered by the boost. During this phase, the following voltage relations are present:

$$\begin{cases} 2V_{\text{out}} + V_{C_{\text{res1}}} = V_{\text{in}} \\ V_{C_{\text{res2}}} = 2V_{\text{out}} + V_{C_{s2}}. \end{cases} \tag{4}$$

$t_3 \rightarrow t_4$: This period represents the HSC dead-time in which Q_1^A, Q_2^B, and Q_3^A are turned-OFF at almost zero-current and Q_5 disconnects the inductor current I_L from the HSC nodes. The boost keeps operating as usual, but its input voltage PH_X is zero during this period. In steady-state operation, considering from t_0 to t_4, C_{s1} has lost a charge Q and C_{s2} has stored the same charge Q. The HSC nodes are charged and discharged by the transformer magnetizing current, allowing ZVS operation: PH_1 is charged to $2V_{\text{out}}$, while PH_2 is discharged to zero. MOSFETs Q_1^B, Q_2^A, and Q_3^B drain–source voltages are being discharged to zero.

$t_4 \rightarrow t_7$: The behavior is symmetrical. The boost is supplied by sigma capacitor C_{s2} and has a positive duty-cycle between t_5 and t_6. The autotransformer is supplied by a symmetrical voltage and the magnetizing current changes direction. During this phase the following equations are valid:

$$\begin{cases} 2V_{\text{out}} + V_{C_{\text{res2}}} = V_{\text{in}} \\ V_{C_{\text{res1}}} = 2V_{\text{out}} + V_{C_{s1}}. \end{cases} \tag{5}$$

The total system conversion ratio can now be calculated. The volt $\times$ second product on the inductor L in a switching period can be used to calculate the voltage on the sigma capacitors C_{s1} and C_{s2} in steady state

$$V_{\text{out}}(1-D)T_{\text{sw}} = V_{\text{csx}}\,(T_{\text{sw}} - 2\text{DT}) \tag{6}$$

where V_{csx} is the voltage on the two sigma capacitors, which is equal in a symmetrical system. Also, D is defined for a boost converter, therefore, is it proportional to Q_7 on-time. Due to the double-frequency operation of this block, the boost duty-cycle is divided into two equal intervals, as reported in Fig. 4. Equation (6) shows that the boost block may be converted into a real noninverting buck–boost using DT. As previously mentioned, DT is solely used in this application to enable the HSC to soft-switch operation: if I_L is negative at instants t_4 and t_7 (light-load condition or load *dump*), this current would flow into the body diodes of Q_4^A or Q_4^B during the HSC dead-time, preventing the HSC soft-switching. Furthermore, during HSC dead time, as there would be no *freewheeling* path when Q_4^A and Q_4^B are both OFF, a positive I_L inductor current would damage them. In general, DT can be expanded to improve robustness or synced with the HSC dead-time.

In this application, DT is very small

$$\left.\frac{T_{\text{sw}} - 2\text{DT}}{T_{\text{sw}}}\right|_{\text{DT} \ll T_{\text{sw}}} \rightarrow 1 \Rightarrow V_{\text{csx}} = V_{\text{out}}(1-D). \tag{7}$$

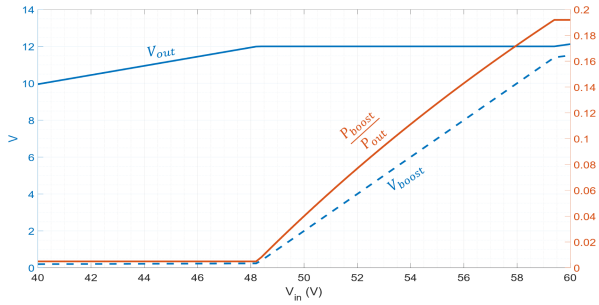

Fig. 6. V_{out} (blue) and $P_{\text{boost}}/P_{\text{out}}$ (red) as a function of V_{in}. $D_{\text{min}} = 0.05$, $D_{\text{max}} = 0.98$.

The difference between the first equations of (4) and (5) yields $V_{C\text{res1}} = V_{C\text{res2}} = V_{C\text{resx}}$, as expected from a symmetrical converter. Also

$$V_{C\text{resx}} = V_{\text{in}} - 2V_{\text{out}}. \tag{8}$$

This equation is useful to define the resonant capacitors maximum voltage. The second equation of (4) or (5) can be used to derive the full conversion ratio

$$V_{\text{out}} = \frac{V_{\text{in}}}{5-D}. \tag{9}$$

This equation sets the intrinsic conversion ratio boundary for this topology, which can range from $V_{\text{in}}/4$ to $V_{\text{in}}/5$. The sigma capacitors' charge balancing system is illustrated in Fig. 5. As previously mentioned, the charge Q is removed from the boost block after being stored in one C_{sx} via the HSC's resonant current. The resonant current is always equal to I_{in} ($I_{\text{in}} = I_{C\text{res1}}$ for the first $T_{\text{sw}}/2$, $I_{\text{in}} = I_{C\text{res2}}$ for the other half). Sigma capacitors make sure that I_{in} is equal to the average input current of both HSC and boost when the system is in steady state. The supplied powers of HSC and boost may be derived since each block's output voltage is equal. The duty-cycle D can be expressed as a function of the input and output voltages using (9). This leads to the following power ratio for the two blocks:

$$\begin{cases} P_{\text{boost}} = V_{\text{out}} \cdot I_{\text{in}}(1-D) = P_{\text{out}} \frac{V_{\text{out}}}{V_{\text{in}}} \left(1 - \frac{5V_{\text{out}} - V_{\text{in}}}{V_{\text{out}}}\right) \\ P_{\text{HSC}} = P_{\text{out}} - P_{\text{boost}}. \end{cases} \tag{10}$$

As the duty-cycle D is limited, the conversion ratio and power share is discontinuous and results in the semiregulated behavior of this solution. Fig. 6 shows these two quantities in the range $40\ \text{V} \leq V_{\text{in}} \leq 60\ \text{V}$: it is obvious that the boost only transports a very small portion of the output power across the whole range, ensuring that the HSC block's overall efficiency is maintained at a high level.

III. 48–5 V: High Step-Down RHSC Version

This high step-down version is compatible with a topological configuration of Fig. 2 with $N_1 = 2$ and $N_2 = 1$ ($K = 8$), where the regulated subconverter is a buck, as reported in Fig. 7. By using a buck as regulated converter, the switches $Q_{4,5}$ of Fig. 2 can be merged with the *high-side* switch of the buck creating the two *high-side* buck reported in Fig. 7. As the previous

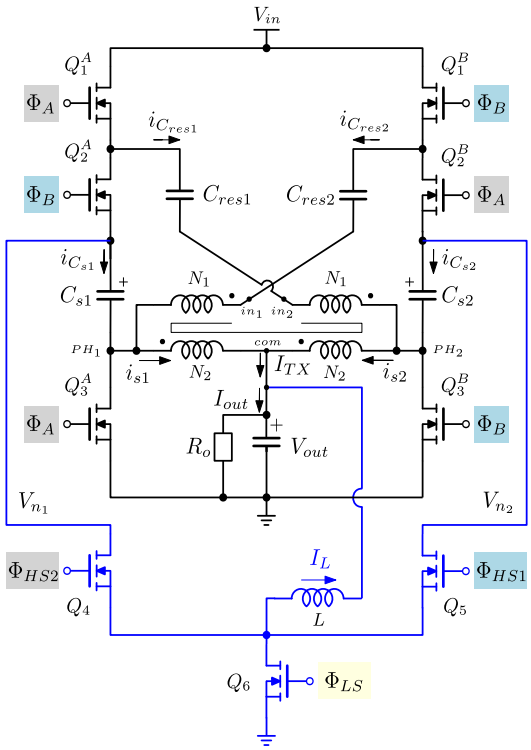

Fig. 7. High step-down RHSC topology with PWM signals.

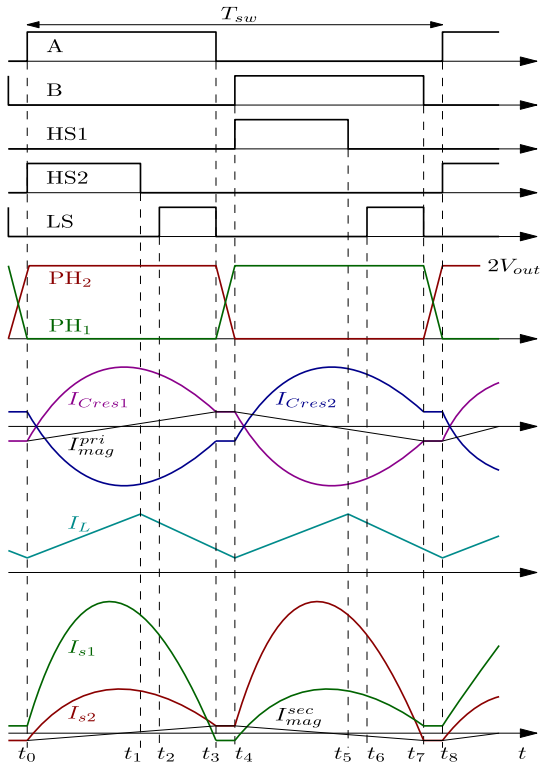

Fig. 8. High step-down RHSC main waveforms.

configuration, this converter is equivalent to a sigma topology as [8] (ISOP connection) between a high-power HSC [19] and a buck. This is achieved without the use of isolated magnetics, but using instead two sigma capacitors C_{s1}, C_{s2} to enforce that the same average current is fed to both subconverters. As it will be shown is this section, during one switching cycle each clamping capacitor is first configured in series along the HSC power path, and then serves as a voltage source for the buck. The steady-state charge balance ensures charge variation to be zero, which translates to input-series connection. Subconverters outputs are instead paralleled, completing the ISOP connection. The group composed by $Q_1^{A,B}$ to $Q_3^{A,B}$ is an HSC converter, featuring high step-down capability and high power density, while the group composed by Q_4 to Q_6 is a buck converter with two high-side switches. The split high-side is necessary to draw energy alternatively from C_{s1} or C_{s2} during the correct phase. At the inductor *phase* node the behavior is identical to a normal buck converter that works at double switching frequency, so the *split-phase* buck behaves exactly like a traditional one. The HSC converter, with PWM signals Φ_A and Φ_B, operates at fixed frequency and fixed duty-cycle. MOSFETs $Q_1^{A,B}$ to $Q_3^{A,B}$ achieve quasi-ZCS and ZVS due to the magnetizing inductance of the transformer. The buck is synchronized with the HSC, as each *high-side* draws power from its clamping capacitor when this is reference to ground. So, in other words, Φ_{HS1} becomes active during the period in which Φ_B is active. To better understand the whole converter operation, each subinterval is here explained.

$t_0 \rightarrow t_1$: Q_1^A, Q_2^B, and Q_3^A are active. C_{s1} is referenced to ground and supplies the buck through Q_7, therefore, the current I_L increases. At t_1, charge Q is removed from C_{s1} (this is also shown in Fig. 9), while C_{s2} is being charged by $I_{C\text{res}2}$ that is negative (as reported in Fig. 8). A resonant current flows from V_{in} through Q_1^A and $C_{\text{res}1}$, which resonates with the leakage inductance of the multiwinding transformer. During this interval, this current is $I_{C\text{res}1}$ and it is forced in windings N_1 and N_2 (on the right side of Fig. 7), ultimately charging V_{out}. At the same time, Q_3^A is connecting PH_1 to ground: another equal resonant current manifests due to the resonance of $C_{\text{res}2}$ with the leakage inductance. This current flows inside windings N_1 (left side), Q_2^B, charges C_{s2} and N_2 (right side), finishing at V_{out}. N_1 windings have $I_{C\text{res}1}$ each, while one N_2 has $2 \times I_{C\text{res}1} = I_{s2}$ (in this phase). The other N_2 winding (on the left) is referenced to ground, and reflects to the output $I_{s1} = \frac{2N_1+2N_2}{N_2} I_{C\text{res}1}$. Also, note that $I_{C\text{res}1} = I_{\text{in}}$, where I_{in} is the current drawn from the input.

$t_1 \rightarrow t_3$: The HSC continues to operate as in the previous phase, while the buck turns OFF Q_4 and turns ON the low-side Q_6 after the dead time $t_2 - t_1$. The inductor current decreases. During this phase, C_{s1} is floating. In the next half of the switching cycle, the transformer will operate in a complementary pattern. For this $T_{\text{sw}}/2$, the *ampere-turn* count yields

$$I_{\text{TX}}(t) = I_{C\text{res}1}(t) \cdot \left(4 + 2\frac{N_1}{N_2}\right) = I_{\text{in}}(t) \cdot \left(4 + 2\frac{N_1}{N_2}\right). \tag{11}$$

$t_3 \rightarrow t_4$: Both subconverters have a dead-time. C_{s2} has stored the charge Q, which will be depleted by the buck in the next phase. The HSC nodes are charged and discharged by the transformer magnetizing current: PH_1 is charged to $2V_{\text{out}}$, while

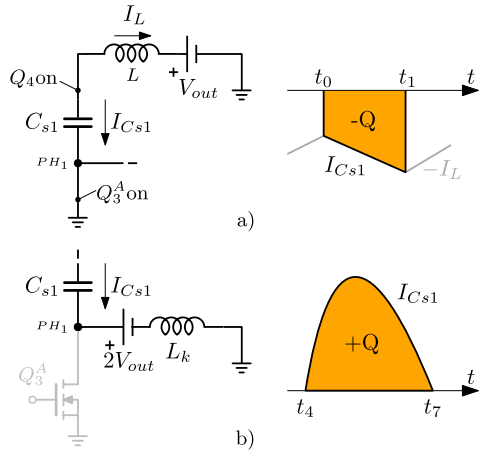

Fig. 9. Charge balance mechanism on *sigma capacitors* C_{sx}, implementing the equivalent input-series connection between the HSC and the buck.

PH_2 is discharged to zero. Also nodes V_{nx} experience the same ZVS transition, together with Q_2^A and Q_2^B drains.

$t_4 \rightarrow t_8$: The behavior is symmetrical. During t_4 to t_5, C_{s2} is referenced to ground and supplies the buck through Q_5 with a charge Q, which is depleted at t_5, when Q_5 turns OFF. C_{s1} is being charged in the opposite direction. Each HSC node will be charged or discharged by the magnetizing inductance during the dead-time $t_8 - t_7$. Equation (11) becomes (12), as the transformer is excited in a symmetrical pattern and $I_{C\text{res}2}$ is supplied by the input through Q_1^B, therefore

$$I_{\text{TX}}(t) = I_{C\text{res}2}(t) \cdot \left(4 + 2\frac{N_1}{N_2}\right) = I_{\text{in}}(t) \cdot \left(4 + 2\frac{N_1}{N_2}\right). \tag{12}$$

Equations (11) and (12) state that a *resonant bump* is always drawn from the input, and the following equation, which expresses the current delivered to the output though the unregulated subconverter (the HSC) is always valid

$$I_{\text{TX}}(t) = I_{\text{in}}(t) \cdot \left(4 + 2\frac{N_1}{N_2}\right). \tag{13}$$

Fig. 9 shows the equivalent *input-series* behavior of the subconverters, which is given by the charge balance on the clamping capacitors, as briefly explained in the operation phases. In this figure, the charge balance of the clamping capacitor C_{s1} is represented. During the subinterval t_0 to t_1, this capacitor supplies the buck with a charge Q, while during t_4 to t_7 the same charge is restored by the resonant current. The charge balance on C_{s1} and C_{s2} (which follows the exact operation) enforces the same average current among the two subconverters, as the whole converter operates at fixed frequency. On the other hand, the steady-state voltage on these capacitors is determined by the buck duty-cycle: this is in fact the input voltage of the buck itself, therefore

$$V_{Cs1} = V_{Cs2} = \frac{V_{\text{out}}}{D}. \tag{14}$$

In steady state, the conversion ratio of the whole converter can be derived by considering the charge balance on a resonant capacitor, such as $C_{\text{res}1}$. In steady state, its voltage must be equal

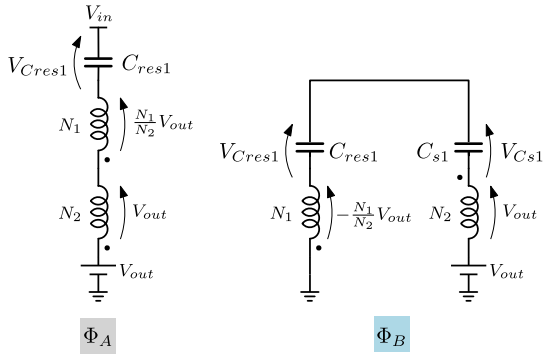

Fig. 10. Charge balance mechanism on *resonant capacitors* C_{resx}.

in both subintervals, as shown in Fig. 10

$$\begin{cases} V_{\text{in}} = V_{C\text{res}1} + V_{\text{out}}\left(\frac{N_1}{N_2} + 2\right) \\ -\frac{N_1}{N_2}V_{\text{out}} + V_{C\text{res}1} = V_{Cs1} + 2V_{\text{out}}. \end{cases} \tag{15}$$

By using (14) and (15), the following relation between input V_{in} and output voltage V_{out} can be written, which highlights the *sigma* nature of the topology

$$V_{\text{in}} = V_{\text{out}}\left(4 + 2\frac{N_1}{N_2}\right) + \frac{V_{\text{out}}}{D} \tag{16}$$

where the first term of the sum is the output voltage V_{out} divided by the conversion ratio of the HSC converter and the second is the output voltage divided by the conversion ratio of the buck. Finally, the total conversion ratio can be written as

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{4 + 2\frac{N_1}{N_2} + \frac{1}{D}}. \tag{17}$$

From (17), it is clear that also this topology is intrinsically bounded in conversion ratio. In particular, the maximum output voltage is obtained when $D \rightarrow 1$. The power share delivered to the output can be derived for the HSC and the buck. The average input current is the same for the two subconverters, and corresponds to the average input current drawn from V_{in} (observe Fig. 1)

$$I_{\text{HSC}}^{\text{in}} = I_{\text{buck}}^{\text{in}} = \frac{P_{\text{out}}}{V_{\text{in}}} \tag{18}$$

where $P_{\text{out}} = P_{\text{in}}$ is assumed for simplicity, and $I_{\text{HSC}}^{\text{in}}$, $I_{\text{buck}}^{\text{in}}$ are the average input currents of the two subconverters. The buck input current depends on the duty-cycle

$$D \cdot I_{\text{buck}}^{\text{out}} = D \cdot \frac{P_{\text{buck}}}{V_{\text{out}}} = I_{\text{buck}}^{\text{in}} = \frac{P_{\text{out}}}{V_{\text{in}}}. \tag{19}$$

This equation can be combined with the transformation ratio (17) to express the power ratio delivered by the buck

$$\frac{P_{\text{buck}}}{P_{\text{out}}} = 1 - \frac{V_{\text{out}}}{V_{\text{in}}}\left(4 + 2\frac{N_1}{N_2}\right). \tag{20}$$

The converter is then designed to operate in a *sweet spot*, i.e., with a voltage ratio that maximizes the power delivered by the high efficiency HSC. As it will be shown, (20) yields values between 15% and 20% for the current design.

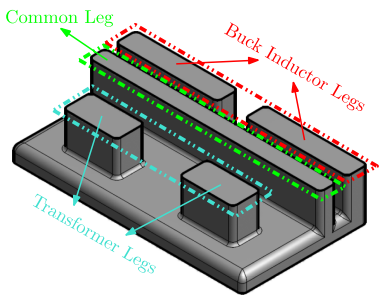

Fig. 11. Structure of the magnetic component.

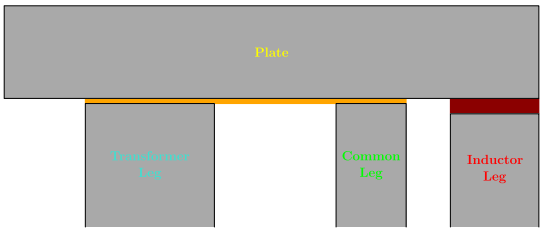

Fig. 12. Cross sections of the magnetic component. It is highlighted the transformer gap (orange) and the inductor gap (dark red).

A. 48–5 V RHSC Magnetic Design

The magnetic components of this converter are the *matrix multitapped autotransformer* (MMTA) of the HSC and the inductance of the buck. The MMTA architecture was explained in [19], where it is designed with two elemental MTAs to distribute the high output current and to reduce winding and *termination loss*. In order to achieve high power density, each magnetic component is mounted in a single core; with the planar autotransformer, the implementation of a nonplanar inductor will dramatically increase the aspect ratio. The structure of the core is shown in Fig. 11. It is the structure of the MMTA of the HSC with two additional legs which are the core of the buck inductance. Two legs have been used to symmetrize the power distribution network (PDN); of course, one single leg can be used.

Two gaps are required to achieve suitable magnetizing and buck inductance. To gain mechanical stability, the MMTA's gap is splitted among the autotransformer legs and the common leg (by placing a thin dielectric layer between the legs and the plate), while the inductor legs are milled-down, as shown in Fig. 12. The value of the buck inductor is selected as for a normal buck converter (tradeoff between copper losses and current ripple, targeting 22% at full load).

Differently from [19], this core experiences a dc flux associated with the inductor. With this solution, the transformer legs are carrying only ac flux and the buck legs ac+dc flux. The flux in the common leg is the summation of fluxes of the MMTA and the buck. Fig. 13 shows the windings configuration, where each arrow follows a clockwise convention and gives the winding reference for the next figures. The buck inductor starts with the phase node ph_B and then splits to reach V_{out}. As previously mentioned, this helps the symmetrization of the PDN.

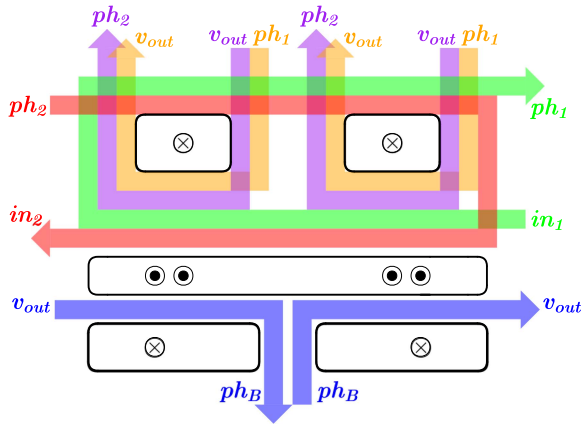

Fig. 13. Top view of the magnetic design with fluxes and currents referenced in clockwise direction.

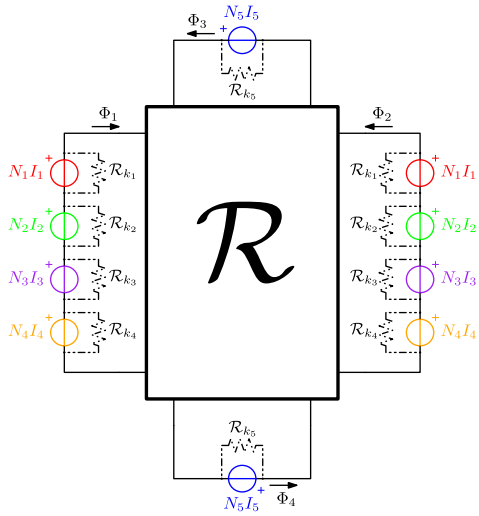

Fig. 14. Equivalent electrical circuit of the magnetic design.

With this winding configuration the buck phase node is *blind* to HSC operation as any shared flux is canceled by the two opposite-signed inductor windings: this is beneficial for the current ripple on the buck devices. The same is valid from buck to HSC. Anyway, the coupling between the two areas is minimized by reducing the common leg gap.

The design of the *merged* magnetic can be carried out simply under the hypothesis of negligible shared flux between the two structures, i.e., by designing the autotransformer and inductor legs separately, and then ensuring a sufficiently large common leg for the desired operating conditions. To provide a complete overview on the magnetic structure, an electrical equivalent circuit is here derived, as shown in Fig. 14. Each MMF generator is referenced to the windings of the four legs in Fig. 13. In the figure, the leakage reluctances are reported for each winding (in parallel to the equivalent MMF generator). This is a simplification of physics because in the case of multiwindings the flux not shared by all the windings does not necessarily close on each single one but, obviously, can be shared by a group. The legs of the magnetic design are connected through the reluctance block

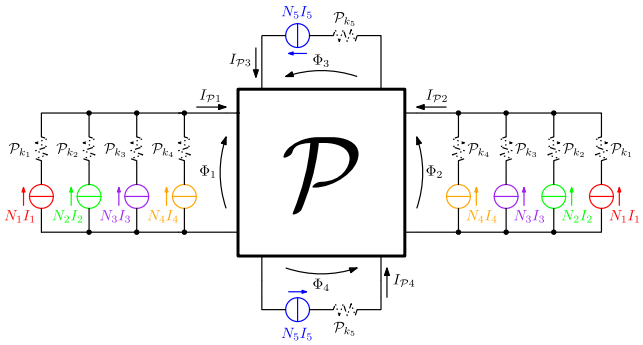

Fig. 15. Equivalent electrical dual circuit of the magnetic design.

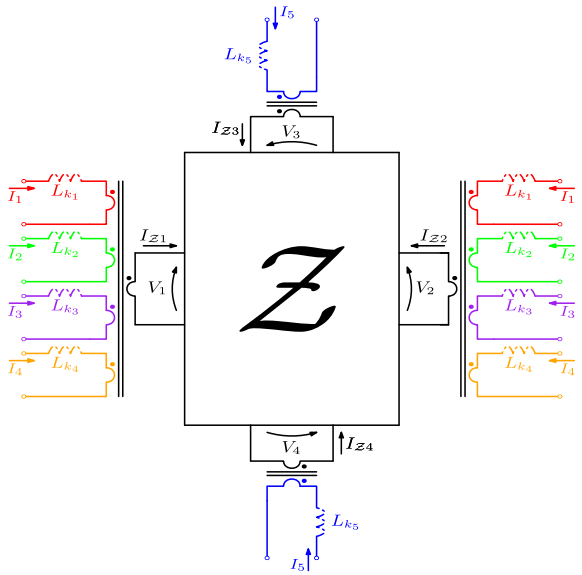

Fig. 16. Equivalent electrical circuit with impedance matrix.

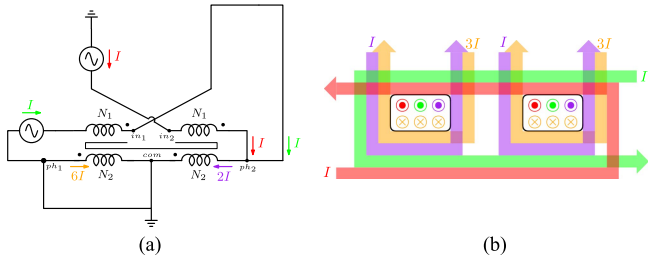

Fig. 17. FEM simulation configuration: (a) electrical equivalent circuit, (b) current flowing in the legs and related fluxes.

that consist of a reluctance matrix. By using the duality principle, the solution of the magnetic circuit of Fig. 14 is the same of the dual one reported in Fig. 15.

The voltage MMF generators become current supplies, the flux currents become the flux voltages and the reluctance matrix becomes the permeance matrix. The total flux in each leg around which windings are present can be expresses as

$$\Phi_i = \sum_{j=1}^{N} \mathcal{P}_{ij} \cdot I_{\mathcal{P}i} \tag{21}$$

where N represents the number of legs. At this point, considering (21), the permeance matrix can be translated into inductance matrix, and, hence, impedance matrix, by multiplying by the number of turns of each winding. Hence, the magnetic model of Fig. 15 can be translated in the electric circuit of Fig. 16. The leakage inductances are referred to the primary of the windings, while the magnetizing inductances are stored in the impedance matrix, which take in account the coupling between the legs. The impedance matrix coefficients are calculated by using FEM simulations on the MMTA geometry: in general, this can be evaluated by exciting each winding with a voltage and measuring the induced voltage on the others. By the described procedure, *MMTA transformer design can be effectively tested at circuit level under all working conditions* in terms of saturation and core losses. In fact, the flux magnitude of each leg can be approximately derived from the current level at the port of the multiport model of Fig. 16 described by $\mathcal{Z}$ matrix. The $\mathcal{Z}$ matrix is reported in (22). Indexes 1 and 2 are, respectively, referred to the left and right MMTA legs. The indexes 3 and 4 are, respectively, referred to the right and left inductance legs

$$\mathcal{Z} = sL. \tag{22}$$

The L matrix, evaluated for the prototype of Section V-B with ANSYS Maxwell, is here shown

$$L = \begin{bmatrix} 926.95 & -187.76 & -74.72 & -108.73 \\ -187.76 & 928.09 & -109.52 & -74.42 \\ -74.72 & -109.52 & 513.69 & -35.98 \\ -108.73 & -74.42 & -35.98 & 511.40 \end{bmatrix} \text{nH}. \tag{23}$$

As expected, L is symmetric. To complete the equivalent circuit of the MMTA, its leakage inductances must be evaluated. To extract them, the structure is excited with two currents, as shown in Fig. 17(a). I current flows in both primaries and the sum of the currents $2I$ flows in one secondary: this mimics the RHSC topology operation. The other secondary is short-circuited; its current is determined by the Faraday's law. In this case, the resulting winding currents are shown in Fig. 17(b).

With this excitation, the leakage inductance can be extracted by the total magnetic energy in the FEM domain, resulting in $L_k = 35.8$ nH. For circuit-level simulation, this inductance can be equally split among the two primaries and determines the resonance frequency of the HSC. The result is that for each primary the leakage inductance is 1.9% of the relative leg magnetizing inductance. Winding losses must be included in the equivalent circuit to also simulate damping effects and efficiency. To take into account the winding losses, R_{ac} is added to the MMTA magnetic model. It is calculated in a similar way of the leakage inductance: the excitations are equal to Fig. 17, but in this case the ohmic losses are evaluated. They are described by the formula $P_{\text{loss}} = R_{\text{ac}} I_{\text{rms}}^2$. The overall ac resistance is extrapolated by FEM results, resulting $R_{\text{ac}} = 30.64$ mΩ.

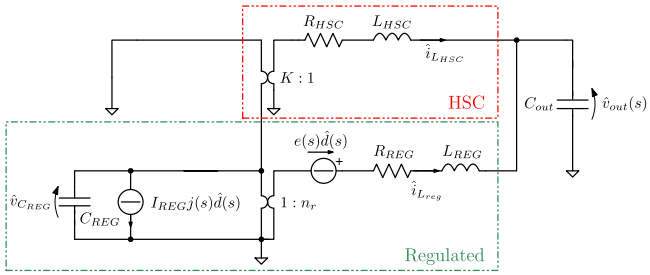

Fig. 18. SSA small-signal model of the proposed converter.

TABLE I
SMALL-SIGNAL TERMS

term	Boost	Buck
L_{REG}	$L/(1-D)^2$	L
$j(s)$	$I_{\text{REG}}/(1-D)^2$	I_{REG}
$e(s)$	$V_{\text{out}}\,(1-sL_{\text{REG}}I_{\text{REG}}/V_{\text{out}})/(1-D)$	V_{out}/D
n_r	$1/(1-D)$	D

IV. SMALL-SIGNAL STATE-SPACE AVERAGING (SSA) ANALYSIS

The frequency behavior of the proposed converter must be known to design the suitable controller of the regulated stage. In this section, the transfer function from duty-cycle to output voltage of all converter is analyzed. The overall small-signal circuit is based on the ISOP connection, demonstrated in the Sections II and III, of the two sub-small-circuits of the regulated converter and the HSC, similar to [20], as shown in Fig. 18. The HSC can be considered as an ideal fixed ratio transformer with its total output impedance referred to the secondary, the regulated converter dynamics is described by the canonical SSA small-signal model, in Table I.

Inductance and resistance parameters in Fig. 18 are extrapolated from previous analysis. The resistance is function of the ohmic losses of the unregulated topologies and the equivalent inductance depends on the total leakage inductance, which resonates with the C_{res} capacitors. As in [20], the equivalent inductance can be evaluated by the formula

$$L_{\text{HSC}} = \frac{\pi^2}{4\,K^2} L_k \tag{24}$$

where L_k is the total leakage inductance evaluated in Section III-A. As described the Sections II and III, the regulated converter input current is alternatively supplied by the two identical capacitors C_{s_1} and C_{s_2} of Fig. 7. According to the waveforms in Figs. 8 and 4, the regulated converter is operating at the double of frequency f_{sw}, therefore, in the first half of the period T_{sw} is taking charge from C_{s_1} and in the second half is taking charge from C_{s_2}. Applying the SSA in T_{sw}, this can be translated to a regulated converter, which is operating at double duty cycle and with the two reservoir capacitor in parallel. Therefore, the equivalent input capacitor C_{REG} in the Fig. 18 is equal to twice the clamp capacitor C_s

$$C_{\text{REG}} = 2C_s. \tag{25}$$

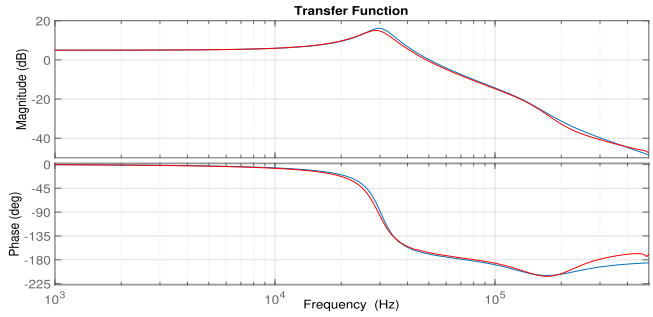

Fig. 19. Hugh step-down RHSC transfer function. Red: circuit simulation; blue: small-signal transfer function.

The transfer function between the output voltage $\hat{v}_{\text{out}}(s)$ and duty cycle $\hat{d}(s)$ is derived from the dynamic system's state equations of Fig. 18 scheme, where the state variables vector is

$$\mathbf{x} = \begin{bmatrix} \hat{v}_{\text{out}} & \hat{v}_{C_{\text{REG}}} & \hat{i}_{L_{\text{REG}}} & \hat{i}_{L_{\text{HSC}}} \end{bmatrix}^T$$

and the input is the duty cycle $\hat{d}(s)$, present in terms of current and voltage generators of Fig. 18.

The transfer function between output voltage $\hat{v}_{\text{out}}(s)$ and $\hat{d}(s)$ can be calculated using the following equation:

$$\frac{\hat{v}_{\text{out}}}{\hat{d}}(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} \tag{26}$$

where A, B, C are derived from the circuit state matrices of circuit of Fig. 18

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & \frac{1}{C_{\text{out}}} & \frac{1}{C_{\text{out}}} \\ 0 & 0 & \frac{1}{KC_{\text{REG}}} & -\frac{D}{C_{\text{REG}}} \\ -\frac{1}{L_{\text{HSC}}} & -\frac{1}{KL_{\text{HSC}}} & -\frac{R_{\text{HSC}}}{L_{\text{HSC}}} & 0 \\ -\frac{1}{L_{\text{REG}}} & \frac{D}{L_{\text{HSC}}} & 0 & -\frac{R_{\text{REG}}}{L_{\text{HSC}}} \end{bmatrix} \mathbf{B} = \begin{bmatrix} 0 \\ -\frac{j(s)}{C_{\text{REG}}} \\ 0 \\ \frac{e(s)}{L_{\text{REG}}} \end{bmatrix}$$

and $\mathbf{C} = [1\,0\,0\,0]$. The transfer function has four complex poles, due to the presence of four independent state variables (L_{HSC}, L_{REG}, C_{out}, and C_{REG}). An approximation of the frequency of the first complex poles, reported in (27), can be derived from the equivalent circuit of Fig. 18 by considering the impedance composed by L_{HSC} and R_{HSC} negligible

$$f_{cc_1} \cong \frac{n_r + 1/K}{2\pi\sqrt{C_{\text{REG}}L_{\text{REG}} + C_{\text{out}}L_{\text{REG}}/K^2}}. \tag{27}$$

The other complex poles of the transfer function are present at high frequency together with a pair of conjugated complex zeros, which make the converter controllable as a normal boost or buck converter, respectively, for the case of Sections II and III. For example, the frequency behavior of (26) in the case of Section III is shown in Fig. 19, where $V_{\text{out}} = 5.1$ V, $I_{\text{out}} = 30$ A, $D = 0.792$, $C_{\text{out}} = 1.1$ mF (where the equivalent series resistance ESR is added), $C_{\text{REG}} = 57.6$ μF, $R_{\text{REG}} = 16$ mΩ, $R_{\text{HSC}} = 1.14$ mΩ, $L_{\text{HSC}} = 1.38$ nH, $L_{\text{REG}} = 300$ nH. As

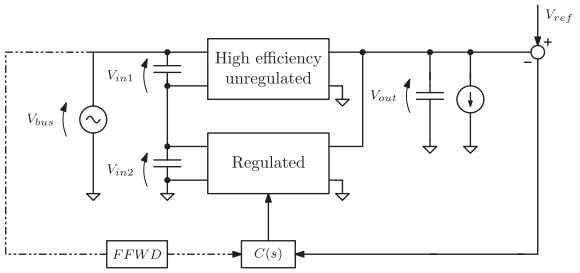

Fig. 20. Control block scheme for a generic sigma converter.

reported in Fig. 19, the transfer function (blue line) of the all sigma converter is similar to a buck with a resonance frequency at $f_{\text{res}} = 25.7$ kHz close to the frequency predicted by (27). The simulation of the proposed converter was performed also through the SIMetrix/Simplis software, which enables ac and transient analysis. The results are also reported in Fig. 19 (red line) in order to get a confirm of the small-signal model derived previously. The control adopted for the proposed converter can be equivalent to a classical voltage mode. The only difference is regarding the modulation, which imposes a duty cycle of less than 50% for the two phases Φ_{HS1} and Φ_{HS2}. Note that when the two phases reach 50% the buck equivalent duty cycle D is 100%.

Voltage regulation is achieved through PID controller, implemented digitally. For this analysis, the PID was converted from the discrete to the continuous domain. The overall block scheme is shown in Fig. 20, with the voltage partition in the output. Subsequently, G_{loop} evaluation is essential to extract significant characteristics of the system, i.e., the bandwidth, the phase margin, and the closed-loop output impedance. The PID parameters are chosen to achieve stability (related to gain margin and phase margin) and maximum bandwidth. As shown in Fig. 20, a feed-forward block is used when selecting a voltage-mode control, increasing input voltage rejection and flattening the *line-to-output* transfer function $V_{\text{out}}/V_{\text{in}}(s)$. This block can be connected to V_{in} or to the sampled regulated voltage, depending on application requirements and controller specifications.

V. Experimental Results

Two prototypes were built to demonstrate the performance and behavior of the common-ground ISOP (sigma) topologies. Two scenarios were targeted: the first one is a down-solution[1] targeting a high-power and high-density 1.2 kW semiregulated 48–12 V conversion; the second scenario is a high-step-down and high-current application in a tight eighth-brick footprint, addressed with a regulated 48–5.1 V module. Both scenarios aim to satisfy common requirements in high-performance computing, which are mainly power density and high efficiency at full load and *half* load. In scenarios, the digital loads are usually kept close to maximum power, to maintain a high computation density.

[1]The converter is implemented with discrete components directly on the main PCB, i.e., the server board.

TABLE II
Low Step-Down RHSC in a Down-Solution Specifications

V_{in}	40–60 V
V_{out}	12 V nominal (see Fig. 6)
P_{out}	1.2 kW TDP, 2 kW peak
f_{sw}	260 kHz
L (boost)	550 nH
L_{mag} (TX magnetizing)	4 μH
Autotransformer turns	1:1
Size	25×51 mm, TX height 14 mm
Power density	1.06 kW/in^3 @ TDP, 25x51x14 mm volume
Base board	8 layers, 2 oz ext., 3 oz int.
Planar TX	12 layers, 4 oz, DMR51W ferrite
$Q_1^{A,B}$, $Q_3^{A,B}$ (4 per side), $Q_4^{A,B}$	IQE013N04LM6, 40 V, 1.3 mΩ
$Q_2^{A,B}$ (2 per side)	ISZ034N06LM5, 60 V, 3.4 mΩ
Q_5	2×ISK024NE2LM5, 25 V, 2.4mΩ
Q_6, Q_7 (2 per side)	BSZ011NE2LS5I, 25 V, 1.1 mΩ
$C_{res1,2}$ (8 per side)	GRM21BZ71H475ME15
$C_{s1,2}$ (8 per side)	GRM21BR61E226ME44
C_{in}	8×GRM31CZ72A475KE11 2×47 μF, electrolytic
C_{out}	14×GRM31CR71E106KA12 4×GRM21BR61E226ME44 4×560 μF, electrolytic
HSC drivers	4×1EDN7550 + 2×2EDN7524G
Buck drivers	3×NCP81155
Controller	XDPP1100-Q024

A. 48–12 V: Low Step-Down RHSC, 1.2 kW Down-Solution

A low step-down RHSC performing a regulated 12 V conversion has been built in a down-solution occupying a 25 × 51 mm area, with a maximum profile of 14 mm corresponding to the autotransformer profile. The converter has been designed to output a continuous 1.2 kW power in thermal steady state thermal design point (TDP) with a forced air flow. Table II summarizes the characteristics of the solution. The autotransformer is composed of single-turn windings on 4 oz copper, paralleled in an interleaved pattern to reach the desired copper resistance. The center leg has been reduced with respect to the lateral core halved legs, in order to push the full-load efficiency to its maximum.

Adaptive dead-time drivers are used to drive the regulated subconverter MOSFETs. In particular, pass-transistors $Q_4^{A,B}$ and the small rectifier Q_5 (PH_X node) are connected to two drivers, which have the low-side outputs in an AND connection. This allows not only to have adaptive dead-time on this node, but also to directly use signals Φ_A and Φ_B for a fast and robust implementation of this part. Instead, Q_6 and Q_7 (PH_Y node) are directly connected to a single half-bridge driver.

Output capacitance is dominated by the electrolytic capacitors, providing 2.24 mF on the 12 V output. The selection of the output capacitance is mainly determined by stability requirements and also represents the input capacitance of VRMs and peripherals: for an IBC, transient performance is usually not critical and it is preferable to decrease switching frequency in favor of efficiency rather than seeking a high bandwidth.

Fig. 21 shows the converter, on the left, and the surface temperature with a load of 1 kW, 54 V input and forced air cooling (5 m/s air speed). All the power MOSFETs are placed on the TOP side, while the BOTTOM side includes drivers,

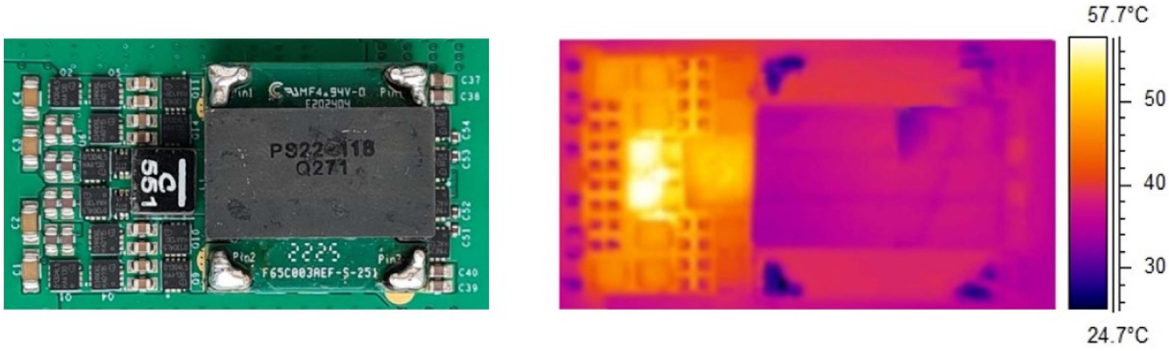

Fig. 21. 1.2 kW 4:1 RHSC prototype in a down-solution (left) and thermal image at $V_{\text{in}} = 54$ V, $f_{\text{sw}} = 260$ kHz, $P_{\text{out}} = 1$ kW, air-cooling at 7 m/s.

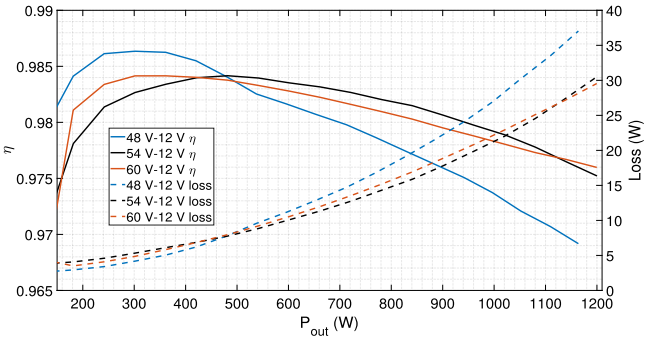

Fig. 22. Efficiency and power loss in the whole power range for three different input voltages. $f_{\text{sw}} = 260$ kHz, air-cooling at 7 m/s, $V_{\text{out}} = 12$ V. Additional bias power: 1.6 W.

Fig. 23. Measured converter waveforms at $V_{\text{in}} = 54$ V, $f_{\text{sw}} = 260$ kHz, $P_{\text{out}} = 1$ kW (conditions on Fig. 21).

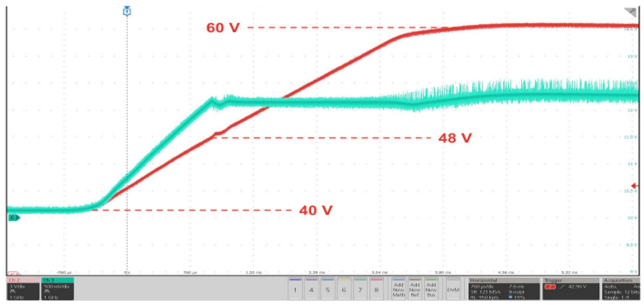

Fig. 24. Input bus transient: V_{in} rises from 40 to 60 V, 5.3 V/ms.

capacitors, and the controller. The autotransformer is an SMD custom component implemented in a planar technology. Efficiency is shown in Fig. 22: full-load efficiency at 54 V input is 97.5 %, while peak efficiency is 98.4 % at the same voltage. The bias power consumption, not included in the efficiency curve, is 1.6 W in the whole conversion range. Also, it must be noted that this prototype has been built for a high full-load efficiency: no-load loss is in fact around 2.5 W, mainly due to core losses.

As shown in the thermal image, a hot-spot exists near the inductor. In particular, this corresponds to PH_X node, which is connected to the hard-switched MOSFETs $Q_4^{A,B}$ and the rectifier Q_5. This area is possibly the most critical to dissipate, as it is in the *core* of the layout and is thermally connected to four different power devices (three MOSFETs and the inductor). A heat spreader can be used to improve heat removal.

Fig. 23 shows the main converter waveforms at 1 kW, 54 V input. At the top, the PWM signals are shown (following the labels of Fig. 8, note that ϕ_b is inverted). In this image, it is clear that the HSC is operating in a high-voltage domain, where PH1 is soft-switching from $2\times V_{\text{out}}$ to 0 V, while the boost subconverter is hard-switching at low voltage. Also, PHX shows the small interval DT and the sigma capacitors voltages, which are equal.

Fig. 24 shows the *line-to-output* behavior of the low step-down RHSC when V_{in} rises and falls. This waveforms show the semiregulation capability of the proposed sigma converter(s), as regulation is achieved for 48 V $\leq V_{\text{in}} \leq$ 60 V. It is also shown that for V_{in} approaching 60 V, i.e., when the conversion ratio is close to 4:1, regulation is also lost: this is due to the *boost* block being close to duty-cycle saturation, which is limited to 98.5% due to bootstrapping requirement. In this situation, Q6 of Fig. 4 is almost-always ON.

B. 48–5.1 V: High Step-Down RHSC, 750 W Eighth-Brick Module

A 750 W prototype for the high step-down RHSC version has been built in an eighth-brick module, targeting the open rack v.3 specifications of the open compute project [13], which fixes a narrow input voltage range of 48–51 V, optimal to maintain this *sigma* topology in its efficiency *sweet spot*. Converter specifications are reported in Table III.

TABLE III
HIGH STEP-DOWN RHSC IN AN EIGHTH-BRICK MODULE SPECIFICATIONS

V_{in}	48–51 V
V_{out}	5.1 V
P_{out}	750 W
f_{sw}	450 kHz
L_{buck} (buck)	300 nH
L_{mag} (magnetizing)	1 μH
N1:N2 (turns ratio)	2:1
Size	58×25×7.6 mm
Power density	1.06 kW/in^3
PCB technology	12 layers, 2 oz ext., 3 oz int.
Core	Custom, DMR51W ferrite
$Q_1^{A,B}$, $Q_2^{A,B}$, $Q_3^{A,B}$, FETs	BSZ040N06LS5, 60 V, 4 mΩ
Q_4, Q_5, Q_6 FETs (4 per phase)	IQE006NE2LM5, 25 V, 600 $\mu\Omega$
Hot swap FETs	2×BSZ040N06LS5, 60 V, 4 mΩ
Buck FETs	25 V, 2.4 mΩ
C_s (6 per phase)	GRM21BR61H106ME43
C_{res} (14 per phase)	GRM21BC81H475KE11
C_{out}	52×GRM21BR61A476ME15
HSC drivers	4×1EDN7550B + 2×2EDN7524G
Buck drivers	2×NCP81155

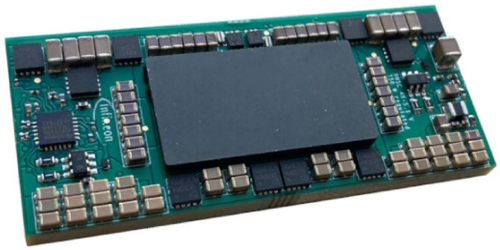

Fig. 25. 750 W, 1/8 brick prototype of the high step-down RHSC.

This module is a stand-alone converter operating as regulated high step-down stage, also embedding hot-swap capability, soft-start, and protections. The HSC multiwinding autotransformer has been embedded with a matrix planar approach to maximize power density, enabling optimal winding interleaving. The buck inductor has also been embedded in the PCB, and the two structures share the same magnetic core. This is clear by observing Fig. 25, where a single magnetic is present. The power brick can be connected to the main board through 24 copper pins, and requires only an additional 12 V auxiliary supply to operate. Power-good and enable signals are also provided, together with PMBUS communication.

Fig. 27 shows converter waveforms at 510 W: the buck phase node (red) shows its double-frequency operation (each *high-side* is turned on during one T_{sw}). The other two node voltages show ZVS operation: the top-field effect transistor (FET) drain (blue) and the synchronous rectifier (green) show the small spike of the leakage energy at the beginning of the commutation, and then they are charged/discharged by the magnetizing energy. Fig. 28 shows the transient response for a wide load step of $\Delta I_{out} =$ 90 A at 7 A/μs, with a measured maximum voltage variation of $|\Delta V_{out}| = 30$ mV.

Efficiency curves at different input voltage are reported in Fig. 29, where peak efficiency is 97.5% at 48 V input. Fig. 26

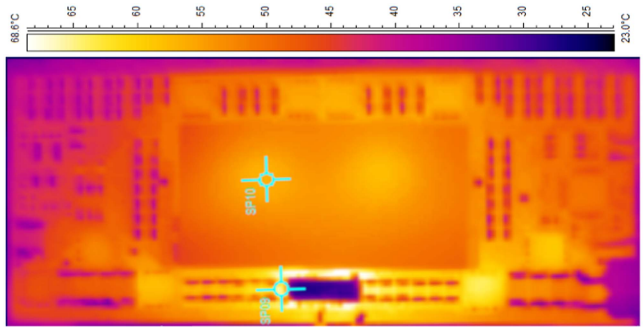

Fig. 26. Thermal image, 100 A output, $V_{in} = 49$ V. Air cooling at 2 m/s.

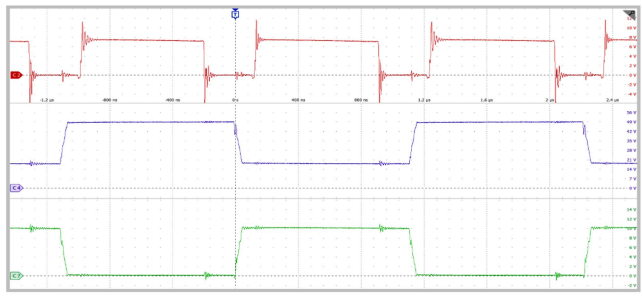

Fig. 27. $V_{in} = 49$ V, $V_{out} = 5.1$ V, $I_{out} = 100$ A. From top to bottom: buck phase node, Q_2 drain, PH_1 node.

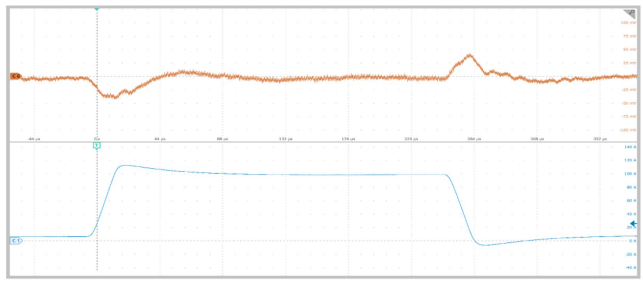

Fig. 28. Transient response. $V_{in} = 49$ V, $V_{out} = 5.1$ V. AC-coupled output voltage (orange), output current (blue). $\Delta I_{out} = 90$ A, 7 A/μs. Maximum measured $|\Delta V_{out}| = 30$ mV.

shows a thermal image at full load, where a hot spot can be identified in the regulated stage area, below an aluminium heat spreader. Efficiency is inversely proportional to input voltage: this behavior can be explained with (20), as buck power share increases from 15% to 18% when V_{in} changes from 48 to 50 V, as the buck is less efficient than the HSC. Moreover, buck efficiency itself is dependent on the input voltage, as this subconverter must withstand increasing input voltage and suffers from increased switching losses. Core losses and, in general, HSC losses, are less dependent on the input voltage: the transformer flux is only dependent on frequency and output voltage, and also ZVS transitions desensitize this subconverter's efficiency from the input. The buck converter, composed by two high-sides, is driven with adaptive dead-times. The driver operates with input signals Φ_{HS1} and Φ_{HS2}: low-side outputs are combined in a power-NOR circuit to generate the gate signal Φ_{LS}, connected to the low-side FET.

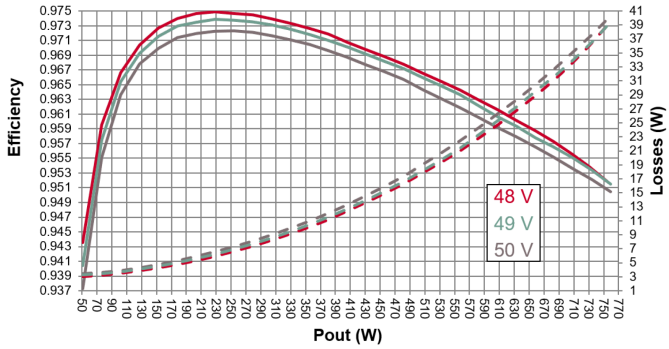

Fig. 29. Efficiency and losses at different input voltages. AUX supply not included.

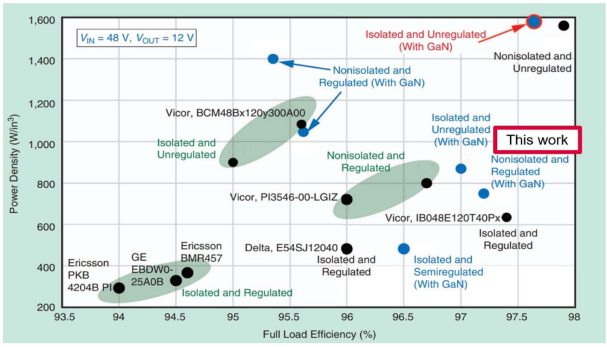

Fig. 30. Low step-down RHSC (48–60 V to 12 V regulated) power density versus full-load efficiency comparison against other topologies [21].

VI. Conclusion

The RHSC is a novel family of sigma/ISOP converters capable of regulation and high power density, which aims to achieve efficiencies similar to and unregulated IBC. The ISOP connection allow us to deliver most of the output power through a high-efficiency converter (HSC), while a regulated block ensures regulation with a fraction of the processed power. Instead of relying on converter isolation, the input-series behavior is here achieved by *sigma* capacitors, alternatively in series with a resonant current and then used as voltage supply for the regulated block: this technique ultimately enables power density increase, as the removal of functional isolation corresponds to electrical current flow from primary to secondary sides, better winding interleaving and relaxed design constraints. Now, both converters are referenced to the same GND domain, further easing driving design. Two prototypes show RHSC performances in two scenarios: a 48–12 V down-solution and a 48–5.1 V module, both exceeding a power density of 1 kW/in^3. Fig. 30 clearly demonstrates the capability of the 48–12 V down-solution (low step-down RHSC) in today's data center power conversion landscape. In high-power applications, full-load efficiency and power density are often the most important factors. The use of RHSC enables a (semi)regulated IBC and maintains a high efficiency, which is a benefit for the VRM stage.

References

[1] P. Sandri, "Increasing hyperscale data center efficiency: A better way to manage 54-V48-V-to-point-of-load direct conversion," *IEEE Power Electron. Mag.*, vol. 4, no. 4, pp. 58–64, Dec. 2017.

[2] S. Oliver, "From 48 V direct to intel VR12.0: Saving 'Big Data' 500,000 per data center, per year," Jul. 2012. [Online]. Available: https://www.mouser.jp/pdfdocs/wp_VR12.pdf

[3] Open Compute Project (OCP), "Google 48 V rack adaptation and on-board power technology update," 2019. [Online]. Available: https://www.youtube.com/watch?v=aBkz2JR4UVs

[4] Y. Ren, M. Xu, J. Sun, and F. Lee, "A family of high power density unregulated bus converters," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1045–1054, Sep. 2005.

[5] K. Radhakrishnan, M. Swaminathan, and B. K. Bhattacharyya, "Power delivery for high-performance microprocessors–challenges, solutions, and future trends," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 11, no. 4, pp. 655–671, Apr. 2021.

[6] IEEE Spectrum, "Cerebras'S Giant Chip Will Smash Deep Learning's Speed Barrier," 2020. [Online]. Available: https://spectrum.ieee.org/cerebrass-giant-chip-will-smash-deep-learnings-speed-barrier

[7] Open Compute Project (OCP), "OCP virtual summit 2020: Survey of 48 V to 12 V architectures for on board DCDC conversion," 2020. [Online]. Available: https://youtu.be/Z_F3-x-Pr74

[8] M. H. Ahmed, F. C. Lee, and Q. Li, "Two-stage 48-V VRM with intermediate bus voltage optimization for data centers," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 702–715, Feb. 2021.

[9] Z. Ye, Y. Lei, and R. C. N. Pilawa-Podgurski, "The cascaded resonant converter: A hybrid switched-capacitor topology with high power density and efficiency," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4946–4958, May 2020.

[10] C. Li and J. A. Cobos, "A switched capacitor and autotransformer hybrid converter with dc current in the windings," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1870–1884, Feb. 2022.

[11] Y. Lei and R. C. N. Pilawa-Podgurski, "A general method for analyzing resonant and soft-charging operation of switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5650–5664, Oct. 2015.

[12] S. Jiang, S. Saggini, C. Nan, X. Li, C. Chung, and M. Yazdani, "Switched tank converters," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5048–5062, Jun. 2019.

[13] Open Compute Project, "Open rack V3 48 V PSU specifications," 2020. [Online]. Available: http://files.opencompute.org/oc/public.php?service=files&t=fcb65624c9c2e05644f486e44a280809

[14] J. Sun, M. Xu, D. Reusch, and F. C. Lee, "High efficiency quasi-parallel voltage regulators," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2008, pp. 811–817.

[15] M. Xu, Y. Liu, J. Sun, and F. C. Lee, "Sigma dc/dc conversion for computing and telecom applications," in *Proc. IEEE Power Electron. Specialists Conf.*, 2008, pp. 1190–1195.

[16] M. H. Ahmed, C. Fei, V. Li, F. C. Lee, and Q. Li, "Startup and control of high efficiency 48/1V sigma converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 2010–2016.

[17] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "Single-stage high-efficiency 48/1 V sigma converter with integrated magnetics," *IEEE Trans. Ind. Electron.*, vol. 67, no. 1, pp. 192–202, Jan. 2020.

[18] M. Ursino, R. Rizzolatti, G. Deboy, S. Saggini, and K. Zufferli, "High density hybrid switched capacitor sigma converter for data center applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 35–39.

[19] R. Rizzolatti, C. Rainer, S. Saggini, and M. Ursino, "Ultra-low profile hybrid switched capacitor converter with matrix multi-tapped autostransformer," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 869–874.

[20] V. Li, M. H. Ahmed, Q. Li, and F. C. Lee, "Modeling and control of sigma converter for 48v voltage regulator application," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 1199–1204.

[21] M. H. Ahmed, M. A. de Rooij, and J. Wang, "High-power density, 900-W LLC converters for servers using GAN fets: Toward greater efficiency and power density in 48 V to 612 V converters," *IEEE Power Electron. Mag.*, vol. 6, no. 1, pp. 40–47, Mar. 2019.