Letters

Online Junction Temperature Extraction With Gate Voltage Under Nontrigger Current for High-Voltage Thyristor

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***Abstract*—This letter proposes a junction temperature (T_j) extraction method for the high-voltage thyristors with the cathode short-circuiting structure. It has been studied that the gate voltage V_{gk} under nontrigger current is a practical temperature-sensitive electrical parameter (TSEP), which can be used for online T_j monitoring by calibrating the linear relationship between the gate voltage V_{gk} under nontrigger current and T_j effect. The proposed TSEP does not affect the operating state of the thyristor and is suitable for complex operating conditions since it is extracted during OFF state. The total error in the T_j estimate obtained from the proposed TSEP is verified within ± 2 °C by comparing with the T_j obtained from the traditional gate voltage V_{GK} based TSEP during ON state.**

***Index Terms*—Cathode short-circuit, gate nontrigger current, gate voltage, junction temperature, thyristor.**

I. Introduction

HIGH-VOLTAGE direct current (HVdc) transmission has significant technical and economic benefits for long-distance and large-capacity transmission applications. Currently, the thyristor converter valve remains the dominant converter valve technology for HVdc transmission, owing to its unparalleled voltage resistance and the maximum output capacity among all single-device power electronic components. The Jinping–Sunan ultra HVdc transmission project has a rated voltage of ±800 kV and a rated current of 4.5 kA, where the adoption of 7.2 kV/4500 A thyristor technology has been applied [1].

Manuscript received 3 April 2023; revised 29 May 2023; accepted 14 June 2023. Date of publication 22 June 2023; date of current version 28 July 2023. This work was supported in part by the National Science Foundation of China under Grant 52107211, in part by the "Pioneer" and "Leading Goose" R&D Program of Zhejiang under Grant 2022C01094, and in part by the Natural Science Foundation of Hebei Province (Science Foundation for Distinguished Young Scholars) under Grant E2021202164. *(Corresponding author: Haoze Luo.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3288675.

Digital Object Identifier 10.1109/TPEL.2023.3288675

According to the reliability research report on power electronic systems, the failure rate of power devices is the highest in the converter system, which accounts for around 31% [2]. Among the various failure factors, about 55% of power electronic system failures are induced by temperature factors [3], [4]. Therefore, online extraction of thyristor T_j is essential to ensure the safe and reliable operation of the thyristor converter valve, even the entire HVdc transmission system.

Traditionally, thyristor T_j is measured by the thermal network model method [5], [6], [7]. To address the challenge of thyristor transient T_j extraction, a thermal model for estimating the thyristor transient T_j is proposed, which has the advantage of simple model parameters extraction [6]. However, this model can only analyze the transient T_j in the case of a single pulse current. To study the thermal behaviors of thyristors in pulsed power applications, a thermal calculation model including an electrothermal model and a finite-element model has been developed [7]. But, the contact thermal resistance in the internal components of press-pack power devices accounts for around 50% of the total thermal resistance, and it decreases as pressure increases on both sides of the device [8], [9]. Hence, the thermal network model method to estimate thyristor T_j is still inaccurate, as it does not account for the influence of pressure. Meanwhile, the response speed of the thermal network model is slow. The time constant of the thermal network model of the thyristor KP03XY7200 is 0.7485 s. Another traditional method for measuring T_j is the temperature-sensitive electrical parameter (TSEP) method, which involves the ON-state voltage of the thyristor and the gate voltage during the ON state [10], [11], [12]. However, the thyristor is blocked with several thousand volts and on with only a few volts, which results in a wide range of voltage variations and makes it difficult to measure the ON-state voltage. Additionally, the ON-state gate voltage V_{GK} is affected by parameters, such as drive current, ON-state current, and T_j, which is unrealistic to adapt to the complex operating conditions of thyristors for online T_j monitoring.

Therefore, this letter proposes a T_j extraction method with the gate voltage under nontrigger current to solve the problems of traditional TSEPs. The gate voltage V_{gk} parameter under nontrigger current is linearly related to T_j, which has the advantages of uninterrupted the thyristor operating state and only depending on the T_j and the nontrigger current. It can

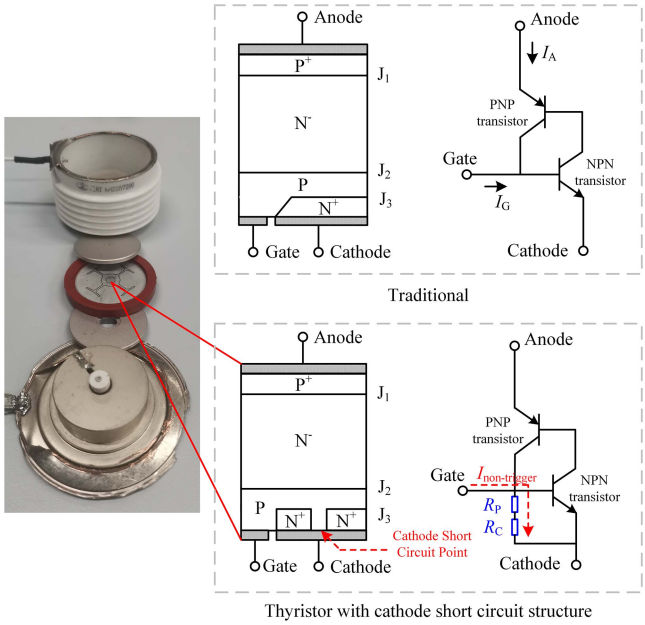

Fig. 1. Internal structure and equivalent circuit of traditional thyristor chip and thyristor chip with cathode short-circuit structure.

be used to monitor the online thyristor T_j without interrupting operation.

II. Relationship Between T_j and Gate Voltage Under Nontriggered Current

A. Thyristors With Cathode Short-Circuit Structure

In Fig. 1, the thyristor chip is composed of a four-layer p-n-p-n structure, which can be equated to a case of two transistors, PNP and NPN. The internal equivalent circuit of the thyristor is depicted in Fig. 1.

The turn-on voltage of a thyristor determines its forward-blocking capability when in a forward-blocking state. When the multiplication factor M_p of the hole current in the PNP transistor and the multiplication factor M_n of the electron current in the NPN transistor are considered, the expression for the anode current can be obtained when the thyristor reaches turn-on voltage as follows:

$$I_A = \frac{M_{SC} I_{SC} + M_p I_{p0} + M_n I_{n0}}{1 - (M_p \alpha_1 + M_n \alpha_2)} \tag{1}$$

where α_1 is the common base current gain of PNP-type transistor. α_2 is the common base current gain of NPN-type transistor. I_{p0} is the diffusion leakage current of light-doped N^- layer. I_{n0} is the diffusion leakage current in P base region. M_{sc} is the multiplier factor of reverse current in the space charge region at J_2 junction. I_{sc} is the reverse current of the space charge region at J_2 junction.

The turn-on voltage is reached when $M_p\alpha_1 + M_n\alpha_2 = 1$. Since $M_n \gg M_p$, the turn-on voltage is highly sensitive to α_2. Thus, to ensure that the forward- and reverse-blocking capacity of the thyristor are the same at low currents, α_2 should be set to 0, which can be achieved by a cathode short-circuit structure. The cathode

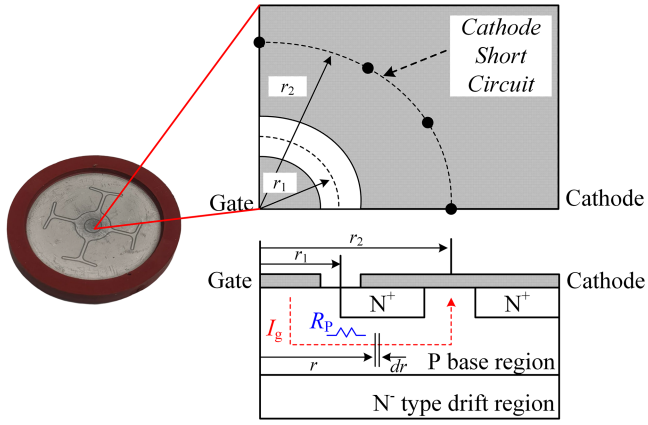

Fig. 2. Thyristor structure with the gate in the center of the chip and concentric with the cathode short structure.

short-circuit is implemented on the thyristor chip itself, where the N^+ cathode region and P base region are short-connected through a cathode metal electrode, as shown in Fig. 1. The body resistance R_P and contact resistance R_C of the P base region form two shunt resistances between the thyristor's gate and cathode, thus reducing the α_2 purpose. The internal structure and equivalent circuit of the thyristor chip with the cathode short-circuit are illustrated in Fig. 1.

B. Relationship Between Gate Voltage V_{gk} Under Nontrigger Current and T_j

When a nontrigger current is injected into the gate of the thyristor with the cathode short-circuit structure, the small current flows through the shunt resistors R_P and R_C between the gate and cathode, as shown in the dashed path in Fig. 1. The voltage generated on the thyristor gate is less than the trigger voltage, so the thyristor is in a blocked state.

The body resistivity of the P base region semiconductor can be expressed as [13]

$$\rho_p = \frac{1}{q\mu_p N_p} \tag{2}$$

where q is the absolute value of the electron charge. μ_p is the hole mobility. N_p is the doping concentration. When the N_p is less than 10^{15} cm^{-3}, the mobility of holes in a silicon-based semiconductor material can be expressed as [13]

$$\mu_p = 495\left(\frac{T_j}{300}\right)^{-2.20}. \tag{3}$$

From (2) and (3), it is clear that when N_p is constant, the P base region body resistivity is a function of T_j. The T_j here refers to the thermodynamic temperature.

As shown in Fig. 2, since the thyristor chip is almost all circular, the body resistance of the P base region can be expressed as

$$R_P = \int_{r_1}^{r_2} \frac{\rho_p}{2\pi}\frac{dr}{r} = \frac{\rho_p}{2\pi}\ln\left(\frac{r_2}{r_1}\right). \tag{4}$$

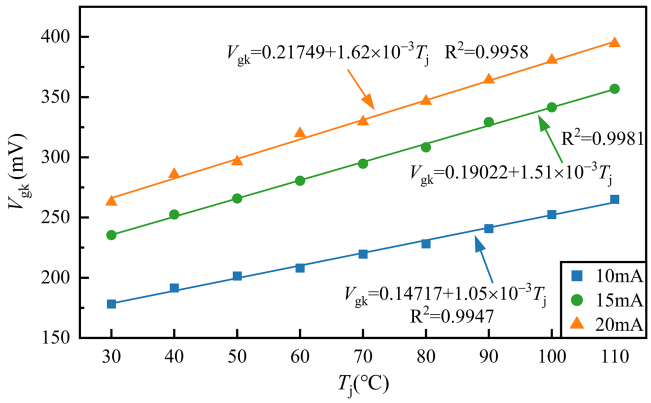

Fig. 3. Dependence of gate voltage V_{gk} on temperature under different nontrigger currents.

It is worth noting that (4) represents the lateral resistance of the P base region, but the P base body resistance also includes the vertical resistance between the two N^+ regions. The vertical resistance value is significantly lower than the lateral resistance value and can be neglected because the thickness of the N^+ region is much smaller than the length of the P base region [14].

Therefore, when the gate is injected with a constant small nontrigger current I_g, the voltage on the P base region body resistance can be expressed as

$$V_P = I_g \cdot R_P = I_g \cdot \frac{1}{2.79 \times 10^8 \bullet \pi q N_p} \bullet T_j^{2.20} \bullet \ln\left(\frac{r_2}{r_1}\right). \tag{5}$$

From the above equation, when constant I_g is injected into the gate, V_P is a function of T_j and proportional to T_j.

The typical contact resistance in power device structures is less than 1×10^{-5} Ω·cm^2. The resistivity of P-type base semiconductors ranges from 0.1–10^5 Ω·cm [13]. Therefore, the voltage of the body resistance R_P is much larger than that of the contact resistance R_C. Consequently, V_C can usually be neglected. Hence, the gate voltage V_{gk} is approximately equal to V_P when a constant nontrigger I_g current is injected into the gate. As a result, the gate voltage V_{gk} under nontrigger current is a function of T_j and can be used as a TSEP candidate. Fig. 3 depicts the relationship between gate voltage V_{gk} and T_j for different nontrigger currents.

Equation (5) is derived based on (3), which only applies to lightly doped P-type semiconductors with N_p less than 10^{15} cm^{-3}. However, the N_p of the P base region in a thyristor is generally between 10^{16}–10^{17} cm^{-3}. Thus, (5) indicates that there is a certain relationship between them. In practice, this relationship can be calibrated in advance for the following application. This monotonous relationship between V_{gk} and T_j depends on the function fitting of the data obtained from the T_j calibration process, as shown in Fig. 3.

The OFF-state leakage current of the thyristor is essentially caused by the leakage current of the J_2 junction (forward-biased thyristor) or the J_1 and J_3 junctions (reverse-biased thyristor) inside the thyristor. Hence, the magnitude of the leakage current is influenced by the thyristor voltage and T_j [15]. The nontrigger current injected into the gate only flows through the P base region and does not pass through J_1, J_2, or J_3. At the same time, the nontrigger current is set to 20 mA. Even in the most extreme case (T_j = 110 °C), the power loss generated by the nontrigger current is only 7.889 mW, so its self-heating effect can be ignored. Therefore, the nontrigger current does not increase the OFF-state leakage current between the anode and cathode.

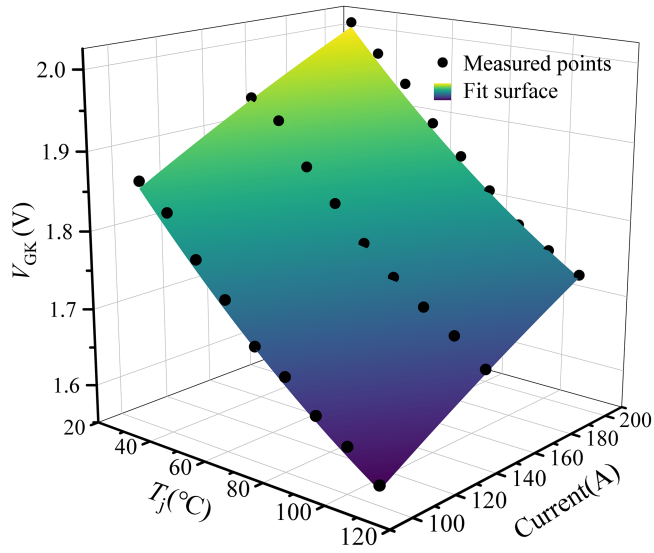

Fig. 4. Dependence of gate voltage V_{GK} on temperature under different ON-state currents.

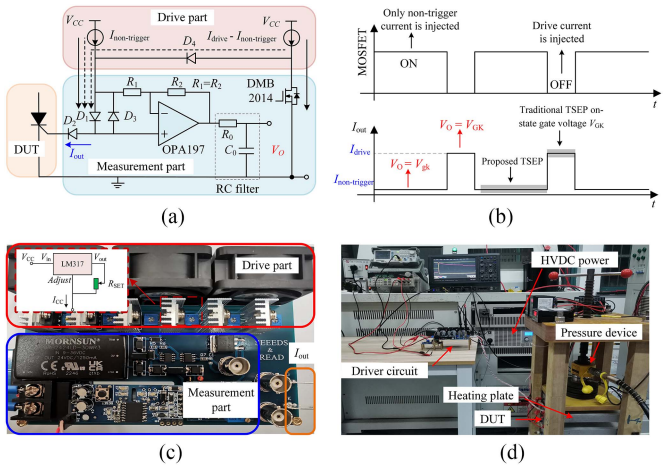

Fig. 5. Driver circuit with gate voltage measurement: (a) schematic diagram; (b) timing diagram; (c) PCB board; and (d) experimental platform.

III. T_j Extraction Approach

A. T_j Calibration With ON-state Gate Voltage V_{GK} TSEP

In the calibration test, the thyristor T_j was adjusted using double-sided heating plates. After 20 min of steady heating, the thyristor T_j is equal to the heating plate temperature T_h. The T_j calibration curve of a 7.2 kV/300 A thyristor KP03XY7200 was tested, and the hardware circuit is shown in Fig. 5(d).

As shown in Fig. 1, there is a PN junction (J_3) between the gate and cathode of the thyristor. The forward voltage drop of

a single PN junction has a negative temperature coefficient and exhibits a linear decrease with increasing T_j within a certain temperature range [16]. Therefore, the traditional TSEP of a thyristor is ON-state gate voltage V_{GK} and the J_3 junction voltage drops [11]. The V_{GK} requires the thyristor to be in the ON-state during T_j calibration. However, the power loss of the thyristor is high due to the large ON-state current, resulting in a severe self-heating effect on the thyristor. The self-heating effect can cause the actual T_j to be different from the set temperature of the double-sided heating plate, which seriously affects the accuracy of the T_j calibration results. In this letter, the average value of gate voltage in the conduction range of 290–300 μs is chosen to reduce the effect of self-heating. For different ON-state currents and T_j during conduction, the relationship between gate voltage V_{GK}, current I, and T_j is shown in Fig. 4. The analytical model between gate voltage V_{GK}, current I, and T_j is created by the polynomial surface fitting algorithm, which can be expressed as

$$V_{\mathrm{GK}} = z_0 + a \cdot T_j + b \cdot I + c \cdot T_j^2 + d \cdot I^2 + f \cdot T_j \cdot I \quad (6)$$

where $z_0 = 1.81488$, $a = -5.26 \times 10^{-3}$, $b = 2.03 \times 10^{-3}$, $c = 1.15923 \times 10^{-5}$, $d = -1.80284 \times 10^{-6}$, and $f = 6.57557 \times 10^{-7}$. These coefficients were obtained based on the experimental results.

B. Proposed Driver Circuit With Gate Voltage Measurement

Both the proposed TSEP gate voltage V_{gk} under nontrigger current and the ON-state gate voltage V_{GK} are required to measure the gate voltage for the T_j database. Hence, the gate voltage measurement function needs to be integrated into the thyristor drive circuit. The gate voltage V_{gk} under nontrigger current is less than the trigger voltage, while an average gate voltage V_{GK} of 290–300 μs is taken to avoid the self-heating effect. Thus, the gate voltage measurement circuit should meet several requirements: high accuracy in the mV range, rapid dynamic response in the μs range, and the ability to inject both drive and nontrigger currents into the gate. Fig. 5(a) illustrates that the driver circuit can both drive the thyristor and measure the gate voltage (V_{gk} and V_{GK}). When the power MOSFET DMB2014 is in the OFF state, both the drive current and the nontrigger current of the thyristor are injected into the gate simultaneously, which results in the thyristor being in a conduction state, as shown in the dashed path in Fig. 5(a). When the power MOSFET is in the ON state, the MOSFET provides a bypass branch for the drive current, and only the nontrigger current is injected into the gate, as shown in the solid line path in Fig. 5(a). The gate voltage of the thyristor can be monitored in real-time by injecting either drive or nontrigger currents. Fig. 5(b) displays the timing diagram that illustrates the operation of the thyristor drive circuit. To eliminate the reverse voltage of D_1 and protect the operation amplifier, an anti-parallel diode D_3 is used. The operation amplifier used in this circuit is an OPA197, which has a low offset and low bias current (±5 pA typical). Additionally, D_1, D_2, and D_3 are the same types, which are low-power SiC Schottky diodes GB02SLT12-214 with fast recovery characteristics. The drive current and nontrigger current can be generated by the voltage regulator chip and its output resistance, such as LM317. When LM317 is operating normally, the voltage at the V_{out} and *Adjust* terminals will be maintained at a stable value of 1.25 V. Hence, the output current of the voltage regulator chip can be adjusted by changing the resistance value of the resistor R_{SET} connected in series between V_{out} and *Adjust*. The hardware circuit of the drive circuit is shown in Fig. 5(c).

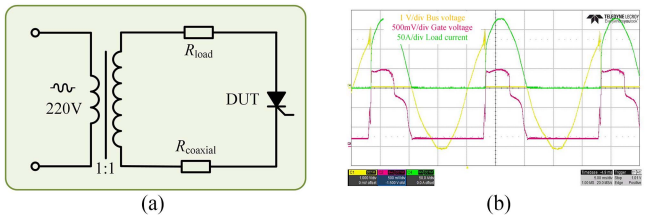

Fig. 6. Single-phase half-wave rectifier circuit: (a) schematic diagram; and (b) experimental waveform.

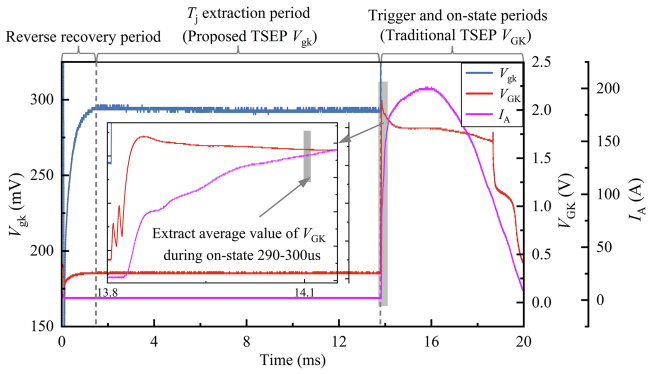

Fig. 7. Time sequence diagram for T_j extraction in a single cycle.

IV. Experimental Verification

In Fig. 6(a), a single-phase half-wave rectifier circuit was used to verify the feasibility of the proposed method. The circuit operated with an RMS bus voltage of 220 V and a load resistance of 1.8 Ω that has a rated power of 20 kW. The nontrigger current and drive current were chosen as 20 and 200 mA, with a trigger angle α of 60°.

The test waveform was periodic as shown in Fig. 6(b), and the following is a specific analysis of T_j online monitoring with one cycle of test data. A switching cycle can be divided into three phases: the reverse recovery period, the T_j extraction period, and the trigger and ON-state periods, as shown in Fig. 7. The T_j extraction period is from the end of the reverse recovery to the next trigger.

To provide a reference T_j for the thyristor, the gate voltage V_{GK} during the ON-state of the traditional used TSEP was selected as the reference. The T_j obtained by the gate voltage V_{GK} based on the relationship between V_{GK} and T_j presented in Fig. 4 was selected for comparison with the lowest T_j obtained by the average gate voltage V_{gk} of 10 μs before the end of the T_j extraction period under the nontrigger current. A comparison of the T_j obtained by inversion of the two TSEPs at different T_h is shown in Table I, while Fig. 8 shows the T_j variation curve.

TABLE I
JUNCTION TEMPERATURE COMPARISON RESULTS

T_h	T_j	TSEP	ΔT_j
30 °C 50 °C	46.56 °C 65.18 °C	Average value of 10μs V_{gk} before the end of the T_j extraction period	-1.84 °C (T_h = 30 °C)
30 °C 50 °C	48.40 °C 63.51 °C	Average value of V_{GK} during the on-state period 290-300μs	1.67 °C (T_h = 50 °C)

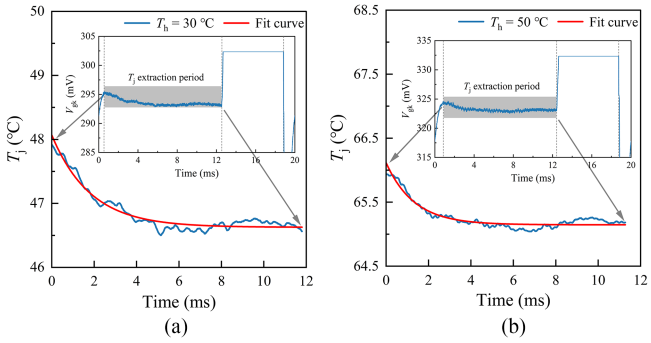

Fig. 8. T_j curve of thyristor obtained by V_{gk} during T_j extraction period at different T_h: (a) 30 °C and (b) 50 °C.

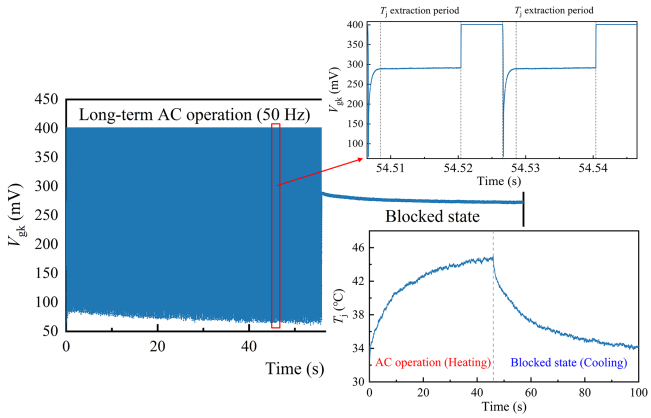

Fig. 9. Gate voltage V_{gk} and T_j fluctuation curve in long-term load cycling test under ac conditions (50 Hz).

To verify the proposed T_j extraction method, a long-term load test was conducted, which operated for 56 s in ac operation followed by 44 s of blocked cooling, as shown in Fig. 9. The amplified waveform of the gate voltage is shown in the top right corner. Data processing was carried out to eliminate invalid data from the reverse recovery and ON-state periods. Then, the V_{gk} during the T_j extraction period was used to invert the T_j rise curve under operating conditions, and the V_{gk} in the blocked state can directly invert the cooling curve, depicted in Fig. 9.

V. CONCLUSION

A method for online extraction of T_j was proposed for high-voltage thyristors with the cathode short-circuiting structure. The theoretical and experimental results show that there exists a linear relationship between gate voltage V_{gk} and T_j under non-trigger current. The proposed drive circuit provides both drive and continuous nontrigger currents, while also being capable of measuring the thyristor gate voltage in real-time operation. During the T_j extraction period, the gate voltage V_{gk} was used to monitor the thyristor T_j in the OFF state. Compared with the traditional TSEP based ON-state gate voltage V_{GK}, the measurement error of T_j is within ±2°C and it is more suitable for complex operation conditions. The proposed method does not affect the thyristor operating states and is only influenced by the T_j and nontrigger current amplitude. Based on the continuous testing, the TSEP proposed in this letter can monitor dynamic changes of thyristor T_j, which can significantly enhance the operation reliability of thyristors in applications.

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