Efficiency Optimization and Control Strategy of Four-Switch Buck–Boost Converter for Wide Conversion Ratio

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***Abstract*—An improved control strategy for the four-switch buck–boost (FSBB) converter is proposed to improve the efficiency in a wide conversion ratio and wide loads. The conventional duty-cycle-controlled FSBB converter cannot achieve the zero voltage switching (ZVS) for all the switches while the converter has a dead zone issue. The proposed control strategy is controlled by the duty cycle and phase shift control. The control law is derived from the analytical solution of the optimized current stress with the constraint of the ZVS for all the switches. The working modes in the proposed control strategy can cover the whole load in a wide conversion ratio. Furthermore, the dead zone issue is removed. The modulation surface and output power surface versus the conversion ratio and control variable demonstrate the working modes are switched seamlessly. The control strategy is implemented in the digital controller. Finally, the experimental results verify the higher efficiency and dynamic performance of the control strategy.**

***Index Terms*—Duty cycle plus phase shift control, optimized current stress, wide conversion ratio, zero voltage switching (ZVS).**

I. Introduction

POWER electronics converters powered by batteries and fuel cells need a wide conversion ratio because of the wide voltage of the power source. The nonisolated buck and boost converters are still prevalent converters due to the simple topology and few components. Compared with the conventional buck, boost, and buck–boost converters, the four-switch buck–boost (FSBB) converter possesses a wide conversion ratio, high efficiency, and noninverting power conversion [1].

However, the turn-ON delay or the limitation of the duty cycle in the FSBB converter will cause a dead zone issue when the input voltage is close to the output voltage [2]. It creates poor output voltage regulation and potential instability. This issue becomes more serious in the analog pulsewidth modulator [3]. In [4], a nonlinear state machine is introduced to solve this dead zone issue. A control strategy with adaptive effective switching frequency is proposed to improve the efficiency in the dead zone [5]. Multiple working mode sections can improve the output voltage regulation capacity in the dead zone operation area, where the converter works in buck–boost mode [6], [7]. To improve the mode transition response, the transition strategy with intermediate combination modes is utilized to distribute the voltage transition [8]. The open-loop frequency response for the FSBB in the buck, boost, and buck–boost modes is different. The control strategy based on the linear parameter varying system model can improve the dynamic response in a wide conversion ratio [9]. The aforementioned FSBB converters work in the continuous conduction mode (CCM). The inductor current ripple is very low. The key concern for the FSBB in the CCM is the dead zone issue and the dynamic response. In the CCM, some switches work in hard switching, which causes more switching loss. When the input voltage deviates from the output voltage, the large switching loss, conduction loss, and core loss in the series inductor will lower the efficiency. Aforementioned research works are concentrated on the control strategy rather than the efficiency improvement.

To reduce the switching loss, the critical regulation mode (CRM) control is utilized in the conventional buck and boost converters [10], [11], [12]. The output voltage and zero voltage switching (ZVS) constraints are regulated by both the duty cycle and switching frequency. An FSBB converter with CRM control is applied to the onboard battery charger for plug-in electric vehicles [13]. It also works in the buck, buck–boost, or boost mode to solve the dead zone issue [13], [14]. In all the working modes, the converter works in the CRM for the ZVS of all the switches. However, the efficiency in the buck–boost mode is very low because of the large current stress. For the wide loads, the switching frequency will be varied in a very wide range, which makes the difficulty in electromagnetic compatibility (EMC) design.

A modulation scheme with more degrees of freedom is proposed for the FSBB by regulating the duty cycle and phase shift angle of the two half-bridges [15]. The control strategy is based on the numerical solution by optimizing the conduction loss and the ZVS constraints. In the boost mode, one switch still works in hard switching. Whether the control strategy can achieve a seamless transition between the buck and boost mode cannot be derived from the numerical solution. A high-efficiency control strategy for the FSBB converter in energy storage systems is

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proposed in [16]. The output is adjusted by the duty cycles of the two half-bridges, the switching frequency, and the phase shift angle. The duty cycles of the two half-bridges are the same. The root-mean-square (rms) current of the series inductor can be designed as the optimal objective to improve efficiency [17]. The control strategy is also derived from the numerical solution of the discrete load power and conversion ratio. The numerical solution can facilitate the design of the control strategy. However, the lookup table derived from an offline calculation should be stored in the digital controller. By using the linear interpolation method, the real-time control variables are generated. Therefore, the numerical solution is an approximate method. For a wider conversion ratio, more lookup tables should be calculated and stored in the controller. If the parameter of the converter is changed, the lookup table should be recalculated. Therefore, the numerical solution is not flexible. Furthermore, the numerical solution is difficult to disclose and demonstrate the seamless transition of the working modes and the inclusion of the wide conversion ratio and load range. A soft-switching control strategy for the FSBB is presented in [18]. The control strategy is based on the precious sample of the series inductor current at the commutation time. A high-speed analog-to-digital converter is necessary, which increases the cost of the converter. A two-phase FSBB converter with a coupling inductor can optimize the volume and efficiency [19]. The inductor current flows through four switches in each time interval, so the conduction loss is still very large. The control strategy in [19] is similar to the triple-phase-shift control for the dual-active-bridge converters [20]. The pulsewidth modulation plus phase shift control possesses more degrees of freedom for the ZVS with minimum conduction loss while it can avoid the dead zone issue. An FSBB with an auxiliary inductor and bidirectional switches improves the efficiency of light loads [21]. However, more inductor increases the volume of the converter, and the conduction loss is not optimal. The series-resonant FSBB converter presents wide ZVS performance [22]. However, the circulating current during the freewheeling period is still very large. The FSBB converter with more degrees of freedom presents high efficiency and wide voltage regulation capacity. However, the aforementioned control strategies did not reveal the optimization of the conduction loss and ZVS by the analytical solution. How to design the unified control strategy for the wide conversion ratio and wide loads is not presented.

The contribution of this article is that an analytical solution is proposed for the FSBB converter in phase shift control. Moreover, the proposed control strategy can overcome the dead-zone issue. The control law is based on minimum current stress and soft switching for all the switches. By regulating the duty cycle and phase shift of the two half-bridges, all the switches can achieve ZVS with minimum conduction loss. The principle of the control scheme is disclosed by the analytical solution. The control strategy is implemented in a real-time digital controller instead of the offline lookup table calculated by the numerical solution. Therefore, the control strategy is more flexible and practicable than the numerical solution. The efficiency of the converter is improved compared with the FSBB working in CCM. Compared with the CRM control, the switching frequency is constant, which eases the EMC design. Finally, the experimental prototype verifies the good performance of the control strategy.

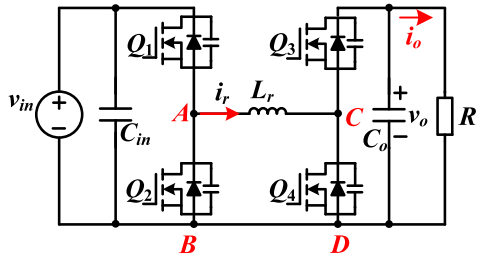


Fig. 1. Circuit of the FSBB converter.

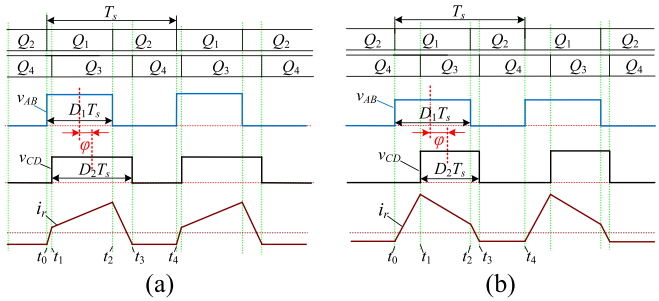


Fig. 2. (a) Key waveforms of Mode 1 (buck mode). (b) Key waveforms of Mode 2 (boost mode).

II. Working Mode Analyses FSBB

A. Working Mode

Fig. 1 shows the circuit of the FSBB converter, in which the two half-bridges are connected by a series inductor L_r. The on-time of Q_1 is complementary to that of Q_2 with a deadtime for ZVS, whereas the same is true for Q_3 and Q_4. The duty cycle of Q_1 is defined as D_1, and the duty cycle of Q_3 is defined as D_2. The conversion ratio of the converter is defined as $M = V_o/V_{in}$, where V_{in} and V_o are quiescent values of the input and output voltage. The key waveforms of the FSBB converter in soft switching modes are shown in Fig. 2, when D_1 and D_2 are both less than 1. In Fig. 2, the deadtime of the switches is ignored to simplify the analysis. Fig. 2(a) shows the buck mode ($M < 1$), which is defined as Mode 1. Fig. 2(b) shows the boost mode ($M > 1$), which is defined as Mode 2. In both modes, there are four working stages in a switching period. The working stages are shown in Fig. 3, where φ is the phase shift angle between v_{AB} and v_{CD}, and T_s is the switching period. The converter works in a constant switching frequency.

Stage 1 ($[t_0, t_1]$) [see Fig. 3(a)]: During t_0 to t_1, Q_1 and Q_4 are turned ON. The voltage across the series inductor L_r is the input voltage. The inductor current is linearly increased. The output capacitor supplies power for the load.

Stage 2 ($[t_1, t_2]$) [see Fig. 3(b)]: At t_1, Q_4 is turned OFF, and Q_3 is turned ON. The voltage across the series inductor is equal to v_{in}-v_o. The output capacitor is charged by the series inductor.

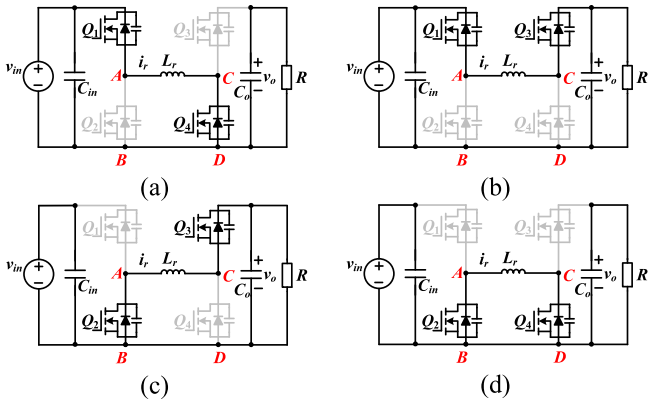


Fig. 3. Topological stages in a switching period: (a) $[t_0, t_1]$, (b) $[t_1, t_2]$, (c) $[t_2, t_3]$, and (d) $[t_3, t_4]$.

Stage 3 ($[t_2, t_3]$) [see Fig. 3(c)]: At t_2, Q_1 is turned OFF, and Q_2 is turned ON. The voltage across the series inductor is equal to -v_o. The energy stored in the series inductor still charges the output capacitor until the inductor current is negative.

Stage 4 ($[t_3, t_4]$) [see Fig. 3(d)]: At t_3, Q_3 is turned OFF, and Q_4 is turned ON. The voltage across the series inductor is equal to zero. The inductor current freewheels through Q_2 and Q_4.

According to the working stages, the current in the series inductor is expressed as

$$i_r(t) = \begin{cases} i_{r0} + \frac{v_{in}}{L_r}(t - t_0)(t_0 \le t \le t_1) \\ i_{r1} + \frac{v_{in} - v_o}{L_r}(t - t_1)(t_1 < t \le t_2) \\ i_{r2} - \frac{v_o}{L_r}(t - t_2)(t_2 < t \le t_3) \\ i_{r3}(t_3 < t \le t_4) \end{cases}$$

$$\begin{cases} t_0 = 0 \\ t_1 = (D_1 + \frac{\varphi}{\pi} - D_2)\frac{T_s}{2} \\ t_2 = D_1 T_s \\ t_3 = (D_1 + \frac{\varphi}{\pi} + D_2)\frac{T_s}{2} \\ t_4 = T_s \end{cases} \tag{1}$$

where i_{r0}, i_{r1}, i_{r2}, i_{r3}, and i_{r4} are the inductor current amplitude at t_0, t_1, t_2, t_3, and t_4, respectively. In the steady state, the current amplitude meets $i_{r0} = i_{r4}$. Therefore, the current amplitude can be derived as the following:

$$\begin{cases} i_{r1} = i_{r0} + \frac{v_{in} T_s}{4L_r}(\varphi_s + 2D_1 - 2D_2) \\ i_{r2} = i_{r0} + \frac{v_o T_s}{4L_r}(\varphi_s - 2D_1 + 2D_2) \\ i_{r3} = i_{r0} \\ i_{r4} = i_{r0} \end{cases} \tag{2}$$

where $\varphi_s = 2\varphi/\pi$ while $D_1 = MD_2$. The output power is expressed in (3). The output power is associated with D_1, D_2, φ, and i_{r0}

$$P_o = \frac{1}{T_s}\int_{t_1}^{t_3} v_o i_r(t)dt = \frac{v_o v_{in} T_s}{8L_r}\Big(D_1\varphi_s + D_2\varphi_s + 2D_1D_2 - D_1^2 - D_2^2 - \frac{\varphi_s^2}{4}\Big) + i_{r0}D_1 v_{in}$$

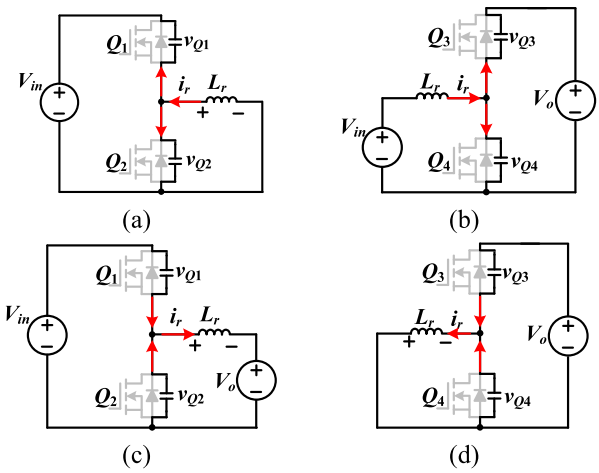


Fig. 4. Equivalent circuit during the deadtime: (a) at t_0, (b) at t_1, (c) at t_2, and (d) at t_3.

$$= \frac{v_o T_s}{8L_r}\Big((D_1 + D_2)\varphi_s v_{in} + 2D_1D_2 v_{in} - D_1^2 v_{in} - D_2^2 v_{in} - \frac{\varphi_s^2 v_{in}}{4}\Big) + i_{r0}D_2 v_o. \tag{3}$$

B. ZVS Analyses

The equivalent circuits during the deadtime at the commutating time are shown in Fig. 4.

The equivalent circuit during the deadtime at t_0 is shown in Fig. 4(a). The initial current in the deadtime is i_{r0}. The voltage across Q_1 during the deadtime is expressed as

$$v_{Q1}(t) = V_{in} + i_{r0}\sqrt{\frac{L_r}{2C}}\sin(\omega t) \tag{4}$$

where C is the junction capacitor of the switches, and $\omega = 1/\sqrt{2L_rC}$. To achieve ZVS, Q_1 should meet the constraint in (5). t_{dead} is the deadtime of the switches

$$v_{Q1}(t_{\text{dead}}) \le 0 \Rightarrow i_{r0} \le -\frac{V_{in}}{\sqrt{\frac{L_r}{2C}}\sin(\omega t_{\text{dead}})}. \tag{5}$$

The equivalent circuit during the deadtime at t_1 is shown in Fig. 4(b). The initial current during the deadtime of Q_3 is i_{r1}. The voltage across Q_3 during the deadtime can be expressed as

$$v_{Q3}(t) = V_{in} + (V_o - V_{in})\cos(\omega t) - i_{r1}\sqrt{\frac{L_r}{2C}}\sin(\omega t). \tag{6}$$

To achieve ZVS, Q_3 should meet the following constraint:

$$v_{Q3}(t_{\text{dead}}) \le 0 \Rightarrow i_{r1} \ge \frac{V_{in} + (V_o - V_{in})\cos(\omega t_{\text{dead}})}{\sqrt{\frac{L_r}{2C}}\sin(\omega t_{\text{dead}})}. \tag{7}$$

The constraint in (7) can be simplified in (8). If i_{r1} is larger than I_{zvs1}, Q_3 must meet the ZVS constraints in (7)

$$i_{r1} \ge \frac{V_{in} + (V_o - V_{in})}{\sqrt{\frac{L_r}{2C}}\sin(\omega t_{\text{dead}})} = \frac{V_o}{\sqrt{\frac{L_r}{2C}}\sin(\omega t_{\text{dead}})} \triangleq I_{zvs1}. \tag{8}$$

The equivalent circuit during the deadtime at t_2 is shown in Fig. 4(c). The initial current during the deadtime of Q_3 is i_{r1}. The voltage across Q_2 during the deadtime can be expressed as

$$v_{Q2}(t) = V_o + (V_{in} - V_o)\cos(\omega t) - i_{r2}\sqrt{\frac{L_r}{2C}}\sin(\omega t). \quad (9)$$

The ZVS constraint for Q_2 is expressed as

$$v_{Q2}(t_{\text{dead}}) \le 0 \Rightarrow i_{r2} \ge \frac{V_o + (V_{in} - V_o)\cos(\omega t_{\text{dead}})}{\sqrt{\frac{L_r}{2C}}\sin(\omega t_{\text{dead}})}. \quad (10)$$

The constraints in (10) can be simplified in (11). If i_{r2} is larger than I_{zvs2}, Q_2 must meet the ZVS constraint in (10)

$$i_{r2} \ge \frac{V_o + (V_{in} - V_o)}{\sqrt{\frac{L_r}{2C}}\sin(\omega t_{\text{dead}})} = \frac{V_{in}}{\sqrt{\frac{L_r}{2C}}\sin(\omega t_{\text{dead}})} \triangleq I_{zvs2}. \quad (11)$$

The equivalent circuit during the deadtime at t_3 is shown in Fig. 4(d). The voltage across Q_4 during the deadtime can be expressed as

$$v_{Q4}(t) = i_{r3}\sqrt{\frac{L_r}{2C}}\sin(\omega t) + V_o\cos(\omega t). \quad (12)$$

Therefore, the ZVS constraint for Q_4 is expressed as

$$v_{Q4}(t_{\text{dead}}) \le 0 \Rightarrow i_{r3} \le -\frac{V_o\cos(\omega t_{\text{dead}})}{\sqrt{\frac{L_r}{2C}}\sin(\omega t_{\text{dead}})}. \quad (13)$$

In the steady state, i_{r0} is equal to i_{r3}. Synthesizing (5) and (13), the ZVS constraint for Q_1 and Q_3 is expressed as

$$i_{r0} = i_{r3} \le -\frac{\text{Max}(V_{in}, V_o\cos(\omega t_{\text{dead}}))}{\sqrt{\frac{L_r}{2C}}\sin(\omega t_{\text{dead}})}. \quad (14)$$

To simplify the analysis and implementation, the constraint in (15) is derived. If i_{r0} and i_{r3} are no greater than I_{zvs0}, Q_1 and Q_3 must meet the ZVS constraint

$$i_{r0} = i_{r3} \le -\frac{\text{Max}(V_{in}, V_o)}{\sqrt{\frac{L_r}{2C}}\sin(\omega t_{\text{dead}})} \triangleq I_{zvs0}. \quad (15)$$

For the specification of $V_o = 150$ V, $V_{in} = 100$–200 V $L_r = 50$ μH, $T_s = 20$ μs, $C = 45$ pF, and $t_{\text{dead}} = 200$ ns, the ZVS constraints in (8), (11), and (15) are expressed as $I_{zvs0} = -1.6$ A, $I_{zvs1} = 1.2$ A, and $I_{zvs2} = 1.6$ A.

The ZVS analysis is verified by the simulation. The simulation of the working modes is implemented in PSIM software, where $V_o = 150$ V, $V_{in} = 100$–200 V $L_r = 50$ μH, $T_s = 20$ μs, $C = 45$ pF, and $t_{\text{dead}} = 200$ ns. The simulation results are shown in Fig. 5. Fig. 5(a)–(c) is the simulation results of Mode 1, where the input voltage is 200 V. Fig. 5(d) shows the simulation result of Mode 2, where the input voltage is 100 V. Fig. 5 illustrates that all the switches work in ZVS, where I_{zvs0}, I_{zvs1}, and I_{zvs2} are set as the same as the derivation of the ZVS analysis. The simulation results demonstrate the ZVS analyses.

C. Working Mode Optimization

The peak-to-peak current in the series inductor during a switching period is defined as the current stress of the converter.

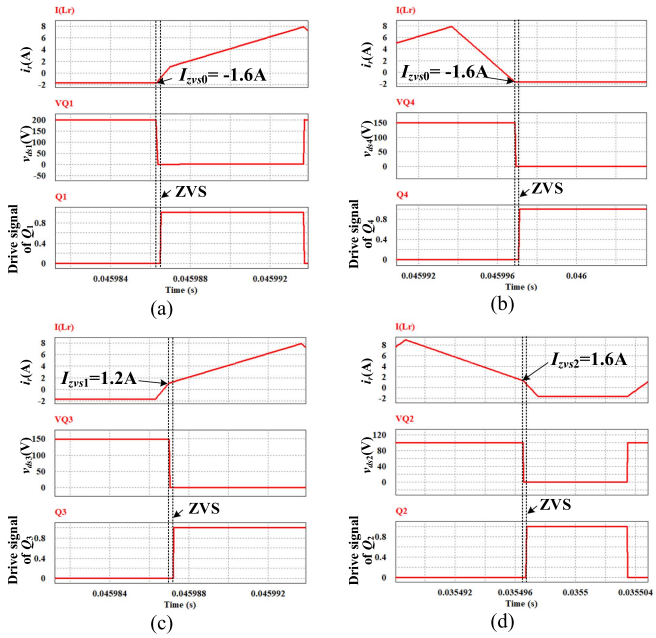


Fig. 5. Simulation results of the ZVS analyses. (a) ZVS of Q_1 in Mode 1. (b) ZVS of Q_4 in Mode 1. (c) ZVS of Q_3 in Mode 1. (d) ZVS of Q_2 in Mode 2.

With the lower current stress, the conduction loss can be reduced. Meanwhile, the ZVS for all the switches can reduce the switching loss. Therefore, the working mode optimization should be formulated, including the current stress and ZVS constraints. In Mode 1, it is expressed in (16), where i_o is the load current

$$\begin{aligned} &\text{Min } I_{pp} = i_{r2} - i_{r0} \\ &\text{Subject to} \\ &P_o = p^* = V_o i_o, i_{r1} \ge I_{zvs1}, i_{r0} \le I_{zvs0}. \end{aligned} \quad (16)$$

Solving the optimization problem by using the Karush–Kuhn–Tucker (KKT) condition [23], [24], the duty cycle of the two half-bridges is expressed in (17). In (3), the output power is also associated with i_{r0}. The optimized working mode in (17) guarantees that i_{r0} is equal to I_{zvs0} and i_{r1} is equal to I_{zvs1}. On the premise of the ZVS, the conduction loss is minimized

$$\begin{aligned} \varphi_{s\_\text{Mode1}} &= \frac{2L_r}{T_s V_o}\left(\begin{array}{l}(I_{\text{zvs1}} - I_{\text{zvs0}})M - I_{\text{zvs0}} \\ +\sqrt{I_{\text{zvs1}}^2 M + \left(\frac{2i_o T_s V_o}{L_r} + I_{\text{zvs0}}^2\right)(1-M)}\end{array}\right) \\ D_{1\_\text{Mode1}} &= \frac{M}{1-M}\left[\frac{\varphi_{\text{s\_Mode1}}}{2} + \frac{2L_r\left(I_{\text{zvs0}} - I_{\text{zvs1}}\right)}{T_s V_{in}}\right] \\ D_{2\_\text{Mode1}} &= \frac{D_{1\_\text{Mode1}}}{M}. \end{aligned} \quad (17)$$

Similar to Mode 1, the working mode optimization problem in Mode 2 is expressed in as

$$\begin{aligned} &\text{Min } I_{pp} = i_{r1} - i_{r0} \\ &\text{Subject to} \\ &P_o = p^* = V_o i_o, i_{r2} \ge I_{\text{zvs2}}, i_{r0} \le I_{\text{zvs0}}. \end{aligned} \quad (18)$$

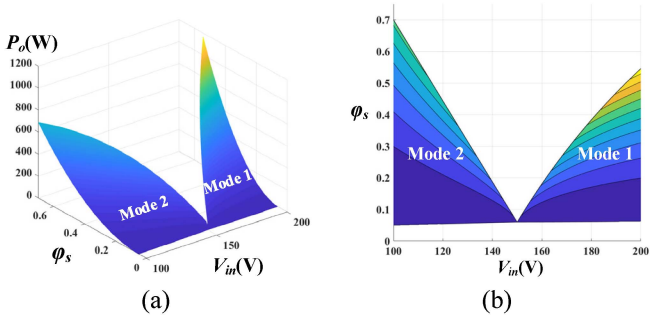


Fig. 6. Diagram of the output power in Mode 1 and Mode 2 versus the phase shift angle cycle and the input voltage. (a) Surface of the output power versus φ_s and v_{in}. (b) Contour lines of the output power versus φ_s and v_{in}.

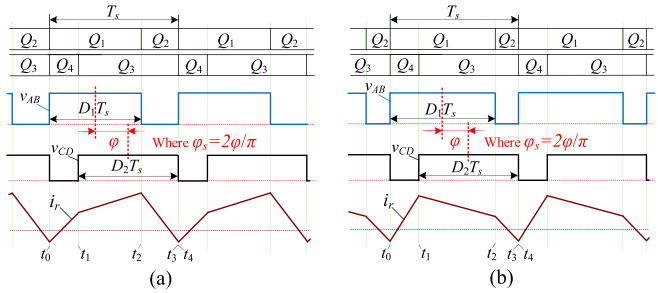


Fig. 7. Key waveforms of Mode 3. (a) Buck mode. (b) Boost mode.

Solving the optimization problem in Mode 2 by using the KKT conditions, the duty cycle of the two half-bridges is expressed in (19). In this case, i_{r0} is equal to I_{zvs0} and i_{r2} is equal to I_{zvs2}. Furthermore, the current stress is minimized, and all the switches work in ZVS

$$\varphi_{s\_\text{Mode2}} = \frac{2L_r}{T_s V_o} \left(\begin{array}{l} (I_{\text{zvs2}} - I_{\text{zvs0}}) - M I_{\text{zvs0}} \\ + \sqrt{M\left[I_{\text{zvs2}}^2 + \left(\frac{2i_o T_s V_o}{L_r} + I_{\text{zvs0}}^2\right)(M-1)\right]} \end{array} \right)$$

$$D_{1\_\text{Mode2}} = \frac{M}{M-1}\left[\frac{\varphi_{s\_\text{Mode2}}}{2} + \frac{2L_r\left(I_{\text{zvs0}} - I_{\text{zvs2}}\right)}{T_s V_o}\right]$$

$$D_{2\_\text{Mode2}} = \frac{D_{1\_\text{Mode2}}}{M}. \tag{19}$$

As seen in (17) and (19), when the load current i_o is equal to zero, the phase shift angle reaches the minimum value. Therefore, the minimum phase shift angle is expressed in (20) shown at the bottom of this page. When the phase shift angle is equal to the minimum value, D_1 and D_2 also attain the minimum values

Substituting (17) and (19) into (3), the surface of the output power versus the phase shift angle and the input voltage is shown in Fig. 6(a), where $V_o = 150$ V, $L_r = 50$ μH, $T_s = 20$ μs, $C = 45$ pF, and $t_{\text{dead}} = 200$ ns. Fig. 6(b) shows the contour lines of the output power.

For the specific input voltage, the output power is increased with the increase of φ_s. However, Fig. 6 illustrates that Mode 1 and Mode 2 cannot cover the whole conversion ratio and load power, especially for the converter ratio close to one. When the conversion ratio is close to one, the value of D_1 and D_2 in (17) and (19) will be larger than one. It is irrational in the converter. The maximum value of D_1 and D_2 is one. In this case, the output voltage loses the regulation capacity, which is defined as the dead zone issue. Such operation requires an isolated drive circuit for the high-side switches. Q_1 and Q_3 conduct in the whole switching period, and there is no phase shift angle between the two half-bridges. The working modes in Fig. 2 do not meet this occasion.

With the increase of φ_s, the key waveforms of the boundary working modes for Mode 1 and Mode 2 are shown in Fig. 6, where t_3 is equal to t_4. In the boundary modes, there are three working stages while the converter meets (21).

$$\frac{D_1 T_s}{2} + \frac{\varphi T_s}{2\pi} + \frac{D_2 T_s}{2} = T_s. \tag{21}$$

In practice, Q_3 must be turned OFF no later than the time when Q_1 is turned ON. Otherwise, the working modes in Figs. 2 and 6 do not exist. Therefore, a time margin between t_3 and t_4 should be set in Mode 3. In this case, the constraint in (21) can be rewritten in (22), where α is set as 0.95 in this article. Therefore, (23) can be derived. In Mode 3, D_1 and D_2 are decreased with the increase of φ_s. The working modes in Fig. 7 are defined as Mode 3. Compared with Mode 1 and Mode 2, Mode 3 can extend φ_s larger. i_{r0} is controlled to be I_{zvs0}. With the increase of φ_s in Mode 3, the current amplitudes of i_{r1} and i_{r2} become larger, so all the switches in Mode 3 still work in ZVS

$$\begin{cases} \frac{D_1 T_s}{2} + \frac{\varphi T_s}{2\pi} + \frac{D_2 T_s}{2} = \alpha T_s \\ D_1 = M D_2 \end{cases} \tag{22}$$

$$\begin{cases} D_{1\_\text{Mode3}} = \frac{M(4\alpha - \varphi_{s\_\text{Mode3}})}{2(1+M)} \\ D_{2\_\text{Mode3}} = \frac{D_{1\_\text{Mode3}}}{M} \end{cases}. \tag{23}$$

Substituting (23) into (3), the differential equation of the output power versus φ_s is expressed in (24) shown at the bottom of next page. When the differential equation is equal to zero, the phase shift angle is expressed in (25). When φ_s is less than φ_{sm}, the differential equation in (24) is larger than zero, i.e., the output power is increased with the increase of φ_s. Otherwise, the output power is decreased with the increase of φ_s

$$\varphi_{sm} = \frac{2\left(1+M^2\right)}{1+M+M^2} - \frac{2I_{zvs0}L_r\left(1+M\right)}{T_s V_{in}\left(1+M+M^2\right)}. \tag{25}$$

$$\varphi_{s\_min} = \begin{cases} \frac{2L_r}{T_s V_o}\left(\left(I_{\text{zvs1}} - I_{\text{zvs0}}\right)M - I_{\text{zvs0}} + \sqrt{I_{\text{zvs1}}^2 M + I_{\text{zvs0}}^2\left(1-M\right)}\right) & M \le 1 \\ \frac{2L_r}{T_s V_o}\left(\left(I_{\text{zvs2}} - I_{\text{zvs0}}\right) - M I_{\text{zvs0}} + \sqrt{M\left[I_{\text{zvs2}}^2 + I_{\text{zvs0}}^2\left(M-1\right)\right]}\right) & M > 1 \end{cases}. \tag{20}$$

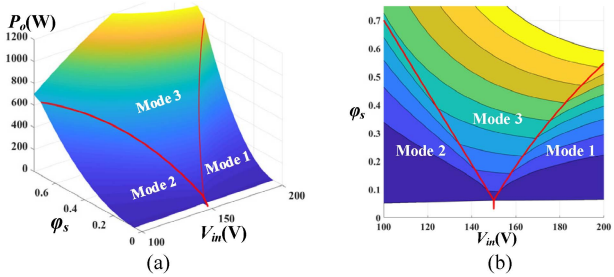


Fig. 8. Diagram of the output power versus the phase shift angle cycle and the input voltage. (a) Surface of the output power versus φ_s and v_{in}. (b) Contour lines of the output power versus φ_s and v_{in}.

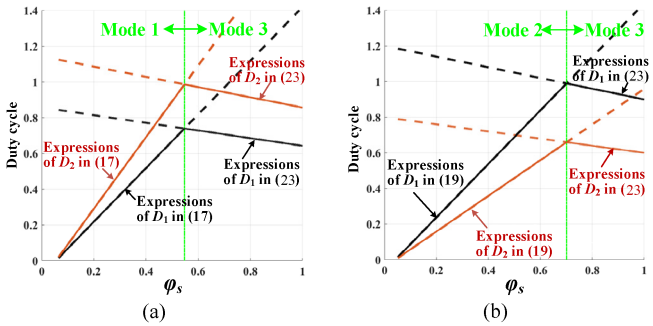


Fig. 9. Curves of D_1 and D_2 versus φ_s in buck mode. (a) $V_{in} = 200$ V (buck mode). (b) $V_{in} = 100$ V (boost mode).

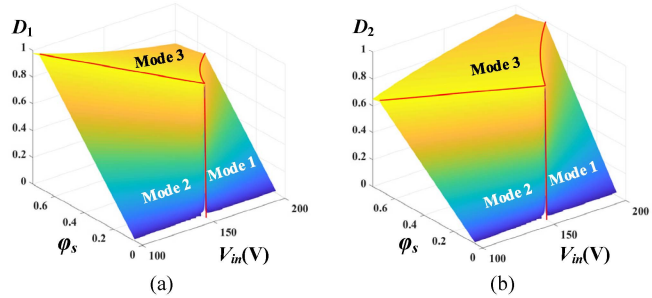


Fig. 10. Surfaces of D_1 and D_2 versus φ_s and V_{in}: (a) D_1 and (b) D_2.

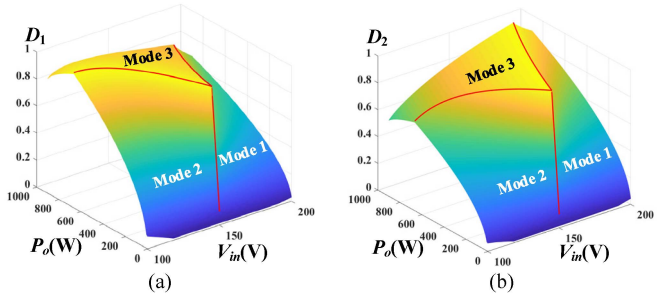


Fig. 11. Surfaces of D_1 and D_2 versus V_{in} and the load power: (a) D_1 and (b) D_2.

When φ_s is less than φ_{sm}, the surface of the output power versus the phase shift angle and the input voltage in Mode 3 is shown in Fig. 8, where $V_o = 150$ V, $L_r = 50$ μH, $T_s = 20$ μs, $C = 45$ pF, and $t_{\text{dead}} = 200$ ns. It illustrates that Mode 1, Mode 2, and Mode 3 cover the whole load range and wide conversion ratio. Meanwhile, the output power is continuously varied with the phase shift angle and the input voltage. Therefore, φ_s can be used as the control variable to regulate the output voltage and output power. The maximum value of the phase shift angle is set as φ_{sm}.

III. Modulation Scheme and Control Strategy

A. Control Strategy

According to the expressions of (17), (19), and (23), the curves of D_1 and D_2 versus φ_s are shown in Fig. 9, where $V_o = 150$ V, $L_r = 50$ μH, $T_s = 20$ μs, $C = 45$ pF, and $t_{\text{dead}} = 200$ ns.

Fig. 9(a) shows the curves of D_1 and D_2 when the converter works in 200-V input voltage. The dashed lines are the curves of the expressions in (17) and (19), and the solid lines are the curves of D_1 and D_2 versus φ_s. In Fig. 8, the intersection of the two dashed lines is the boundary between Mode 1 and Mode 3. Therefore, D_1 and D_2 in the buck mode are selected as the minimum value of the two expressions in (17) and (23). Fig. 9(b) shows the curves of D_1 and D_2 when the converter works in 100-V input voltage. When the converter works in the boost mode, D_1 and D_2 are also selected as the minimum value of the two expressions in (19) and (23). Synthesizing the two cases, D_1 and D_2 can be selected as the minimum values of the expressions in (17), (19), and (23). Therefore, the values of the duty cycle of the two half-bridges are expressed as

$$\begin{cases} D_1 = \text{Min}(D_{1\_\text{Mode1}}, D_{1\_\text{Mode2}}, D_{1\_\text{Mode3}}) \\ D_2 = \frac{D_1}{M} \end{cases}. \tag{26}$$

The surface of the duty cycles versus the input voltage and phase shift angle is shown in Fig. 10, where $V_o = 150$ V, $L_r = 50$ μH, $T_s = 20$ μs, $C = 45$ pF, and $t_{\text{dead}} = 200$ ns. It illustrates that the duty cycles are seamlessly varied with the phase shift angle and input voltage. Fig. 11 shows the duty cycles versus the input voltage and load power. For the specific input voltage, the duty cycle can be determined by the load power. The surfaces in Fig. 11 demonstrate that the optimized working modes expressed in (26) can cover the whole load range and a wide conversion ratio.

According to the analyses in Section II-C, the phase shift angle can be used to control the output voltage. According to (3), i_{r0} is also associated with the output power. However, by controlling the phase shift angle and duty cycle, the initial value of the series inductor, i.e., i_{r0}, is still not controllable. Fig. 12 shows the gate signal generation logic. The control strategy is implemented in

$$\frac{\partial P_o}{\partial \varphi_s} = \frac{MV_{in}\left[4T_sV_{in}\left(1+M^2\right) - 2T_sV_{in}\varphi_s\left(1+M+M^2\right) - 4I_{zvs0}L_r\left(1+M\right)\right]}{8L_r(1+M)^2} \tag{24}$$

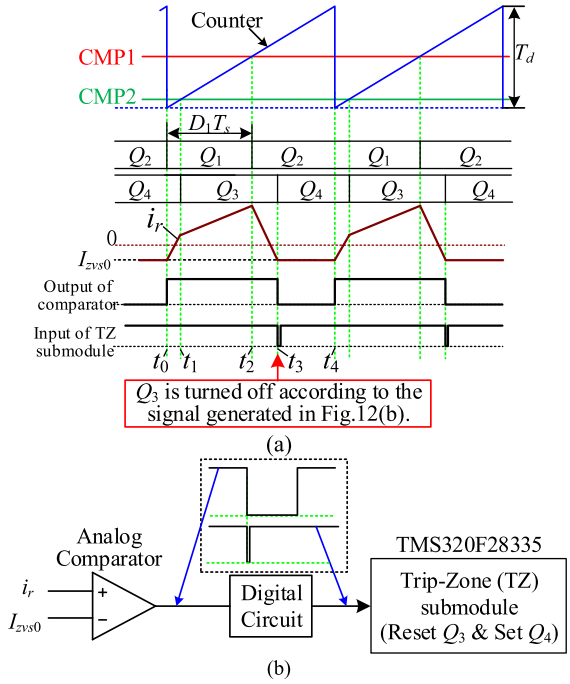


Fig. 12. Gate signal generation logic. (a) Gate signal generation. (b) Circuit to generate the gate signals of Q_3 and Q_4.

the TMS320F28335. As seen in Fig. 12(a), when the increment counter is equal to zero, Q_1 is turned ON and Q_2 is turned OFF. When the increment counter is equal to the comparator value #1 (CMP1), Q_1 is reset and Q_2 is set. When the increment counter is equal to the comparator value #2 (CMP2), Q_3 is set and Q_4 is reset. The values of CMP1 and CMP2 are expressed in (27), where T_d is the peak value of the increment counter

$$\begin{cases} \text{CMP1} = D_1 T_d \\ \text{CMP2} = (0.5D_1 + \varphi_s - 0.5D_2)\, T_d \end{cases}. \tag{27}$$

The time when Q_3 is turned OFF determines the value of i_{r3} and i_{r0}. To guarantee that i_{r0} is equal to I_{zvs0} at t_3, the circuit in Fig. 12(b) is applied to generate the signal to reset Q_3 and set Q_4. The series inductor current i_r is sampled by using a current Hall sensor, and it is compared with I_{zvs0} by using an analog comparator. When i_r is less than I_{zvs0}, the output of the comparator generates a square waveform. By using a digital circuit, a pulsed signal is generated in terms of the falling edge of the square waveform. The low level of the pulsed signal triggers the trip-zone submodule in TMS320F28335 to reset Q_3 and set Q_4. The deadtime of the two half-bridges is preset in the TMS320F28335.

The control diagram is shown in Fig. 13. $G_{vc}(s)$ is the voltage loop controller, which is a proportional-integral controller. The output of the controller is the phase shift angle, which is dynamically varied to regulate the output power. The input and output voltages are sampled to calculate the conversion ratio. According to the conversion ratio and φ_s, the value of the duty cycles D_1 and D_2 can be calculated by using (26). In terms of

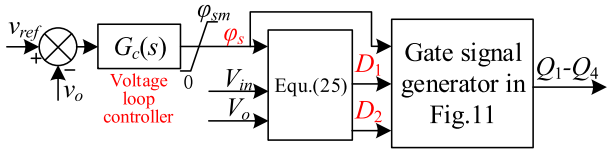


Fig. 13. Control diagram of the FSBB converter.

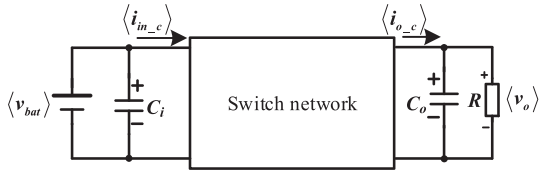


Fig. 14. FSBB converter in the average switch network.

Fig. 12, the gate signals are generated to drive the converter for closed-loop control.

B. Small-Signal Analysis of the Control Loop

The FSBB converter can be modeled by using a switching network shown in Fig. 14, where <•> is expressed as the average value.

In terms of (3), $<i_{o\_c}>$ is defined as (28)

$$\begin{aligned} \langle i_{o\_c} \rangle &= \frac{p_o}{\langle v_o \rangle} = \frac{T_s}{8L_r} \begin{pmatrix} (D_1 + D_2)\,\varphi_s \langle v_{in} \rangle + 2D_1 D_2 \langle v_{in} \rangle \\ -D_1^2 \langle v_{in} \rangle - D_2^2 \langle v_{in} \rangle - \frac{\varphi_s^2 \langle v_{in} \rangle}{4} \end{pmatrix} \\ &\quad + i_{r0} D_2 \\ &= g\left(\langle v_{in} \rangle, \varphi_s \right). \end{aligned} \tag{28}$$

The small-signal ac descriptions of i_{o_c} can be derived by linearizing the average equation of $<i_{o\_c}>$. Substituting (26) into (28), the small-signal ac descriptions of i_{o_c} can be expressed as

$$\begin{aligned} \hat{i}_{o\_c} &= \left. \frac{\partial g\left(\langle v_{in} \rangle, \varphi_s \right)}{\partial v_{in}} \right|_{v_{in}=V_{in}} \cdot \hat{v}_{in} + \left. \frac{\partial g\left(\langle v_{in} \rangle, \varphi_s \right)}{\partial \varphi_s} \right|_{\varphi_s=\Phi_s} \cdot \hat{\varphi}_s \\ &= k_1 \cdot \hat{v}_{in} + k_2 \cdot \hat{\varphi}_s. \end{aligned} \tag{29}$$

In Mode 1, k_1 and k_2 are expressed as equation (30) shown at the bottom of the next page

In Mode 2, k_1 and k_2 are expressed as equation (31) shown at the bottom of the next page

In Mode 3, k_1 and k_2 are expressed as

$$k_1 = -\frac{\left(4\alpha^2(M-1)^2 - 4\alpha\left(1+M^2\right)\Phi_s + \left(1+M+M^2\right)\Phi_s^2\right) T_s}{8L_r(1+M)^2}$$

$$k_2 = -\frac{2I_{zvs0}L_r\,(1+M) + \left(\left(1+M+M^2\right)\Phi_s - 2\alpha\left(1+M^2\right)\right) T_s V_{in}}{4L_r(1+M)^2}. \tag{32}$$

The capital letters are the corresponding quiescent values. The equivalent circuit to the small-signal ac capacitor node is shown

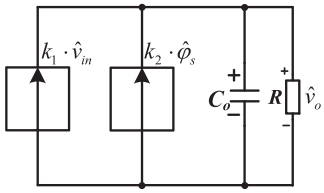


Fig. 15. Small-signal equivalent circuit in the output side.

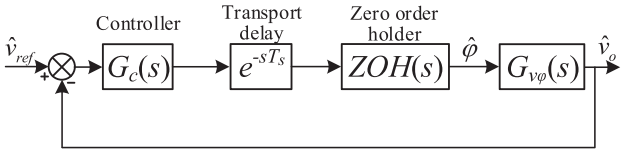


Fig. 16. Control loop in small-signal analysis.

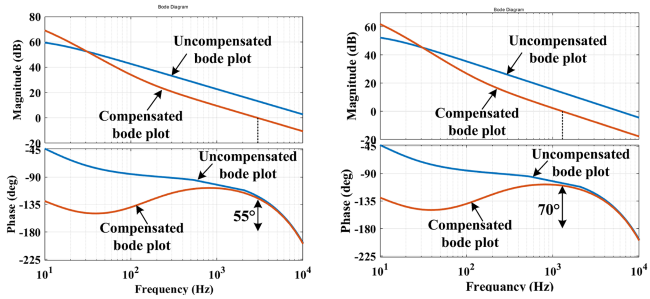


Fig. 17. Bode plot in an open loop with and without a controller. (a) 200-V input voltage. (b) 100-V input voltage.

in Fig. 15. Ignoring the disturbance of the input voltage, the small-signal control-to-output transfer function $G_{v\varphi}(s)$ is shown in (33). Considering the transport delay and zero-order holder in the digital controller, the control loop in the small-signal analysis is shown in Fig. 16

$$\hat{v}_o = G_{v\varphi}(s) \cdot \hat{\varphi} = \frac{k_2 R}{1 + sC_o R} \frac{2}{\pi} \hat{\varphi}. \tag{33}$$

The bode plots in an open loop with and without a controller for 200-V input voltage are shown in Fig. 17(a), where $V_o = 150$ V, $L_r = 50$ μH, $T_s = 20$ μs, $P_o = 600$ W, $R = 37.5$ Ω, and $C_o = 400$ μF. The converter works in Mode 1, and the controller

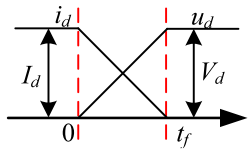


Fig. 18. Turn-OFF procedure.

TABLE I
CURRENT AND VOLTAGE AMPLITUDE DURING THE TURN-OFF

Switch	Time	Current (I_d)	Voltage (V_d)
Q_1	t_2	i_{r2}	V_{in}
Q_2	t_0	i_{r0}	V_{in}
Q_3	t_3	i_{r3}	V_o
Q_4	t_1	i_{r1}	V_o

is expressed in (34). The crossover frequency with the controller is 3 kHz, and the phase margin is 55°. When the input voltage is 100 V and the load power is 600 W, the bode plots with and without the controller are shown in Fig. 17(b). The converter works in Mode 3, and the converter is still stable in 100-V input voltage

$$G_c(s) = 0.216\left(1 + \frac{880}{s}\right). \tag{34}$$

IV. Loss Analysis and Comparison

A. Loss Breakdown Analysis

1) Switching Loss: The switching loss includes the turn-OFF loss and turn-ON loss. Because all the switches work in ZVS, the turn-ON loss is ignored. The turn-OFF procedure is shown in Fig. 18. V_d is the drain-source voltage after the switch is turned OFF, and I_d is the turn-OFF current. t_f is the turn-OFF time. To simplify the loss analysis during the turn-OFF interval, assuming the current drops linearly and the drain-source voltage rises linearly, the turn-OFF loss is expressed as

$$P_{sw\_off} = \frac{1}{T_s}\int_0^{t_f} u_d(t) i_d(t) dt = \frac{V_d I_d t_f}{6T_s}. \tag{35}$$

The current and voltage corresponding to the switches at the turn-OFF interval are shown in Table I. Substituting the current

$$k_1 = \frac{16\left(I_{zvs0} - I_{zvs1}\right) I_{zvs0} L_r^2 + 4L_r^2 \left(I_{zvs0} - I_{zvs1}\right)^2 (M-1) - M\Phi_s^2 T_s^2 V_{in}^2}{8L_r T_s V_{in}^2 (M-1)}$$
$$k_2 = \frac{2I_{zvs0} L_r + 2L_r M\left(I_{zvs0} - I_{zvs1}\right) + M\Phi_s T_s V_{in}}{4L_r(1-M)}. \tag{30}$$

$$k_1 = \frac{4Lr^2 (M-1)\left(I_{zvs0} - I_{zvs2}\right)^2 - 16 I_{zvs0} L_r^2 M\left(I_{zvs0} - I_{zvs2}\right) + M^2 \Phi_s^2 T_s^2 V_{in}^2}{8L_r T_s V_{in}^2 M^2 (M-1)}$$
$$k_2 = \frac{2\left(I_{zvs0} - I_{zvs2}\right) L_r + 2I_{zvs0} L_r M + M\Phi_s T_s V_{in}}{4L_r M(M-1)}. \tag{31}$$

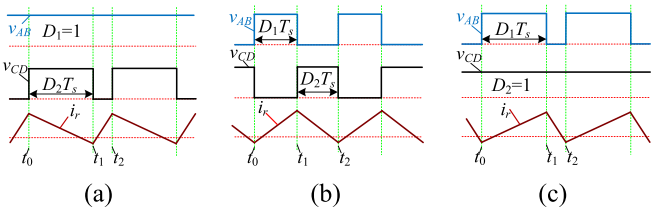


Fig. 19. Key waveforms of the CRM: (a) boost, (b) buck–boost, and (c) buck.

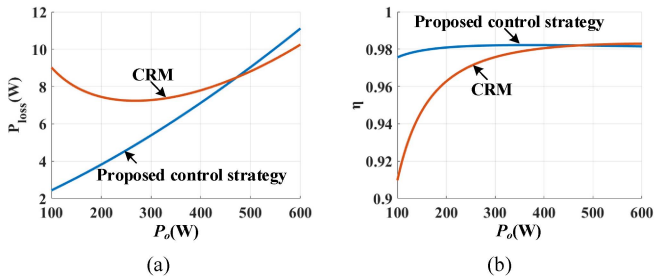


Fig. 20. Calculated loss and efficiency for v_{in} = 200 V: (a) loss and (b) efficiency.

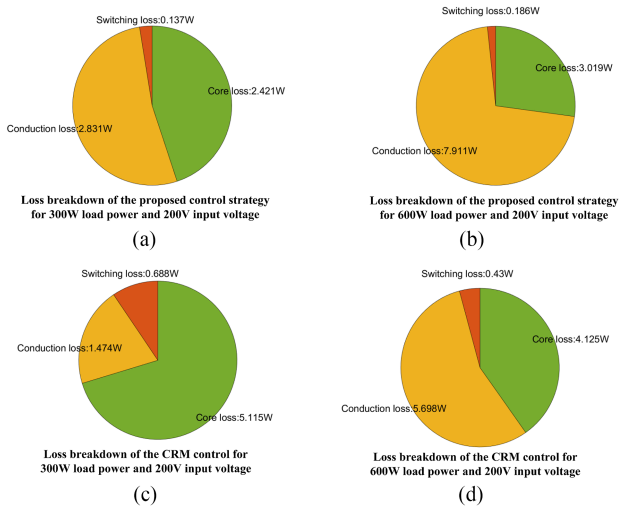


Fig. 21. Pie chart of the loss breakdown for 200-V input voltage. (a) Loss breakdown of the proposed control for 300-W load power. (b) Loss breakdown of the proposed control for 600-W load power. (c) Loss breakdown of the CRM control for 300-W load power. (d) Loss breakdown of the CRM control for 600-W load power.

and voltage amplitude at the switching time, the turn-OFF loss is evaluated.

2) Conduction Loss: Ignoring the deadtime, two switches are conducting at any time. Therefore, the conduction loss in the switches can be calculated as

$$P_{\text{loss\_}on} = 2\int_0^{Ts} i_r^2 R_{ds\_on} dt \tag{36}$$

where R_{ds_on} is the turn-ON resistance of the switches. Similarly, the inductor copper loss can be calculated in (37), where R_{Lr} is the equivalent series resistance (ESR) of the series inductor

$$P_{\text{copper\_}Lr} = \int_0^{Ts} i_r^2 R_{Lr} dt. \tag{37}$$

3) Core Loss: The core loss of the series inductor can be evaluated by using the improved generalized Steinmetz equation [25], which is expressed as

$$\bar{P}_v = \frac{1}{T_s}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta}$$

$$P_{Fe} = P_V \cdot V_e \tag{38}$$

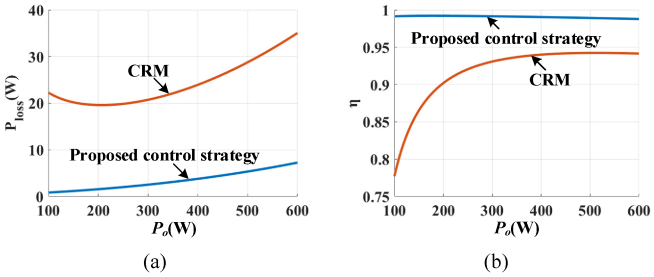
where ΔB is the peak-to-peak flux density. V_e is the volume of the core. The parameters k, α, and β are the same parameters used in the conventional Steinmetz equation, which is obtained from the datasheet of the manufacturer. The flux density in the series inductor is expressed as $B = L_r i_r/(NA_e)$, where N is the turns of the series inductor. A_e is the cross section of the core. According to the working stages in Fig. 2, the core loss can be derived according to (38).

B. Loss Comparison With CRM Control

The proposed control strategy in the FSBB converter is compared with the CRM control strategy [14] in the same converter. The key waveform of CRM is shown in Fig. 19, the converter can work in the boost, buck–boost, and boost modes. In the CRM control, the converter is controlled by the duty cycle and the switching frequency for the ZVS. The CRM control works in variable switching frequency, which makes the EMC design difficult. When the input voltage is close to the output voltage, i.e., the conversion ratio M is close to one, the converter works in the buck–boost mode to deal with the dead zone issue.

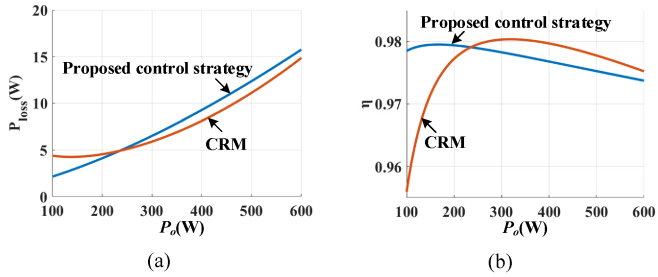
The loss of the CRM control in the FSBB converter can be calculated in terms of the analysis in Section IV-A, where V_{in} = 100–200 V, V_o = 150 V, and L_r = 50 μH. For the CRM control, the converter works in boost mode from 100 to 140 V input voltage. In the range from 140 to 160 V input voltage, the converter works in buck–boost mode. From 160 to 200 V input voltage, the converter works in buck mode.

The switching frequency in the proposed control strategy is 50 kHz, i.e., T_s = 20 μs. PQ32/32 core with eight turns of winding is selected to fabricate the series inductor. The calculated loss and efficiency for 200-V input voltage are shown in Fig. 20. Fig. 21(a) and (c) shows the pie chart of the loss breakdown for the proposed control and CRM control in 300-W load power and 200-V input voltage. In light loads, the CRM can achieve ZVS by increasing the switching frequency, which causes more switching loss and core loss. Therefore, the efficiency of the proposed control is higher than that of the CRM control in light loads. Fig. 21(b) and (d) shows the pie chart of the loss breakdown for the proposed control and CRM control in 600-W load power and 200-V input voltage. The core loss in the proposed control is lower due to the lower current ripple. However, the conduction loss is larger, where the conduction loss includes the conduction loss in the switches and copper loss in the series inductor. In



(a) (b)

Fig. 22. Calculated loss and efficiency for $v_{in} = 150$ V: (a) loss and (b) efficiency.



(a) (b)

Fig. 24. Calculated loss and efficiency for $v_{in} = 100$ V: (a) loss and (b) efficiency.

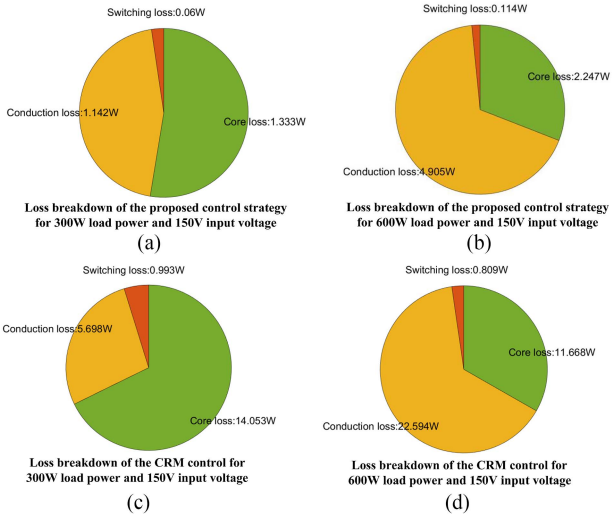


Fig. 23. Pie chart of the loss breakdown for 150-V input voltage. (a) Loss breakdown of the proposed control for 300-W load power. (b) Loss breakdown of the proposed control for 600-W load power. (c) Loss breakdown of the CRM control for 300-W load power. (d) Loss breakdown of the CRM control for 600-W load power.

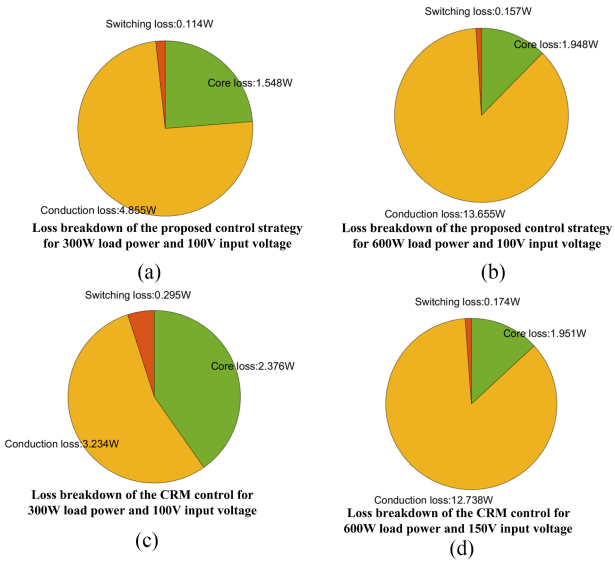


Fig. 25. Pie chart of the loss breakdown for 100-V input voltage. (a) Loss breakdown of the proposed control for 300-W load power. (b) Loss breakdown of the proposed control for 600-W load power. (c) Loss breakdown of the CRM control for 300-W load power. (d) Loss breakdown of the CRM control for 600-W load power.

heavy loads, the efficiency of the two control strategies is almost the same.

Fig. 22 shows the calculated loss and efficiency for 150-V input voltage. Fig. 23 shows the pie chart of the loss breakdown of the proposed control and CRM control for 150-V input voltage. As seen Fig. 23(a) and (c), the switching frequency for 300-W load power in the proposed control strategy is lower than that of the CRM, which causes lower turn-OFF loss and core loss. Therefore, the efficiency of the proposed control is still larger than the CRM. In Fig. 23(b) and (d), the switching frequency for 600-W load power in the CRM control is lower than 50 kHz. The series inductor and switches suffer from large peak currents, which cause more turn-OFF loss and larger core loss. Therefore, the efficiency of the proposed control in heavy loads is much higher.

Fig. 24 shows the calculated loss and efficiency for 100-V input voltage. In light loads, the efficiency is higher than that of the CRM control because of low switching loss and low core loss. Fig. 25 shows the pie chart of the loss breakdown of the proposed control and CRM control for 100-V input voltage. For the loss breakdown of 300-W load power in Fig. 25(a) and (c), the turn-OFF loss and core loss in the proposed control strategy are lower because of the lower switching frequency. In heavy loads, the efficiency in CRM is only a little higher than that in the proposed control strategy. The pie charts in Fig. 25(b) and (d) illustrate that the loss breakdown of the proposed control in heavy loads is similar to that of the CRM control.

The efficiency comparisons demonstrate that the proposed control strategy in the FSBB meets high efficiency in the wide conversion ratio and wide loads. The proposed control strategy meets the constant switching frequency requirement, which eases the EMC design.

C. Loss Comparison With FSBB in CCM

The CCM control strategy for the FSBB converter is also a prevenient solution. In the comparisons, the series inductor is selected as 1 mH to meet less than 20% inductor current ripple for the conventional buck or boost mode in CCM. The filter inductor is designed as PQ50/50 core with 80 turns of winding. The switching frequency in CCM is also selected as 50 kHz.

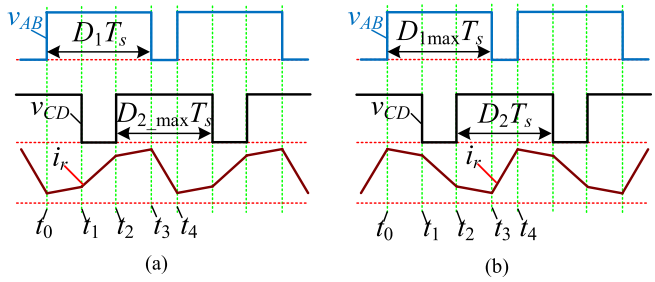


Fig. 26. Key waveforms of Method 1: Extended buck and (b) extended boost.

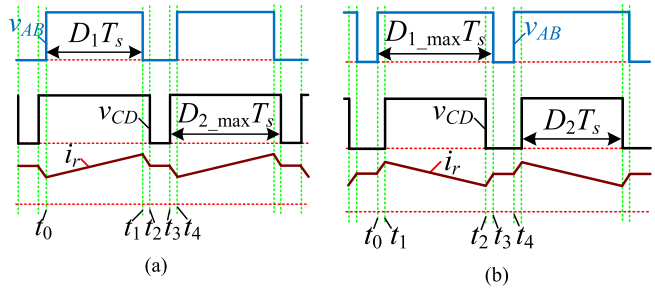


Fig. 27. Key waveforms of Method 2: Extended buck and (b) extended boost.

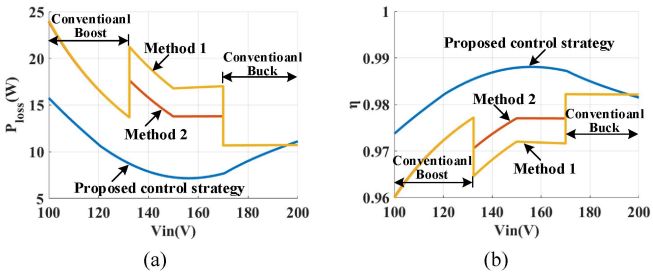


Fig. 28. Loss and efficiency curves versus the input voltage in the rated 600-W load power: (a) loss curves and (b) efficiency curves.

When the input voltage is 100 to 132 V, the converter works in the conventional boost mode. When the input voltage is 170 to 200 V, the converter works in the conventional buck mode. In the range from 132 to 170 V input voltage, the converter works in the extended buck or extended boost mode to solve the dead zone issue. The key waveforms of the extended buck and extended boost of Method 1 [26] are shown in Fig. 26. The key waveforms of the extended buck and extended boost of Method 2 [27] are shown in Fig. 27.

Fig. 28 shows the loss and efficiency curves versus the input voltage in the rated 600-W load power. To meet the low current ripple in the CCM, the filter inductor in the CCM is much larger than that in the proposed scheme. Therefore, the size of the filter inductor in CCM is much larger. Furthermore, the ESR of the inductor in the CCM also becomes larger. Designing the filter inductor in the CCM by the same litz wire as the proposed prototype, the ESR of the filter inductor in the CCM is 0.4 Ω. Therefore, the copper loss of the filter inductor in the CCM is the dominant loss in the converter. As seen in Fig. 28(a), the loss of the conventional boost and buck converter is larger than the proposed control strategy. In the extended boost and extended buck modes for eliminating the dead zone issue, the average current in the series inductor becomes larger. Therefore, the conduction loss in the switches and copper loss in the series inductor is increased. Furthermore, the switching loss is also larger than the conventional buck and boost converter. The loss in the extended buck and extended boost mode is significantly increased. Therefore, the efficiency curves drop dramatically when the input voltage becomes close to the output voltage. The proposed control strategy can meet ZVS, and low series inductance has lower core loss and copper loss. Therefore, the efficiency curves in Fig. 28(b) illustrate that the efficiency of the proposed control strategy in wide input voltage is higher than the converter in the CCM.

TABLE II
DETAILED SPECIFICATIONS

Items	Symbol	Parameter
Input voltage	V_{in}	100–200 V
Output voltage	V_o	150 V
Switching frequency (period)	$f_s(T_s)$	50 *k*Hz (20 μs)
Switches	$Q_{1\text{-}4}$	C3M0120065J (Cree)
Inductance	L_r	50 μH
Dead time	t_{dead}	200 *ns*

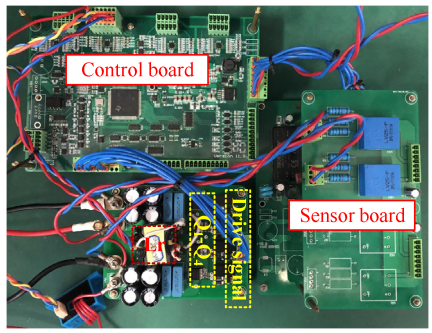


Fig. 29. Prototype for the test.

V. EXPERIMATAL VALIDATION

An experimental prototype was built to verify the control strategy of the FSBB converter. The detailed specifications are shown in Table II. The control strategy is implemented in TMS320F28335, whose internal ADC module is used to sample the output voltage. The analog comparator is MAX941 produced by Maxim Integrated Products. The analogy reference is generated by a 12-bit digital-to-analog converter MCP4726 produced by Microchip. Fig. 29 is the prototype for the test.

Fig. 30 shows the key waveforms of the boost mode in 100-V input voltage. Fig. 19(a) shows the result of 300-W load power. The converter works in Mode 2. Fig. 19(b) shows the experimental results of 600-W load power. As seen, the converter is switched to Mode 3 with the increase of the load power.

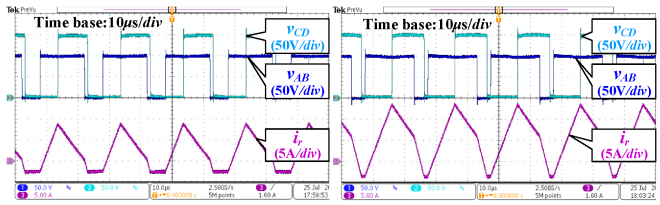


Fig. 30. Steady-state waveforms of the boost mode in 100-V input voltage. (a) 300-W load power. (b) 600-W load power.

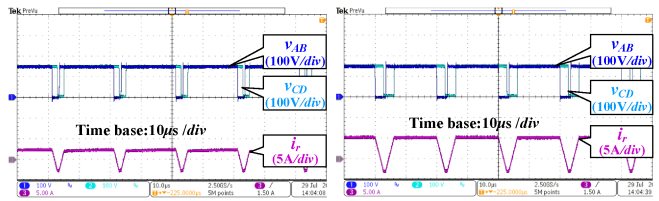


Fig. 31. Steady-state waveform for $M = 1$. (a) 300-W load power. (b) 600-W load power.

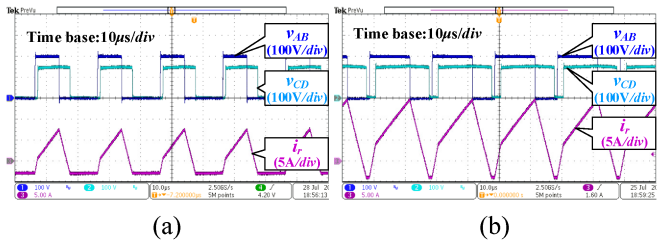


Fig. 32. Steady-state waveform in buck mode. (a) 300-W load power. (b) 1000-W load power.

Fig. 31 shows the key waveforms when the input voltage is equal to the output voltage. As seen in Fig. 8(b), the converter works in Mode 3 for the whole load power, when the conversion ratio is 1. Fig. 31(a) shows the experimental results for 300-W load power, and Fig. 31(b) shows the experimental results for 600-W load power. In both cases, the converter works in Mode 3. Because the input voltage is equal to the output voltage, the slew rate of the inductor current during the power transmission period is zero.

Fig. 32 shows the key waveforms of the buck mode in 200-V input voltage. Fig. 32(a) shows the experimental results of 300-W load power while the converter works in Mode 1. Fig. 32(b) shows the experimental result of 1000-W load power. In this case, the converter works in Mode 3. The experimental results demonstrate that the control strategy can meet a wide conversion ratio and wide loads.

Fig. 33 shows the drain-source voltages and gate signals of the four switches in boost mode. All the drain-source voltages of the four switches are dropped to zero before the switches are turned ON. Therefore, all the switches can achieve ZVS in buck mode. Fig. 34 shows the drain-source voltages and gate signals

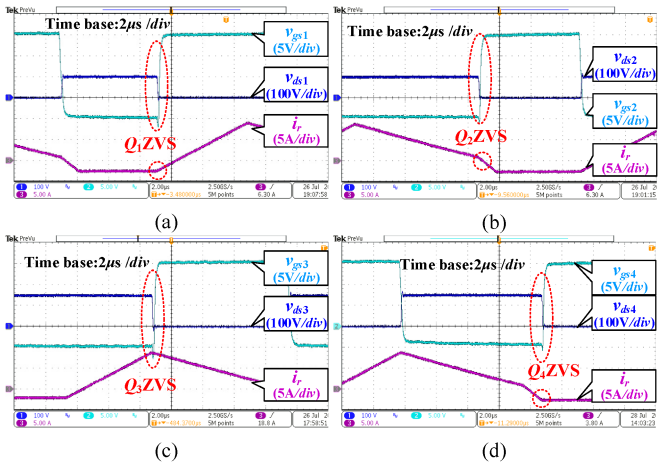


Fig. 33. Gate signals and drain-source voltage of the switches in boost mode: (a) Q_1, (b) Q_2, (c) Q_3, and (d) Q_4.

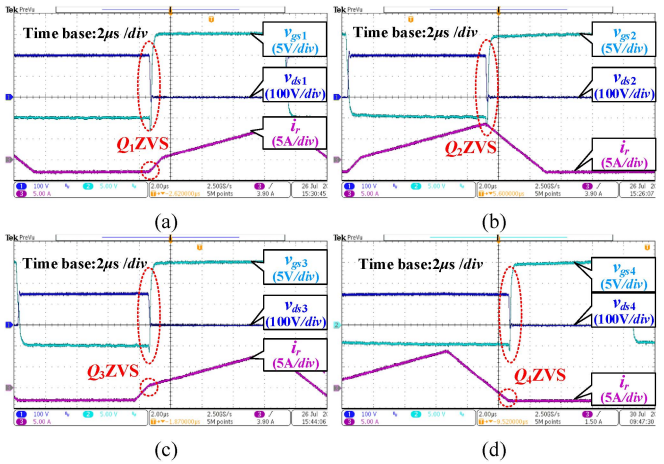


Fig. 34. Gate signals and drain-source voltage of the switches in buck mode: (a) Q_1, (b) Q_2, (c) Q_3, and (d) Q_4.

of the four switches in buck mode. All the switches also can achieve the ZVS.

Fig. 35 shows the dynamic response for the load step change. Fig. 35(a) shows the dynamic response in boost mode from 300 to 600 W load power, where the converter is switched from Mode 2 to Mode 3. Fig. 35(b) shows the dynamic response in buck mode from 300 to 1000 W load power, where the converter is switched from Mode 1 to Mode 3. In both boost and buck modes, the converter possesses a good dynamic response. The working modes are switched seamlessly during the load step change.

Efficiency curves of the proposed control strategy and CRM control are shown in Fig. 36. The proposed control strategy can reduce the conduction loss with the constant switching frequency. Meanwhile, the core loss in the series inductor is reduced because of a lower peak current. The proposed control strategy also solves the dead zone issue when the conversion ratio is close to one. Therefore, the proposed converter can achieve higher efficiency in a wide conversion ratio and wide loads.

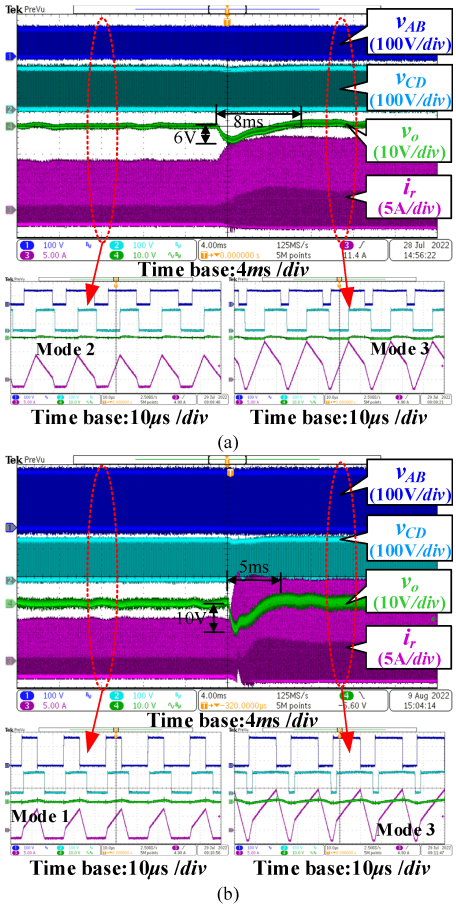


Fig. 35. Dynamic response of the load step change: (a) boost mode and (b) buck mode.

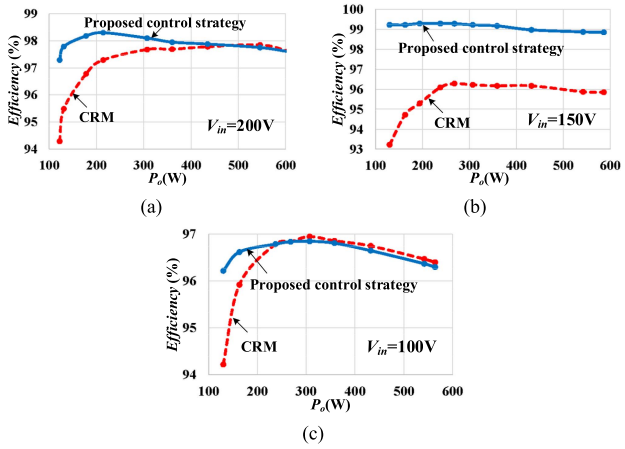


Fig. 36. Efficiency curves for proposed control strategy and CRM control strategy: (a) $V_{in} = 200$ V, (b) $V_{in} = 150$ V, and (b) $V_{in} = 100$ V.

VI. Conclusion

In this article, a control strategy for the FSBB converter is proposed to improve the efficiency in the wide conversion ratio and wide loads. The control strategy is based on the optimized current stress and ZVS constraints. To achieve the seamless transition between the different working modes, load power surfaces and the modulation surface versus the conversion ratio and control variable are analyzed. It demonstrates that the working modes can cover the whole load power in a wide conversion ratio. The control strategy implemented in the digital controller is proposed with the aid of an analog comparator, which can guarantee the initial current in a switching period meet the ZVS constraint with lower conduction loss. Because of the constant switching frequency, the proposed strategy can ease the EMC design. Furthermore, the dead zone issue is solved by using the proposed control strategy. The experimental prototype verifies the control strategy and efficiency improvement.

References

[1] M. Gaboriault and A. Notman, "A high efficiency, noninverting, buck-boost DC-DC converter," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2004, pp. 1411–1415.

[2] Y.-J. Lee, A. Khaligh, and A. Emadi, "A compensation technique for smooth transitions in a noninverting buck–boost converter," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 1002–1015, Apr. 2009.

[3] Y. Tsai, Y. Tsai, C. Tsai, and C. Tsai, "Digital noninverting-buck–boost converter with enhanced duty-cycle-overlap control," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 64, no. 1, pp. 41–45, Jan. 2017.

[4] D. C. Jones and R. W. Erickson, "A nonlinear state machine for dead zone avoidance and mitigation in a synchronous noninverting buck–boost converter," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 467–480, Jan. 2013.

[5] D. C. Jones and R. W. Erickson, "Buck-boost converter efficiency maximization via a nonlinear digital control mapping for adaptive effective switching frequency," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 153–165, Sep. 2013.

[6] J. Chen, P. Shen, and Y. Hwang, "A high-efficiency positive buck–boost converter with mode-select circuit and feed-forward techniques," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4240–4247, Sep. 2013.

[7] C. Wei, C. Chen, K. Wu, and I. Ko, "Design of an average-current-mode noninverting buck–boost dc–dc converter with reduced switching and conduction losses," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4934–4943, Dec. 2012.

[8] Y. Lee, A. Khaligh, A. Chakraborty, and A. Emadi, "Digital combination of buck and boost converters to control a positive buck–boost converter and improve the output transients," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1267–1279, May 2009.

[9] J. Ma, M. Zhu, Y. Li, and X. Cai, "Dynamic analysis of multimode buck–boost converter: An LPV system model point of view," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 8539–8551, Jul. 2021.

[10] X. Huang, F. C. Lee, Q. Li, and W. Du, "High-frequency high-efficiency GaN-based interleaved CRM bidirectional buck/boost converter with inverse coupled inductor," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4343–4352, Jun. 2016.

[11] J.-H. Park and B.-H. Cho, "The zero voltage switching (ZVS) critical conduction mode (CRM) buck converter with tapped-inductor," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 762–774, Jul. 2005.

[12] X. Ren, Z. Guo, Y. Wu, Z. Zhang, and Q. Chen, "Adaptive LUT-based variable on-time control for CRM boost PFC converters," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8123–8136, Sep. 2018.

[13] H. V. Nguyen, D.-C. Lee, and F. Blaabjerg, "A novel SiC-based multifunctional onboard battery charger for plug-in electric vehicles," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5635–5646, May 2021.

[14] Z. Yu, H. Kapels, and K. F. Hoffmann, "High efficiency bidirectional DC–DC converter with wide input and output voltage ranges for battery systems," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Manage.*, 2015, pp. 1–8.

[15] S. Waffler and J. W. Kolar, "A novel low-loss modulation strategy for high-power bidirectional buck-boost converters," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1589–1599, Jun. 2009.

[16] Z. Yu, H. Kapels, and K. F. Hoffmann, "Extreme high efficiency non-inverting buck-boost converter for energy storage systems," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2016, pp. 1–8.

[17] Z. Zhou, H. Li, and X. Wu, "A constant frequency ZVS control system for the four-switch buck–boost DC–DC converter with reduced inductor current," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 5996–6003, Jul. 2019.
[18] J. Yu, M. Liu, D. Song, J. Yang, and M. Su, "A soft-switching control for cascaded buck-boost converters without zero-crossing detection," *IEEE Access*, vol. 7, pp. 32522–32536, 2019.
[19] A. Rodríguez-Lorente, A. Barrado, C. Calderón, C. Fernández, and A. Lázaro, "Non-inverting and non-isolated magnetically coupled buck–boost bidirectional DC–DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11942–11954, Nov. 2020.
[20] Z. Guo, "Modulation scheme of dual active bridge converter for seamless transitions in multiworking modes compromising ZVS and conduction loss," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7399–7409, Sep. 2020.
[21] H. Higa, A. Sagawa, and J. Itoh, "Improvement of light load efficiency for buck–boost DC–DC converter with ZVS using switched auxiliary inductors," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, 2018, pp. 1–6.
[22] W. Han and L. Corradini, "Wide-range ZVS control technique for bidirectional dual-bridge series-resonant DC–DC converters," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10256–10269, Oct. 2019.
[23] S. Mu, Z. Guo, and Y. Luo, "Universal modulation scheme to suppress transient DC bias current in dual active bridge converters," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1322–1333, Feb. 2022.
[24] J. Huang, Y. Wang, Z. Li, and W. Lei, "Unified triple-phase-shift control to minimize current stress and achieve full soft-switching of isolated bidirectional DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4169–4179, Jul. 2016.
[25] J. Muhlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Core losses under the DC bias condition based on Steinmetz parameters," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 953–963, Feb. 2012.
[26] N. Zhang, S. Batternally, K. C. Lim, K. W. See, and F. Han, "Analysis of the non-inverting buck-boost converter with four-mode control method," in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, 2017, pp. 876–881.
[27] Y. Bai, Z. Zhu, Z. Yang, S. Zha, and S. Hu, "Analysis and comparison of inductor current characteristics for non-inverting buck–boost converter with four-mode modulation," in *Proc. IEEE 5th Int. Elect. Energy Conf.*, 2022, pp. 2534–2540.

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