D-Q Impedance Modeling and Stability Analysis of a Three-Phase Four-Wire System With Single-Phase Loads

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***Abstract*—The impedance-based method has been widely adopted for the stability analysis of ac systems. The *d-q* frame impedance modeling method is commonly used for balanced three-phase three-wire system analysis because it transforms the system into a time-invariant one and makes linearization achievable. However, for three-phase four-wire systems with considerable neutral line impedance, it is not feasible to directly apply the conventional *d-q* frame impedance modeling method. This article exploits the virtual frame concept to model and analyze the stability of a three-phase four-wire system with single-phase loads in a time-invariant framework. The upstream and downstream impedance models are proposed, which can accurately predict system stability conditions. The proposed models can be used for impedance specifications and assist system-level design from the stability perspective. Both simulation and experimental results validate the model and demonstrate its effectiveness in analyzing the stability of a three-phase four-wire system.**

***Index Terms*—*D-Q* model, impedance-based stability analysis, low-frequency oscillations, three-phase four-wire system, time-invariant framework.**

I. Introduction

SEVERAL data center power systems with a three-phase four-wire configuration have been reported to suffer from low-frequency oscillation instability [1], [2], [3], as shown in Fig. 1. It is a result of the dynamic interactions among the power source, distribution lines, and the many single-phase power supply unit (PSU) loads. This instability may happen in other systems with similar structures, for example, a charging station with many electric vehicle chargers working together [4]. To understand and avoid similar phenomena, it is essential to model and analyze the stability of such three-phase four-wire systems.

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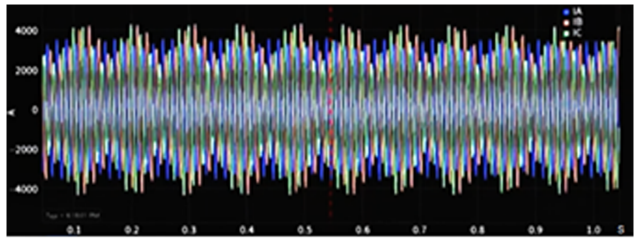

Fig. 1. Main switchboard current in a resonance incident in a Facebook data center in 2017 [1].

The method of impedance-based stability analysis has been developed for cascaded power electronics systems [5], [6]. This method offers practical advantages as it does not necessarily require knowledge of the internal parameters of the system [7], [8], [9], [10], [11], [12]. Instead, system designers can use instrumentation to measure the upstream impedances and set requirements for the downstream impedances or vice versa, based on their desired stability margins [13], [14].

The use of impedance-based stability analysis is widespread in both dc and ac systems [15], [16]. While dc systems are relatively straightforward to analyze due to their inherent equilibrium operating point, ac systems present more complex challenges due to their time-varying and multi-input-multioutput (MIMO) system properties. Researchers have developed various impedance-based approaches for ac system stability analysis, including the sequence impedance approach, the *d-q* impedance method, the dynamic phasors method, etc. These methods have been used to model and study three-phase balanced systems, such as the voltage source converter [17], [18], [19]. The sequence impedance method is based on harmonic linearization under a time-periodic framework [20], [21]. Initially, it was defined separately for positive and negative sequences [22]. However, coupling between the two sequences was later identified, leading to the development of a modified sequence impedance concept [23], [24]. The *d-q* impedance method is widely used for analyzing balanced three-phase systems. It involves a coordinate transformation to establish an equilibrium point for classical ac analysis, similar to a dc system [17]. The relationship between the 2×2 sequence impedance and *d-q* impedance is also established in [25]. The dynamic phasor method utilizes an average modeling of the time-varying Fourier series coefficients

of the system variables. It is more commonly used in state-space modeling [26], [27].

The above-mentioned methods have also been applied to model other types of systems, such as single-phase systems and three-phase unbalanced systems. For instance, the authors in [3], [28], and [29] employed the sequence impedance concept to model and analyze the stability of systems with single-phase converters. Based on *d-q* domain analysis, the authors in [30], [31], [32], and [33] created virtual frames for single-phase loads and transformed the artificial "balanced three-phase systems" into their virtual *d-q* frames to obtain dc operating points and conduct small-signal analysis. The dynamic phasor method presented in [34] modeled a single-phase rectifier, demonstrating its equivalence with the *d-q* frame-based method when neglecting 0-phasor components such as dc voltage. However, stability issues can arise due to dc dynamics, which must be carefully considered.

A three-phase four-wire system is another type of system that cannot always be analyzed using techniques applicable to a balanced three-phase three-wire system. This is due to the presence of non-negligible neutral line impedance, possible unbalanced conditions, and single-phase load dynamics. While Sun et al. [3] analyzed the stability of such a system using sequence impedance, it may be difficult for some engineers and students to understand the time-periodic framework, since it may involve challenging concepts such as frequency domain linearization, exponentially modulated periodic signals, etc. [20]. Therefore, investigating the possibility of analyzing such systems' stability in a linear-time-invariant framework is desirable. The virtual frame concept, which is used for single-phase converter modeling to achieve a time-invariant system, holds promise for this purpose. When there is no neutral line impedance in the four-wire system, the three phases of the four-wire system can be treated as independent single-phase systems since they are wholly decoupled. However, modeling the system becomes challenging when there are non-negligible neutral impedances.

While some literature has addressed a four-wire system with a three-phase four-wire converter, there is little research on analyzing three-phase four-wire systems with single-phase loads. Jacobina et al. [35] and Khadkikar and Chandra [36] designed the current control of an unbalanced three-phase four-wire voltage source converter by creating virtual circuits of each phase. Zhang et al. [37] utilized the *dq*0 modeling method for an unbalanced four-wire converter, but its effectiveness for four-wire systems with single-phase loads is uncertain due to the differing dc bus dynamics of the loads among the three phases.

To the authors' knowledge, no existing literature has explored impedance-based stability analysis of three-phase four-wire systems with single-phase loads in a time-invariant framework. However, such an application is important. To address this gap, this article proposes a model within the time-invariant framework applicable to both balanced and unbalanced conditions.

The contributions of this article are summarized as follows.

1) This article developed a new *d-q* frame impedance model that enables the use of time-invariant system linearization theory for a three-phase four-wire system with non-negligible neutral impedance and single-phase loads.
2) This article proposed a 6×6 matrix format minor loop gain model that applies to both balanced and unbalanced scenarios for a three-phase four-wire system. This model simplifies to a 2×2 matrix for scenarios with a large neutral line inductor and a 1×1 matrix for balanced cases. These simplified models provide a simple analytical tool to assess the system stability quickly and express the impact of the neutral-line impedance and load power on the system stability margin.
3) The proposed model accurately predicts stability and oscillation frequency, therefore the proposed impedance model can characterize the system properties, which can further provide design guidelines, such as sizing distribution lines, PFC controller parameters specifications, and load power capacity.
4) This article identified the detrimental impact of the neutral line on low-frequency instability and the damping benefits on high-frequency resonance, providing a guideline for the design of neutral line reactors.

The rest of this article is organized as follows. Section II illustrates the virtual *d-q* frame modeling method of the studied three-phase four-wire system. Section III proposed the upstream and downstream impedance models based on the *d-q* model. Sections IV and V verified the proposed models using simulation and experiments. Section VI discusses the neutral-line impedance's stability impact and system impedance specifications. Finally, Section VII concludes this article.

II. Proposed Virtual D-Q Frame Model of a Three-Phase Four-Wire System

This section proposes a virtual *d-q* frame model for a three-phase four-wire system with single-phase loads, as shown in Fig. 2(a). The main idea of the modeling approach is shown in Fig. 2. By regarding each phase as a single-phase circuit while still considering the coupling among the three single-phase circuits, another two virtual frames *y* and *z* are constructed for each phase, and a *d-q* frame model can be obtained by Park's transformation. This process can also be derived mathematically using the circuit equations as shown below. First, the equations describing the original system are

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} - \begin{bmatrix} Z_{ga}+Z_{gn} & Z_{gn} & Z_{gn} \\ Z_{gn} & Z_{gb}+Z_{gn} & Z_{gn} \\ Z_{gn} & Z_{gn} & Z_{gc}+Z_{gn} \end{bmatrix} \times \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix}. \tag{1}$$

Defining transformation matrix $\mathbf{T_a}$, $\mathbf{T_b}$, $\mathbf{T_c}$ so that

$$\begin{bmatrix} v_{ax} \\ v_{ay} \\ v_{az} \end{bmatrix} = \mathbf{T_a} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \quad \begin{bmatrix} v_{bx} \\ v_{by} \\ v_{bz} \end{bmatrix} = \mathbf{T_b} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \quad \begin{bmatrix} v_{cx} \\ v_{cy} \\ v_{cz} \end{bmatrix} = \mathbf{T_c} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2}$$

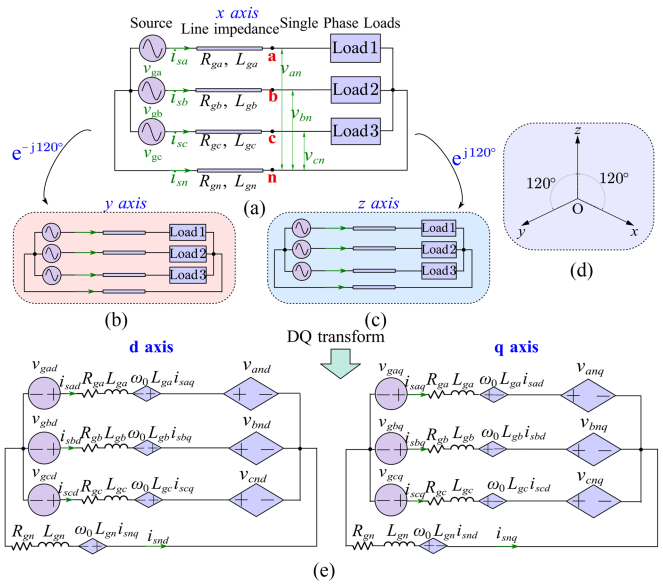

Fig. 2. Virtual *d-q* frame modeling method. (a) Original systems. (b) Virtual frame *y* system. (c) Virtual *z* frame system. (d) Frame difference of *x*, *y*, and *z*. (e) *D-Q* model.

$$\mathbf{T_a} = \begin{bmatrix} 1 & 0 & 0 \\ a & 0 & 0 \\ a^2 & 0 & 0 \end{bmatrix}, \mathbf{T_b} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & a & 0 \\ 0 & a^2 & 0 \end{bmatrix},$$

$$\mathbf{T_c} = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & a \\ 0 & 0 & a^2 \end{bmatrix} \tag{3}$$

$$a = e^{-j120^\circ}. \tag{4}$$

Multiplying $\mathbf{T_a}$, $\mathbf{T_b}$, and $\mathbf{T_c}$ respectively to the (1) yield

$$\begin{bmatrix} v_{anx} \\ v_{any} \\ v_{anz} \end{bmatrix} = \begin{bmatrix} v_{gax} \\ v_{gay} \\ v_{gaz} \end{bmatrix} - Z_{ga} \begin{bmatrix} i_{sax} \\ i_{say} \\ i_{saz} \end{bmatrix} + Z_{gn} \begin{bmatrix} i_{snx} \\ i_{sny} \\ i_{snz} \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} v_{bnx} \\ v_{bny} \\ v_{bnz} \end{bmatrix} = \begin{bmatrix} v_{gbx} \\ v_{gby} \\ v_{gbz} \end{bmatrix} - Z_{gb} \begin{bmatrix} i_{sbx} \\ i_{sby} \\ i_{sbz} \end{bmatrix} + Z_{gn} \begin{bmatrix} i_{snx} \\ i_{sny} \\ i_{snz} \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} v_{cnx} \\ v_{cny} \\ v_{cnz} \end{bmatrix} = \begin{bmatrix} v_{gcx} \\ v_{gcy} \\ v_{gcz} \end{bmatrix} - Z_{gc} \begin{bmatrix} i_{scx} \\ i_{scy} \\ i_{scz} \end{bmatrix} + Z_{gn} \begin{bmatrix} i_{snx} \\ i_{sny} \\ i_{snz} \end{bmatrix} \tag{7}$$

where

$$\begin{bmatrix} i_{snx} \\ i_{sny} \\ i_{snz} \end{bmatrix} = -\left(\begin{bmatrix} i_{sax} \\ i_{say} \\ i_{saz} \end{bmatrix} + \begin{bmatrix} i_{sbx} \\ i_{sby} \\ i_{sbz} \end{bmatrix} + \begin{bmatrix} i_{scx} \\ i_{scy} \\ i_{scz} \end{bmatrix} \right). \tag{8}$$

By applying the *d-q* transformation to (5), (6), and (7), the system's *d-q* frame model can be derived as

$$\begin{bmatrix} v_{and} \\ v_{anq} \end{bmatrix} = \begin{bmatrix} v_{gad} \\ v_{gaq} \end{bmatrix} - \mathbf{Z_{ga}} \begin{bmatrix} i_{sad} \\ i_{saq} \end{bmatrix} + \mathbf{Z_N} \begin{bmatrix} i_{snd} \\ i_{snq} \end{bmatrix} \tag{9}$$

$$\begin{bmatrix} v_{bnd} \\ v_{bnq} \end{bmatrix} = \begin{bmatrix} v_{gbd} \\ v_{gbq} \end{bmatrix} - \mathbf{Z_{gb}} \begin{bmatrix} i_{sbd} \\ i_{sbq} \end{bmatrix} + \mathbf{Z_N} \begin{bmatrix} i_{snd} \\ i_{snq} \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} v_{cnd} \\ v_{cnq} \end{bmatrix} = \begin{bmatrix} v_{gcd} \\ v_{gcq} \end{bmatrix} - \mathbf{Z_{gc}} \begin{bmatrix} i_{scd} \\ i_{scq} \end{bmatrix} + \mathbf{Z_N} \begin{bmatrix} i_{snd} \\ i_{snq} \end{bmatrix} \tag{11}$$

$$-\begin{bmatrix} i_{snd} \\ i_{snq} \end{bmatrix} = \begin{bmatrix} i_{sad} \\ i_{saq} \end{bmatrix} + \begin{bmatrix} i_{sbd} \\ i_{sbq} \end{bmatrix} + \begin{bmatrix} i_{scd} \\ i_{scq} \end{bmatrix}. \tag{12}$$

Equation (13) shows the expressions of $\mathbf{Z_{ga}}$, $\mathbf{Z_{gb}}$, $\mathbf{Z_{gc}}$, and $\mathbf{Z_N}$

$$\mathbf{Z_{ga}} = \begin{bmatrix} R_{ga} + sL_{ga} & -\omega_0 L_{ga} \\ \omega_0 L_{ga} & R_{ga} + sL_{ga} \end{bmatrix},$$

$$\mathbf{Z_{gb}} = \begin{bmatrix} R_{gb} + sL_{gb} & -\omega_0 L_{gb} \\ \omega_0 L_{gb} & R_{gb} + sL_{gb} \end{bmatrix}$$

$$\mathbf{Z_{gc}} = \begin{bmatrix} R_{gc} + sL_{gc} & -\omega_0 L_{gc} \\ \omega_0 L_{gc} & R_{gc} + sL_{gc} \end{bmatrix},$$

$$\mathbf{Z_N} = \begin{bmatrix} R_{gn} + sL_{gn} & -\omega_0 L_{gn} \\ \omega_0 L_{gn} & R_{gn} + sL_n \end{bmatrix}. \tag{13}$$

With (9)–(12), the original system's model in the virtual *d-q* frame can be pictured in a circuit diagram, as shown in Fig. 2(e). This method is essentially treating each phase as a single-phase circuit while preserving the coupling effects among the three phases because they are in the same three-phase system.

Since the two virtual frame circuits are created by phase-shifting the original system, the stability condition of the original three-phase system is equivalent to that of the two virtual circuits and the new system in the *xyz* coordinate. Therefore, the stability of the original system can be assessed by performing an impedance analysis on the small-signal model of the system based on Fig. 2(e).

III. Proposed Virtual D-Q Frame Impedance Model for Stability Analysis

For impedance-based small-signal stability analysis, the main steps include first defining an interface for analysis, then obtaining the upstream impedance and downstream admittance, defining the minor loop gain matrix, and finally applying the generalized Nyquist criterion (GNC) to the minor-loop-gain. For impedance analysis, this article groups the power source and the distribution line as the upstream subsystem, and the single-phase loads as the downstream subsystem. With the time-invariant system *d-q* model in Fig. 2(e), it is feasible to perform a small-signal analysis. In this section, the impedance models of a four-wire system with single-phase PSU loads are first derived. Then they are simplified for a dominant neutral inductor scenario and further simplified for three-phase balanced cases.

A. Generic Model

Assuming a certain equilibrium operating point, the following small-signal relationships can be obtained after linearizing (9)–(12)

$$\begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} = -\mathbf{Z_{ga}} \begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} + \mathbf{Z_N} \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} \tag{14}$$

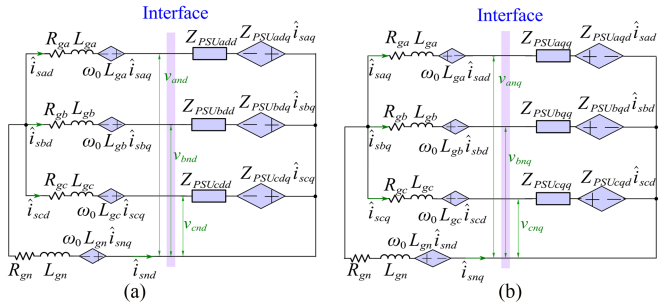

Fig. 3. Small-signal model of a four-wire system in the *d-q* frame. (a) *d* axis model. (b) *q* axis model.

$$\begin{bmatrix} \hat{v}_{bnd} \\ \hat{v}_{bnq} \end{bmatrix} = -\mathbf{Z_{gb}} \begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix} + \mathbf{Z_N} \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} \tag{15}$$

$$\begin{bmatrix} \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix} = -\mathbf{Z_{gc}} \begin{bmatrix} \hat{i}_{scd} \\ \hat{i}_{scq} \end{bmatrix} + \mathbf{Z_N} \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} \tag{16}$$

$$-\begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} = \begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} + \begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix} + \begin{bmatrix} \hat{i}_{scd} \\ \hat{i}_{scq} \end{bmatrix}. \tag{17}$$

For each single-phase PSU load, the relationship between its input voltage and current small-signal components is its *d-q* admittance, as shown in (18)–(20)

$$\begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \end{bmatrix} = \mathbf{Y_{PSUa}} \begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} = \begin{bmatrix} Y_{PSUadd} & Y_{PSUadq} \\ Y_{PSUaqd} & Y_{PSUaqq} \end{bmatrix} \times \begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} \tag{18}$$

$$\begin{bmatrix} \hat{i}_{sbd} \\ \hat{i}_{sbq} \end{bmatrix} = \mathbf{Y_{PSUb}} \begin{bmatrix} \hat{v}_{bnd} \\ \hat{v}_{bnq} \end{bmatrix} = \begin{bmatrix} Y_{PSUbdd} & Y_{PSUbdq} \\ Y_{PSUbqd} & Y_{PSUbqq} \end{bmatrix} \times \begin{bmatrix} \hat{v}_{bnd} \\ \hat{v}_{bnq} \end{bmatrix} \tag{19}$$

$$\begin{bmatrix} \hat{i}_{scd} \\ \hat{i}_{scq} \end{bmatrix} = \mathbf{Y_{PSUc}} \begin{bmatrix} \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix} = \begin{bmatrix} Y_{PSUcdd} & Y_{PSUcdq} \\ Y_{PSUcqd} & Y_{PSUcqq} \end{bmatrix} \times \begin{bmatrix} \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix}. \tag{20}$$

Given (14)–(20), the small-signal model in the virtual *d-q* frame is shown in Fig. 3.

The interface for impedance analysis is chosen to be the input of the PSU loads, as shown in Fig. 3. From the interface, the upstream impedance is defined as follows:

$$\begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \\ \hat{v}_{bnd} \\ \hat{v}_{bnq} \\ \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix} = \mathbf{Z_{source}} \cdot \begin{bmatrix} -\hat{i}_{sad} \\ -\hat{i}_{saq} \\ -\hat{i}_{sbd} \\ -\hat{i}_{sbq} \\ -\hat{i}_{scd} \\ -\hat{i}_{scq} \end{bmatrix}. \tag{21}$$

From (14)–(17) and (21), the upstream impedance is

$$\mathbf{Z_{source}} = \begin{bmatrix} \mathbf{Z_N} + \mathbf{Z_{ga}} & \mathbf{Z_N} & \mathbf{Z_N} \\ \mathbf{Z_N} & \mathbf{Z_N} + \mathbf{Z_{gb}} & \mathbf{Z_N} \\ \mathbf{Z_N} & \mathbf{Z_N} & \mathbf{Z_N} + \mathbf{Z_{gc}} \end{bmatrix}. \tag{22}$$

The off-diagonal terms of (22) denote the coupling among the three phases. Looking at the interface, the downstream admittance is defined as follows:

$$\begin{bmatrix} \hat{i}_{sad} \\ \hat{i}_{saq} \\ \hat{i}_{sbd} \\ \hat{i}_{sbq} \\ \hat{i}_{scd} \\ \hat{i}_{scq} \end{bmatrix} = \mathbf{Y_{load}} \begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \\ \hat{v}_{bnd} \\ \hat{v}_{bnq} \\ \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix}. \tag{23}$$

From (18)–(20) and (23), the downstream impedance is defined as follows:

$$\mathbf{Y_{load}} = \begin{bmatrix} \mathbf{Y_{PSUa}} & 0 & 0 \\ 0 & \mathbf{Y_{PSUb}} & 0 \\ 0 & 0 & \mathbf{Y_{PSUc}} \end{bmatrix}. \tag{24}$$

Notably, $\mathbf{Y_{PSUa}}$, $\mathbf{Y_{PSUb}}$, and $\mathbf{Y_{PSUc}}$ are defined with the *d*-axis aligned with v_{anx}. The system minor loop gain is defined as

$$\mathbf{L_{sys}} = \mathbf{Z_{source}} \cdot \mathbf{Y_{load}}. \tag{25}$$

Since $\mathbf{Z_{ga}}$, $\mathbf{Z_{gb}}$, $\mathbf{Z_{gc}}$, $\mathbf{Z_N}$, $\mathbf{Y_{PSUa}}$, $\mathbf{Y_{PSUb}}$, and $\mathbf{Y_{PSUc}}$ are all 2×2 matrices, $\mathbf{Z_{source}}$, $\mathbf{Y_{load}}$, and $\mathbf{L_{sys}}$ are 6×6 matrices. If the system has negligible neutral-line impedance, (22) and (25) become

$$\mathbf{Z_{source}} = \begin{bmatrix} \mathbf{Z_{ga}} & 0 & 0 \\ 0 & \mathbf{Z_{gb}} & 0 \\ 0 & 0 & \mathbf{Z_{gc}} \end{bmatrix} \tag{26}$$

$$\mathbf{L_{sys}} = \begin{bmatrix} \mathbf{Z_{ga}}\mathbf{Y_{PSUa}} & 0 & 0 \\ 0 & \mathbf{Z_{gb}}\mathbf{Y_{PSUb}} & 0 \\ 0 & 0 & \mathbf{Z_{gc}}\mathbf{Y_{PSUc}} \end{bmatrix}. \tag{27}$$

Therefore, the three phases are decoupled and become three independent single-phase circuits. Thus, the model in (27) is the same as using the existing virtual *d-q* frame modeling method to analyze each phase as a single-phase circuit.

B. System With Dominant Neutral-Line Inductor

In some data center power systems, a three-phase four-wire system may equip with a high neutral-line inductor due to the purpose of limiting short-circuit currents in fault conditions, or due to thinner cable design with lower current capacity compared with three-phase lines. The system model can be simplified from the generic one discussed above. Since the phase impedance is much smaller than the neutral-line impedance, it is neglected. Equations (14)–(16) can then be written as follows:

$$\begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} = \begin{bmatrix} \hat{v}_{bnd} \\ \hat{v}_{bnq} \end{bmatrix} = \begin{bmatrix} \hat{v}_{cnd} \\ \hat{v}_{cnq} \end{bmatrix} = \mathbf{Z_N} \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix}$$

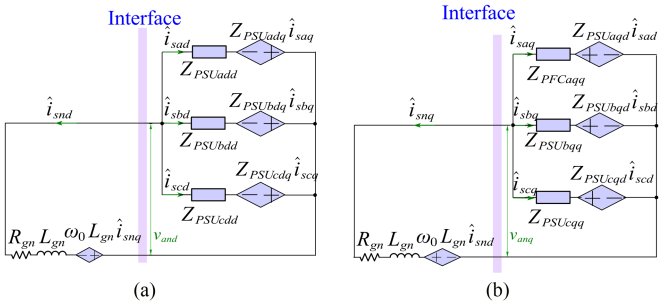

Fig. 4. Small-signal model of a four-wire system with a dominant neutral inductor in the *d-q* frame. (a) *d* axis model. (b) *q* axis model.

$$= \begin{bmatrix} Z_{Ndd} & Z_{Ndq} \\ Z_{Nqd} & Z_{Nqq} \end{bmatrix} \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix}. \tag{28}$$

Equations (17)–(20) and (28) yield the following:

$$\begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix} = (\mathbf{Y_{PSUa}} + \mathbf{Y_{PSUb}} + \mathbf{Y_{PSUc}}) \begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix}. \tag{29}$$

From (28) and (29), the system's small-signal model in the virtual *d-q* frame can be pictured in Fig. 4. From the interface, the upstream impedance is defined as

$$\begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} = \mathbf{Z_{source}} \begin{bmatrix} \hat{i}_{snd} \\ \hat{i}_{snq} \end{bmatrix}. \tag{30}$$

From (28), $\mathbf{Z_{source}}$ is equal to $\mathbf{Z_N}$. Looking at the interface, the downstream admittance is defined as follows:

$$\begin{bmatrix} \hat{v}_{and} \\ \hat{v}_{anq} \end{bmatrix} = \mathbf{Y_{load}} \begin{bmatrix} -\hat{i}_{snd} \\ -\hat{i}_{snq} \end{bmatrix}. \tag{31}$$

Therefore, for dominant neutral inductor scenarios, $\mathbf{Z_{source}}$, $\mathbf{Y_{load}}$, and $\mathbf{L_{sys}}$ are 2×2 matrices. Notably, the operating points on the *d-q* frame of PSU for phase *a*, phase *b*, and phase *c* are different because they are transferring to the *d-q* frame aligning with the same angle.

From (29), the downstream impedance is

$$\mathbf{Y_{load}} = \mathbf{Y_{PSUa}} + \mathbf{Y_{PSUb}} + \mathbf{Y_{PSUc}}. \tag{32}$$

For the three-phase balanced case, the difference among $\mathbf{Y_{PSUa}}$, $\mathbf{Y_{PSUb}}$, and $\mathbf{Y_{PSUc}}$ results from a different operating point only because of the phase-angle difference

$$\begin{cases} \mathbf{Y_{PSUb}} = \mathbf{T}_{-\frac{2\pi}{3}} \mathbf{Y_{PSUa}} \mathbf{T}^{-1}_{-\frac{2\pi}{3}} \\ \mathbf{Y_{PSUc}} = \mathbf{T}_{\frac{2\pi}{3}} \mathbf{Y_{PSUa}} \mathbf{T}^{-1}_{\frac{2\pi}{3}} \end{cases} \tag{33}$$

$$\mathbf{T}_{\Delta\theta} = \begin{bmatrix} \cos\Delta\theta & \sin\Delta\theta \\ -\sin\Delta\theta & \cos\Delta\theta \end{bmatrix}. \tag{34}$$

The single-phase PSU's admittance is diagonally dominant if the *d*-axis is aligned with the input voltage [30]. Therefore, $\mathbf{Y_{PSUa}}$ is diagonally dominant, and $\mathbf{Y_{PSUb}}$ and $\mathbf{Y_{PSUc}}$ can be approximated as (35) and (36) from (33) and (34)

$\mathbf{Y_{PSUb}}$

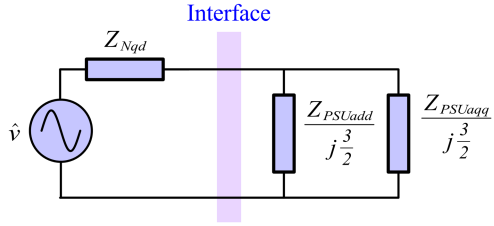

Fig. 5. Equivalent small-signal model of a balanced-four-wire system with dominant neutral line inductance in the *d-q* frame.

$$= \begin{bmatrix} \frac{1}{4}Y_{PSUadd} + \frac{3}{4}Y_{PSUaqq} & -\frac{\sqrt{3}}{4}\left(Y_{PSUadd} - Y_{PSUaqq}\right) \\ -\frac{\sqrt{3}}{4}\left(Y_{PSUadd} - Y_{PSUaqq}\right) & \frac{3}{4}Y_{PSUadd} + \frac{1}{4}Y_{PSUaqq} \end{bmatrix} \tag{35}$$

$\mathbf{Y_{PSUc}}$

$$= \begin{bmatrix} \frac{1}{4}Y_{PSUadd} + \frac{3}{4}Y_{PSUaqq} & \frac{\sqrt{3}}{4}\left(Y_{PSUadd} - Y_{PSUaqq}\right) \\ \frac{\sqrt{3}}{4}\left(Y_{PSUadd} - Y_{PSUaqq}\right) & \frac{3}{4}Y_{PSUadd} + \frac{1}{4}Y_{PSUaqq} \end{bmatrix}. \tag{36}$$

With a large neutral-line inductance, the grid-side impedance is off-diagonal dominant at low frequencies, such that,

$$|Z_{Ndd}|, |Z_{Nqq}| \approx 0. \tag{37}$$

With (35)–(37), the minor loop gain of the system can be simplified as

$\mathbf{L_{sys}} \approx$

$$\begin{bmatrix} 0 & Z_{Ndq}\left(Y_{PSUaqq} + 2Y_{PSUbqq}\right) \\ Z_{Nqd}\left(Y_{PSUadd} + 2Y_{PSUbdd}\right) & 0 \end{bmatrix}. \tag{38}$$

The characteristic equation of (38) can be derived as

$$\lambda^2 + Z_{Nqd}^2 \left(\frac{3}{2}Y_{PSUadd} + \frac{3}{2}Y_{PSUaqq}\right)^2 = 0. \tag{39}$$

So the two eigenvalues can be solved as follows:

$$\begin{cases} \lambda_1 = jZ_{Nqd}\left(\frac{3}{2}Y_{PSUadd} + \frac{3}{2}Y_{PSUaqq}\right) \\ \lambda_2 = -jZ_{Nqd}\left(\frac{3}{2}Y_{PSUadd} + \frac{3}{2}Y_{PSUaqq}\right) \end{cases}. \tag{40}$$

From (40), λ_1 and λ_2 have a negative phase. In this study, λ_1 is in the left half-plane, which is the critical one for stability analysis. The MIMO system stability analysis is equivalent to analyzing a single-input-single-output (SISO) system, such as that shown in Fig. 5. For the SISO system, it is sufficient to use a Bode plot criterion to assess system stability. The upstream impedance Z_{source} and downstream impedance Z_{load} are

$$Z_{source} = Z_{Nqd} \tag{41}$$

$$Z_{load} = 1/\left(1/\left(\frac{Z_{PSUadd}}{j\frac{3}{2}}\right) + 1/\left(\frac{Z_{PSUaqq}}{j\frac{3}{2}}\right)\right). \tag{42}$$

At low frequencies, the gain of Z_{PSUadd} and Z_{PSUaqq} is negatively proportional to the power level, and Z_{Nqd} is proportional to the neutral-line inductor value, (41) and (42) reveal

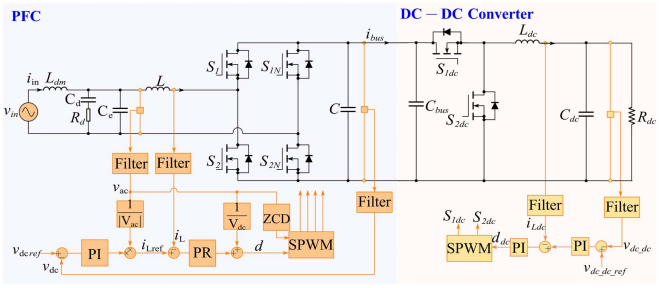

Fig. 6. PSU structure and control diagrams.

that to achieve a similar stability margin when increasing PSU load power by N times, the neutral-line inductor needs to be reduced to $1/N$ of its original value. This finding is important for performing impedance specifications in such scenarios.

IV. Simulation Verification

In a power-electronics-based system, typical instability issues occur because of the constant-power load behavior of the converters and their dynamic interactions with the inductive line impedance. To verify the proposed impedance-based models for stability analysis of a four-wire system, single-phase PSU loads with circuit and control diagrams shown in Fig. 6 are studied in Plecs. A PSU is composed of a front-end PFC and a cascaded dc-dc converter load. A totem-pole topology PFC converter operating in continuous-current mode is studied. Its controller contains a proportional-resonant (PR) based current controller, a proportional-integral (PI) based dc voltage controller, a phase-tracking unit, and an input voltage feedforward control. At low frequencies, both an isolated dc-dc converter and a nonisolated converter can be modeled as a negative resistor [38]. A buck converter is thus selected as the cascaded dc-dc converter in the simulation study because it is much easier to model. Its controller contains an inner current controller and an output dc voltage controller. Both use a PI controller. The parameters of the PFC and the dc-dc converter are shown in Table I. The subsystem impedance model in Section III requires the PSU load's d-q impedance. Based on the modeling and measurement method described in [30], the d-q impedance of the PSU loads when aligning the d-axis with its input voltage is shown in Fig. 7. The analytical model is shown in the Appendix. The Z_{dd} presents as a negative resistor below the PFC's dc voltage-loop bandwidth [39]. The three-phase four-wire system in the simulation is shown in Fig. 8.

Three ideal voltage sources provide power for the three PFC loads. There is some impedance at the cable in each phase and the neutral cable. To verify the 6×6 impedance matrix models for a generic four-wire system, four cases are conducted. The line impedance, voltage, and power level of each case are shown in Table II. All cases have an unbalanced level of 10%. The grid's three-phase line impedance is increased for Case 2 compared to Case 1. The neutral inductor is increased for Case 3a compared to Case 1. The PFC controller parameters of Case 1, Case 2,

TABLE I
PSU Parameters

Symbol	Description	Value
P	PSU Rated Power	5 kW
V_{ac}	PSU-rated input voltage	240 V_{rms}
f_0	PSU input voltage fundamental frequency	60 Hz
$\boldsymbol{\omega_0}$	PSU input voltage angular frequency	376.8 rad/s
V_{dc}	Front-end PFC output voltage	400 V
V_{dc_dc}	Cascaded DC-DC converter output voltage	48 V
C	Output capacitance of PFC converter	1.7 mF
C_{bus}	Input capacitance of DC-DC converter	275 μF
k_{ii}	PFC Current PR controller integral gain	0.125
k_{pi}	PFC Current PR controller proportional gain	0.02
k_{iv}	PFC DC voltage PI controller integral gain	5.44
k_{pv}	PFC DC voltage PI controller proportional gain	0.136
k_{ii_dc}	DC-DC current PI controller integral gain	3.35
k_{pi_dc}	DC-DC current PI controller proportional gain	0.00304
k_{iv_dc}	DC-DC DC voltage PI controller integral gain	18 400
k_{pv_dc}	DC-DC DC voltage PI controller proportional gain	0
f_{sw}	Switching frequency of PFC and DC-DC converter	100 kHz

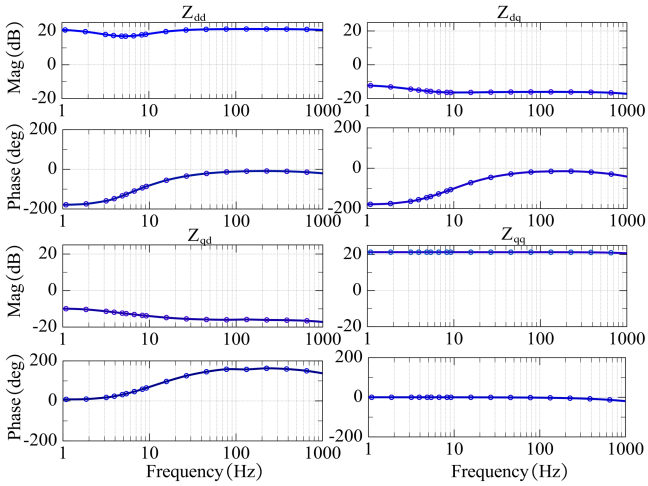

Fig. 7. Modeled d-q impedance of a single-phase PSU.

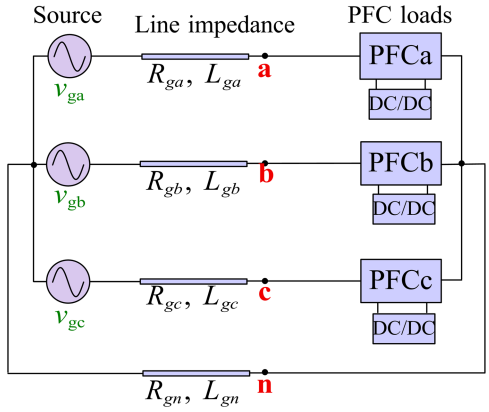

Fig. 8. System configuration of the simulation study.

TABLE II
LINE IMPEDANCE, AND POWER OF CASE 1–CASE 3

Case	Phase Impedance	Neutral Inductor	Phase *a* Power	Phase *b* Power	Phase *c* Power
1	0.5 Ω + 390 μH	10 mH	4.5 kW	5 kW	5.5 kW
2	1 Ω + 810 μH	10 mH	4.5 kW	5 kW	5.5 kW
3a/3b	0.5 Ω + 390 μH	12 mH	4.5 kW	5 kW	5.5 kW

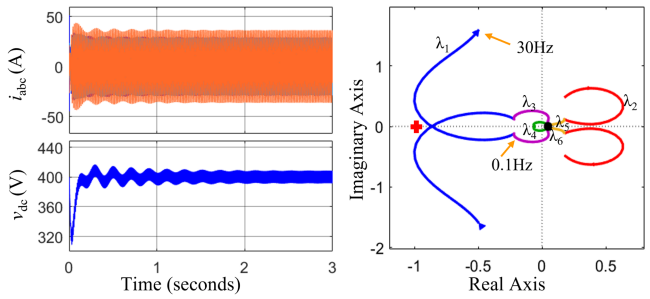

Fig. 9. AC current, one PSU's DC voltage, and Nyquist plot of Case 1.

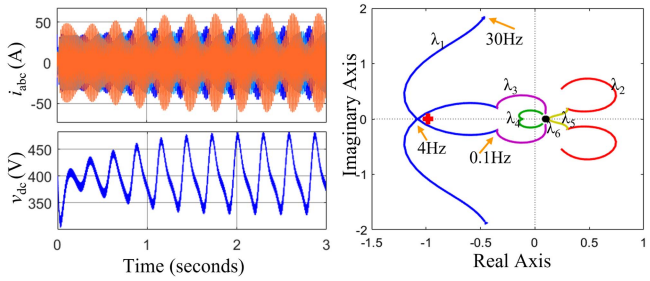

Fig. 10. AC current, one PSU's DC voltage, and Nyquist plot of Case 2.

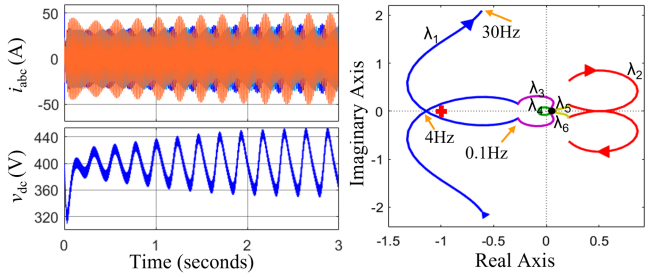

Fig. 11. AC current, one PSU's DC voltage, and Nyquist plot of Case 3a.

and Case 3a are the same. For Case 3b, the PFC voltage PI controller's proportional and integral gains are decreased to 1/3 that of Case 3a.

The three-phase current, one of the PSU load's dc bus voltages, and the eigenvalue loci obtained in (22), (24), and (25) of the four cases are shown in Figs. 9 –12, respectively. Case 1 and Case 3b both show stable operation in the time domain and no encirclements of (−1, 0) in the Nyquist plot. Case 2 and Case 3a exhibit 3.7 Hz and 4.3 Hz oscillations respectively and two encirclements of (−1, 0) in their Nyquist plot. The frequency of the point close to (−1, 0) in the Nyquist plot is also close to the corresponding oscillation frequency. The impedance analysis

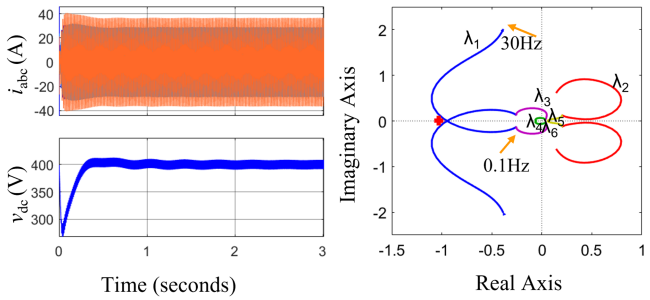

Fig. 12. AC current, one PSU's DC voltage, and Nyquist plot of Case 3b.

TABLE III
LINE IMPEDANCE, AND POWER OF CASE 4–CASE 6

Case	Neutral Inductor	Phase *a* Power	Phase *b* Power	Phase *c* Power
4	5 mH	9 kW	10 kW	11 kW
5	8 mH	9 kW	10 kW	11 kW
6	5 mH	13.5 kW	15 kW	16.5 kW

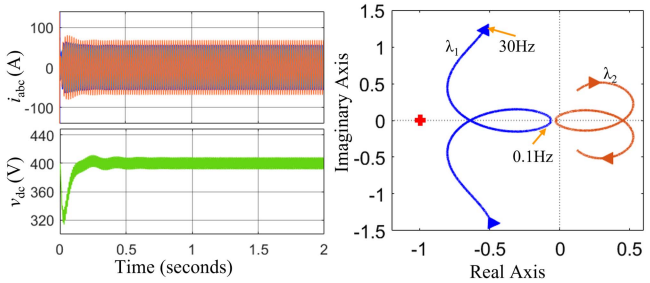

Fig. 13. AC current, one PSU's DC voltage, and Nyquist plot of Case 4.

matches the time-domain results. These four cases verify the 6 × 6 impedance matrix models for stability analysis. They also show that increasing either phase impedance or neutral line impedance is detrimental to stability while changing the PFC controller parameters could help to resolve the instability issues.

To verify the 2 × 2 impedance matrix model derived for the four-wire system with dominant neutral line inductance, three cases are studied. The neutral inductance, voltage, and power of each case are shown in Table III. For Case 4 and Case 5, there are two identical PSU loads connected to each phase. For Case 6, there are three identical PSU loads connected to each phase. All three cases are at a 10% unbalance level. The neutral inductor is increased for Case 5 compared to Case 4. The power level of Case 6 is increased compared with Case 4. The three-phase current, one of the PSU load's dc bus voltages, and the eigenvalue loci obtained through (25), (28), and (32) of the three cases are shown in Figs. 13 –15 respectively.

Case 4 is stable in the time domain and shows no encirclements of (−1, 0) in its Nyquist plot. Case 5 and Case 6 exhibit 4 Hz and 4.5 Hz oscillations respectively and two encirclements of (−1, 0) in their Nyquist plot. The frequency of the point close to (−1, 0) in the Nyquist plot is also close to the corresponding

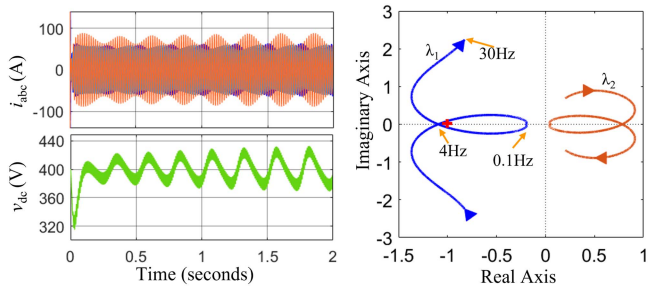

Fig. 14. AC current, one PSU's DC voltage, and Nyquist plot of Case 5.

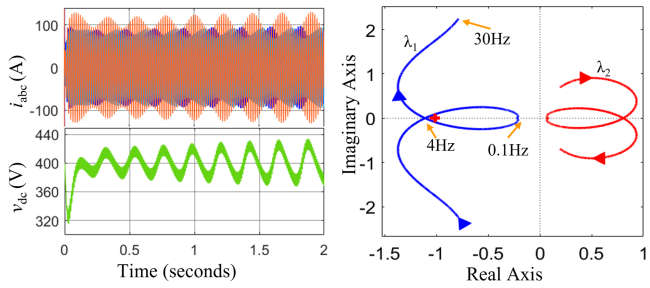

Fig. 15. AC current, one PSU's DC voltage, and Nyquist plot of Case 6.

TABLE IV
LINE IMPEDANCE, VOLTAGE, AND POWER OF CASE 7 AND CASE 8

Case	Neutral Inductor	Phase *a/b/c* Power
7	10 mH	5 kW
8	18 mH	

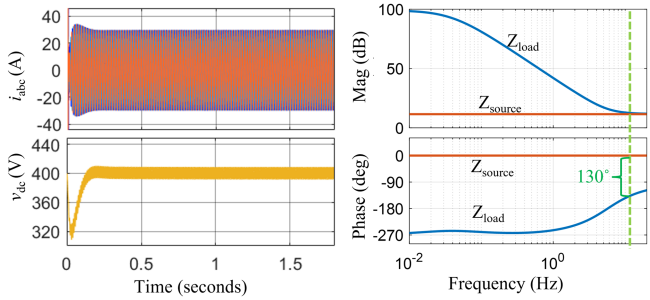

Fig. 16. AC current, one PSU's DC voltage, and bode plot of source and load impedance of case 7: $L_{gn} = 10$ mH.

oscillation frequency. The impedance analysis results match the time-domain results, thus verifying the 2×2 impedance matrix models for the dominant neutral inductor scenarios. They also show that increasing either neutral line impedance or system power level is detrimental to stability.

To verify the effectiveness of the simplified SISO model for a balanced four-wire system with dominant neutral inductance, two cases are studied, with parameters shown in Table IV. The neutral inductor for Case 8 is increased compared to Case 7. The three-phase current, one of the PSU load's dc bus voltages, and the upstream and downstream impedance obtained from (41) and (42) of the two cases are shown in Figs. 16 and 17

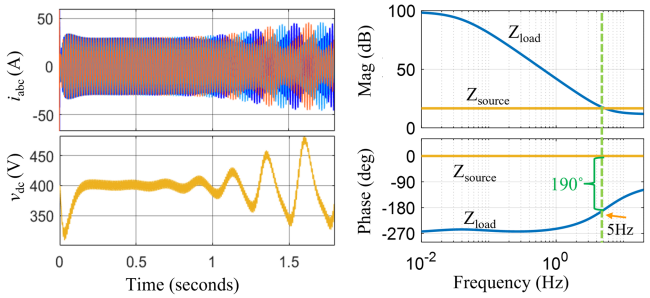

Fig. 17. AC current, one PSU's DC voltage, and bode plot of source and load impedance of case 8: $L_{gn} = 18$ mH.

respectively. Case 7 is stable in the time domain. Case 8 shows around 4.5 Hz oscillations. In the impedance Bode plot, at the point of intersection of Z_{source} and Z_{load}, the phase difference of Case 7 is lower than 180°, while for Case 8 it is larger than 180°. According to the Bode plot criterion, the impedance analysis matches the time-domain results.

In summary, this section verified the proposed impedance models of the upstream and downstream for stability analysis. Instability issues are a compound result of improper design or operations of both the upstream and the downstream. For example, in a data center power system, the upstream impedance is mainly composed of the distribution line impedance, transformer leakage inductance, and sometimes reactors added for protection. By the proposed model, Case 1–Case 3a, Case 4, Case 5, Case 7, and Case 8 show that increasing upstream impedance to an extent could lead to instability; on the contrary, keeping it within a limit is a way to avoid such oscillation issues. Accordingly, in practice, the system operator could reduce the distance and cable length between the substation and the server rooms, redesign the transformer to limit the leakage impedance, or choose other protection schemes to avoid large reactor installation. Some of these changes are related to data center architecture reconstruction, which may require high costs and complexity. Therefore, on the other hand, system operators could choose to modify the downstream side, including asking the power supply vendors to modify their product design or reduce the power of the workload. By the proposed model, Case 3a and Case 3b, Case 4–Case 6 show that reducing the total load power or reducing the PFC controller gain could resolve instability.

The proposed impedance model utilizes the *d-q* impedance of one PFC converter, which exhibits negative resistor characteristics in the $Z_{\rm dd}$ term. Lin et al. [39] show that reducing the PI controller gain of the PFC voltage controller would shift the phase of $Z_{\rm dd}$ higher and further away from $-180°$, so the negative resistor characteristic is diminished. For Case 3b, the PFC voltage PI controller proportional and integral gains are decreased to 1/3 of that of Case 3a. The phase of the eigenvalue locus 1 of Case 3b around 4 Hz decreases; thus, it moves to the right of the $(-1, 0)$, so no encirclements are exhibited. From a qualitative analysis aspect, the proposed model could characterize the impact of PFC parameters on the system stability. On another note, reducing the PFC PI parameters means degrading

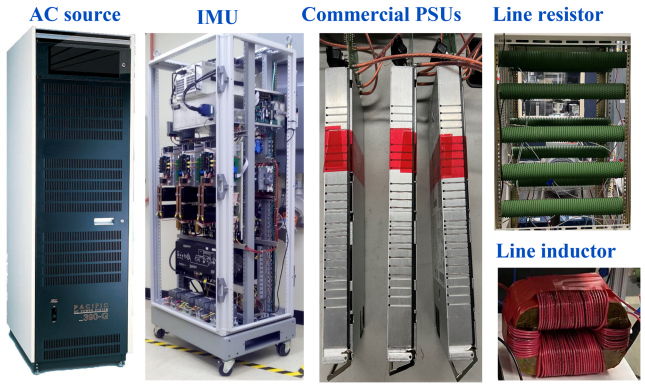

Fig. 18. Experimental setup.

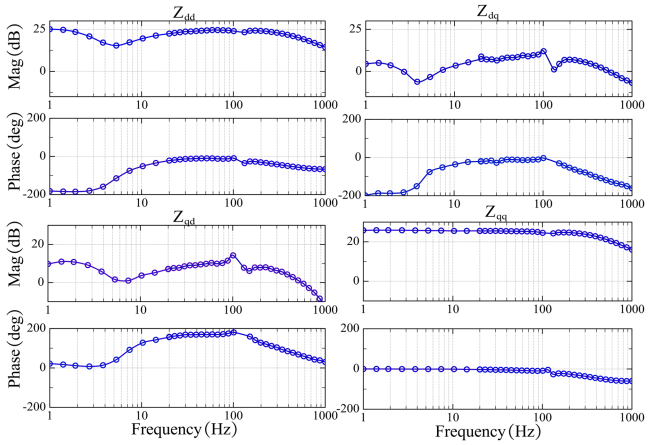

Fig. 19. Measurement *d-q* impedance of one PSU load.

the performance of the dc voltage loop. At the same time, it is not critical for the studied system because the cascaded dc-dc converter maintains the high performance of load dc voltage regulation. However, for some other systems, when the cascaded dc-dc converter is absent, some novel active damping control schemes can be designed based on the proposed model to solve the oscillations issues and maintain output voltage regulation performance [40].

V. Experimental Verification

This section aims to verify the proposed impedance-based stability analysis model in Section III using experimental tests. Fig. 18 shows the experimental setup. With the same three-phase-four-wire configuration as in Fig. 8, some resistors and inductors representing line impedance are connected between a three-phase ac source and the PSU loads, which are three commercial PSUs with part number FLATPACK2241119. 905B. These PSUs are with isolated dc-dc converters in the dc stage. The PSUs are connected to resistor loads. Noted that these PSUs' internal parameters are not available, which are different from the ones in the simulation study. These PSUs operating voltage range is 100–275 V_{rms}. Due to the available equipment, the test is carried out at about 150 V_{rms}. The models can work for any other voltage level as long as the PFC impedance is measured at the corresponding voltage.

Each PSU's *d-q* impedance at different powers and voltages according to the test conditions is measured using an Impedance Measured Unit. For example, Fig. 19 shows the measured impedance of one PSU load at around 150 V_{rms}, 1 kW. Meanwhile, because the PSU impedance is measured with the *d*-axis aligning with the input voltage when constructing the system impedance matrix, the *d-q* impedance PSU in phase *b* and phase *c* need to be modified using (33) and (34) considering the reference frame angle difference between the measured impedance and system impedance model (all are referring to phase *a*' PSU input voltage).

Case 1–Case 3 is designed to verify the 6 × 6 impedance matrix models. Table V shows the parameters of the four-wire system. With other parameters being the same, the system total power is changed from 3 to 2.8 kW, and 2.6 kW in Case 1, Case 2, and Case 3, respectively. The time-domain test and the Nyquist plots using (22), (24), and (25) of the three cases are shown in Figs. 20 –22, respectively. Case 1 and Case 2 both have low-frequency oscillations at around 4 Hz while Case 3 is stable. Correspondingly, the eigenvalue loci of the calculated 6 × 6 minor loop gain of Case 1 and Case 2 have encirclements of $(-1, 0)$ while Case 3's does not. The test results of Case 1–Case 3 verify the effectiveness of the 6 × 6 impedance model to assess the stability of the four-wire system in both balanced and unbalanced conditions.

Case 4–Case 7 showcase negligible phase impedance compared with a dominant neutral line inductor to verify the 2 × 2 impedance matrix model for such a scenario. The system parameters of Case 4–Case 7 are shown in Table VI. Case 4 and Case 5 are balanced. Case 6 and Case 7 are 10% unbalanced.

TABLE V
Four-Wire System Parameters of Case 1–Case 3

Case	Line Impedance	Neutral Inductor	PSU AC Voltage	Phase *a* Power	Phase *b* Power	Phase *c* Power
1				1 kW	1 kW	1 kW
2	1 Ω + 2 mH	10 mH	150 Vrms	0.8 kW	1 kW	1 kW
3				0.8 kW	0.8 kW	1 kW

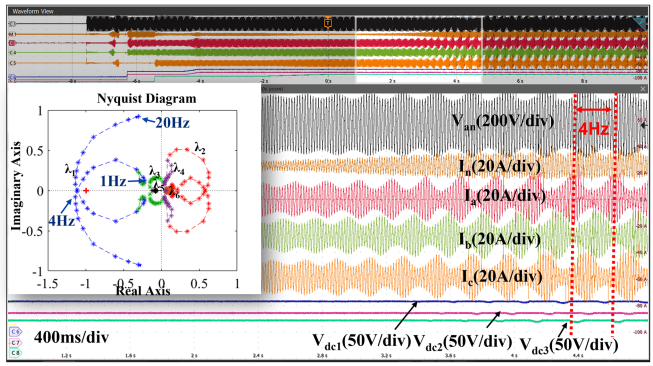

Fig. 20. Test results and Nyquist plot of Case 1.

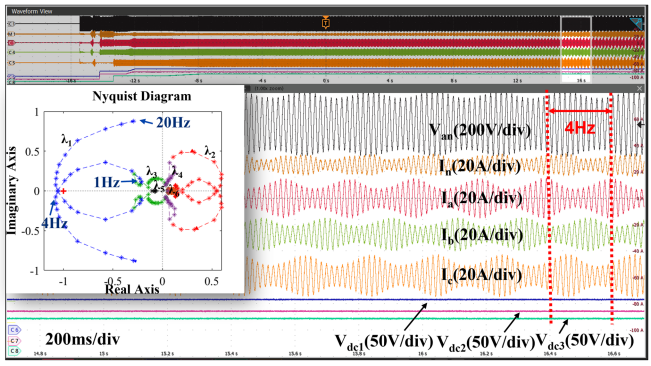

Fig. 21. Test results and Nyquist plot of Case 2.

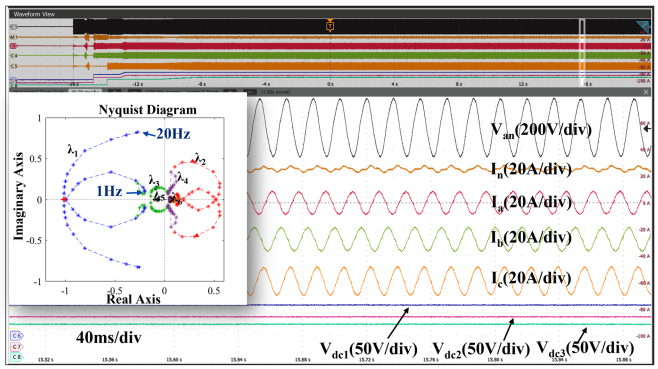

Fig. 22. Test results and Nyquist plot of Case 3.

TABLE VI
FOUR-WIRE SYSTEM PARAMETERS OF CASE 4–CASE 7

Case	Neutral Inductor	PSU AC Voltage	Phase *a* Power	Phase *b* Power	Phase *c* Power
4	10 mH	150 Vrms	1 kW	1 kW	1 kW
5	10 mH		1.1 kW	1.1 kW	1.1 kW
6	10 mH		1 kW	1.1 kW	1.2 kW
7	4 mH		1 kW	1.1 kW	1.2 kW

The total power of Case 5–Case 7 is 3.3 kW, while that of Case 4 is 3 kW. Compared with Case 6, the neutral line inductor is reduced from 10 to 4 mH for Case 7. The time-domain test and the Nyquist plots using the derived 2×2 impedance matrix models as (25), (28), and (29) of the four cases are shown in Figs. 23 –26 respectively. Case 4 is stable, at the same time, there are no encirclements of $(-1, 0)$ in its Nyquist plot. When its total power increases as in Case 5, around 5 Hz low-frequency oscillations occur. Keeping the same total power, by increasing the unbalanced level to 10% as in Case 6, the system still has low-frequency oscillations. Its loci are like that of Case 5. If further decreasing its neutral inductor is as in Case 7, the system returns to a stable condition. The loci shrink to the right and have no encirclements of $(-1, 0)$. The results of Case 4–Case 7 verify the effectiveness of using the 2×2 impedance matrix model to assess system stability when the neutral line impedance is much larger than the phase line's impedance.

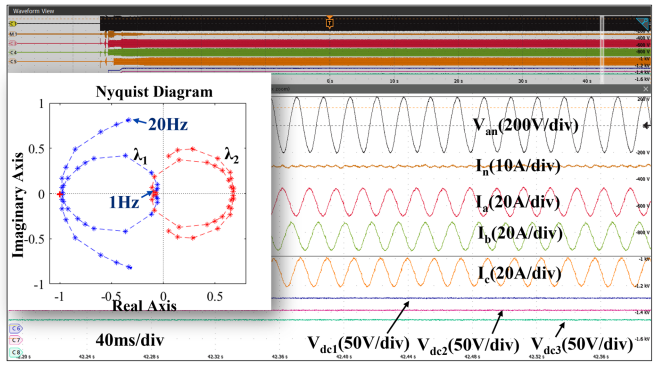

Fig. 23. Test results and Nyquist plot of Case 4.

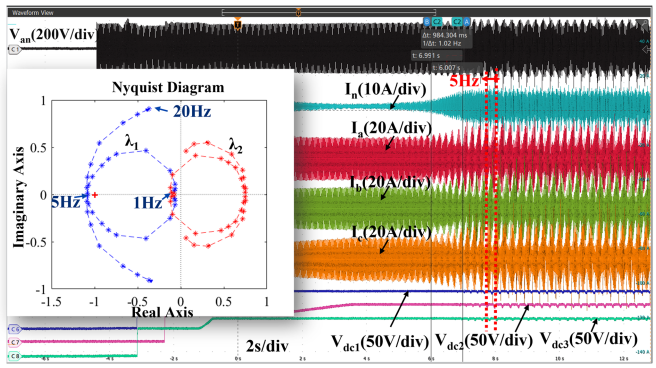

Fig. 24. Test results and Nyquist plot of Case 5.

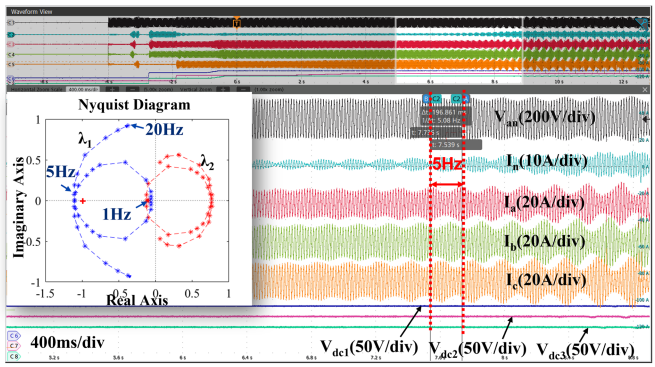

Fig. 25. Test results and Nyquist plot of Case 6.

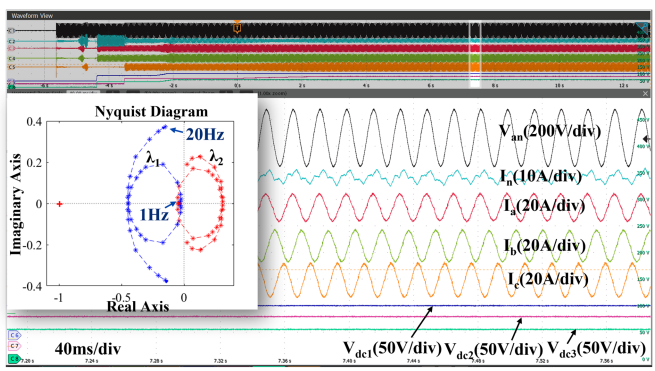

Fig. 26. Test results and Nyquist plot of Case 7.

TABLE VII
FOUR-WIRE SYSTEM PARAMETERS OF CASE 8 AND CASE 9

Case	PSU AC Voltage	Power	Neutral Inductor
8	150 Vrms	1 kW	4 mH
9			14 mH

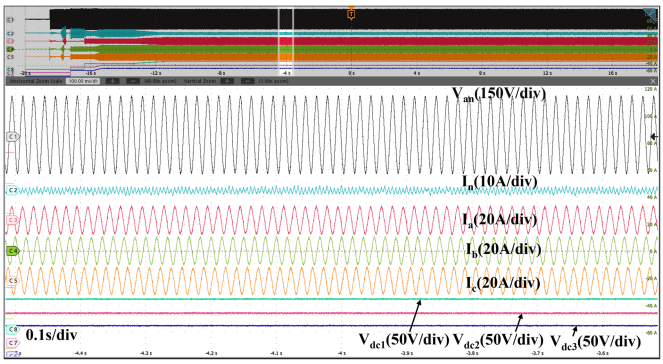

Fig. 27. Test results of Case 8.

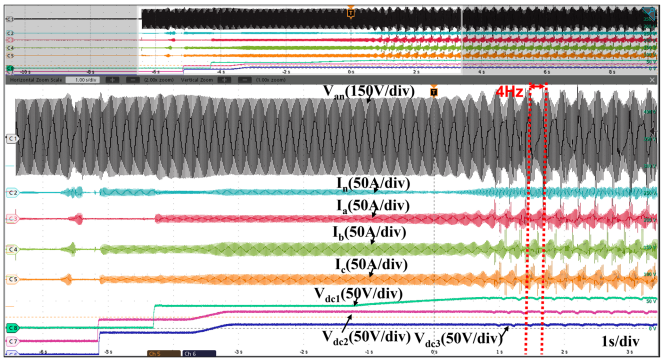

Fig. 28. Test results of Case 9.

To verify the Bode plot criterion for the balanced cases of the four-wire system with a dominant neutral inductor, Case 8 and Case 9 are conducted. The system parameters are shown in Table VII. The neutral line inductor is increased from 4 to 14 mH in Case 9 compared to Case 8. The time-domain test results of the three cases are shown in Figs. 27 and 28. Case 8 shows stable operation while Case 9 exhibits around 4 Hz low-frequency oscillations. Under a balanced condition, the stability of Case 8 and Case 9 can be assessed using the proposed model of an equivalent SISO system. With the measured PSU load impedance and neutral line impedance, the upstream impedance and downstream impedance of the equivalent SISO system can be calculated using (41) and (42), which are shown in Fig. 29. For Case 8, the load impedance gain is always larger than the upstream impedance gain, therefore the system should be stable. For Case 9, the gain of the upstream impedance and the gain of the downstream impedance have an intersection at around 4 Hz, at which the phase difference is larger than 180°, indicating an unstable operation. The impedance analysis using the Bode plot criterion of both Case 8 and Case 9 match the time-domain test results. Figs. 11 and 12 show that changing the

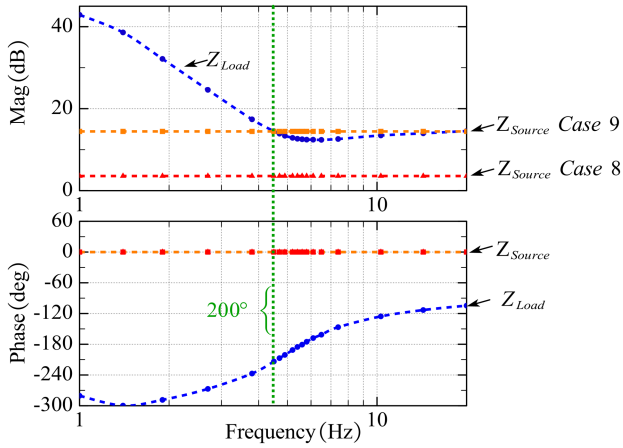

Fig. 29. Upstream and downstream impedance plot of Case 8 and Case 9.

PFC controller parameters could resolve the instability issues. Because the parameters of the commercial PSUs are not able to be changed in the lab test, such cases are not demonstrated.

VI. DISCUSSION ON THE NEUTRAL LINE DESIGN AND SYSTEM IMPEDANCE SPECIFICATIONS

When designing line impedance for medium to high-voltage grids, current limiting reactors must be considered alongside current capacity, length, and power loss. By increasing inductive reactance, an extra line reactor can limit fault current, slowing the rate of current rise and transient overvoltage during a fault. Inductive reactance must be low enough to prevent unacceptable voltage drops during normal operation, but high enough to restrict short circuits to switchgear ratings. In low-voltage distribution systems, such as those found in data centers, the application and design of such reactors vary. Some facilities may not use extra line reactors due to cost, construction, or availability considerations. The neutral wire in four-wire systems may still have a higher inductance due to a smaller cross-sectional area compared with the three-phase wires with a larger current capacity. Some facilities may choose to use the same reactor in all four wires to reduce fault current, while others may only place a high reactor in the neutral line to minimize voltage drops during normal operation and reduce cost. The analysis in the previous section shows that the stability impact of neutral wire impedance must be considered.

For the data center application, the unbalance is usually limited to a relatively small level (around 10%). For such scenarios, (41) and (42) reveal that to achieve a similar stability margin, when increasing PSU load power by N times, the neutral inductor needs to be reduced to around $1/N$ of its original value. For example, for the studied system in simulation, with 5 kW per phase, the system can be stable with up to around 15 mH neutral inductance, while with 15 kW per phase, the system will not be stable if the neutral inductance increases above 5 mH.

On the other hand, the proposed impedance model provides another aspect that a larger neutral line inductor could help to damp potential high-frequency oscillations. The input filter of

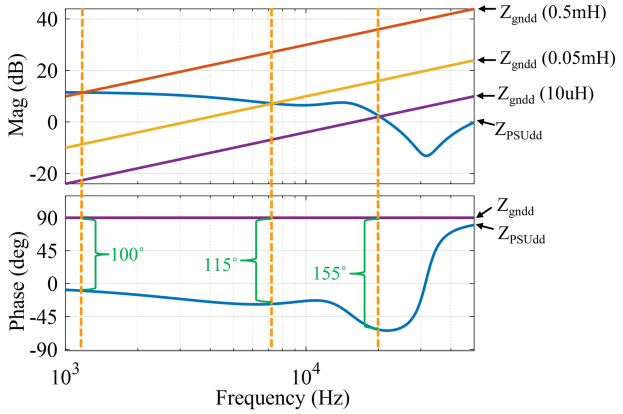

Fig. 30. Z_{gndd} and Z_{PSUdd} with different neutral inductance.

the PSU in Fig. 6 is composed of a 15 μH differential mode inductor L_{dm}, both 2 μF for the C_e and C_d of the differential mode capacitor, and a 2 Ω damping resistor R_d. At high frequency (>1 kHz), all three phases' PSU loads' impedances are mainly shaped by their input EMI filter and current loop, which is not impacted by the operating points. Both upstream and downstream impedance are diagonally dominant in the high-frequency range. The system minor loop gain can be simplified as (43) based on (25), (28), and (32)

$$\mathbf{L_{sys}} \approx 3\begin{bmatrix} Z_{Ndd}Y_{PSUadd} & 0 \\ 0 & Z_{Nqq}Y_{PSUaqq} \end{bmatrix}. \quad (43)$$

At high frequency ($>$ 1 kHz), the dd and qq element of the neutral line and PSU impedance are equal, therefore, assessing (43) is equivalent to just checking either the dd or qq element of (43) using the Bode plot criterion. If using the dd element, the Z_{Ndd} and Y_{PSUadd} should be overplotted. Fig. 30 shows a four-wire system with 5 kW per phase and with a different neutral inductor. With 10 μH of neutral inductance, high-frequency oscillations may occur with some perturbations because the system stability margin is just 25°. Increasing the neutral inductance largely increases the stability margin. With 0.5 mH of neutral inductance, the stability margin increases to 80°.

Therefore, when designing the neutral inductor, it is necessary to consider its detrimental impact on the system's low-frequency stability, and its positive impact on the system's high-frequency stability. If the load impedance is given, the impedance of the neutral inductor could be specified within a certain range considering its stability impact. Fig. 31 provides an example of the design process. The neutral impedance is labeled as Z_n.

The proposed model provides a framework for analyzing the stability of a three-phase four-wire system, which can be useful in impedance specifications. If the source and cable impedance is known, the model can be used to map the characteristic loci in the complex plane to the PSU load impedance. Using this mapping, it is possible to define a forbidden region in the complex plane that represents the instability boundary of the system. Conversely, an allowable region can be defined based on the desired system stability margin. By designing the PSU converter control properly, manufacturers can ensure that the PSU impedance is shaped within the allowable region.

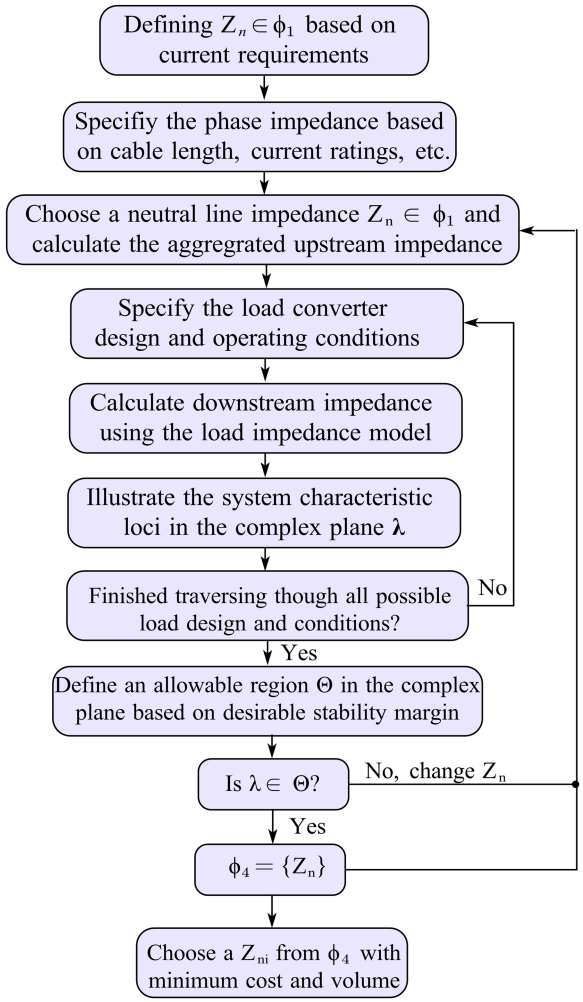

Fig. 31. Process of designing neutral line inductor.

During system operation, if the characteristic loci enter the forbidden region, it may be necessary to adjust the PSU impedance to maintain stability. This can be accomplished using the proposed model, which can provide recommendations on the required adjustments based on the system parameters.

VII. Conclusion

Within the time-invariant framework, this article proposed impedance models of a three-phase four-wire system with single-phase loads for stability analysis purposes. Both the simulation and experiments verify the impedance models. Some useful conclusions are drawn below.

1) The stability of a three-phase four-wire system with single-phase loads in either balanced or unbalanced conditions can be accurately predicted with 6 $\times$ 6 impedance models and GNC. It can be simplified as 2 $\times$ 2 impedance models for a system with dominant neutral line inductance. It can be further simplified as 1 $\times$ 1 impedance for three-phase-balanced cases; thus, the Bode plot criterion can be used.

2) A high neutral line inductor design is detrimental to the system's low-frequency stability while it can help damp potential high-frequency resonance.
3) The proposed model can be applied to the impedance specifications of a three-phase four-wire system.

APPENDIX

Equations (44) and (45) show the analytical expression of the PFC impedance matrix

$$\mathbf{Z_{filter\_PFC}} = (\mathbf{Z_{PFC}^{-1}} + \mathbf{Y_{C_e}} + (\mathbf{Z_{C_d}} + \mathbf{Z_{R_d}})^{-1})^{-1} + \mathbf{Z_{L_{dm}}} \tag{44}$$

$$\mathbf{Z_{PFC}} = \begin{pmatrix} \mathbf{Z^{-1}} + \mathbf{G_{id}}(\mathbf{I} - \mathbf{G_{del}}\mathbf{G_{ci}}\mathbf{G_{cv}}\mathbf{G_{vd}})^{-1} \cdot \\ (\mathbf{G_{del}}\mathbf{G_{ci}}(\mathbf{G_{cv}}\mathbf{G_{vv}} - \mathbf{G_q}) + \mathbf{G_{del}}\mathbf{G_v})^{-1} \end{pmatrix} \cdot (\mathbf{I} - \mathbf{G_{id}}(\mathbf{I} - \mathbf{G_{del}}\mathbf{G_{ci}}\mathbf{G_{cv}}\mathbf{G_{vd}})^{-1}\mathbf{G_{del}}\mathbf{G_{ci}}) \tag{45}$$

where $\mathbf{Z_{PFC}}$ is the *d-q* impedance of the PFC without the input filter, $\mathbf{Y_{Ce}}$ is the *d-q* admittance of the cap $\mathbf{C_e}$, $\mathbf{Z_{Cd}}$, $\mathbf{Z_{Rd}}$, and $\mathbf{Z_{Ldm}}$ are the *d-q* impedance of the cap C_d, resistor R_d, and inductor $\mathbf{L_{dm}}$ respectively. $\mathbf{G_{id}}$, $\mathbf{Z}$, $\mathbf{G_{vd}}$, and $\mathbf{G_{vv}}$ identify the power stage dynamics, which can be derived from the small-signal circuit model. $\mathbf{G_{id}}$ denotes the transfer function matrix from the duty cycle to the boost inductor current, $\mathbf{Z}$ denotes the transfer function matrix from the boost inductor current to the input voltage, $\mathbf{G_{vd}}$ denotes the transfer function matrix from the duty cycle to the dc voltage, and $\mathbf{G_{vv}}$ denotes the transfer function matrix from input voltage to dc voltage. $\mathbf{G_{ci}}$ denotes the current controller dynamics, and $\mathbf{G_{del}}$ corresponds to the digital control delay. $\mathbf{G}_\theta$ is defined to represent the dynamics of the input voltage phase tracking. $\mathbf{G_{cv}}$ denotes the voltage controller dynamics. $\mathbf{G_v}$ describes the input voltage feedforward control dynamics. The expressions of these transfer function matrixes can be found in [30].

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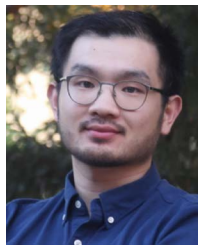

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