A Three-Level Buck–Boost Converter With Planar Coupled Inductor and Common-Mode Noise Suppression

Yuliang Cao, *Graduate Student Member, IEEE*, Yijie Bai, *Graduate Student Member, IEEE*, Vladimir Mitrovic, *Graduate Student Member, IEEE*, Boran Fan, *Member, IEEE*, Dong Dong, *Senior Member, IEEE*, Rolando Burgos, *Senior Member, IEEE*, Dushan Boroyevich, *Life Fellow, IEEE*, Radha Sree Krishna Moorthy, *Member, IEEE*, and Madhu Chinthavali, *Senior Member, IEEE*

***Abstract*—The demand for a bidirectional dc–dc converter with a flexible dc bus is driven by the fast development of renewable energy system, transportation electrification, and microgrid. In order to accommodate different dc bus, two-stage ac–dc–dc architecture has been widely used, and the dc output regulation was handled by a rear-end dc–dc converter. If the galvanic isolation is not required, the four-switch buck-boost (FSBB) converter with quadrangle control is a good candidate because of the bidirectional noninverting output, step-up/down capability, and zero voltage switching. However, to achieve the minimum rms current and soft switching, the calculation of quadrangle control is complicated and often requires the resource-consuming loop-up tables, or additional high-frequency current detection circuits. Moreover, due to the unbalanced circuit topology, the common-mode (CM) noise is another concern. In this article, a symmetric three-level (3-L) buck–boost converter was first proposed to suppress the CM noise. To increase the power density and efficiency, a planar coupled inductor was designed for this 3-L buck–boost converter with a 30% winding loss reduction. And then, to realize a simple close-loop output control, a real-time simplified minimum rms current calculation for quadrangle modulation was found without look-up tables or ZCD circuits. Based on this simplified output control, a decoupled mid-points balance control for both input and output sides were also proposed. Finally, the simplified close-loop control, the decoupled active balance control, and the CM mode noise reduction were all verified by a 30 kHz 50 kW 3-L buck–boost converter. Compared with the typical FSBB converter, the proposed 3-L buck–boost converter has a up to 25 dB CM noise reduction from 150 kHz to 30 MHz. This article is accompanied by two videos demonstrating the effect of decoupled active balance control.**

***Index Terms*—Common-mode (CM) noise reduction, decoupled active balance control, four- switch buck–boost (FSBB) converter, planar coupled inductor, quadrangle control, simplified minimum rms current calculation, three-level (3-L) buck–boost converter, zero voltage switching (ZVS).**

Manuscript received 23 September 2022; revised 21 January 2023 and 31 March 2023; accepted 16 May 2023. Date of publication 25 May 2023; date of current version 28 July 2023. This work was supported by Oak Ridge National Laboratory and funded by the Department of Energy—Office of Electricity's, Transformer Resilience and Advanced Components program led by the program manager A. Pereira. Recommended for publication by Associate Editor O. Trescases. *(Corresponding author: Boran Fan.)*

Yuliang Cao, Yijie Bai, Vladimir Mitrovic, Boran Fan, Dong Dong, Rolando Burgos, and Dushan Boroyevich are with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061-0131 USA (e-mail: yuliangcao@vt.edu; byj414@vt.edu; vlmitr@vt.edu; brianfan@vt.edu; dongd@vt.edu; rburgos@ieee.org; dushan@vt.edu).

Radha Sree Krishna Moorthy and Madhu Chinthavali are with the Oak Ridge National Laboratory, Oak Ridge, TN 37831-2008 USA (e-mail: krishnamoorr@ornl.gov; chinthavalim@ornl.gov).

This article has supplementary material provided by the authors and color versions of one or more figures available at https://doi.org/10.1109/TPEL.2023.3279987.

Digital Object Identifier 10.1109/TPEL.2023.3279987

I. Introduction

In RECENT years, the dc–dc converter with a flexible dc output plays a significant role in the energy storage system (EES) [1], [2], [3], electrical vehicle (EV) charging system [4], [5], [6], [7], [3], [8], [6], and solid-state transformer (SST) system [9], [10], [11], [12], [13]. For this demand, as shown in Fig. 1, a wide range output bidirectional ac–dc converter is desirable to connect distribution line with different dc loads. For compatibility with different dc buses, the two-stage ac–dc–dc architecture shown in Fig. 2 is usually selected.

Since the front-end ac–dc stage has a limited range for the dc output, a rear-end dc–dc converter can be dedicated to dc output regulation. For instance, the dc bus for a typical photovoltaic (PV) system is 1 or 1.2 kV, and the dc bus for EV charging system is 400 or 800 V. For the isolation application, the dual active bridge (DAB) converter [14] and the LLC/CLLC series resonant converter [15], [16], [17], [18] are both very popular topologies. However, if the galvanic isolation is not required, four-switch buck–boost (FSBB) converter [19], [20], [31] is a good candidate because of noninverting output, bidirectional power flow, and step-up/down capability.

Among three soft switching control methods: buck-boost control [19], [20], [21], two-mode control [22], [23], [24], [25], and quadrangle control [26], [27], [28], [29], [30], [31], [32], [33], [34], quadrangle control is more desirable because it has the minimum inductor current. However, in order to modulate an optimal quadrangular inductor current, the negative valley current should be minimized, and the calculation block is very complicated. The look-up table method [27], [28], [29], [30], [31], [32], [33] was proposed to avoid the complex real-time calculation. However, this method was resource-consuming because all the optimized control variables should be stored as

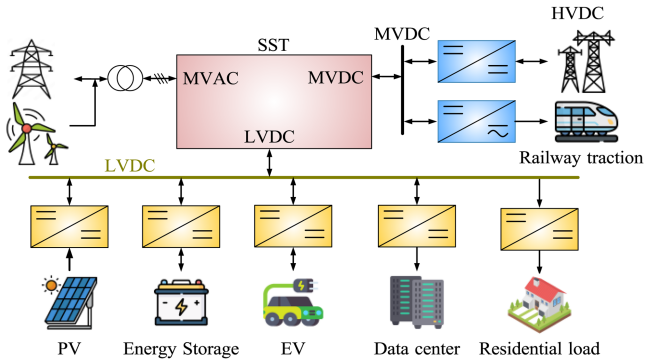


Fig. 1. Applications for the bidirectional DC–DC converter.

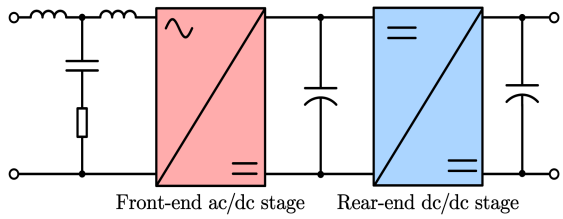


Fig. 2. Typical two-stage AC–DC–DC architecture.

look-up table data in advance. Moreover, due to large time consumption for invoking these data, this method also has a poor dynamic performance [34]. To obtain a real-time calculation block, a simplified method [34] has been proposed with an extra high-frequency (HF) current detection circuit. However, this additional circuit will increase the cost and decrease the power density. The HF current detection circuit is very difficult to implement in high voltage and high voltage applications. Besides extra circuits, this simplified method requires a variable switching frequency, which might lead to difficulty for magnetics design.

Apart from the complex calculation, the CM noise is another concern because the typical FSBB converter is an unbalanced circuit topology [35]. The symmetric unfolded topologies such as three-level (3-L) buck converter were usually adopted to reduce the CM noise because they should have zero CM voltage emission theoretically. However, with the consideration of circuit tolerances such as the propagation delay from the gate driver [36], the CM noise will still exist in these topologies. Furthermore, an unfolded topology often requires a mid-point balance control, which will also have an impact on the CM noise. Therefore, a quantitative CM noise comparison between balanced and unbalanced topologies is desirable.

The rest of this article is organized as follows. Section II proposed a symmetric 3-L buck–boost converter with the CM noise reduction. Due to the zero-voltage switching (ZVS) and the minimum rms inductor current, quadrangle modulation was selected. Furthermore, considering 30% less winding loss and higher power density, two separate inductors in 3-L buck–boost converter were coupled together. The design of this coupled inductor was also given to cover the full range of voltage

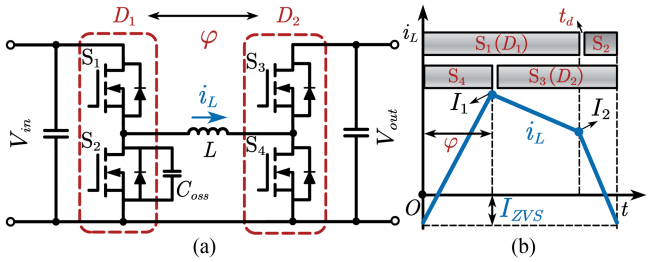


Fig. 3. (a) Circuit diagram of a typical four-switch buck-boost (FSBB) converter. (b) Corresponding inductor current i_L with a quadrangle control [26], [27], [28], [29], [30], [31], [32], [33], [34].

and power. In order to realize a real-time calculation without look-up table or extra HF current detection circuit, Section III simplified the existing minimum rms current calculation block with a ZVS factor. An approximate linear relationship between the ZVS factor and negative ZVS current was found. Thanks to this simplified minimum rms current calculation, a simple close-loop output voltage control for 3-L buck–boost converter was developed. And then, Section IV proposed a decoupled active balance control to equalize both input and output sides mid-points voltages. With the introduction of two small variables, the input and output side balance control can be decoupled, and the overall output close-loop control will not be affected. Finally, in Section V, a 30 kHz 50 kW symmetric 3-L buck–boost converter with planar coupled inductor was built to verify all the proposed functionalities, such as the simplified close-loop control, decoupled active balance control, and CM noise reduction. In order to obtain a fair quantitative CM noise comparison, a typical FSBB with the same specifications was implemented. Compared with typical FSBB, from 150 kHz to 30 MHz, the proposed 3-L buck–boost converter has a up to 25 dB CM noise conduction under different output voltage cases.

It should be notated that to visualize the effects of decoupled active balance control, and close-loop soft start-up, two scope recording videos are attached to this article. On the other hand, to explain the details of equation derivation (15)–(19), a *Mathematica notebook* file is also attached to this article.

II. Proposed 3-L Buck–Boost Converter

A. Quadrangle Modulation for FSBB Converter

The circuit diagram of traditional FSBB was depicted in Fig. 3(a). $V_{\rm in}$ and $V_{\rm out}$ are the input and output voltages, respectively. The gating signals and corresponding inductor current i_L are shown in Fig. 3(b). D_1 and D_2 are the duty cycle for half bridge $S_{1,2}$ and $S_{3,4}$, and the phase shift between D_1 and D_2 is φ. D_1, D_2, and φ are three basic control variables for FSBB converter, and they can control the shape of i_L. Due to the soft-switching and minimum rms current, quadrangle modulation has been widely used in FSBB converter [26], [27], [28], [29], [30], [31], [32], [33], [34]. I_1 and I_2 in Fig. 3(b) are two peak currents of i_L. This modulation has total three merits as explained in the following.

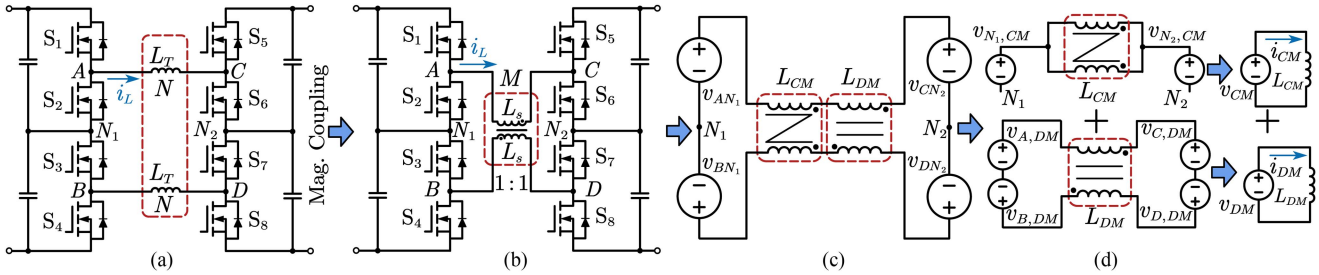


Fig. 4. Proposed 3-L buck–boost converter. (a) With separate inductor. (b) With coupled inductor. (c) Simplified equivalent circuit. (d) DM and CM equivalent circuits.

Merit 1 is the simple output regulation: due to the volt-second balance, the voltage gain of a typical FSBB converter can be easily controlled by D_1 and D_2

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{D_1}{D_2}\,. \tag{1}$$

Merit 2 is the soft switching with minimum negative current. To realize the ZVS during the deadtime t_d, a small negative current I_{ZVS} is required to charge and discharge the device output capacitance C_{oss} as shown in Fig. 3(a). The amplitude of this negative current can be given as follows:

$$|I_{\text{ZVS}}| \geqslant \frac{2C_{oss}V_{\text{out,max}}}{t_d} \tag{2}$$

where $V_{\text{out,max}}$ is the maximum output voltage.

Merit 3 is the minimum rms value of the inductor current i_L. To obtain this, the inductor current i_L is controlled as a quadrangular waveform as shown in Fig. 3(b), the inductance L in Fig. 3(a) should meet the requirement as follows [27]:

$$L = \frac{V_{\text{in}}^2 V_{\text{out}}^2}{2P_{\text{max,ZVS}} f_s \left(V_{\text{in}}^2 + V_{\text{in}}V_{\text{out}} + V_{\text{out}}^2\right)} \tag{3}$$

where $P_{\text{max,ZVS}}$ is the maximum power that the FSBB converter could achieve ZVS with minimum rms current.

B. Proposed 3-L Buck–Boost Converter With Coupled Inductor

Based on the typical FSBB converter with a quadrangle modulation, a 3-L buck–boost converter was proposed in Fig. 4(a) to reduce the CM noise. S_{14}, S_{23}, S_{58}, and S_{67} are four switch pairs, and each pair has the identical gate signals. For example, switch S_1 and S_4 have the same driving signal. N_1 and N_2 are two mid-points on the input and output side, respectively.

Moreover, to increase the power density and decrease the winding loss, two separate inductors L_T in Fig. 4(a) can be integrated as a 1:1 coupled inductor as shown in Fig. 4(b). The L_s and M are the self-inductance and mutual inductance. Fig. 4(c) depicts the simplified equivalent circuit with the coupled inductor. v_{AN1}, v_{BN1}, v_{CN2}, and v_{DN2} are four voltage sources which are used to replace four half bridges. Due to the symmetrical modulation, without the consideration of circuit tolerance, the amplitude of v_{AN1} and v_{CN2} are exactly equal to v_{BN1}, v_{DN2}, respectively

$$\begin{cases} v_{AN_1} = -v_{BN_1} \\ v_{CN_2} = -v_{DN_2}. \end{cases} \tag{4}$$

The influence of the circuit tolerance will be discussed in Section IV.

L_{DM} and L_{CM} are DM and CM inductance and can be given as follows:

$$\begin{cases} L_{\text{DM}} = 2L_s + 2M \\ L_{\text{CM}} = \left(L_s^2 - M^2\right)/\left(2L_s + 2M\right) \end{cases} \quad M \approx L_s \quad \rightarrow \quad \begin{cases} L_{\text{DM}} \approx 4L_s \\ L_{\text{CM}} \approx 0. \end{cases} \tag{5}$$

When the coupling coefficient is close to 1, L_{DM} and L_{CM} can be approximated as $4L_s$ and 0. Compared with two separate inductors design shown in Fig. 4(a), the coupled inductor design can decrease the turns number from N to $\sqrt{2}/2N$ with a same value L_{DM}. Therefore, the winding loss can be reduced by 30% with a sacrifice of CM inductance. This cost is acceptable because this proposed symmetric 3-L buck–boost converter can reduce the CM voltage emission as explained in the following.

The equivalent circuit in Fig. 4(c) can be decomposed into two DM and CM equivalent circuits as shown in Fig. 4(d). From (4), two CM voltages sources $v_{N1(2),\text{CM}}$ and the total CM voltage v_{CM} can be derived as follows:

$$\begin{cases} v_{N_1,\text{CM}} = 0.5\left(v_{AN_1} + v_{BN_1}\right) = 0 \\ v_{N_2,\text{CM}} = 0.5\left(v_{CN_2} + v_{DN_2}\right) = 0 \end{cases} \tag{6}$$

$$v_{\text{CM}} = v_{N_1,\text{CM}} - v_{N_2,\text{CM}} = 0. \tag{7}$$

From (7), this proposed topology has the zero CM voltage emission theoretically, which means the coupled inductor is suitable in this case.

As for the DM equivalent circuit depicted in Fig. 4(d), four DM voltages $v_{A(BCD),\text{DM}}$ and the total DM voltage v_{DM} can be given as follows:

$$\begin{cases} v_{A(B),\text{DM}} = v_{A(B)N_1} - v_{N_1,\text{CM}} \\ v_{C(D),\text{DM}} = v_{C(D)N_2} - v_{N_2,\text{CM}} \end{cases} \tag{8}$$

$$v_{\text{DM}} = \left(v_{A,\text{DM}} - v_{B,\text{DM}}\right) - \left(v_{C,\text{DM}} - v_{D,\text{DM}}\right). \tag{9}$$

From (7), the CM current i_{CM} is theoretically equal to 0 and the inductor should be equal to the DM current.

$$\begin{cases} i_{\text{CM}} = 0 \\ i_{\text{DM}} = i_L\,. \end{cases} \tag{10}$$

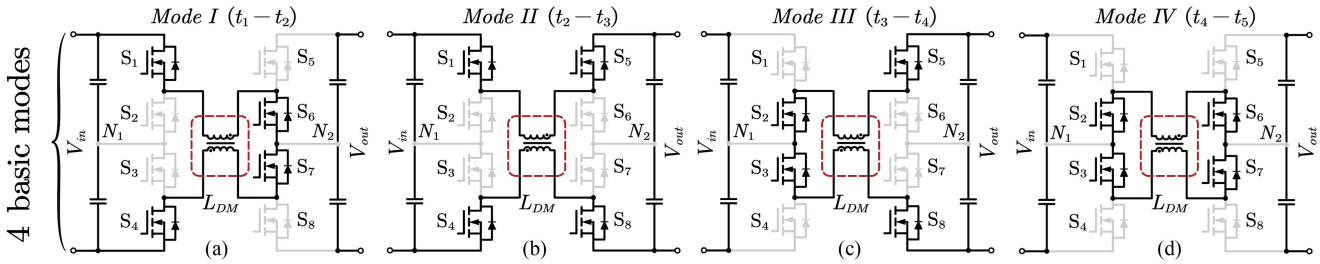


Fig. 5. Equivalent circuit diagrams of four basic modes. (a) *Mode I* (t_1–t_2). (b) *Mode I* (t_2–t_3). (c) *Mode I* (t_3–t_4). (d) *Mode I* (t_4–t_5).

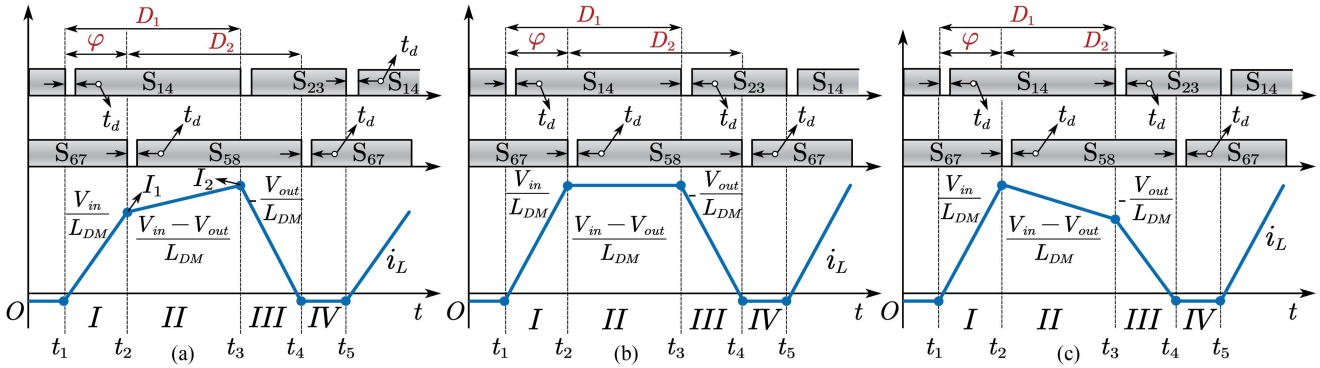


Fig. 6. Corresponding waveforms of 3-L buck–boost converter. (a) Step-down case when $V_{\rm in} > V_{\rm out}$. (b) Unit-gain case when $V_{\rm in} = V_{\rm out}$. (c) Step-up case when $V_{\rm in} < V_{\rm out}$.

C. Operation Principle

With the symmetrical modulation, the operation principle of the 3-L buck–boost converter is very similar as the typical FSBB. For example, the voltage gain, the negative ZVS current $I_{\rm ZVS}$, and the inductance requirement can follow (1)–(3).

Fig. 5 shows the equivalent circuit diagrams of four basic operation modes of 3-L buck–boost converter. And the corresponding current waveforms and driving signals are depicted in Fig. 6 with three different cases. In order to realize ZVS at all switches, deadtime t_d is adopted. Each operation mode is illustrated as follows.

Mode I: As depicted in the Fig. 5(a), four switches $\rm S_1$, $\rm S_4$, $\rm S_6$, and $\rm S_7$ are turned ON during t_1 to t_2. Since only the input voltage $V_{\rm in}$ is applied on the coupled inductor $L_{\rm DM}$, the inductor current i_L will increase linearly with the slope $m_{\rm I}$ as shown in Fig. 5

$$m_{\rm I} = V_{\rm in}\,/L_{\rm DM}. \tag{11}$$

Mode II: In the Figs. 5(b) and 6, switches $\rm S_1$, $\rm S_4$, $\rm S_5$ and $\rm S_8$ are in the ON state from t_2 to t_3. The difference voltage between $V_{\rm in}$ and $V_{\rm out}$ is applied on the coupled inductor $L_{\rm DM}$, and the current slop $m_{\rm II}$ can be given as follows:

$$m_{\rm II} = \left(V_{\rm in} - V_{\rm out}\right)/L_{\rm DM}. \tag{12}$$

Mode III: In Figs. 5(c) and 6, $\rm S_2$, $\rm S_3$, $\rm S_5$, and $\rm S_8$ are conducting during t_3 to t_4. Since only the output voltage $V_{\rm out}$ is applied to $L_{\rm DM}$, the current slope $m_{\rm III}$ can be derived as follows:

$$m_{\rm III} = -V_{\rm out}/L_{\rm DM}. \tag{13}$$

Mode IV: In Figs. 5(d) and 6, four switches $\rm S_2$, $\rm S_3$, $\rm S_6$, and $\rm S_7$ are turned ON during t_4 to t_5. The voltage across $L_{\rm DM}$ is zero, and the inductor current will free-wheel slope $m_{\rm IV}$ can be given as follows:

$$m_{\rm IV} = 0. \tag{14}$$

Since this free-wheeling mode will increase the rms value of i_L, *Mode IV* is not expected and should be avoided at heavy load. With the combinations of these four operation modes, the inductor current shape can be controlled as a quadrangle. Three difference cases: step-down, unit-gain, and step-up cases are depicted in Fig. 6(a)–(c), respectively. The definition of D_1, D_2, and φ in Fig. 6 is same as traditional FSBB in Fig. 3.

TABLE I
SPECIFICATIONS OF THE PROPOSED 3-L BUCK–BOOST CONVERTER

Variable	Value	Variable	Value
Input voltage V_{in}	900 V	Rating Power P	50 kW
Output voltage V_{out}	500 V to 1 kV	Switching frequency f_s	30 kHz

D. DM Inductor Design and Marginal Power

The specifications of proposed 3-L buck–boost converter are listed in Table I. The input voltage $V_{\rm in}$ is constant as 900 V, and the output voltage $V_{\rm out}$ is from 500 V to 1 kV. The rating power P is 50 kW, and the switching frequency f_s is 30 kHz.

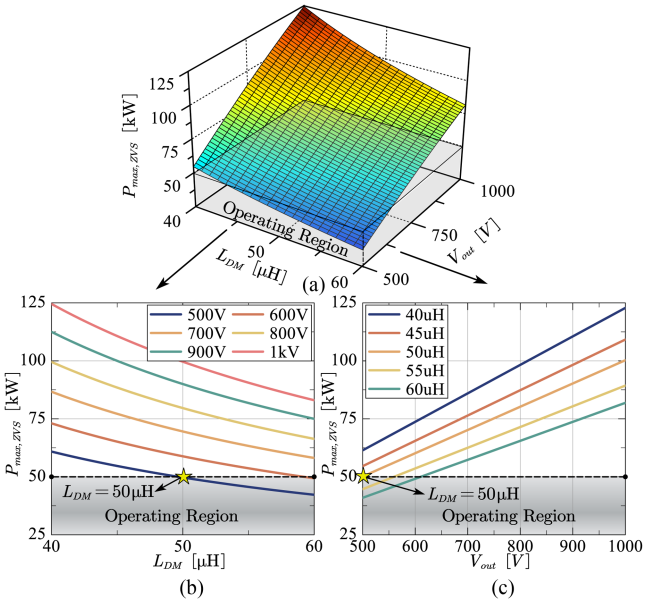


Fig. 7. Relationship between (a) $P_{\mathrm{max,ZVS}}$ with different L_{DM} and V_{out}; (b) $P_{\mathrm{max,ZVS}}$ and L_{DM}; (c) $P_{\mathrm{max,ZVS}}$ and V_{out}.

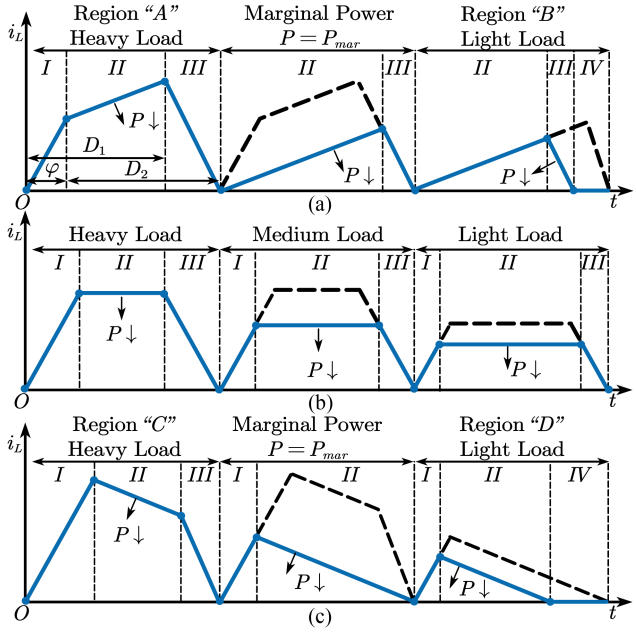


Fig. 8. Inductance current waveforms with different load conditions. (a) Step-down. (b) Unit-gain. (c) Step-up.

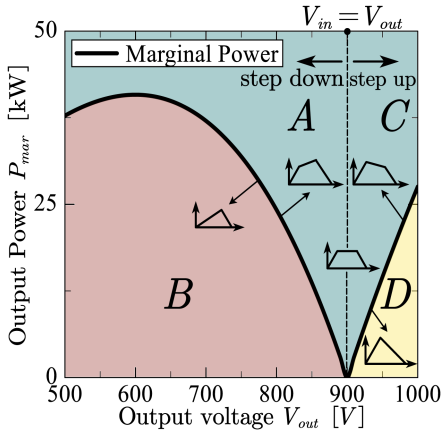


Fig. 9. Relationship between marginal power P_{mar} and output voltage V_{out}.

Due to the similar operation principle as FSBB converter explained in Section II-A, the DM inductance L_{DM} in Fig. 4(b) should be determined by requirement (3). With a fixed $V_{\mathrm{in}} = 900$ V, Fig. 7(a) depicts the maximum ZVS power $P_{\mathrm{max,ZVS}}$ with L_{DM} and V_{out}. To achieve the ZVS, $P_{\mathrm{max,ZVS}}$ should be larger than the rated power P, which means the required operating region should be lower than 50 kW. To simplify the explanation, Fig. 7(b) projects $P_{\mathrm{max,ZVS}}$ in Fig. 7(a) to a two-dimensional (2-D) plane with different V_{out}. Only when L_{DM} is smaller than 50 μH, $P_{\mathrm{max,ZVS}}$ with the full V_{out} range can exceed the rating power 50 kW. If L_{DM} is larger than 50 μH, $P_{\mathrm{max,ZVS}}$ at $V_{\mathrm{out}} = 500$ V will be smaller than 50 kW, which means full load range ZVS will lose. On the other hand, a smaller L_{DM} will cause a larger current ripple from (11)–(13), which means the rms current on inductor will also increase. And then, Fig. 7(c) projects $P_{\mathrm{max,ZVS}}$ to another 2-D plane with different L_{DM}. With a similar analysis, in order to achieve whole range ZVS and minimum rms current, the optimized value of L_{DM} can be reconfirmed as 50 μH.

With a determined L_{DM}, Fig. 8 shows the inductance current i_L waveforms with different load conditions. Under a heavy load, to obtain a minimum rms current, i_L can be controlled as a quadrangle without *Mode IV*. However, if the load becomes more and more lighter, the current shape will change to triangle because of the smaller output current. The marginal power is defined as the power boundary when i_L exactly transforms to a triangle without *Mode IV*. As for the step-down operation as shown in Fig. 8(a), the marginal power case only consists of *Modes II* and *III*. As for the unit gain case, marginal power is equal to zero because i_L always keeps as an isosceles trapezoid as shown in Fig. 8(b). As for the step-up operation, the marginal power case is composed of only *Modes I* and *II* as shown in Fig. 8(c). When the operation power is smaller than P_{mar}, to obtain a smaller output current, *Mode IV* will occur to fill up the blank time. With a determined V_{out}, V_{in}, f_s, and L_{DM}, the marginal power P_{mar} can be given as follows:

$$P_{\mathrm{mar}} = \begin{cases} V_{\mathrm{out}}^2 \left(V_{\mathrm{in}} - V_{\mathrm{out}}\right) / \left(2 f_s L_{\mathrm{DM}} V_{\mathrm{in}}\right) & V_{\mathrm{in}} > V_{\mathrm{out}} \\ V_{\mathrm{in}}^2 \left(V_{\mathrm{out}} - V_{\mathrm{in}}\right) / \left(2 f_s L_{\mathrm{DM}} V_{\mathrm{out}}\right) & V_{\mathrm{in}} \leqslant V_{\mathrm{out}}. \end{cases} \tag{15}$$

The detailed derivation of (15) can be found in the *Appendix*. According to the specifications listed in Table I, Fig. 9 depicts the relationship between the marginal power P_{mar} and the output voltage V_{out}. *Region* "*A*" and "*B*" show the step-up case with heavy load and light load, respectively. And *Region* "*C*" and "*D*" depict the step-down case with heavy and light load. As shown in Fig. 9, the unit gain case is presented by a dashed line ($V_{\mathrm{in}} = V_{\mathrm{out}}$) and its marginal power is equal to zero, which means the shape of i_L keeps as an isosceles trapezoid at the full load range.

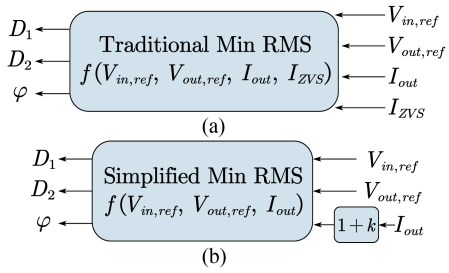


Fig. 10. Minimum rms current calculation blocks for quadrangle control FSBB converter. (a) Traditional calculation. (b) Simplified calculation.

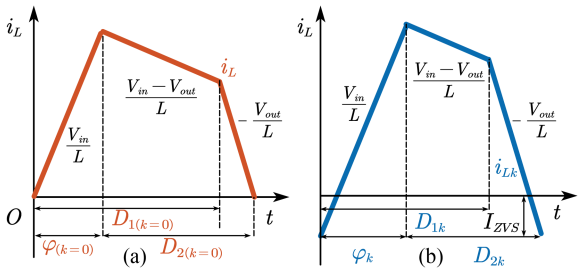


Fig. 11. Inductance current waveforms with different ZVS factor k. (a) When $k = 0$. (b) When $k \neq 0$.

III. Simplified Close-Loop Control

A. Simplified Minimum RMS Current Calculation

As shown in Fig. 3, three basic control variables D_1, D_2, and φ can be used to control the current shape and achieve the three merits: output regulation, soft-switching, and minimum rms current. Fig. 10(a) shows a typical minimum rms current calculation block, which has been widely used to determine D_1, D_2, and φ with four input variables: input and output voltage reference $V_{\text{in,ref}}$, $V_{\text{out,ref}}$, output dc current I_{out}, and negative current I_{ZVS}. In order to avoid the complex real-time calculation, look-up table and extra I_{ZVS} current detection methods have been adopted. However, an external flash is required to store huge look-up table data. And an extra high-frequency current detection circuit is costly and difficult to implement at high power application.

In order to achieve a real-time calculation without extra current detection circuit, a simplified minimum rms current calculation block was proposed as depicted in Fig. 10(b). The input variable I_{ZVS} has been replaced by a ZVS factor "k." This new variable was adopted to simplify the calculation and describe the amplitude of I_{ZVS}. Fig. 11 shows the inductance current i_L with different ZVS factor "k." For example, when the factor k is equal to 0 as shown in Fig. 11(a), the ZVS current I_{ZVS} is also equal to 0. When k is not equal to 0, the negative ZVS current I_{ZVS} will occur as shown in Fig. 11(b), the relationship between I_{ZVS} and k will be explained in Section III-B. Fig. 12 shows the flowchart of the simplified minimum rms current calculation. The first step is to determine load condition. If the output power is larger than marginal power P_{mar} from (15), the current can be controlled as a quadrangle without *Mode IV*, and

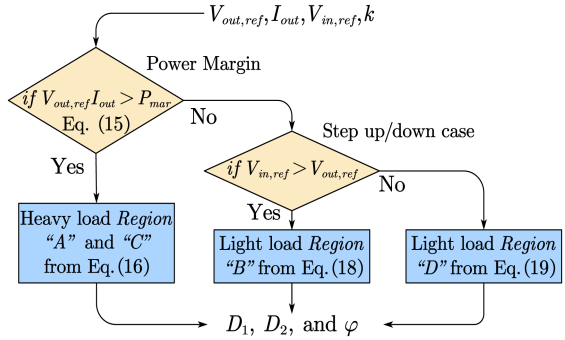


Fig. 12. Flowchart of the simplified minimum rms current calculation.

three basic control variables D_1, D_2, and φ can be derived as follows:

$$\begin{aligned} D_1 &= \frac{V_{\text{out}}}{V_{\text{in}} D_2} \\ D_2 &= 1 - \varphi \\ \varphi &= \frac{1 - \sqrt{V_{\text{in}}^3 V_{\text{out}}^{-3} - 2\,(1+k)\, I_{\text{out}} L_{\text{DM}} f_s \cdot X}}{Y} \end{aligned} \tag{16}$$

where terms "X" and "Y" can be given as follows:

$$\begin{aligned} X &= V_{\text{in}}\, V_{\text{out}}^{-2} + V_{\text{in}}^2 V_{\text{out}}^{-3} + V_{\text{in}}^3 V_{\text{out}}^{-4} \\ Y &= V_{\text{in}}^2\, V_{\text{out}}^{-2} + V_{\text{in}} V_{\text{out}}^{-1} + 1. \end{aligned} \tag{17}$$

Therefore, under the heavy load, *Region* "A" and "C" in Fig. 9 share a unified (16).

When output power is smaller than the marginal power P_{mar}, the second step is to determine the step-up or step-down case. If V_{in} is larger than V_{out}, the derivation for D_1, D_2, and φ under *Region* "B" can be given as follows:

$$\begin{aligned} D_1 &= \frac{\sqrt{2 L_{\text{DM}}\,(1+k)\, I_{\text{out}} V_{\text{out}}}}{V_{\text{in}} \sqrt{\left(1 - \frac{V_{\text{out}}}{V_{\text{in}}}\right) f_s}} \\ D_2 &= \frac{V_{\text{in}}}{V_{\text{out}}} \\ D_1 \varphi &= 0. \end{aligned} \tag{18}$$

As for step-up case ($V_{\text{in}} < V_{\text{out}}$), the derivation for D_1, D_2, and φ under *Region* "D" can be given as follows:

$$\begin{aligned} D_1 &= \frac{\sqrt{2 L_{\text{DM}}\,(1+k)\, I_{\text{out}} V_{\text{out}}}}{V_{\text{in}} \sqrt{\left(1 - \frac{V_{\text{in}}}{V_{\text{out}}}\right) f_s}} \\ D_2 &= \frac{V_{\text{in}}}{V_{\text{out}}}\, D_1 \\ \varphi &= D_1 - D_2. \end{aligned} \tag{19}$$

It should be noted that the marginal power P_{mar} for unit gain case ($V_{\text{in}} = V_{\text{out}}$) is zero, which means only (16) will be adopted for calculation and the inductance current i_L will keep as a

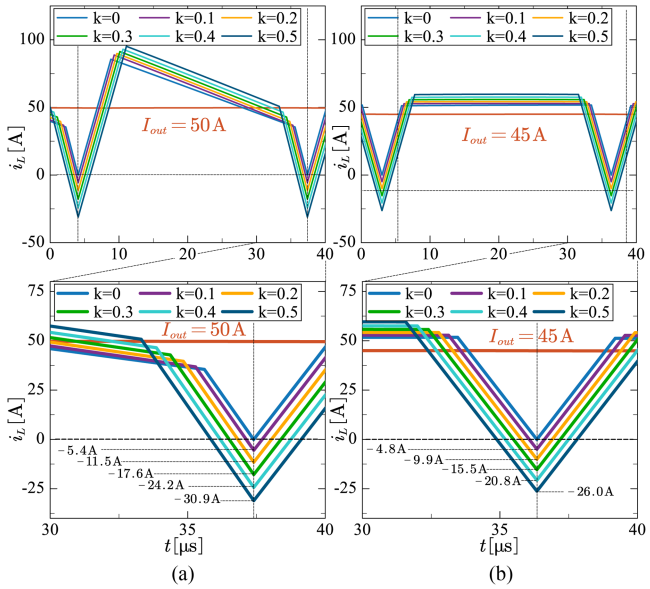


Fig. 13. Inductor current i_L with different ZVS factor k. (a) $V_{\rm in} = 900$ V, $V_{\rm out} = 1$ kV, $P = 50$ kW, and (b) $V_{\rm in} = 900$ V, $V_{\rm out} =$ V, $P = 40.5$ kW.

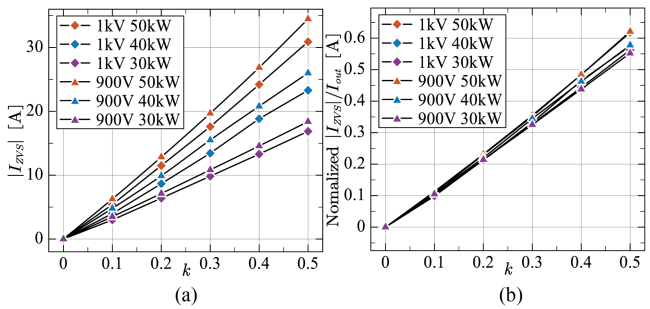


Fig. 14. Relationship between $I_{\rm ZVS}$ and k under different load conditions and output voltages. (a) Before normalization. (b) After normalization.

quadrangle even though under light load condition. The detailed derivation of (15) can be found in the *Appendix*.

B. Linearization and Normalization for I_{ZVS} and k

The relationship between $I_{\rm ZVS}$ and ZVS factor "k" will be discussed in this section. Fig. 13 depicts the simulation results of inductance current i_L with different k. Under a certain load, adopting different k will obtain different amplitude of $I_{\rm ZVS}$. Fig. 13(a) and (b) show the step-up case (900 V to 1 kV) under 50 kW and unit gain case (900–900 V) under 40.5 kW, respectively. The dc output current $I_{\rm out}$ in these two cases are equal to 50 and 45 A. As shown in Fig. 13, with a larger ZVS factor "k," a larger negative $I_{\rm ZVS}$ will be obtained. Fig. 14(a) depicts the amplitude of $I_{\rm ZVS}$ with k under different load conditions and different output voltages (input voltage keeps constant as 900 V). It can be easily found that $I_{\rm ZVS}$ and k are approximately linear relationship. Since different power levels and different output voltages will get different output current $I_{\rm out}$, as shown in Fig. 14(b), the amplitude of $I_{\rm ZVS}$ in Fig. 14(a) are normalized based on $I_{\rm out}$. After the normalization and linearization, the relationship between $I_{\rm ZVS}$ and k can be approximated as below especially when k is close to 0

$$|I_{\rm ZVS}| \,/\, I_{\rm out} = \ 1.1k. \tag{20}$$

With a required I_{ZVS} value from (2), the corresponding k can be obtained from (20). In practice, the value k will be slightly larger than the calculated value to guarantee the ZVS.

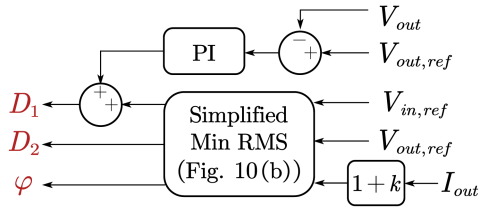


Fig. 15. Close-loop control diagram with simplified minimum rms current calculation block.

C. Close-Loop Control With Simplified Calculation Block

With a simplified minimum rms current calculation block as shown in Fig. 10(b), the close-loop control diagram for this 3-L buck–boost converter was plotted in Fig. 15. Based on $V_{\rm in,ref}$, $V_{\rm out,ref}$, $I_{\rm out}$, and k, the open-loop values of three basic control variables D_1, D_2, and φ can be obtained. However, if there is a tolerance on the value of $L_{\rm DM}$ and measured $I_{\rm out}$, the actual output voltage $V_{\rm out}$ might have a slightly difference from the reference value $V_{\rm out,ref}$. In order to compensate these tolerances and regulate the output voltage accurately, an extra "PI" controller was adopted to slightly change D_1. From (1), the output voltage $V_{\rm out}$ is proportional with D_1. For instance, if the measured $V_{\rm out}$ is larger than the reference value $V_{\rm out,ref}$, the output of "PI" controller is negative. And then, this close-loop control will decrease D_1 to guarantee the actual output voltage $V_{\rm out}$ is exactly equal to the reference value $V_{\rm out,ref}$.

IV. Decoupled Active Balance Control

A. Proposed ΔD_1 and ΔD_2 for Voltage Balance

As mentioned before, in order to reduce CM voltage, this proposed 3-L buck–boost converter should have the symmetric driving gate signal theoretically. Fig. 16 shows the detailed circuit diagram of this proposed 3-L buck–boost converter. At the input side, both top and bottom duties $D_{1\,T}$ and $D_{1\,B}$ should be equal to D_1. As for the output side, both $D_{2\,T}$ and $D_{2\,B}$ should be equal to D_2

$$\begin{cases} D_{1T} = D_{1B} \ = D_1 \\ D_{2T} = D_{2B} \ = D_2. \end{cases} \tag{21}$$

The duties D_1 and D_2 could be obtained by the close-loop control as shown in Fig. 15. As shown in Fig. 16, at the input side, V_{iT} and V_{iB} are the voltages across the split top and bottom capacitors. V_{oT} and V_{oB} are the voltages across the output side split capacitors. The relation between total input (output) voltages and split V_{iT} and V_{iB} (V_{oT} and V_{oB}) can be easily

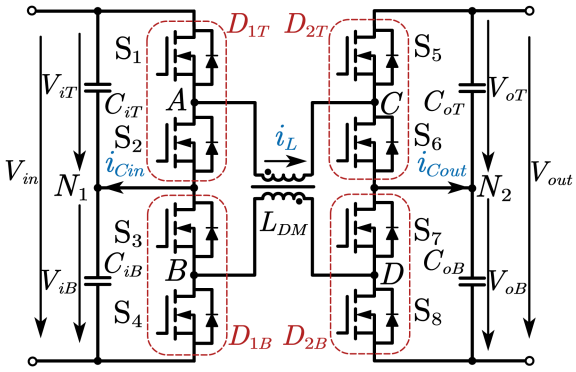


Fig. 16. Circuit diagram of the 3-L buck–boost converter with decoupled balance control.

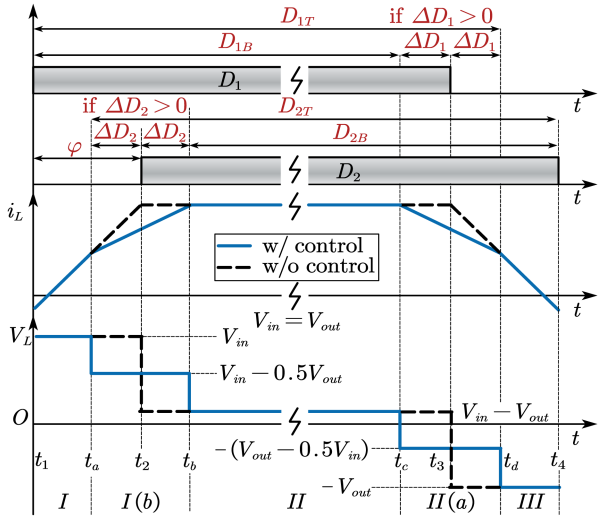


Fig. 17. Corresponding waveforms of the gate signals, inductor current i_L, and inductor voltage V_L.

derived as follows:

$$\begin{cases} V_{\text{in}} = V_{iT} + V_{iB} \\ V_{\text{out}} = V_{oT} + V_{oB}. \end{cases} \tag{22}$$

Due to the tolerance between top and bottom half bridges, such as the gate driver propagation delay, the split capacitor voltages imbalance might happen on both input and output side ($V_{iT} \neq V_{iB}$ and $V_{oT} \neq V_{oB}$). However, four basic operation modes *Modes I–IV* in Fig. 5 have no capability to regulate the balance on either input or output side because both sides split capacitor currents $i_{C\text{in}}$ and $i_{C\text{out}}$ in Fig. 16 are always 0. Therefore, the ideal symmetric 3-L buck–boost converter with only four basic modes might suffer from the imbalance issue on both input and output side.

In order to decouple the balance control of the input and output sides, two small duty differences ΔD_1 and ΔD_2 have been introduced as shown in Fig. 17. With these two control variables, the top side duties $D_{1(2)\text{T}}$ will not equal to the bottom side $D_{1(2)\text{B}}$ anymore, and the new relationship can be given as

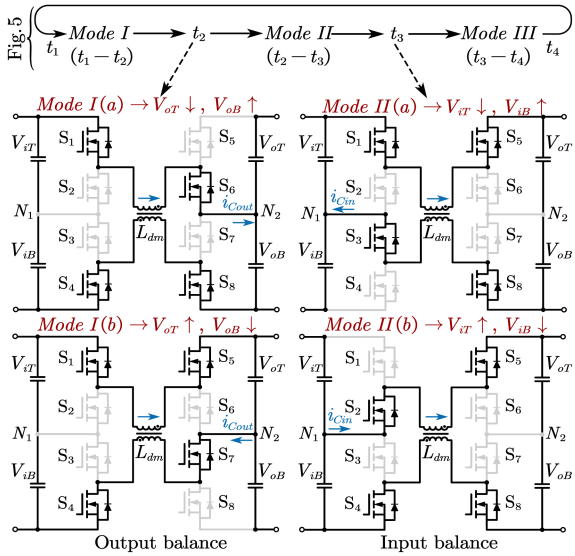


Fig. 18. Equivalent circuits of four intermediate modes.

follows:

$$\begin{cases} D_{1(2)T} = D_{1(2)} + \Delta D_{1(2)} \\ D_{1(2)B} = D_{1(2)} - \Delta D_{1(2)}. \end{cases} \tag{23}$$

From (23), the total voltage gain $V_{\text{out}}/V_{\text{in}}$ can be still maintained as D_1/D_2 as shown in (24), which means that the midpoint balancing control will not influence the output regulation

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{D_{1T} + D_{1B}}{D_{2T} + D_{2B}} = \frac{D_1}{D_2}. \tag{24}$$

B. Four Intermediate Operation Modes

After introducing ΔD_1 and ΔD_2, Fig. 17 shows the gating signals $D_{1(2)}$, $D_{1(2)\,T}$, $D_{1(2)\,B}$, and inductor current i_L and voltage V_L. The inductor voltage V_L applied to the coupled inductor can be expressed as follows:

$$V_L = V_{AC} + V_{DB}. \tag{25}$$

As shown in Fig. 17, compared with no balancing control, the current i_L will have two small differences during t_a-t_b and t_c-t_d. These two small differences on i_L are caused by different voltages V_L across the coupled inductor. According to the polarity of ΔD_1 and ΔD_2, four possible new intermediate modes *Mode I*(a), *Mode I*(b), *Mode II*(a), and *Mode II*(b) will be introduced as shown in Fig. 18. Each intermediate mode has the capability to control either the input or output side balancing. The detailed balancing effects of these four modes are listed in Table II. Since *Mode I*(a) and *Mode I*(b) can only impact the output side split capacitor current $i_{C\text{out}}$, ΔD_1 is dedicated to controlling the output side balance. As for the output side, ΔD_2 can be adopted to control the input side split capacitor current $i_{C\text{in}}$.

For example, if ΔD_1 and ΔD_2 are both positive as shown in Fig. 17, *Mode I*(b) and *Mode II*(a) will be introduced during t_a-t_b and t_c-t_d. Based on the balancing effect in Table II, *Mode*

TABLE II
BALANCING EFFECT OF FOUR INTERMEDIATE OPERATION MODES

Mode	Side	i_{Cin} and i_{Cout}	Balancing Effect	$\Delta D_{1(2)}$ polarity
Mode I(*a*)	output	i_{Cin}=0, i_{Cout}>0	$V_{oT}\downarrow$ $V_{oB}\uparrow$	negative ΔD_2
Mode I(*b*)		i_{Cin}=0, i_{Cout}<0	$V_{oT}\uparrow$ $V_{oB}\downarrow$	positive ΔD_2
Mode II(*a*)	input	i_{Cin}>0, i_{Cout}=0	$V_{iT}\downarrow$ $V_{iB}\uparrow$	positive ΔD_1
Mode II(*b*)		i_{Cin}<0, i_{Cout}=0	$V_{iT}\uparrow$ $V_{iB}\downarrow$	negative ΔD_1

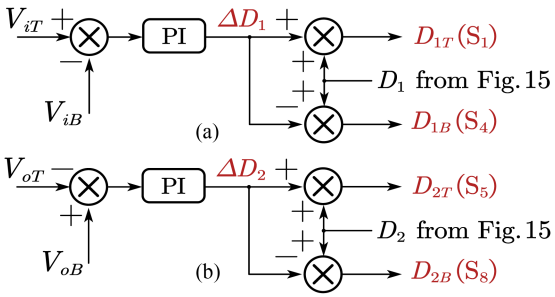


Fig. 19. Decoupled active balance control. (a) Input side. (b) Output side.

I(*b*) will increase the V_{oT} and decrease the V_{oB}, and *Mode II*(*a*) will decrease the V_{iT} and increase the V_{iB}. Therefore, the input and output side balance control can be decoupled by ΔD_1 and ΔD_2.

C. Close-Loop Control and Simulation

Since the input and output split capacitor voltages can be separately controlled by ΔD_1 and ΔD_2, the decoupled active balance was proposed in Fig. 19. By measuring the split capacitor voltages V_{iT}, V_{iB}, V_{oT}, and V_{oT}, the input and output voltage differences (V_{iT} -V_{iB}) and (V_{oB} -V_{OT}) can be feedbacked. According to the balance mechanism listed in Table II, two "PI" controller can be adopted to regulate the input and output balance, respectively. The outputs of these two "PI" controllers are the ΔD_1 and ΔD_2. Based on the total output voltage close-loop control as shown in Fig. 15, three basic control variables D_1, D_2, and φ can be obtained in advance. With these three basic variables and $\Delta D_{1(2)}$, from (23), the duties $D_{1\,T(B)}$ for the input side, and $D_{2\,T(B)}$ for output side can be determined, respectively. As shown in Fig. 16 and 19, $D_{1\,T(B)}$ are the driving signals for switches $S_{1(4)}$, and $D_{2\,T(B)}$ are the driving signals for $S_{5(8)}$.

In order to verify the proposed active decoupled balance control shown in Fig. 19, a unit gain case from 900 to 900 V under 45 kW has been simulated as shown in Fig. 20. To create some imbalance because of the circuit tolerance, the initial value of the input and output split capacitor voltages V_{iT}, V_{iB} V_{OT} V_{oB} were set to 500, 400, 400, and 500 V. Before 3 ms, only output voltage close-loop control shown in Fig. 15 was adopted. As explained in Section IV-A, this close-loop control has no capability to control either input or output balance because of the zero split capacitor currents $i_{C\text{in}}$ and $i_{C\text{out}}$.

At 3 ms, the proposed decoupled active balance control shown in Fig. 19 was added on both input and output side. After 3 ms, with this decoupled control, the input and output split capacitor voltages V_{iT}, V_{iB} V_{OT} V_{oB} begin to converge toward the equilibrium value 450 V. After zooming in the inductor

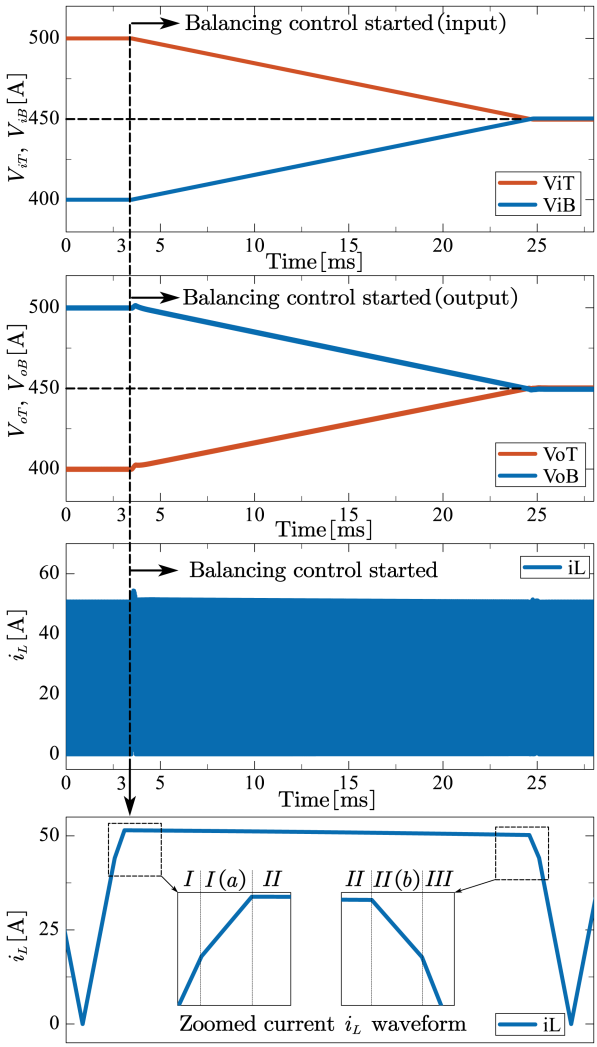


Fig. 20. Simulation results for the decoupled active balance control under 45 kW unit gain case (900–900 V).

current i_L at 3 ms, intermediate modes *Mode I*(a) and *Mode II*(b) can be seen because V_{iT} is larger than V_{iB} at the input side, and V_{oT} is smaller than V_{oB} at the output side. More experimental results for this decoupled active control will be provided in following Section V.

V. HARDWARE PROTOTYPE AND EXPERIMENTAL RESULTS

A. Prototype Implementation and Hardware Setup

As shown in Fig. 21, a 50 kW 3-L buck–boost converter with planar coupled inductor was built first. The specifications have been listed in Table I, and more technical details of this proposed 3-L buck–boost converter are listed in Table III. In order to improve the power density and handle large dc bias flux, planar magnetics was adopted with amorphous AMCC core from *Hitachi*. And then, the heavy copper printed circuit board (PCB) technique has been used for inductor windings to handle the large current. The turns numbers are 7:7, and the thickness of the trace is 15 oz. To reduce the fringing effect loss, two-board

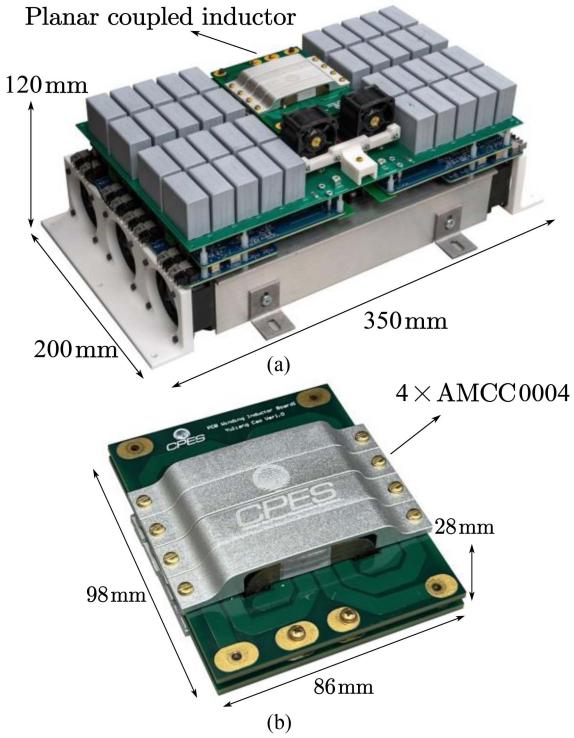


Fig. 21. 50 kW 3-L buck–boost converter prototype with a planar coupled inductor. (a) Whole power stage. (b) Heavy copper coupled inductor.

TABLE III
TECHNICAL DETAILS OF 3-L BUCK–BOOST CONVERTER

	Component		Parameter	Description
Coupled Inductor	core		AMCC-0004 × 4	Hitachi amorphous core
	Pri. turns		7 (two layers parallel)	Heavy copper PCB (15 oz)
	Sec. turns		7 (two layers parallel)	Heavy copper PCB (15 oz)
	L_{DM}		50.4 μH	Differential mode inductance
	Air gap		1.8 mm	Ceramic pad for the air gap
Capacitors & Devices	C_{iT}		20 μF × 10	Split dc bus film capacitor
	C_{iB}		20 μF × 10	Split dc bus film capacitor
	C_{oT}		20 μF × 10	Split dc bus film capacitor
	C_{oT}		20 μF × 10	Split dc bus film capacitor
	SiC Module		1.2 kV half bridge × 4	*GE12047CCA3* 4 mΩ at 25 °C
Cooling System	Fan	Planar Inductor	24 V_{DC} (5 W) × 2	25× 25×20 mm^3 (10.5 CFM)
		Module heatsink	24 V_{DC} (3 W) × 6	60×60 ×25 mm^3 (5.5 CFM)

design was adopted. Following the design procedure of L_{DM} in Fig. 7, the airgap is designed as 1.8 mm and a coupled inductor with 50.4 μH $L_{\rm DM}$ has been obtained. Due to the low-profile design, as shown in Fig. 21(b), the power density of this planar inductor is 3.5 kW/in^3. As for the split dc-link capacitors C_{iT}, C_{iB}, C_{oT}, and C_{oB} shown in Fig. 16, ten 20 μF film capacitors are connected in parallel. Due to the small turn-ON resistance $R_{ds,\rm on}$ (4 mΩ at 25 °C), four 1.2 kV SiC half bridge modules *GE12047CCA3* from *GE* have been adopted. Finally, two 25 mm fans are used for planar coupled inductor cooling, and six 60 mm fans are used for total four SiC modules cooling.

To verify the CM noise reduction, Fig. 22(a) and (b) show the testing setups for the proposed 3-L buck–boost converter and typical FSBB converter, respectively. For both setups, a 50 arms

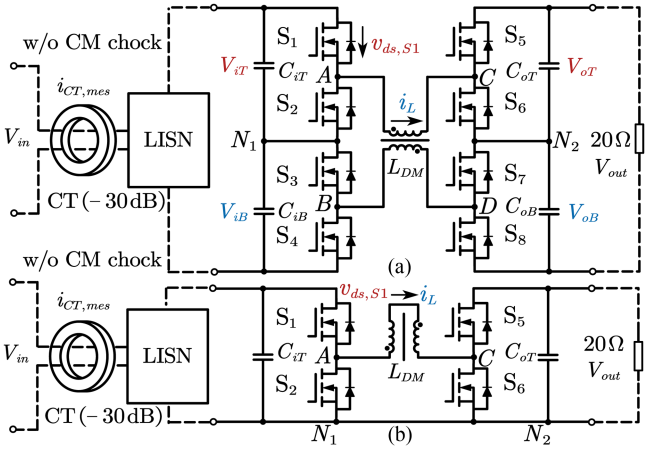


Fig. 22. Diagrams of the experimental setups. (a) Proposed 3-L buck–boost converter. (b) Typical FSBB converter.

line impedance stabilization network was connected at the input side, and a current transducer (CT) was used to measure the CM current. The current $i_{\rm CT,mes}$ is the output of the CT. Since the selected CT has a 30 dB external attenuation, the measured CM current $i_{\rm CM}$ can be expressed as follows:

$$i_{\rm CM} = 10^{1.5} \cdot i_{\rm CT,mes}/2. \tag{26}$$

The experimental results in the next part will only show the CM current $i_{\rm CM}$ after converting. A 900 V dc source was connected at input side, and the output side adopts a 20 Ω resistance load. As shown in Fig. 22(b), the top half of 3-L buck–boost converter in Fig. 22(a) was adopted as a typical FSBB converter, and two mid-points N_1 and N_2 were connected. To obtain the same inductor current i_L in the typical FSBB converter (same value of $L_{\rm DM}$), the coupled inductor was connected as shown in Fig. 22(b). It should be noted that no CM choke was used in these two setups. The following experimental results for both 3-L buck–boost converter and typical FSBB will keep the same setup as shown in Fig. 22. Since this 3-L buck–boost converter was adopted on the rear-end, more details about the whole grid-interface converter including gate driver design and communication design can be found in [37], [38], and [39].

B. Experimental Results for CM Noise Suppression

Fig. 23 shows the experimental results for the 3-L buck–boost converter with decoupled active balance control. The input voltage $V_{\rm in}$ is kept as 900 V. With four different output voltages $V_{\rm out}$, the step-up case ($V_{\rm out} = 1$ kV), unit gain case ($V_{\rm out} = 900$ V), and step-down cases ($V_{\rm out} = 800$ V, $V_{\rm out} = 500$ V) are depicted in Fig. 23(a)–(d), respectively. As shown in Fig. 22(a), since the load is a constant 20 Ω resistance, the output powers for these four cases are 50, 40.5, 32, and 12.5 kW. And the corresponding output current are 50, 45, 40, and 25 A. As shown in Fig. 23, it can be easily seen that both the input and output side voltages V_{iT}, V_{iB}, V_{oT}, and V_{oT} have been balanced well, which could verify the proposed decoupled active balance control.

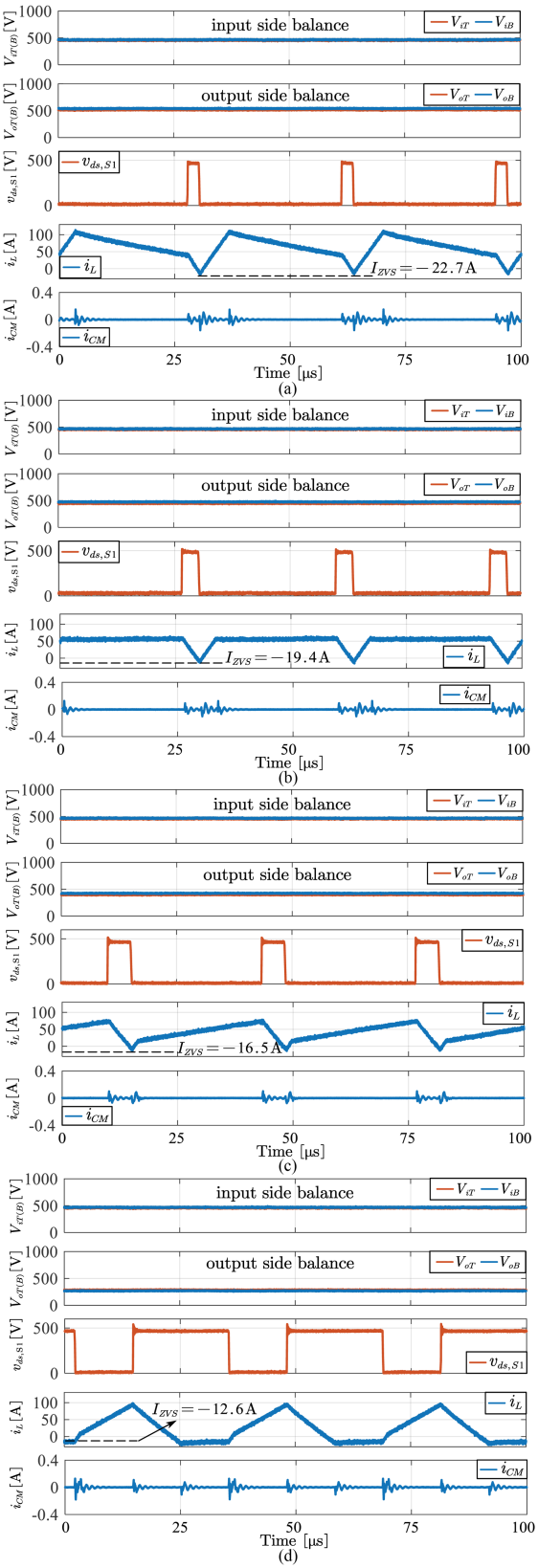


Fig. 23. Experimental results of the 3-L buck–boost converter with decoupled balance control. (a) $V_{\text{out}} = 1$ kV. (b) $V_{\text{out}} = 900$ V. (c) $V_{\text{out}} = 800$ V. (d) $V_{\text{out}} = 500$ V.

As for the soft switching, with 300 ns deadtime and 3.2 nF time-related output capacitance from 0 to 500 V, the required negative ZVS current I_{ZVS} can be calculated as –21.3 A from (2). According to the approximate relationship between I_{out} and I_{ZVS} from (20), the ZVS factor k was set as 1.4 with a small margin. As shown in Fig. 23, under different output currents, 50 A ($V_{\text{out}} = 1$ kV), 45 A ($V_{\text{out}} = 900$ V), 40 A ($V_{\text{out}} = 800$ V), and 25 A ($V_{\text{out}} = 500$ V), the measured I_{ZVS} are –22.7, –19.4, –16.5, and –12.2 A. With these measured I_{ZVS}, the approximate linear relationship in (20) between I_{out} and I_{ZVS} can also be verified.

The experimental results without the decoupled active control were plotted in Fig. 24. Except for the balance control, Fig. 24 keeps the same testing conditions as Fig. 23. As mentioned before, due to the circuit tolerances, distinguished voltage differences (up to 92 V) existed at both input and output sides without a balance control.

Following the setup shown in Figs. 22(b) and 25 shows the experimental results for a typical FSBB converter. Since the rating voltage of the SiC module is 1.2 kV, for a safety operation, only 900, 800, and 500 V output cases have been conducted in typical FSBB converter. The testing results of these three cases have been plotted in Fig. 25(a)–(c), respectively. Compared with results 3-L buck–boost converter shown in Figs. 24 and 25, the inductance current i_L should be same because the inductance value L_{DM} has been kept same.

Fig. 26 plots all the measured CM current results from Figs. 23–25 in the frequency domain (150 kHz–30 MHz). The results of 900, 800, and 500 V output voltages are represented in Fig. 26(a)–(c), respectively. The results of 3-L buck–boost converter with balance control, without balance control, and typical FSBB converter are depicted together with the standard requirement DO-160.

From 150 to 500 kHz, the amplitude of CM current i_{CM} are close in all three cases. From 500 kHz to 1 MHz, compared with typical FSBB, CM current i_{CM} of 3-L buck–boost with or without balance control both have up to 15 dB attenuation. After 1 MHz, the merits of 3-L buck–boost are more obvious. From 3 to 30 MHz, the 3-L buck–boost with or without balance control both have about 15 dB (up to 25 dB) attenuation.

The dynamic experimental results for the soft start-up and close-loop output voltage regulation have been shown in Fig. 27(a) and (b), respectively. The load is still a 20 Ω resistance. During the close-loop soft start-up, the input voltage V_{in} has been pre-charged to 900 V first. To increase the output voltage V_{out} from 0 V to 1 kV, a ramp reference volage $V_{\text{out,ref}}$ is adopted in the close-loop control.

After finishing the start-up procedure, to verify the close-loop output regulation capability, a triangular output voltage reference $V_{\text{out,ref}}$ from 500 V to 1 kV and back again was given as shown in Fig. 27(b). With the simplified close-loop control, the output can be well-regulated because V_{out} can follow the reference $V_{\text{out,ref}}$.

Remark: In order to visualize the close-loop balance control and soft start-up shown in Figs. 23, 24, and 27, this article is accompanied with two additional recordings *Video A* and *B*. Following the same set-up shown in Fig. 22(a), *Video A*

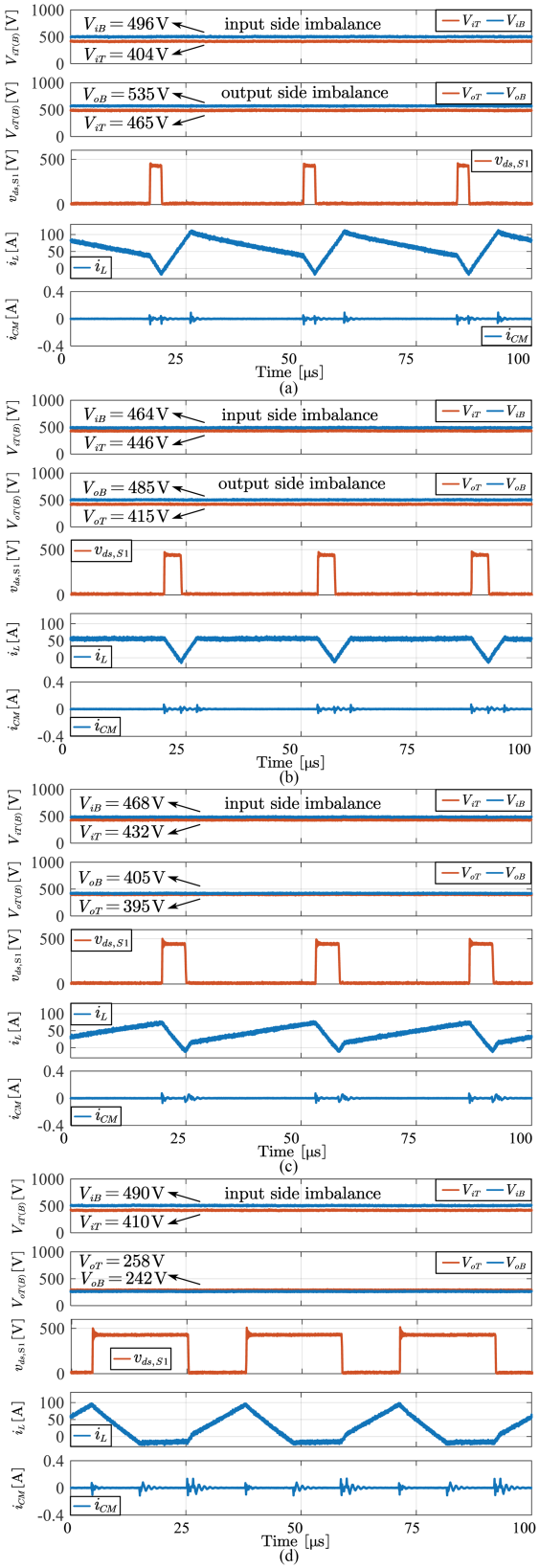


Fig. 24. Testing results of the 3-L buck–boost converter without decoupled balance control. (a) $V_{\text{out}} = 1$ kV. (b) $V_{\text{out}} = 900$ V. (c) $V_{\text{out}} = 800$ V. (d) $V_{\text{out}} = 500$ V.

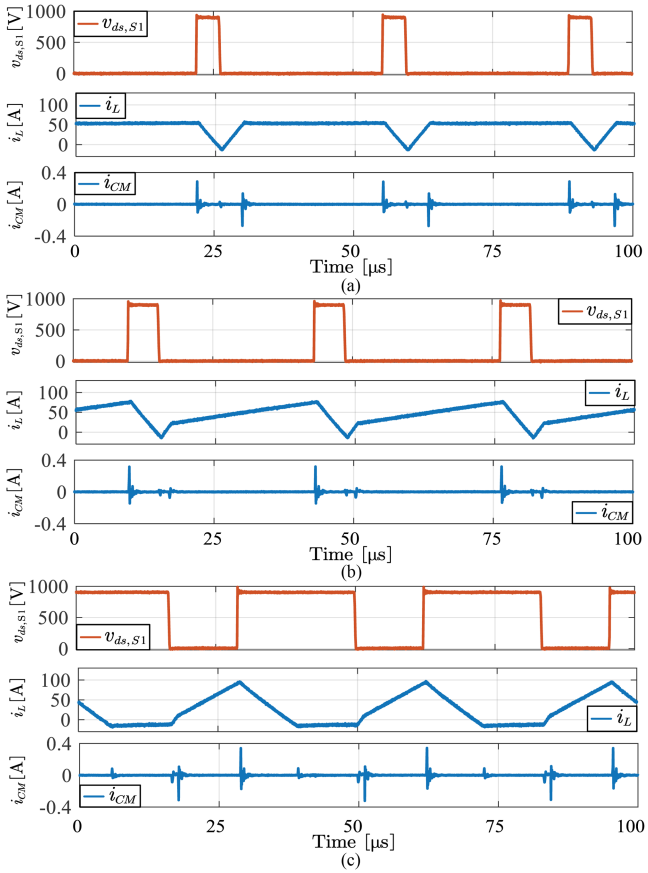


Fig. 25. Testing results of the typical FSBB converter. (a) $V_{\text{out}} = 900$ V. (b) $V_{\text{out}} = 800$ V. (c) $V_{\text{out}} = 500$ V.

and *B* record the soft start-up with or without balance control, respectively. The oscilloscope screen shows several waveforms (from top to bottom): Channel C3 (red) and C4 (green) show the input side split capacitor voltages V_{iT} and V_{iB}; Channel C1 (yellow) and C2 (blue green) show the output side split capacitor voltages V_{oT} and V_{oB}; Channel C5 (brown) shows the voltage v_{N1N2} across the input and output midpoints N_1 and N_2; Channel C8 (dark green) shows the drain–source voltage $v_{ds,S1}$ of switch S_1, Channel C7 (pink) shows the measured current $i_{\text{CT,mes}}$ from the CT which has an external 30 dB attenuation, and Channel C6 (blue) shows the measured inductor current i_L through the heavy copper planar coupled inductor.

C. *Switching Transition Results and* I_{ZVS} *With Different* "k"

Following the setup shown in Figs. 22(a), 28, and 29 plot the zoomed waveforms for proposed 3-L buck–boost converter without or with the balance control. The deadtime t_d has been changed from 300 to 600 ns in these two cases. In Figs. 28 and 29, from the top to bottom, eight channels scope was used to record the waveforms of $v_{ds,S2}$, $v_{ds,S3}$, ($v_{ds,S2}$- $v_{ds,S3}$), $v_{ds,S6}$, $v_{ds,S7}$, ($v_{ds,S6}$ - $v_{ds,S7}$), $i_{\text{CT,mes}}$, v_{N1N2}, i_L. The steady-state values of $v_{ds,S2}$, $v_{ds,S3}$ and $v_{ds,S6}$, $v_{ds,S7}$ can indicate the split dc cap voltages on both input and output sides V_{iT}, V_{iB}, V_{oT}, V_{oB}.

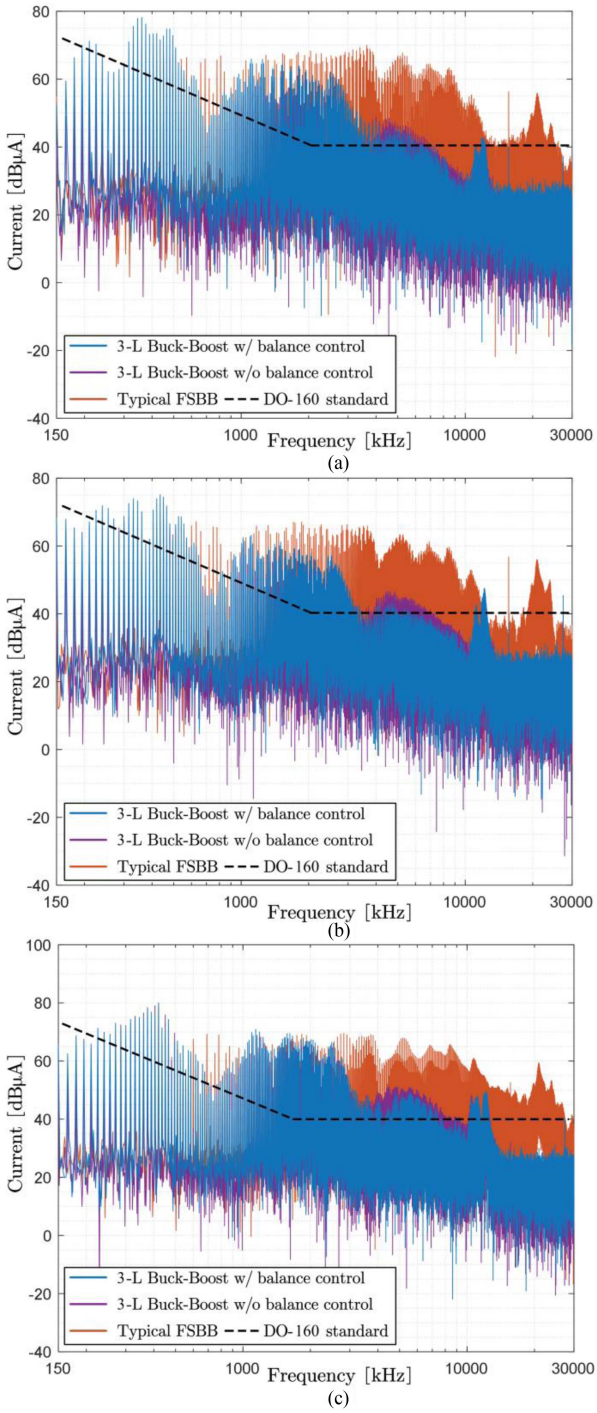


Fig. 26. Measured CM current results under different cases. (a) $V_{\rm out} = 900$ V. (b) $V_{\rm out} = 800$ V. (c) $V_{\rm out} = 500$ V.

($v_{ds,S2}$–$v_{ds,S3}$) and ($v_{ds,S6}$ –$v_{ds,S7}$) are two CM noise sources in this topology.

As shown in Fig. 28(b) and (c), the falling edges of $v_{ds,S2}$, $v_{ds,S3}$ and the rising edges of $v_{ds,S6}$, $v_{ds,S7}$ hardly have any delay. However, due to no balance control, the steady state will have the difference. After adding the balance control as shown in Fig. 29(b) and (c), $v_{ds,S6}$ and $v_{ds,S7}$ can match very well in both switch transition and steady state.

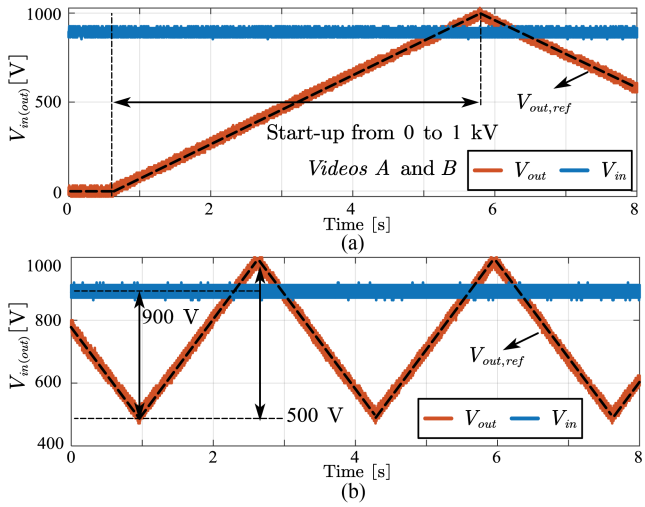


Fig. 27. Dynamic close-loop experimental results. (a) Soft start-up. (b) Output voltage regulation.

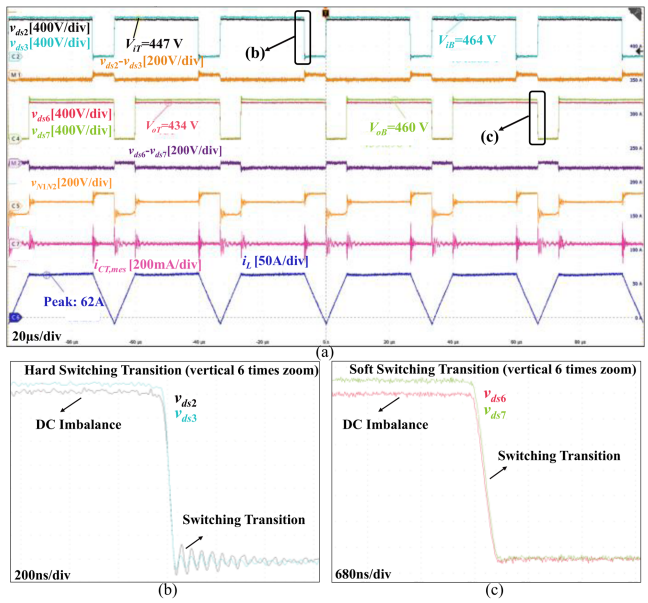


Fig. 28. Experimental results ($V_{\rm out} = 900$ V, $P = 45.5$ kW t_d= 600 ns) without decoupled active balance control. (a) Large-scale voltage and current waveforms. (b) Zoomed $v_{ds,2}$ and $v_{ds,3}$ during hard switching transition. (c) Zoomed $v_{ds,6}$ and $v_{ds,7}$ during soft-switching transition.

To verify the approximate linear relationship between "ZVS factor" k and negative ZVS current $I_{\rm ZVS}$, the experimental results with different k under $V_{\rm out} = 900$ V, $P = 45$ kW, $t_d = 600$ ns are plotted in Fig. 30. When k = 0.2, 0.3, 0.4, 0.5, the negative current $I_{\rm ZVS}$ are equal to –10, –15.6, –20.8, and –26 A, respectively. Therefore, the approximate linear relationship between $I_{\rm ZVS}$ and "k" in (20) can be verified.

D. Thermal Performance and Efficiency

Fig. 31 shows the thermal result of the coupled inductor. Benefits from 15 oz heavy copper PCB technique, the hot spot temperature is 47.1 °C under 50 kW, 1 kV output voltage.

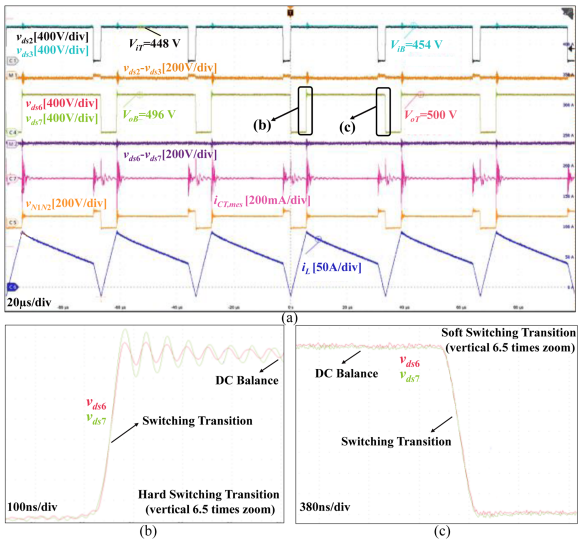


Fig. 29. Experimental results ($V_{\rm out}$ = 1 kV, P = 50 kW t_d = 600 ns) with decoupled active balance control. (a) Large-scale voltage and current waveforms. (b) Zoomed $v_{ds,6}$ and $v_{ds,7}$ during hard switching transition. (c) Zoomed $v_{ds,6}$ and $v_{ds,7}$ during soft-switching transition.

More details about this heavy copper coupled inductor design and core loss measurement can be found in [40] and [41].

With the consideration of auxiliary losses such as gate driving losses, controller losses, and cooling fans losses, the conversion efficiency of the proposed 3-L buck–boost converter and 2-L FSBB are both shown in Fig. 32. The peak efficiency of the 3-L buck–boost converter is 98.9% and occurs at full load unit gain case ($V_{\rm out}$ = 900 V). Compared with the 3-L buck–boost, 2-L FSBB with the same setup has a slightly higher efficiency because only the top half circuit was used as shown in Fig. 22(b). Theoretically, 2-L FSBB and 3-L buck–boost should have similar efficiency because half voltage rating device can be selected on 3-L buck–boost topology. More discussion on the difference between 3-L buck–boost and 2-L FSBB will be explained in the next part.

In addition, the loss breakdown of the proposed 3-L buck–boost converter at 50 kW is plotted in Fig. 33. Among step-up, step-down, and unit gain cases, unit-gain case has the lowest peak current because of a flat trapezoidal current waveform. Therefore, the conduction loss $P_{\rm cond}$ of the unit case is relatively small. Due to the ZVS, the switching loss $P_{\rm sw}$ is dominated by turn-OFF switching loss. With the smallest current ripple, unit-gain case has the lowest $P_{\rm sw}$ among these four cases.

As for the coupled inductor winding loss $P_{\rm wind}$ and core loss $P_{\rm core}$, the results are derived from Q3D finite element analysis simulation and improved generalized Steinmetz equation calculation. As for the P_{other}, it includes the power for all the fans, controller, gate drivers, voltage and current sensors.

E. Comparison of 3-L Buck–Boost Converter and 2-L FSBB

The comparison between the proposed 3-L buck–boost converter and traditional 2-L FSBB converter is listed in Table IV. It should be noted that except switch number, gate driver number, other variables have been normalized based on 2-L FSBB. For example, if the conventional 2-L FSBB has 1 per unit (p.u.) voltage stress on each device, the proposed 3-L buck-boost converter only has 0.5 p.u.

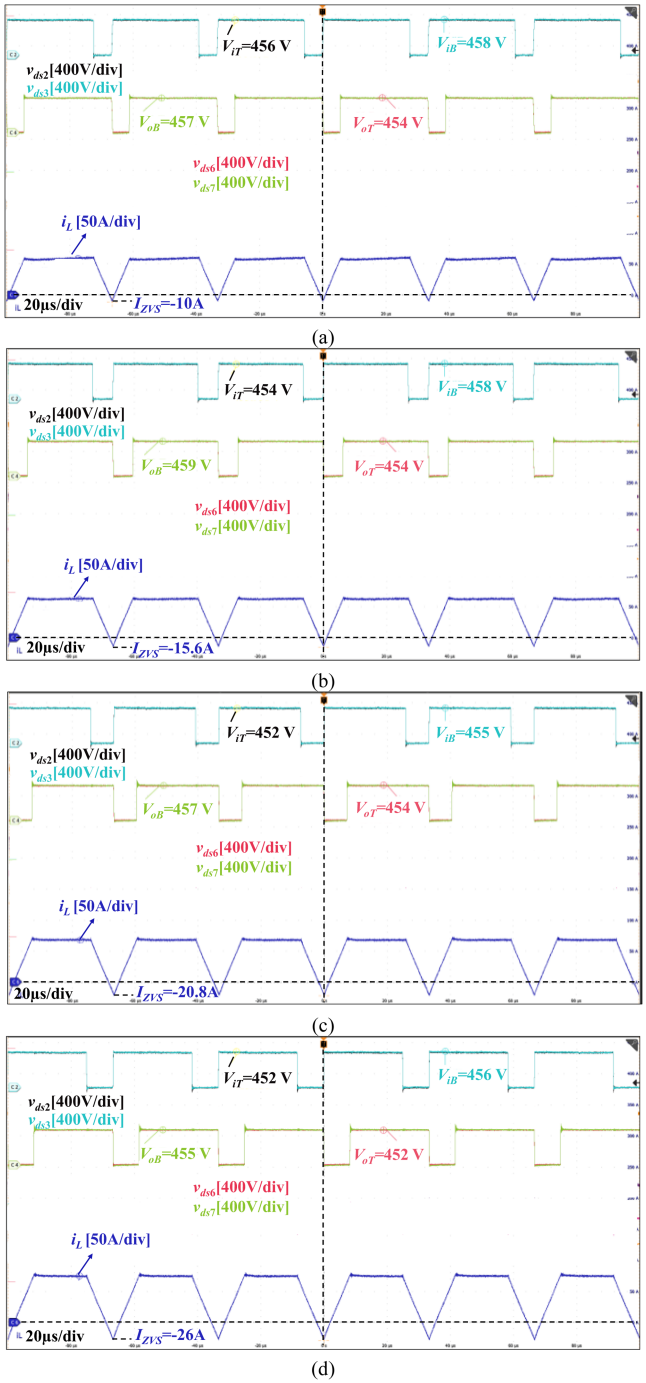


Fig. 30. Experimental results with different "ZVS factor" k under $V_{\rm out}$ = 900 V, P = 45 kW, t_d = 600 ns. (a) k = 0.2. (b) k = 0.3. (c) k = 0.4. (d) k = 0.5.

Based on Table IV, the loss comparison can be explained as follows.

1) Device switching loss: Considering the device number, device voltage and current stress, the total switching loss of these two topologies should be very similar with the same inductor current waveform i_L.

Fig. 31. Thermal testing results for the planar coupled inductor under 50 kW step-up case (900 V to 1 kV).

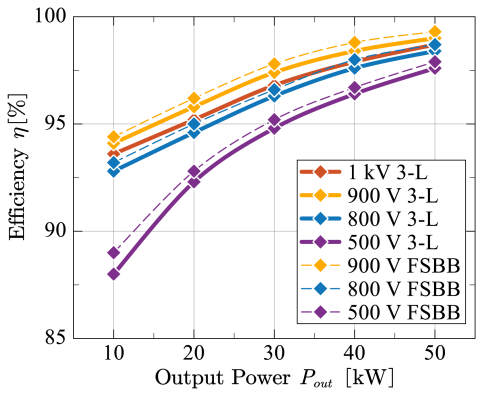


Fig. 32. Efficiency of the 3-L buck-boost converter and 2-L FSBB with different output voltage. The 2-L FSBB cannot run at 1 kV because the device rating is only 1.2 kV.

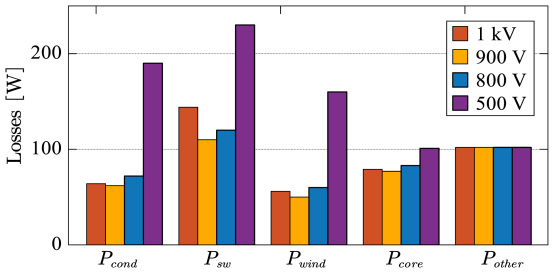


Fig. 33. Loss breakdown of 3-L buck–boost converter at 50 kw with different output voltages.

TABLE IV
COMPARISON OF THE PROPOSED 3-L BUCK–BOOST CONVERTER AND 2-L FSBB

Variable	3-L buck-boost	2-L FSBB
Switch voltage stress (P.U.)	0.5	1
Switch current stress (P.U.)	1	1
Switch number	8	4
Capacitor voltage stress (P.U.)	0.5	1
Capacitor Value (P.U.)	2	1
Inductor voltage stress (P.U.)	1	1
Inductor voltage stress (P.U.)	1	1
Gate driver number	8	4
Mid-points balance control	Yes	No
CM noise	Small	Large

2) Device conduction loss: With the assumption that double voltage rating device will have double $R_{ds(\mathrm{on})}$, the total device conduction loss will be similar.
3) Inductor loss: Due to the same voltage and current stress on the inductor, the conduction loss and core loss of the inductor should be very similar between these two topologies.

In addition to the loss comparison, with up to 25 dB CM noise, the CM filter for the proposed 3-L buck–boost converter will be smaller than traditional FSBB.

It should be noted that this article focuses on the CM noise reduction. And thus, the 2-L FSBB in this article is only for the purpose of CM noise comparison. With 1.2 kV SiC module, the output voltage of 2-L FSBB can be pushed up to 900 V. However, the required maximum V_{out} is 1 kV, which means 2-L FSBB cannot meet this requirement. If 2-L FSBB was selected, 1.7 kV SiC devices should be adopted to meet 1 kV V_{out}. However, the availability of 1.7 kV SiC modules is a concern when more 1.2 kV commercial SiC modules exist from multiple vendors in the market. Therefore, there is a tradeoff between device availability and converter complexity.

VI. CONCLUSION

In this article, a symmetric 3-L buck–boost converter with coupled inductor is presented for CM noise reduction. The operation principle of the proposed 3-L buck–boost converter with quadrangle control is illustrated first. In order to realize a real-time close-loop control without look-up table or extra circuits, a simplified minimum rms current calculation block is developed. In addition, a decoupled active balance control for both input and output sides is proposed.

Finally, to verify the CM noise reduction, the simplified close-loop control, and the decoupled balance control, a 30 kHz 50 kW symmetric 3-L buck–boost converter was built with a 98.9% peak efficiency. Compared with typical FSBB converter, the symmetric 3-L buck–boost converter has up to 25 dB CM noise reduction. Thus, this proposed topology with its related control methods has great potential to improve the performance of grid-interface converter in PV system, and EV charging system.

APPENDIX

The derivation details of (15)–(19) will be explained as follows. (A1) can be easily derived first as the definitions in Fig. 6. The derivation of (A2) can be found in [27]

$$\begin{cases} I_1 - I_{\mathrm{ZVS}} = V_{\mathrm{in}}/L_{\mathrm{DM}} \cdot (t_2 - t_1) \\ I_2 - I_1 = (V_{\mathrm{in}} - V_{\mathrm{out}})/L_{\mathrm{DM}} \cdot (t_3 - t_2) \\ I_2 - I_{\mathrm{ZVS}} = V_{\mathrm{out}}/L_{\mathrm{DM}} \cdot (t_4 - t_3) \end{cases} \tag{A1}$$

$$P = \frac{V_{\mathrm{in}}}{2T_s\left((I_1 + I_2) \cdot t_3 - (I_{\mathrm{ZVS}} + I_2) \cdot t_2\right)}. \tag{A2}$$

Based on (A1) and (A2), (15)–(19) can all be derived with different additional limitations. As for (15), the additional conditions for step-down case in Fig. 8(a) and step-up case in Fig. 8(c)

can be given as (A3) and (A4), respectively

$$\begin{cases} t_1 = t_2 = 0 \\ t_3 = T_s \\ I_{\text{ZVS}} = 0 \end{cases} \tag{A3}$$

$$\begin{cases} t_1 = 0 \\ t_3 = t_4 = T_s \\ I_{\text{ZVS}} = 0. \end{cases} \tag{A4}$$

Combining (A1)–(A4), the marginal power P_{mar} in (15) can be derived. And then, three basic control variables D_1, D_2, and φ can be expressed by t_1–t_4

$$\begin{cases} D_1 = t_3 - t_1 \\ D_2 = t_4 - t_2 \\ \varphi = t_2 - t_1. \end{cases} \tag{A5}$$

For the heavy load region "*A*" and "*C*" in Fig. 9, the current shape should be a quadrangle. Therefore, besides (A1) and (A2), the additional limitations can be given as follows:

$$\begin{cases} t_1 = 0 \\ t_4 = T_s \\ I_{\text{ZVS}} = 0. \end{cases} \tag{A6}$$

Combining (A1), (A2), (A5), and (A6), D_1, D_2 and φ in Region "*A*" and "*C*" can be derived in (16) and (17). As for the light load Region "*B,*" the additional limitations can be given as follows:

$$\begin{cases} t_1 = t_2 = 0 \\ I_{\text{ZVS}} = 0. \end{cases} \tag{A7}$$

Combining (A1), (A2), (A5), and (A7), (18) can be derived. Finally, as for the light load Region "*B,*" the additional limitations can be given as follows:

$$\begin{cases} t_1 = 0 \\ t_3 = t_4 \\ I_{\text{ZVS}} = 0. \end{cases} \tag{A8}$$

Combining (A1), (A2), (A5), and (A8), (19) can be derived. *Remark:* In order to explain the derivation of (15)–(19), this article is accompanied with a *Mathematica Notebook* file.

REFERENCES

[1] Y.-C. Liu, C. Chen, K.-D. Chen, Y.-L. Syu, and N. A. Dung, "High-frequency and high-efficiency isolated two-stage bidirectional DC–DC converter for residential energy storage systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 1994–2006, Sep. 2020.

[2] D. Dong et al., "A PV residential microinverter with grid-support function: Design, implementation, and field testing," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 469–481, Jan./Feb. 2018.

[3] M. Ngo, Y. Cao, D. Dong, R. Burgos, K. Nguyen, and A. Ismail, "Forced air-cooling thermal design methodology for high-density, high-frequency, and high-power planar transformers in 1U applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 2, pp. 2015–2028, Apr. 2023.

[4] Y. Cao, M. Ngo, N. Yan, D. Dong, R. Burgos, and A. Ismail, "Design and implementation of an 18-kW 500-kHz 98.8% efficiency high-density battery charger with partial power processing," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7963–7975, Dec. 2022.

[5] F. Jin, A. Nabih, Z. Li, and Q. Li, "A scalable matrix integrated transformer with controllable leakage inductance for a bi-directional resonant converter," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2023.3270400.

[6] Y. Cao, M. Ngo, D. Dong, and R. Burgos, "Bidirectional architectures with partial energy processing for DC/DC converters," U.S. Patent 20220069719A1, Mar. 29, 2022.

[7] Y. Cao et al., "Design and implementation of high-density isolated bi-directional soft-switching resonant DC-DC converter with partial power processing," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 640–646.

[8] M. Ngo, Y. Cao, D. Dong, and R. Burgos, "Design of 500 kHz, 18 kW low leakage inductance intraleaved litz wire transformer for bi-directional resonant DC-DC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 1153–1161.

[9] J. Liu, D. Dong, and D. Zhang, "A hybrid modular multilevel converter family with higher power density and efficiency," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9001–9014, Aug. 2021.

[10] Z. Li, E. Hsieh, Q. Li, and F. Lee, "High-frequency transformer design with medium-voltage insulation for resonant converter in solid-state transformer," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2023.3279030.

[11] J. Liu, S. Yue, W. Yao, W. Li, and Z. Lu, "DC voltage ripple optimization of a single-stage solid-state transformer based on the modular multilevel matrix converter," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12801–12815, Dec. 2020.

[12] Y. Cao, M. Ngo, N. Yan, Y. Bai, R. Burgos, and D. Dong, "DC distribution converter with partial power processing for LVDC/MVDC systems," in *Proc. IEEE 4th Int. Conf. DC Microgrids*, 2021, pp. 1–8.

[13] Y. Cao, M. Ngo, and D. Dong, "An isolated bi-directional series bridge DC transformer without resonant tank," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 374–381, doi: 10.1109/APEC43599.2022.9773422.

[14] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[15] Y. Cao, M. Ngo, R. Burgos, A. Ismail, and D. Dong, "Switching transition analysis and optimization for bidirectional CLLC resonant DC transformer," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 3786–3800, Apr. 2022.

[16] Y. Cao, M. Ngo, D. Dong, and R. Burgos, "A simplified time-domain gain model for CLLC resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 3079–3086.

[17] T. Guillod, D. Rothmund, and J. W. Kolar, "Active magnetizing current splitting ZVS modulation of a 7 kV/400 V DC transformer," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1293–1305, Feb. 2020.

[18] Y. Cao, M. Ngo, D. Dong, and R. Burgos, "The ZVS transition analysis and optimization for CLLC-type resonant DC transformer," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 3126–3133.

[19] B. Sahu and G. A. Rincon-Mora, "A low voltage, dynamic, noninverting, synchronous buck-boost converter for portable applications," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 443–452, Mar. 2004.

[20] M. Gaboriault and A. Notman, "A high efficiency, noninverting, buck-boost DC-DC converter," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2004, vol. 3, pp. 1411–1415.

[21] P. Rajarshi and D. Maksimovic, "Analysis of PWM nonlinearity in non-inverting buck-boost power converters," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 3741–3747.

[22] Y. Lee, A. Khaligh, and A. Emadi, "A compensation technique for smooth transitions in a noninverting buck–boost converter," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 1002–1015, Apr. 2009.

[23] P.-C. Huang, W.-Q. Wu, H.-H. Ho, and K.-H. Chen, "Hybrid buck–boost feedforward and reduced average inductor current techniques in fast line transient and high-efficiency buck–boost converter," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 719–730, Mar. 2010.

[24] Y. Lee, A. Khaligh, A. Chakraborty, and A. Emadi, "Digital combination of buck and boost converters to control a positive buck–boost converter and improve the output transients," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1267–1279, May 2009.

[25] Y. Bai, S. Hu, Z. Yang, Z. Zhu, and Y. Zhang, "Model predictive control for four-switch buck-boost converter based on tuning-free cost function with smooth mode transition," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 6607–6618, Dec. 2022.

[26] P. Vinciarelli, "Buck-boost DC-DC switching power conversion," U.S. Patent no. US006788033B2, Sep. 2004.

[27] S. Waffler and J. W. Kolar, "A novel low-loss modulation strategy for high-power bidirectional buck-boost converters," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1589–1599, Jun. 2009.

[28] Z. Zhou, H. Li, and X. Wu, "A constant frequency ZVS control system for the four-switch buck–boost DC–DC converter with reduced inductor current," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 5996–6003, Jul. 2019.
[29] K. Xia, Z. Li, Y. Qin, Y. Yuan, and Q. Yuan, "Minimising peak current in boundary conduction mode for the four-switch buck–boost DC/DC converter with soft switching," *Inst. Eng. Technol. Power Electron.*, vol. 12, no. 4, pp. 944–954, 2019.
[30] Q. Liu, Q. Qian, M. Zheng, S. Xu, W. Sun, and T. Wang, "An improved quadrangle control method for four-switch buck-boost converter with reduced loss and decoupling strategy," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10827–10841, Sep. 2021.
[31] Q. Liu, Q. Qian, B. Ren, S. Xu, W. Sun, and L. Yang, "A two-stage buck-boost integrated LLC converter with extended ZVS range and reduced conduction loss for high-frequency and high-efficiency applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 727–743, Feb. 2021.
[32] J. Fang, X. Ruan, X. Huang, R. Dong, X. Wu, and J. Lan, "A PWM plus phase-shift control for four-switch buck-boost converter to achieve ZVS in full input voltage and load range," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12698–12709, Dec. 2022.
[33] F. Liu, J. Xu, Z. Chen, R. Huang, and X. Chen, "A constant frequency ZVS modulation scheme for four-switch buck-boost converter with wide input and output voltage ranges and reduced inductor current," *IEEE Trans. Ind. Electron.*, vol. 70, no. 5, pp. 4931–4941, May 2023.
[34] L. Tian, X. Wu, C. Jiang, and J. Yang, "A simplified real-time digital control scheme for ZVS four-switch buck–boost with low inductor current," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 7920–7929, Aug. 2022.
[35] M. Shoyama, M. Ohba, and T. Ninomiya, "Balanced buck-boost switching converter to reduce common-mode conducted noise," in *Proc. IEEE 33rd Annu. IEEE Power Electron. Specialists Conf.*, 2002, vol. 4, pp. 2056–2061.
[36] X. Zhao et al., "Design of ultra-compact gate driver integrated with current sensor and commutation path for a 211-kW three-level SiC aircraft propulsion inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, to be published, doi: 10.1109/JESTPE.2023.3247378.
[37] V. Mitrovic et al., "Real-time network protocol for gate driver communication and control," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–6, doi: 10.1109/ECCE50734.2022.9947452.
[38] V. Mitrovic, B. Fan, Y. Cao, Y. Bai, R. Burgos, and D. Boroyevich, "Distributed communication and control architecture for an intelligent power stage," in *Proc. IEEE 23rd Workshop Control Model. Power Electron.*, 2022, pp. 1–8, doi: 10.1109/COMPEL53829.2022.9829952.
[39] Y. Cao et al., "A 75 kVA intelligent power stages (IPS) unit design for future grid-interface application," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–8, doi: 10.1109/ECCE50734.2022.9947815.
[40] Y. Cao et al., "3.5 kW/in3 planar coupled inductor design and optimization for a 50 kW 3-level four-switch buck-boost (3L-FSBB) converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–8, doi: 10.1109/ECCE50734.2022.9947382.
[41] Y. Cao, M. Ngo, N. Yan, D. Dong, and R. Burgos, "Core loss characterization and measurement," U.S. Patent 20220065950A1, Apr. 19, 2022.

Yuliang Cao (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2017, and the M.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2019. He is currently working toward the Ph.D. degree in electrical engineering with the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA.

His research interests include bidirectional resonant dc–dc converter, nonisolated dc–dc converter, ac–dc converter and magnetics design.

Dr. Cao was the recipient of two Best Presentation Awards at IEEE Applied Power Electronics Conference and Exposition (APEC) in 2021 and 2022 respectively, and the First Place Awards of the IEEE Energy Conversion Congress and Exposition (ECCE) Best Student Project Demonstration Competition in 2022, and the Best Technical Presentation Award at CPES Annual Conference in 2022.

Yijie Bai (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from Virginia Tech, Blacksburg, VA, USA, in 2020, and the M.S. degree in electrical engineering from the Center for Power Electronics Systems, Virginia Tech, in 2022.

His research interests include silicon carbide gate driver design, solid-state transformer, and dc–dc converter modeling and control.

Vladimir Mitrovic (Graduate Student Member, IEEE) received the B.S. degree in computer engineering from the School of Electrical and Computer Engineering of Applied Studies, Belgrade, Serbia, in 2015 and the M.S. degree in electrical engineering from the Center for Power Electronics Systems, Virginia Polytechnic and State University, Blacksburg, VA, USA, in 2022.

His research focus interests include real-time protocol for fast communication between nodes (gate drivers, sensors, and controllers) inside a power cell and communication between power cells in large systems (e.g., modular multilevel converters).

Boran Fan (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2013 and 2018, respectively.

In 2018, he joined the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, as a Postdoctoral Fellow and became a Research Scientist in 2021 and a Research Assistant Professor in 2023. His research interests include medium-voltage power conversion covering topology, auxiliary circuitry, insulation technique, advanced control and intelligent communication and control systems; aircraft powertrain converters covering multiphase drive, EMI mitigation, high-density electric drive train integration, thermal management, and high-altitude insulation technique.

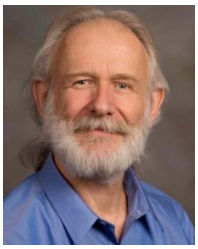
Dong Dong (Senior Member, IEEE) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2007, and the M.S. and Ph.D. degrees from Virginia Tech, Blacksburg, VA, USA, in 2009 and 2012, both in electrical engineering.

From 2012 to 2018, he was with GE Global Research Center (GRC), Niskayuna, NY, USA, as an Electrical Engineer. At GE, he participated in and led multiple technology programs including MV/HVDC power distribution and power delivery, SiC high-frequency high-power conversion systems, solid-state transformers, and energy storage system. Since 2018, he has been with the Bradley Department of Electrical and Computer Engineering, Virginia Tech. He has authored or coauthored more than 50 referred journal publications and more than 100 IEEE conference publications. He currently holds 35 granted US patents. His research interests include wide-band-gap power semiconductor-based high frequency power conversion, soft-switching and resonant converters, high-frequency transformers, and MV and HV power conversion system for grid, renewable, and transportation applications. Dr. Dong was the recipient of two Transaction Prize Paper Awards from the IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, William Portnoy Prize Paper Award and Transportation Systems Prize Paper Award from IEEE IAS, and NSF CAREER award, also multiple technology awards including GE silver and gold medallion patent awards and GE technology transition awards. He is currently an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS. He served as the Vice Chair of IEEE Industry Application Society Schenectady Region Chapter in 2017 and the General Chair of IEEE International Conference on DC Microgrids in 2021.

Rolando Burgos (Senior Member, IEEE) received the B.S. degree in electronics engineering, the Electronics Engineering Professional degree, and the M.S. and Ph.D. degrees in electrical engineering from the University of Concepción, Concepción, Chile, in 1995, 1997, 1999, and 2002 respectively.

In 2002, he joined, as a Postdoctoral Fellow, the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, becoming Research Scientist in 2003, and Research Assistant Professor in 2005. In 2009, he joined ABB Corporate Research, Raleigh, NC, USA, where he was a Scientist (2009–2010), and a Principal Scientist (2010–2012). In 2010, he was appointed an Adjunct Associate Professor in the Electrical and Computer Engineering Department, North Carolina State University at the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center. In 2012, he returned to Virginia Tech as an Associate Professor in The Bradley Department of Electrical and Computer Engineering, where he earned his tenure in 2017 and was promoted to Professor in 2019. Since 2021 he has been the Director of CPES. His research interests include high power density wide-bandgap semiconductor-based power conversion—low voltage and medium voltage applications, packaging and integration, electromagnetic interference and electromagnetic compatibility, multiphase multilevel power converters, modeling and control, grid power electronics systems, and the stability of ac and dc power systems.

Dr. Burgos is a Member of the IEEE Power Electronics Society where he currently serves as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is the past Chair of the Technical Committee on Power and Control Core Technologies. He is also a member of the IEEE Industry Applications Society, the IEEE Industrial Electronics Society, and the IEEE Power and Energy Society.



Dushan Boroyevich (Life Fellow, IEEE) received the Ph.D. degree in electrical engineering from Virginia Tech, Blacksburg, VA, USA, in 1986.

From 1986 to 1990, he was an Assistant Professor and Director of the Power and Industrial Electronics Research Program with the Institute for Power and Electronic Engineering, University of Novi Sad. He then joined the Bradley Department of Electrical and Computer Engineering, Virginia Tech, as an Associate Professor. He is currently a university distinguished Professor at the department and Deputy Director with the Center for Power Electronics Systems. He was the President of the IEEE Power Electronics Society for 2011–2012. His research interests include electronic power distribution systems, multiphase power conversion, power electronics systems modeling and control, and integrated design of power converters.

Dr. Boroyevich was the recipient of four honorary professorships in China and Taiwan, as well as numerous other awards, including the IEEE William E. Newell Power Electronics Technical Field Award and the European Power Electronics Association Outstanding Achievement Award. He is a member of the US National Academy of Engineering.

Radha Sree Krishna Moorthy (Member, IEEE) received the B.E. degree in electrical and electronics engineering from Anna University, Chennai, India in 2012. She received the Ph.D. degree in electrical and computer engineering from National University of Singapore (NUS), Singapore in 2016. She is an R&D Associate Staff Member with Oak Ridge National Laboratory (ORNL), Knoxville, TN, USA. Her research at ORNL focuses predominantly on Solid State Power Substations for the grid of the future and their fundamental building blocks—Smart Universal Power Electronics Regulators and Intelligent Power Stages. She is actively involved in the validation of grid/system architectures in hardware in loop platforms and in hardware. Prior to ORNL, she held a postdoctoral appointment with North Carolina State University, Raleigh, NC, USA. At NC state, she focused on SiC based high power inverters for vehicular applications. Her work has been published in major journals including IEEE TRANSACTIONS IN INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, and *Journal of Emerging and Selected Topics in Power Electronics*. Her research interests include grid modernization and futuristic grid architectures, futuristic charging solutions and grid architecture validation in real-time systems.

Madhu Chinthavali (Senior Member, IEEE) received the M.S. and Ph.D. degrees in electrical engineering from the University of Tennessee, Knoxville, TN, USA, in 2003 and 2015, respectively.

He is currently a Section Head for Electric Energy Systems Integration and Controls and also the Director of Grid Research Integration and Deployment Center GRID-C, Oak Ridge National Laboratory, Oak Ridge, TN, USA. His research interests include developing power electronics systems with advanced semiconductor devices and developing device and system level models.