A Simple and Fast Start-Up Strategy for Dual-Active-Bridge Converters With DC Bias Suppression

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***Abstract*—High-power dual-active-bridge (DAB) converters are widely adopted in dc and hybrid ac–dc microgrids, for which *fast start-up dynamics* of DAB converters is a key requirement. Conventional start-up methods usually require complex operation stages, and a time-consuming parameter-tuning process, resulting in slow dynamics. In this work, we propose a new simple and optimal start-up method for DAB converters. Major contributions lie in three-folds. First, we theoretically analyze the transmission power and the peak inductor current of extended phase-shift modulation. Second, a new Lagrange multiplier method is proposed to solve the optimal phase-shift ratios of the underlying control problem, resulting in very fast control dynamics at maximum power transmission, fully respecting the system permissible current limit. Third, an effective and simple strategy by *solely* manipulating the gate signals in the first switching period is newly proposed to eliminate the magnetic bias. The proposed method avoids complex parameter-tuning procedures. Experimental results demonstrate the effectiveness of the proposed method. Results confirm that with the proposed solution a *much faster* start-up process with a controllable inductor current *without* dc bias is achieved, in comparison with the recently reported start-up methods.**

***Index Terms*—Dual-active-bridge (DAB) converter, extended phase-shift (EPS) modulation, magnetic bias elimination, start-up dynamics.**

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I. Introduction

OVER the past decades, dual-active-bridge (DAB) converters have become a popular dc–dc typology thanks to their high power density, electrical isolation, and inherently zero-voltage switching [1]. High-power DAB converters are widely applied to dc and hybrid ac–dc microgrids or distribution networks, power electronic transformers, and electrical vehicles. For most of the aforementioned applications, a fast and effective start-up procedure, especially to realize "zero-volt" DAB start-up is particularly significant.

The secondary H-bridge of the DAB converter usually works as an active rectifier, for which the rectification current contains a large spectrum of ripples, leading to the necessity of an indispensable filter capacitor located at the output port. At the initial phase of the start-up procedure, the output dc capacitor is fully discharged, which acts as a virtual short circuit. When the primary switching device is switched ON, the inductor current increases rapidly, and the maximum value of which will not be decided and reflected by the phase-shift ratios, but by the input voltage, the switching period, and the series inductor. If control strategies for steady state, e.g., single-phase shift (SPS) modulation, do not distinguish this special phase to take proper control actions, magnetic saturation and overcurrent of switching devices will inevitably occur, which will damage the underlying converters [2].

Targeting to solve the abovementioned problems, techniques via additional hardware circuits are first introduced, see, e.g., [3], [4]. However, the system becomes more complex, expensive, and less reliable. As another direction, a series of soft start-up methods are proposed, e.g., the authors in [5] and [6] proposed extended phase-shift (EPS) modulation technique, which decreases the pulse width of the primary H-bridge and suppresses the inrush current of the inductor. The authors in [2] employed dual-phase-shift (DPS) modulation to suppress the inrush current. In [7], the authors increase the switching frequency, which is equivalent to decreasing the pulse width. However, higher switching frequency leads to higher undesirable switching loss.

Besides, numerous multistep start-up methods are proposed, e.g., in [7], [8], and [9], the authors divided the start-up procedure into two phases. The first one is an *open-loop* phase, where the secondary H-bridge works as a diode rectifier and the inner

phase-shift ratio is increased gradually without feedback. When the output voltage reaches the maximum rectification voltage, the system enters into the second phase, in which the secondary H-bridge starts switching and *closed-loop* control methods are applied to ensure that the output voltage is regulated to the reference value. Since the first phase applies open-loop control, a time-consuming parameter tuning process is inevitably required to assure under all working conditions the current limit will not be violated. In [10], the authors presented a *three-step* start-up method, while in [11], a *five-step* start-up method was presented. These methods fully utilize the current carrying capacity and shorten the start-up time, and are essentially open-loop-based techniques. Besides, sequential multiple start-up steps will complicate the tuning process. Very careful and tedious tuning process are inevitable to guarantee the system dynamic performance and to restrain the inductor current within a safe limit.

Differently, in [7], [12], [13], [14], and [15], the input voltage of DAB converters is controlled by an active front-end converter, and the DAB starts up while the input voltage gradually increases to the normal value. These methods effectively limit the current stress but are not suitable for all conditions due to that the input voltage range is limited and its changing dynamics will slow down the whole start-up process.

Several closed-loop start-up methods are proposed (see [15], [16], [17], [18], [19], etc.). In [16], the authors propose a boundary control scheme for DAB converters to speed up the start-up procedure. However, the control law was drawn based on the analysis of the output side filter capacitor, which is assumed to have very small capacitance, and complex geometrical and numerical computation is unavoidable, which increases the burden of the processor. In [15], the authors proposed a novel model predictive control (MPC) with current-stress-optimized scheme based on DPS modulation for DAB-based power electronic traction transformer. MPC is widely adopted in the control of power converters, and demonstrates superior control performance [20], [21], [22], [23], [24]. However, the input voltage of DAB converters gradually increases from zero to the rated value, which limits the applications of that method. In [17], the authors proposed a long-dead-time control to reduce the inrush current without introducing additional pulsewidth modulation channel requirements. Nevertheless, the maximum transmission power *solely for the first switching period* is achieved, respecting its current stress limit. However, for the rest of the start-up procedure, maximum power transmission and start-up speed cannot be guaranteed. In [18], [19], a novel closed-loop start-up method applying the combination of the EPS and triple phase-shift (TPS) modulation schemes is presented to speed up the start-up process respecting the maximum permissible current. Additionally, this method employs EPS with the trapezoidal current modulation and TPS with the trapezoidal-current modulation, which associate phase-shift ratios and reduce the complexity of calculation. Hence, the control freedom is limited and the optimal transmission power cannot be achieved.

Inspired by the above, in this work, we propose a new simple start-up scheme based on EPS modulation, which accelerates the start-up process (by more than 40% in terms of the start-up time) with very few efforts. Furthermore, the proposed method overcomes the dc bias in the initial period, without any complex parameter-tuning processes. Major contributions of this paper include the following three points.

1) The current stress and transmission power of DAB converters under each mode of EPS modulation and discontinuous current mode (DCM), continuous current mode (CCM) mode are derived (see Section II).
2) The Lagrange multiplier method and Karush–Kuhn–Tucker (KKT) conditions are employed to obtain the optimal phase-shift ratio, forming a new solution able to maximize the transmission power within the permissible current stress constraint (see Section IV-A).
3) A simple solution to eliminate the dc current bias in the first switching period is proposed (see Section IV-B).

The rest of this article is organized as follows. The EPS modulation, transmission power, and peak inductor current are introduced in Section II. In Section III, the properties and drawbacks of the conventional closed-loop start-up scheme are stated. In Section IV, the details of the proposed start-up strategy are elaborated. In Section V, the experimental results and analyzes are provided. Finally, Section VI concludes this article.

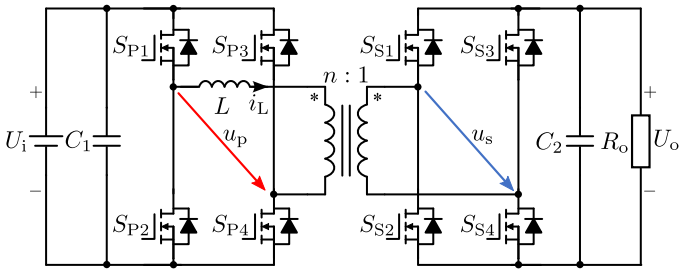

Fig. 1. DAB converter.

II. System Description and Modeling

In this section, the system modeling, modulation, peak inductor current, and transmission power of the underlying DAB power converters are stated.

As shown in Fig. 1, the DAB dc–dc converter mainly consists of two H-bridges connected on both sides of a high-frequency transformer with a turn ratio n, which provides galvanic isolation. A dc voltage source and a capacitor are connected to the dc side of the H-bridge at the input side, which is called the primary (P) bridge. Similarly, at the output side, a capacitor, and a dc load are connected to the dc side of the H-bridge, which is called the secondary (S) bridge. S_{PX} and S_{SY} ($\mathrm{X}, \mathrm{Y} \in [1, 2, 3, 4]$) are the switching devices at the P and S bridge, while G_{PX} and G_{SY} are the driving signals of S_{PX} and S_{SY}. The inductor L composes of the transformer leakage and the series inductor.

A. Extend Phase-Shift Modulation

EPS modulation with two degrees of freedom is widely adopted in DAB converters due to, e.g., enhanced regulating flexibility, reduced current stress, and improved system efficiency. In each bridge arm of DAB, the upper and lower switches conduct alternately and the duty cycle of each driving signal is 50%. In

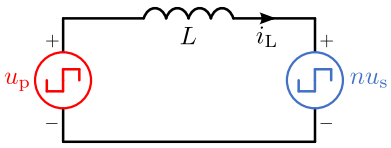

Fig. 2. AC side equivalent circuit of the DAB converter.

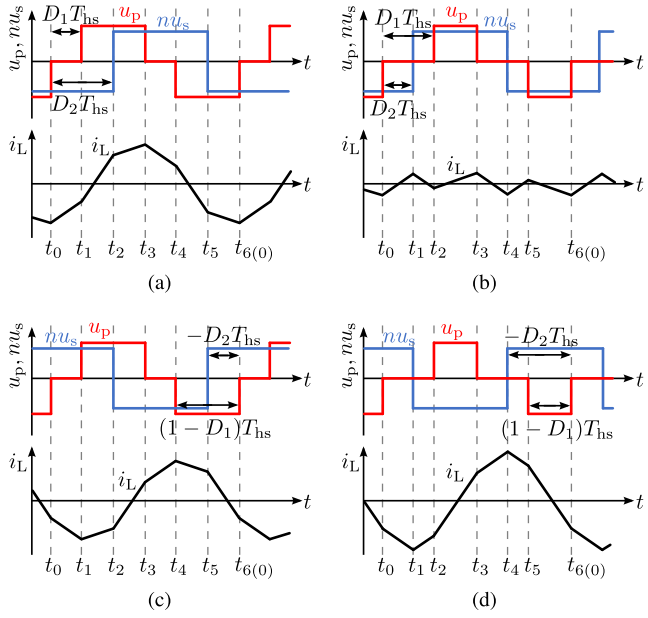

Fig. 3. AC side voltage and inductor current of DAB converters under EPS modulation. (a) Mode I, $0 \le D_1 \le D_2 \le 1$. (b) Mode II. $0 \le D_2 \le D_1 \le 1$. (c) Mode III, $-1 \le D_1 - 1 \le D_2 \le 0$. (d) Mode IV, $-1 \le D_2 \le D_1 - 1 \le 0$.

EPS modulation, G_{S3} lags behind G_{S1} by $180°$ ($T_s/2$), where T_s is the switching period. As shown in Fig. 3(a), the phase-shift ratio between G_{P1} and G_{S1} is the outer phase-shift ratio D_2, while the phase-shift ratio between G_{P1} and G_{P3} is the inner phase-shift ratio D_1.

To analyze the inductor current, assuming that the input voltage and the output voltage are constant in one period, the circuit could be simplified as two voltage sources and an inductor connected in series, as shown in Fig. 2.

The inductor current is associated with the output voltage of the two H-bridges, as

$$L\frac{\mathrm{d}i_\mathrm{L}}{\mathrm{d}t} = u_\mathrm{p} - nu_\mathrm{s} \tag{1}$$

where i_L is the inductor current, u_p and u_s are the ac-side voltage of the primary and secondary H-bridges, respectively.

According to the magnitudes of D_1 and D_2, EPS modulation can be divided into four modes, i.e., $0 \le D_1 \le D_2 \le 1$, $0 \le D_2 \le D_1 \le 1$, $-1 \le D_1 - 1 \le D_2 \le 0$, $-1 \le D_2 \le D_1 - 1 \le 0$, as shown in Fig. 3.

Besides, when the secondary H-bridge stays passive, as shown in Fig. 4, based on whether the inductor current i_L returns to and remains at zero, the waveform can be divided into two modes, DCM and CCM.

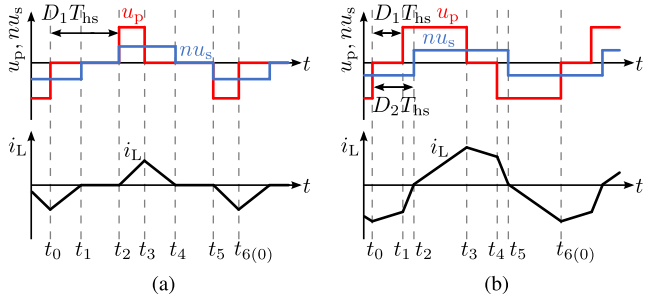

Fig. 4. AC side voltage and inductor current waveforms of DAB converters with uncontrolled secondary H-bridge. (a) DCM mode. (b) CCM mode.

B. Peak Inductor Current and Transmission Power

Taking the case of $0 \le D_1 \le D_2 \le 1$ as an example, according to (1), and the symmetry of the inductor current, $i_\mathrm{L}(t_0) = -i_\mathrm{L}(t_3), i_\mathrm{L}(t_1) = -i_\mathrm{L}(t_4), i_\mathrm{L}(t_2) = -i_\mathrm{L}(t_5)$, the inductor current values at the switching moment are

$$\begin{cases} i_\mathrm{L}(t_0) = -i_\mathrm{L}(t_3) = I_\mathrm{N}\left[k(D_1-1)+1-2D_2\right] \\ i_\mathrm{L}(t_1) = -i_\mathrm{L}(t_4) = I_\mathrm{N}\left[k(D_1-1)+1+2D_1-2D_2\right] \\ i_\mathrm{L}(t_2) = -i_\mathrm{L}(t_5) = I_\mathrm{N}\left[k(2D_2-D_1-1)+1\right] \end{cases} \tag{2}$$

where I_N and k are defined as follows:

$$I_\mathrm{N} = \frac{nU_\mathrm{o}T_\mathrm{s}}{4L} \tag{3}$$

and $k = U_\mathrm{i}/nU_\mathrm{o}$. The peak inductor current is

$$i_{\mathrm{L,max}} = \begin{cases} i_\mathrm{L}(t_3), & k > 1 \\ i_\mathrm{L}(t_2), & 0 < k \le 1. \end{cases} \tag{4}$$

The transmission power is

$$\begin{aligned} P &= \frac{2}{T_\mathrm{s}}\int_{t_0}^{t_3} u_\mathrm{p}(t) i_\mathrm{L}(t)\,\mathrm{d}t \\ &= \frac{nU_\mathrm{i}U_\mathrm{o}T_\mathrm{s}}{8L} 2\left(-D_1^2 + 2D_1D_2 - D_1 - 2D_2^2 + 2D_2\right) \\ &= P_\mathrm{N}P_1' \end{aligned} \tag{5}$$

where P_N and P_1' are defined as follows:

$$P_\mathrm{N} = \frac{nU_\mathrm{i}U_\mathrm{o}T_\mathrm{s}}{8L} \tag{6}$$

$$P_1' = 2(-D_1^2 + 2D_1D_2 - D_1 - 2D_2^2 + 2D_2). \tag{7}$$

Similarly, the peak current and transmission power of modes II, III, IV, and DCM, CCM can be derived, which are collected by Table I. The relationship of unified transmission power with D_1 and D_2 is shown in Fig. 5.

III. Problems Statement and Conventional Solutions

This section aims to illustrate the issues to be solved during the start-up procedure of DAB converters, e.g., inrush current, dc current bias, long start-up time, and complex parameter tuning process.

TABLE I
EXPRESSIONS OF THE UNIFIED TRANSMISSION POWER AND PEAK INDUCTOR CURRENT

Mode	Unified transmission power	Submode	Power flow direction	Inductor current stress
DCM	$P'_{\mathrm{DCM}}=2(k-1)(1-D_1)^2$	DCM	Forward	$2I_{\mathrm{N}}(1-D_1)(k-1)$
CCM	$P'_{\mathrm{CCM}}=-D_1^2-\frac{1}{k^2}+1$	CCM	Forward	$I_{\mathrm{N}}\frac{k(1-D_1)+1}{k}(k-1)$
I ($0\le D_1\le D_2\le 1$)	$P'_1=2(-D_1^2+2D_1D_2-D_1-2D_2^2+2D_2)$	IA ($k>1$)	Forward	$I_{\mathrm{N}}\left[k(1-D_1)+2D_2-1\right]$
		IB ($0\le k\le 1$)		$I_{\mathrm{N}}\left[k(2D_2-D_1-1)+1\right]$
II ($0\le D_2\le D_1\le 1$)	$P'_2=2(D_1^2-2D_1D_2-D_1+2D_2)$	IIA ($k\le\frac{1-D_2}{1-D_1}$)	Uncertain	$I_{\mathrm{N}}\left[k(D_1-1)+1\right]$
		IIB ($k>\frac{1-D_2}{1-D_1}, D_1\le 2D_2$)	Forward	$I_{\mathrm{N}}\left[k(1-D_1)+2D_2-1\right]$
		IIC ($k>\frac{1-D_2}{1-D_1}, D_1>2D_2$)	Backward	$I_{\mathrm{N}}\left[k(1-D_1)+2D_1-2D_2-1\right]$
III ($-1\le D_1-1\le D_2\le 0$)	$P'_3=2(D_1^2-2D_1D_2-D_1+2D_2^2+2D_2)$	IIIA ($k\ge 1$)	Backward	$I_{\mathrm{N}}\left[k(1-D_1)+2D_1-2D_2-1\right]$
		IIIB ($0<k<1$)		$I_{\mathrm{N}}\left[k(D_1-2D_2+1)+1\right]$
IV ($-1\le D_2\le D_1-1\le 0$)	$P'_4=2(-D_1^2+2D_1D_2+3D_1-2D_2-2)$	IVA ($-D_1+2D_2\le 1$)	Forward	$I_{\mathrm{N}}\left[k(1-D_1)U_{\mathrm{i}}+1\right]$
		IVB ($-D_1+2D_2>1$)	Backward	

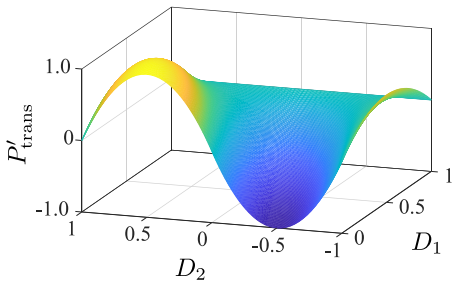

Fig. 5. Relationship of unified transmission power P'_{trans} with D_1 and D_2.

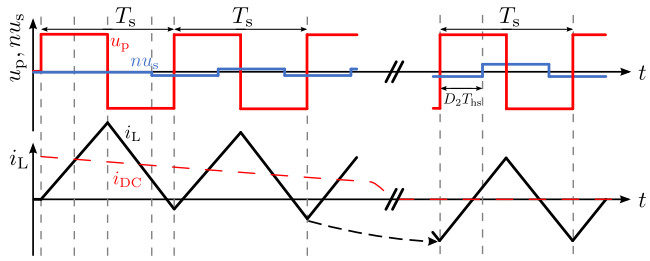

Fig. 7. Start-up DC bias and inrush current under SPS modulation in DAB converter.

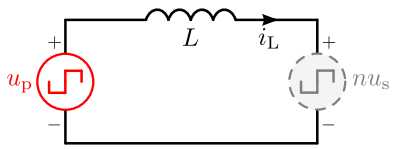

Fig. 6. AC side equivalent circuit of the DAB converter during start-up.

A. Inrush Current and DC Current Bias

DAB converters are commonly used in dc microgrids and electrical vehicles. In these applications, there is no power source on the output side, and before the start-up procedure, the output voltage is zero. Consequently, the output voltage of the secondary H-bridge is zero, and the equivalent circuit is illustrated as Fig. 6.

Under this condition, if SPS modulation is still applied, the inductor current will exceed the maximum allowed value. Easy to find, SPS modulation is a special case of EPS modulation, where the inner phase-shift value D_1 is zero. Therefore, from Table I, the current stress of DAB converters under SPS modulation is divided as

$$I_{\mathrm{L,max,SPS}}=\begin{cases}\frac{T_{\mathrm{s}}}{4L}[U_{\mathrm{i}}+nU_{\mathrm{o}}(2D_2-1)], & U_{\mathrm{i}}>nU_{\mathrm{o}}\\ \frac{T_{\mathrm{s}}}{4L}[U_{\mathrm{i}}(2D_2-1)+nU_{\mathrm{o}}], & U_{\mathrm{i}}\le nU_{\mathrm{o}}.\end{cases}\tag{8}$$

Therefore, SPS modulation is unable to reduce the current stress when $U_{\mathrm{i}}\gg nU_{\mathrm{o}}$ or $U_{\mathrm{i}}\ll nU_{\mathrm{o}}$. Particularly, in the first several switching periods of the start-up procedure, $U_{\mathrm{o}}\approx 0$, the current stress is only relevant with U_{o}, L, and T_{s}. Besides, the inductor current remains at zero before the start-up procedure. Therefore, the current stress in the first switching period is $\frac{T_{\mathrm{s}}}{2L}U_{\mathrm{i}}$, as shown in Fig. 7.

Nevertheless, from the perspective of system efficiency and dynamic performance, the phase-shift ratio of SPS modulation is generally less than 0.2. The efficiency of DAB converters reaches the peak when the unified power is in the range of 0.1–0.6, and the efficiency decreases when the unified power is greater than 0.6 [25]. Correspondingly, the converter efficiency reaches the peak when the phase-shift ratio D_2 is in the range of 0.04–0.2, while the maximum current stress is about $0.4\frac{T_{\mathrm{s}}}{4L}U_{\mathrm{i}}$. In this condition, the current stress during the start-up procedure is about 2.5 times the current stress in the steady state. Besides, when considering the inductor saturation, the overcurrent will be much more serious, which would trigger the protection of driver integrated circuits (ICs), with the converter shutting down.

B. Start-Up Time and Parameter Tuning

As illustrated in Fig. 8, conventional start-up methods, e.g., [7], [8], [9], [10], [11], usually divide the start-up procedure into several phases. In those phases except the last one, the

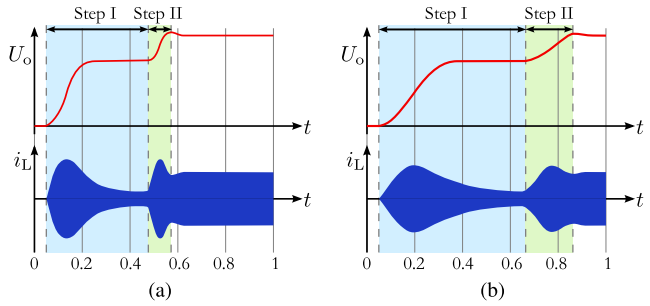

Fig. 8. Waveforms of conventional soft start-up method in [8]. (a) Fast start-up. (b) Slow start-up.

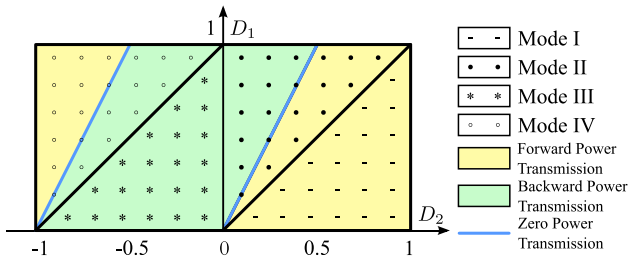

Fig. 9. Power direction, modes with D_1 and D_2.

control parameters change in an open loop behavior, e.g., the phase-shift ratio, and the switching frequency. The following analyzes introduce a two-stage start-up method proposed in [8].

The first phase is an open-loop start phase. In this phase, only the gate signals of the primary H-bridge are activated, while the secondary H-bridge works as a diode rectifier. The inner phase-shift ratio D_1 decreases gradually from 1 to 0 linearly with a slope $\frac{\mathrm{d}D_1}{\mathrm{d}t}$, and the pulse width on the ac side of the primary side widens, with the output voltage increasing. When the output voltage U_o reaches the maximum rectification voltage, the system enters the second phase, where the gate signals of the secondary H-bridge are enabled and closed-loop control methods are applied. In this phase, the reference of the output voltage U_o^* gradually increases to the desired output voltage with a slope $\frac{\mathrm{d}U_\mathrm{o}^*}{\mathrm{d}t}$. Fig. 8(a) illustrates a fast start-up procedure with greater current stress and larger $\frac{\mathrm{d}D_1}{\mathrm{d}t}$ and $\frac{\mathrm{d}U_\mathrm{o}^*}{\mathrm{d}t}$, while Fig. 8(b) illustrates a slow start-up procedure with less stress and smaller parameters.

However, the inductor current stress of this method could not be precisely regulated, for the reason that the method is an open-loop control method for the inductor. The maximum inductor current stress is not only indirectly regulated by the key parameters, $\frac{\mathrm{d}D_1}{\mathrm{d}t}$ and $\frac{\mathrm{d}U_\mathrm{o}^*}{\mathrm{d}t}$, but also influenced by the load condition and the input voltage. Nevertheless, the load condition and the input voltage are usually untraceable, leading to a complex and compromised parameter tuning process. Additionally, these parameters shall be carefully designed and tuned for the full load conditions. Particularly, at light load cases, the inductor current is less than the maximum allowed value, which increases the time consumed in the start-up phase. In addition, the mathematical relationship between the peak inductor current and the parameters ($\frac{\mathrm{d}D_1}{\mathrm{d}t}$ and $\frac{\mathrm{d}U_\mathrm{o}^*}{\mathrm{d}t}$) cannot be divided accurately and theoretically, resulting in that parameters can solely be tuned via tedious simulations or experimental trials.

During most time of the start-up procedure, the inductor current is less than the maximum allowed current, which means the procedure does not adequately utilize the current carrying capacity and the start-up time is, therefore, extended. To further accelerate the start-up procedure, methods with more steps are proposed, to enlarge the inductor current, see, e.g., [7], [8], [9], [10], [11]. However, more steps lead to more complex parameter tuning. Without feedback in the first few stages, resulting in poor knowledge for short-circuit protection capabilities, hence, poor reliability.

IV. Proposed Solution

In this section, we develop a new and simple start-up control solution to achieve very fast dynamic performance, respecting current stress limit and without complex parameter-tuning process. The proposed solution can be divided into two parts, i.e., a) maximum transmission power tracking design, and b) dc bias suppression technique.

A. Maximum Transmission Power Tracking Design

Based on the aforementioned analyzes in Section II, the control target to shorten the start-up time with inductor current constraints is equivalent to an optimization problem of finding a combination of optimized phase-shift ratio (D_1^opt, D_2^opt) to maximize the transmission power respecting inductor current limit. Hence, the optimization target is to maximize the transmission power, and the constraints are the given inductor current stress and the boundary of the operating mode, i.e.,

$$\begin{aligned} &\max \quad P_\mathrm{EPS}(D_1, D_2) \\ &\text{s.t.} \quad \begin{cases} i_{\mathrm{L}\max}(D_1, D_2) \le I_\mathrm{set} \\ B_i(D_1, D_2) \le 0, i = 1, \ldots, q \end{cases} \end{aligned} \tag{9}$$

where P_EPS is the transmission power under EPS modulation, I_set is the given current stress constraint value, $B_i(D_1, D_2)$ is the boundary condition of the operating mode, and q is the number of constraints.

During the start-up process, only modes with positive transmission power are considered. Based on Table I and Fig. 5, the transmission power is positive when $0 \le D_1 \le 2D_2$ or $-D_1 + 2D_2 \le -2$, as shown in Fig. 9, and in DCM, CCM. However, in DCM, i_L will have chances to remain zero. The transmission power is, therefore, limited. CCM is an exceptional case of mode I. Modes I, II, IV of EPS modulation can be analyzed based on our former development. In the following, we take mode I as an example to solve the optimal phase-shift ratio D_1^opt, D_2^opt.

Based on the current stress (4) and transmission power (5), the optimal problem described by (9) can be solved by the Lagrange multiplier method and KKT conditions. The problem described by (9) can be reshaped as (10)

$$\begin{aligned} &\min \quad -P_\mathrm{EPS}(D_1, D_2) \\ &\text{s.t.} \quad \begin{cases} i_{\mathrm{L}\max}(D_1, D_2) \le I_\mathrm{set} \\ B_i(D_1, D_2) \le 0, i = 1, \ldots, q. \end{cases} \end{aligned} \tag{10}$$

TABLE II
LOCAL OPTIMAL SOLUTION IN EACH MODE OF EPS MODULATION

(Sub)Mode	Local optimal solution
IA	$D_1^{\rm opt}=\left(\frac{I_{\rm set}}{I_{\rm N}}-k\right)\frac{1-k}{k^2-2k+2}$, $D_2^{\rm opt}=\left(\frac{I_{\rm set}}{I_{\rm N}}-k\right)\frac{2-k}{2(k^2-2k+2)}+\frac{1}{2}$
IB	$D_1^{\rm opt}=0$, $D_2^{\rm opt}=\left(\frac{I_{\rm set}}{I_{\rm N}}-1\right)\frac{1}{2k}+\frac{1}{2}$
IIA	No optimized solution inside
IIB	$D_1^{\rm opt}=\frac{I_{\rm set}}{2I_{\rm N}(1-k)}+1$, $D_2^{\rm opt}=\frac{(2-k)I_{\rm set}}{4I_{\rm N}(1-k)}$
IIC	Backward power transmission
III	Backward power transmission
IV	No optimized solution inside

The KKT conditions for the optimization program (10) are as follows:

$$\begin{cases}\mathcal{L}(D_1,D_2,\boldsymbol{\mu})=-P_{\rm EPS}(D_1,D_2)+\sum_{i=1}^{q}\mu_i B_i(D_1,D_2)\\ \left.\frac{\partial\mathcal{L}}{\partial D_1}\right|_{D_1=D_1^{\rm opt}}=0,\quad \left.\frac{\partial\mathcal{L}}{\partial D_2}\right|_{D_2=D_2^{\rm opt}}=0,\quad \mu_i\geq 0\\ B_i(D_1,D_2)\leq 0,\quad \mu_i B_i(D_1,D_2)=0, i=1,\ldots,q\end{cases}\tag{11}$$

where $\mathcal{L}$ is the Lagrange Multiplier, μ_i is the KKT multiplier, and $\boldsymbol{\mu}=[\mu_1,\mu_2,\ldots,\mu_q]$.

Taking mode IA as an example, the KKT constraints can be established as (12), shown at the bottom of the this page. solving which yielding

$$\begin{cases}D_1^{\rm opt}=\left(\frac{I_{\rm set}}{I_N}-k\right)\frac{1-k}{k^2-2k+2}\\ D_2^{\rm opt}=\left(\frac{I_{\rm set}}{I_N}-k\right)\frac{2-k}{2(k^2-2k+2)}+\frac{1}{2}.\end{cases}\tag{13}$$

However, the optimal solution obtained by (13) will sometimes outside the boundary of IA ($0\leq D_1\leq D_2\leq 1$), which means that the optimal solution cannot be reached in $0\leq D_1\leq D_2\leq 1$. Consequently, further optimization in other modes of EPS modulation is required.

Similarly, the local optimal phase-shift ratio combination can be obtained in other modes. Table II shows the local optimal solutions in all mode. By comparing the local optimal solutions, the global optimal solution is obtained.

In short, the steps to obtain $D_1^{\rm opt}$ and $D_2^{\rm opt}$ can be summarized into the offline and online procedures, as follows.

1) The *offline* procedure. Based on Table I, employ the Lagrange multiplier method to obtain the local optimal solution for each mode, with maximizing the transmission power as the optimization objective, the current stress limitation and operation boundary of each mode as the constraints. The analytical optimal solutions for this part are collected in Table II. Then is the online procedure.
2) The *online* procedure.

a) In each control period, sample input voltage $U_{\rm i}$ and output voltage $U_{\rm o}$.
b) Then, based on Table II, calculate local optimal solutions for each mode.
c) Based on Table I, calculate the transmission power corresponding to each set of optimal solutions.
d) Thereafter, compare the transmission power and choose the local optimal solution with the highest power as the global optimal solution ($D_1^{\rm opt}$, $D_2^{\rm opt}$).

B. DC Bias Suppression

The method proposed in Section IV-A tries to assure that the output voltage will increase to the steady-state value, while the inductor current will respect the current limitation. Nevertheless, the analysis of the inductor current is based on the hypothesis that the system runs in steady-state operation point. This means that the inductor current $i_{\rm L}(t_0)$ equals to its opposite number of the inductor current, $i_{\rm L}(t_3)$. However, in practice, the current at the first switching period, i.e., $i_{\rm L}(t_0)=0$. Therefore, following the instruction in Fig. 3(a), the maximum current of the first period can be put as

$$i'_{\rm L,max}=i'_{\rm L}(t_3)=\frac{T_{\rm s}}{2L}\left[(1-D_1)U_{\rm i}+(2D_2-1)nU_{\rm o}\right]=2I_{\rm set}.\tag{14}$$

This excessive current $i'_{\rm L,max}$ will lead to a system fault, e.g., magnetic saturation of the transformer and the inductor, overcurrent of switching devices. In most severe cases, during magnetic saturation, this maximum value will be up to 7–8 times larger than its normal one, which is destructive to the switching device.

To limit the inrush current in the first switching period, authors in [26] proposed a dynamic reference generation method. Nonetheless, the method decreases the current limit at the first several periods, which slows the start-up speed.

In this article, we limit the current inrush in the first period by decreasing the first pulse width of the primary bridge. A simple way to realize this is via shortening the first pulse $\overline{G_{\rm P3}}/G_{\rm P4}$.

$$\begin{cases}\mathcal{L}=-\frac{nU_{\rm i}U_{\rm o}T_{\rm s}}{4L}(-D_1^2+2D_1D_2-D_1-2D_2^2+2D_2)+\mu_1(-D_1)+\mu_2(D_1-D_2)+\mu_3(D_2-1)\\ \quad+\mu_4(1-k)+\mu_5\left\{I_N[k(-D_1+1)+2D_2-1]-I_{\rm set}\right\},\\ \frac{\partial\mathcal{L}}{\partial D_1}=0,\quad \frac{\partial\mathcal{L}}{\partial D_2}=0,\quad -D_1\leq 0,\quad D_1-D_2\leq 0,\quad D_2-1\leq 0,\quad 1-k\leq 0,\quad I_N[k(-D_1+1)+2D_2-1]-I_{\rm set}\leq 0\\ \mu_1(-D_1)=0,\mu_2(D_1-D_2)=0,\mu_3(D_2-1)=0,\mu_4(1-k)=0,\\ \quad\mu_5\left\{I_N[k(-D_1+1)+2D_2-1]-I_{\rm set}\right\}=0,\mu_i\geq 0,i=1,\ldots 5.\end{cases}\tag{12}$$

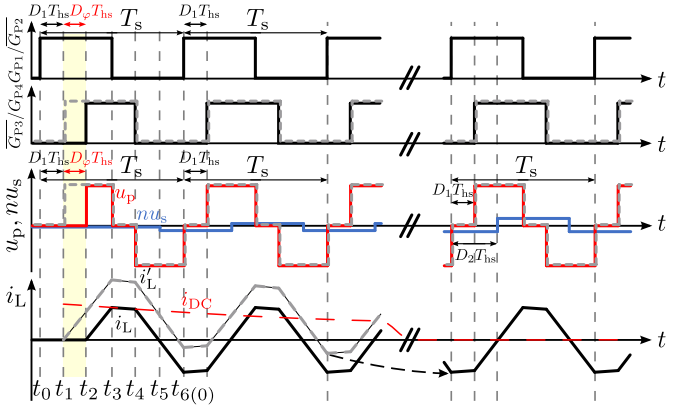

Fig. 10. Theoretical waveform of DC bias suppression. Solid line: DC bias suppression is applied. Dashed line: DC bias suppression is not applied.

TABLE III
KEY PARAMETERS OF THE TEST BENCH

Parameters	Value
Input dc Voltage	80 V
Output dc voltage reference	160 V
Total leakage inductance	27.25 μH
Switching frequency	25 kHz
Transformer turns ratio	1:2
Output capacitance	520 μF
Inductor current limitation	17 A
Resistance load	40 Ω/80 Ω

From time point t_1 to t_2, $\overline{G_{P3}}/G_{P4}$ changes from 1 to 0. The theoretical difference of whether applying this solution is indicated by the gray-dashed line and the solid line in Fig. 10. Assuming the first pulse width decreased by $D_\varphi T_{hs}$ (marked with light yellow background in Fig. 10), the inductor current at t_3 can be rewritten as

$$i''_L(t_3) = \frac{T_s}{2L}(1 - D_1 - D_\varphi)U_i. \tag{15}$$

Taking $i''_L(t_3) = i_L(t_3)$, $U_0 = 0$, and (2) into consideration, solving D_φ in (15) will yield

$$D_\varphi = \frac{1 - D_1}{2}. \tag{16}$$

V. EXPERIMENTAL VERIFICATION

In this section, the realization and experimental verification of the proposed technique at a lab-constructed DAB power converter test-bench (see Fig. 11) is presented. Different operating and testing scenarios are carried out to verify the effectiveness of the proposed approach. Comparison study between the conventional method, method proposed in [18], and the proposed one have been thoroughly performed as well.

As shown in Fig. 11, a DAB power converter described in Section II is built at our laboratory, the parameters of which are collected in Table III.

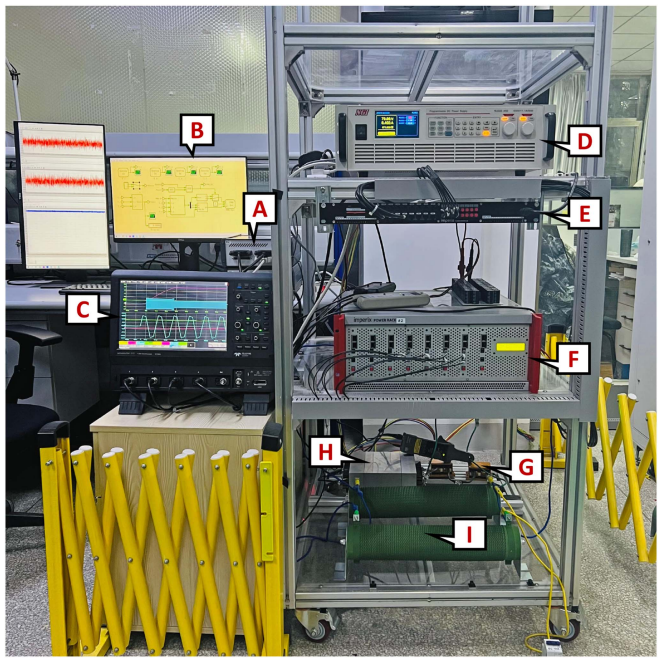

Fig. 11. Experimental setup. A: Real-time controller, B: Monitor, C: Scope, D: DC power supply, E: Interface board, F: DAB power converters, G: Series inductor, H: High frequency transformer, and I: Load resistance.

A. DC Bias Suppression Test

Fig. 12 illustrates the experimental results of whether the dc bias suppression is applied, where the primary H-bridge output voltage u_p, the secondary H-bridge output voltage u_s, and the inductor current i_L are presented. As can be clearly seen, when the dc bias suppression method is applied, the peak inductor current is 17 A, which is equal to the set value. The set time of dc current bias is zero. On the contrary, when the dc bias suppression method is not applied, the peak inductor current is 31 A, which is 1.82 times the set value, and the set time of the dc current bias is 0.3 ms.

B. Start-Up Without Loads

Fig. 13 illustrates the experimental results of three control strategies during a start-up procedure, with no load connected to the output side of the converter. The output voltage U_o and the inductor current i_L are presented. For the conventional method, the parameters $\frac{dD_1}{dt}$ and $\frac{dU_o^*}{dt}$ are tuned to 0.085/ms and 13.25 V/ms. As a consequence, the start time is 28.4 ms and the peak inductor current is 16.9 A. Besides, when the method proposed in [18] is adopted, the start-up time is 16.2 ms, as shown in Fig. 13(b). When the proposed method is applied, the output voltage rises to the desired voltage of 160 V, with only 14.4 ms, as shown in Fig. 13(c). The start-up time of the proposed method is reduced by 49.3% compared to the conventional method, and by 11.1% compared to the method in [18]. Additionally, compared with the conventional method, in the start-up process the inductor current stress is limited to 17 A and remains closely to the maximum permissible current stress.

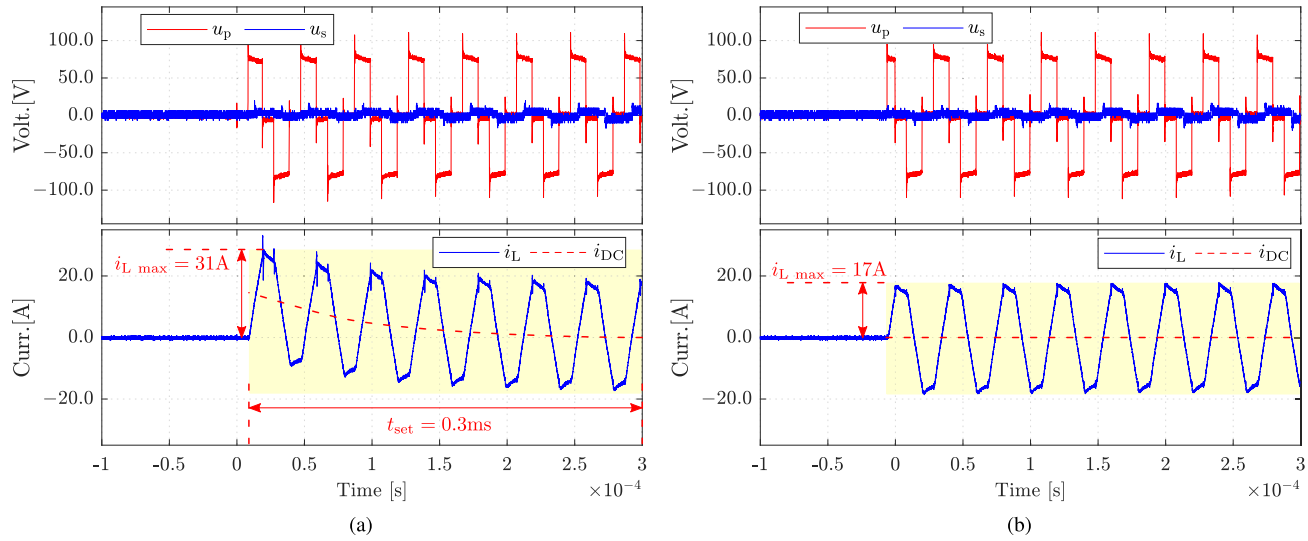

Fig. 12. Experimental data of AC side voltages and inductor current. (a) DC bias suppression is not applied. (b) DC bias suppression is applied.

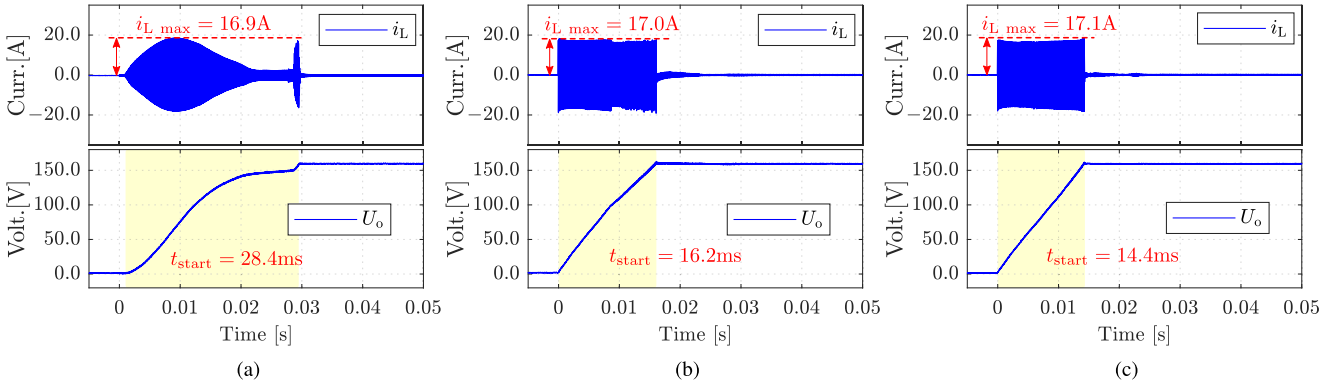

Fig. 13. Experimental data of inductor current and output voltage: no load. (a) Conventional method. (b) Method in [18]. (c) Proposed method.

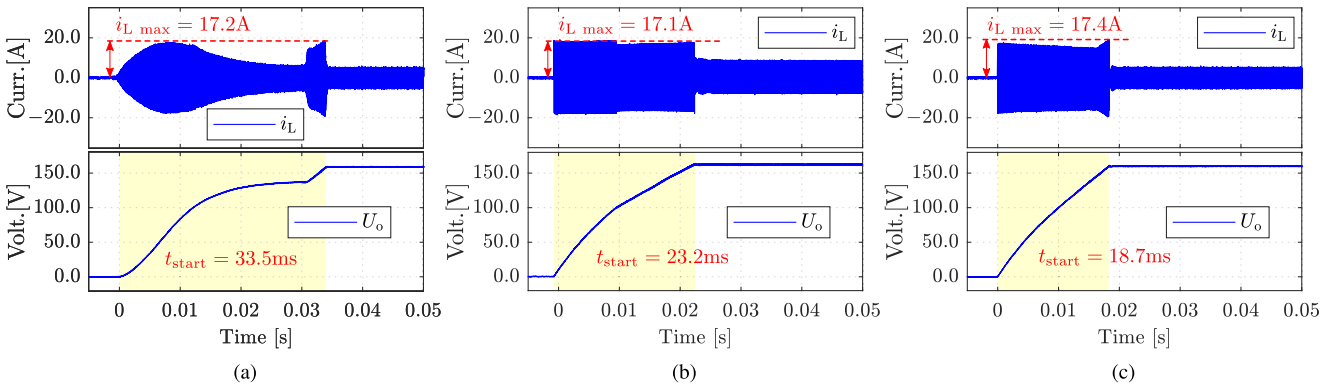

Fig. 14. Experimental data of inductor current and output voltage: half-load. (a) Conventional method. (b) Method in [18]. (c) Proposed method.

C. Start-Up With Loads

Fig. 14 illustrates the experimental results of the start-up performance with the classical method and proposed method under half-load condition ($R_{\text{load}} = 80\ \Omega$, $P_o = 320\ W$). For the conventional method, the parameters $\frac{dD_1}{dt}$ and $\frac{dU_o^*}{dt}$ are tuned to 0.075/ms and 8 V/ms. As a consequence, the start time is 33.5 ms and the peak inductor current is 17.2 A. Besides, when the method proposed in [18] is adopted, the start-up time is 23.2 ms, as shown in Fig. 14(b). When the proposed method is applied, the output voltage rises to the desired voltage of 160 V, within only 18.7 ms, as shown in Fig. 14(c). The start-up

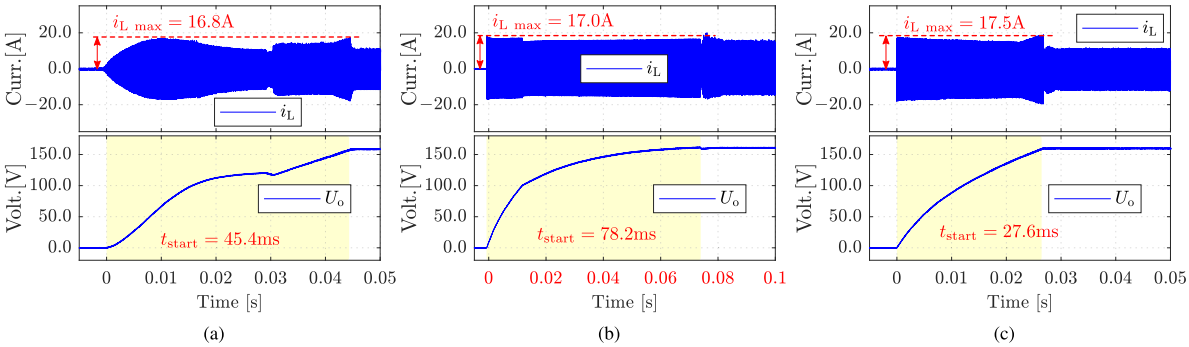

Fig. 15. Experimental waveforms of inductor current and output voltage: full-load. (a) Conventional method. (b) Method in [18]. (c) Proposed method.

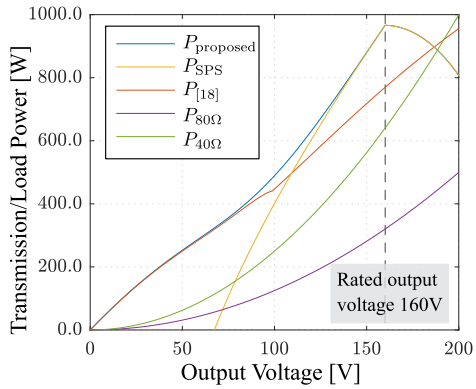

Fig. 16. Relationship of output voltage U_o and the maximum transmission power under current limitation. $P_{proposed}$ is the transmission power of the proposed method, P_{SPS} is the transmission power of SPS modulation, $P_{[18]}$ is the transmission power of the method in [18], $P_{80\ \Omega}$ is the load power when $R_{load} = 80\ \Omega$, and $P_{40\ \Omega}$ is the load power when $R_{load} = 40\ \Omega$.

time of the proposed method is prominently reduced by 44.18% compared to the conventional method, and by 19.4% compared to the method in [18].

Fig. 15 illustrates the experimental results of the start-up performance with the classical method and proposed method under full-load condition ($R_{load} = 40\ \Omega$, $P_o = 640\,W$). The output voltage U_o and the inductor current i_L are presented. For the conventional method, the parameters $\frac{dD_1}{dt}$ and $\frac{dU_o^*}{dt}$ are tuned to 0.050/ms and 3.25 V/ms. With the conventional method, the output voltage rises slowly at the end of step II, for the reason of the large load current. All the aforementioned factors lead to a long start-up time of 45.4 ms. While the start-up time of the proposed method is only 27.6 ms, with an improvement of 39.21%. In addition, the start-up time of the method in [18] is even 72% longer than that of the conventional method, and 183% longer than that of the proposed method.

When the output voltage is close to the rated value and the load resistance is 40 Ω, the method in [18] shows the smallest voltage ramp slope, close to zero, and even less than the conventional methods, which indicates that the method in [18] has the smallest transmission power, approximately equal to the output power. To explain this phenomenon, we plot the maximum transmission power with current limitation, under SPS, the proposed method, and the method in [18] separately, as shown in Fig. 16.

When the proposed method is applied, the peak inductor current gradually decreases as the voltage rises. However, when the output voltage approaches the rated value, the peak inductor current gradually increases. A possible explanation is that the modeling of DAB converters ignores the resistance of the switching device, the inductor, and the transformer.

VI. Conclusion

DAB power converters are widely adopted in the dc and hybrid ac–dc microgrids or distribution networks, power electronic transformers, electrical vehicles, etc. A fast and effective start-up procedure of DAB converters is important. In this work, we propose a simple while fast start-up strategy for DAB power converters. The relationship among the transmission power, peak inductor current, and the phase-shift ratios of DAB converters is theoretically developed and a way to obtain the phase-shift ratio in combination with maximum transmission power under the decided current limit is proposed. Moreover, a *dc-bias suppression* method, which modifies the drive signals in the first period is newly introduced to avoid the inrush current at the beginning of the start-up procedure. The proposed method avoids complex parameter tuning procedures and is simple in realization. Finally, experimental results demonstrate that the proposed strategy considerably outperforms the classical and a newly reported solutions in different testing scenarios. Future work will focus on the extending of the proposed techniques to the start-up of multiterminal and large power dc–dc converters.

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