# A Novel Non-Isolated Dual-Input Single-Output High Step-Up DC/DC Converter With Coupled Inductors

Chao Li, *Student Member, IEEE*, Hongzhu Li, *Member, IEEE*, Lihong Cheng, Xuanjin Sun, *Student Member, IEEE*, Ning Wang, and Wenjing Li

***Abstract*—This article proposes a novel nonisolated dual-input single-output high step-up dc/dc converter with coupled inductor (NI-DISO-CI) for the distributed sources. The coupled inductor along with the passive clamp circuits is employed to the NI-DISO-CI, which can achieve the high voltage conversion ratio without operating at an extremely duty cycle. The energy stored in leakage inductor is recycled by the passive clamp circuits, which can minimize the voltage spikes across power switches. Therefore, the power switches with low parasitic parameters can be selected. The power switches can achieve the zero current switching performance by utilizing the leakage inductor from coupled inductor. The operating principle, steady-state analysis, design and performance of the NI-DISO-CI are described in detail. Finally, the experimental prototype with the switching frequency of 100 kHz and the power rating of 400 W is built to verify the accuracy of the theoretical analysis.**

***Index Terms*—Coupled inductor, dual input, high step-up, low voltage stress.**

## I. Introduction

TO achieve the goal of carbon neutrality, the structure of the world energy system is constantly adjusted, and the proportion of renewable energy sources connected to the grid is increasing. However, the output voltage level of the renewable energy sources is low (12–48V), which is unable to provide sufficient voltage for the inverter. Therefore, a high step-up, high performance dc/dc converter is necessary to raise the output voltage of renewable energy sources to the voltage needed by the inverter (200–400 V) [1], [2], [3], [4], [5], [6], [7]. The environment, such as irradiance and temperature, has an impact on the renewable source like wind and solar energy. Therefore, the renewable source is unreliable, which can easily result in energy waste and instability of the generation system. Therefore, many scholars have researched the multi-input dc/dc converter to ensure the stability of the generation system, which is necessary for the renewable energy generation systems. The multi-input renewable energy generation system is shown in Fig. 1.

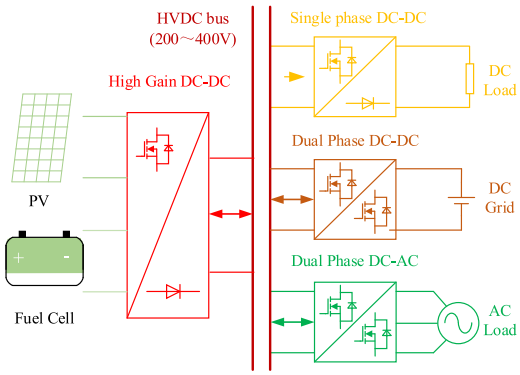


Fig. 1. Structure of distributed power generation system.

The multi-input converters can be divided into isolated and nonisolated dc/dc converters. The isolated multi-input converters have the advantage of high voltage levels and the ability of high-power transfer [8], [9], [10], [11]. However, the cost and volume of the isolated multi-input converters are larger than the nonisolated multi-input dc/dc converters.

Therefore, the classic converters were integrated to achieve the nonisolated multi-input converter. The simple structure and high reliability of nonisolated multi-input converter were proposed in [12], [13], [14], [15], [16], [17], [18], [19], and [20]. The principle and topology derivation of multi-input converters was explained in [21] and [23]. However, the voltage conversion ratio of above nonisolated multi-input converters cannot meet the requirements. Therefore, the switched capacitors were introduced to dual-input converter in [24], [25], and [26].

Compared to other voltage boosting techniques, the coupled inductor is the most straightforward, simple, and convenient way, so coupled inductor was widely used. The voltage conservation ratio had significantly improved by employing the coupled inductor in [27] and [28]. However, the leakage inductor may result in the high voltage spike. Therefore, the passive clamp circuit was employed to solve the voltage spike in [29] and [30]. Nevertheless, the above converters were unable to offer a wide range of output voltage. Therefore, the coupled inductor along with switch-capacitors was utilized to dual-input single-output

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dc/dc converter. The input inductor of the dual-input converter was changed by the coupled inductor in [31]. The energy of the leakage inductor was minimized by utilizing the switched capacitor cell. The coupled inductor was added in the switched capacitor cell in [32], which has low voltage spikes in power switches and achieve a high voltage conversion ratio. Moreover, other dual-input single-output dc/dc converters with coupled inductor and switch capacitor cell were proposed in [33], [34], [35], and [36]. But, the mentioned converters require many components, increasing the size, cost, and semiconductor devices.

Inspired by the above references, a novel nonisolated dual-input single-output high step-up dc/dc converter with coupled inductor (NI-DISO-CI) is proposed. By utilizing the passive clamp circuits to absorb the leakage energy, the voltage spikes of the power switches are minimized. The components and the cost of the NI-DISO-CI are reduced by integrating the passive clamp circuits.

In this article, a novel noNI-DISO-CI is proposed. The key benefits of the NI-DISO-CI can be summarized as follows.

1) By utilizing the coupled inductor, the high voltage conversion ratio of the NI-DISO-CI can be accomplished without an extremely duty.
2) The power density and efficiency of the NI-DISO-CI are significantly increased by integrating the passive clamp circuits to decrease the components.
3) The leakage inductor ensures ZCS performance of all power switches. Additionally, the current falling rates of most diodes are regulated by the leakage inductor, which significantly reduces reverse-recovery losses.
4) The voltage stress on the semiconductors is lower than the output voltage.

The rest of this article is organized as follows. The topology of the NI-DISO-CI is presented, and the operating principles are analyzed in Section II. Section III is devoted to the steady-state analysis of the NI-DISO-CI. The efficiency and loss analysis of the NI-DISO-CI are described in Section IV. The design procedure of the NI-DISO-CI is provided in Section V. Section VI is devoted to the comparison study and the experimental results analysis of the NI-DISO-CI. Finally, the conclusion is drawn in Section VII.

## II. Proposition and Operating Principles of Converters

### A. Structure of the NI-DISO-CI

The proposed NI-DISO-CI is shown in Fig. 2. The NI-DISO-CI consists of two coupled inductors, two power switches ($S_1$, $S_2$) with interleaved conduction, passive clamp circuits ($D_1$, $D_5$, $C_1$), and voltage multipliers ($C_2$-$D_2$, $C_3$-$D_4$). The coupled inductors include magnetizing inductors ($L_{m1}$, $L_{m2}$), leakage inductors ($L_{k1}$, $L_{k2}$) and secondary windings $N_{s1}$ and $N_{s2}$.

### B. Operating Principles of the NI-DISO-CI

The following assumptions are made to facilitate the analysis.

1) All switching components are ideal components.
2) The parasitic parameters of inductive and capacitive components are ignored.

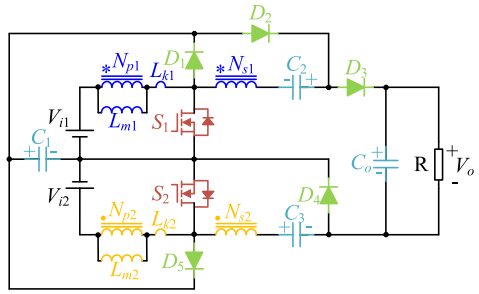


Fig. 2. Equivalent circuit of the NI-DISO-CI.

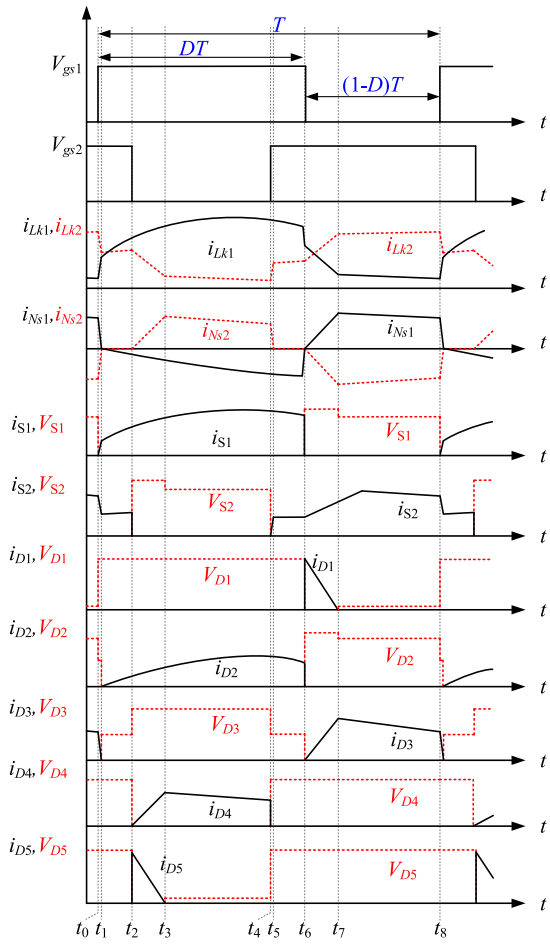


Fig. 3. Key waveform of the NI-DISO-CI.

3) The capacitance of the capacitors is infinite, and the voltage ripple is disregarded.
4) The turns-ratio of the coupled inductors are: $n_{s1} = N_{s1}/N_{p1}$ and $n_{s2} = N_{s2}/N_{p2}$.
5) The coupling coefficient $k$ of the coupled inductors can be defined as follows:

$$k = \frac{L_{m1}}{L_{m1} + L_{k1}} = \frac{L_{m2}}{L_{m2} + L_{k2}}.$$

The key waveforms of the NI-DISO-CI are shown in Fig. 3. According to the ON-OFF state of the semiconductors, the operating modes of the NI-DISO-CI can be divided into eight modes.

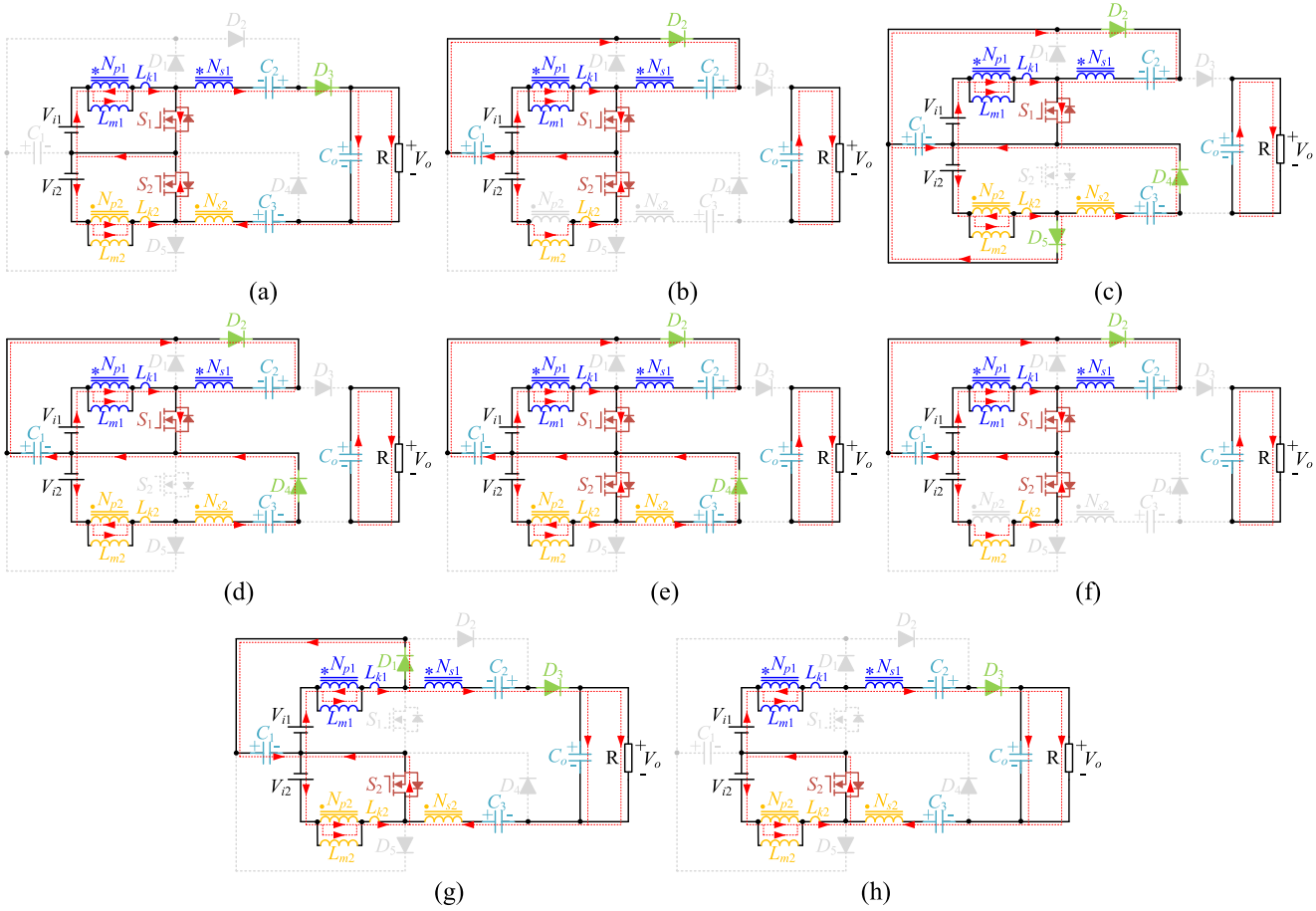


Fig. 4. Operation modes in one period. (a) Mode 1 [$t_0$~$t_1$]. (b) Mode 2 [$t_1$~$t_2$]. (c) Mode 3 [$t_2$~$t_3$]. (d) Mode 4 [$t_3$~$t_4$]. (e) Mode 5 [$t_4$~$t_5$]. (f) Mode 6 [$t_5$~$t_6$]. (g) Mode 7 [$t_6$~$t_7$]. (h) Mode 8 [$t_7$~$t_8$].

The key equivalent circuits of the operating modes are shown in Fig. 4, and the description of those modes are given as follows.

*Mode 1* {$t_0 \le t \le t_1$, Fig. 4(a)}: At $t = t_0$, the power switches $S_1$ starts to ON-state and $S_2$ remains ON-state. The diode $D_3$ is forward biased, and the rest of diodes are reverse biased. The power switch $S_1$ achieve the ZCS performance with the help of leakage inductor. And the magnetizing inductors are charged by the $V_{i1}$ and $V_{i2}$. The secondary windings $N_{s1}$&$N_{s2}$ with $C_2$&$C_3$ provide power to load and the capacitor $C_o$ via $D_3$. Because of the $S_1$ turns ON-state, $i_{Lk1}$ increases rapidly and linearly, and $i_{Lk2}$ decreases rapidly and linearly. Moreover, this mode is a short transition mode which ends when the current of $i_{D3}$ drops to zero. According to the Fig. 4(a), the following relationships can be expressed as follows:

$$\begin{cases} i_{Lm1}(t) = i_{Lm1}(t_0) + \frac{kV_{i1}}{L_{m1}}(t - t_0) \\ i_{Lk1}(t) = i_{Lm1}(t) - \frac{2n_{s1}I_o}{D}(t - t_0) \\ i_{Lm2}(t) = i_{Lm2}(t_0) + \frac{kV_{i2}}{L_{m2}}(t - t_0) \\ i_{Lk2}(t) = i_{Lm2}(t) + \frac{2n_{s2}I_o}{1-D}(t - t_0) \end{cases}. \quad (1)$$

*Mode 2* {$t_1 \le t \le t_2$, Fig. 4(b)}: In this mode, the power switches $S_1$ and $S_2$ remain on-state and the diode $D_2$ is forward biased while the rest of diodes are reverse biased. The magnetizing and leakage inductors are charged by the $V_{i1}$ and $V_{i2}$. The capacitor $C_2$ is charged by the capacitor $C_1$ and the secondary winding $N_{s1}$ via diode $D_2$. This load is powered by the capacitor $C_o$ as the diode $D_3$ is turned OFF. This mode ends when the power switches $S_2$ is completely turned OFF. According to the Fig. 4(b), the following relationships can be described as follows:

$$\begin{cases} i_{Lm1}(t) = i_{Lm1}(t_1) + \frac{kV_{i1}}{L_{m1}}(t - t_1) \\ i_{Lk1}(t) = i_{Lm1}(t) + \frac{2n_{s1}I_o}{D}(t - t_1) \\ i_{Lk2}(t) = \mathrm{i}_{Lm2}(t) = i_{Lk2}(t_1) + \frac{kV_{i2}}{L_{m1}}(t - t_1) \end{cases}. \quad (2)$$

*Mode 3* {$t_2 \le t \le t_3$, Fig. 4(c)}: In this mode, the power switch $S_1$ remains ON-state and $S_2$ starts to OFF-state. The diodes of $D_2$, $D_4$, and $D_5$ are forward biased and the diodes of $D_1$ and $D_3$ are reverse biased. The energy of the leakage inductor $L_{k2}$ is absorbed by the capacitors $C_1$ and $C_2$ through the diode $D_5$. The magnetizing inductors ($L_{m1}$ and $L_{m2}$) are charged by $V_{i1}$ and $V_{i2}$. And the capacitors $C_2$ and $C_3$ are charged by the secondary windings $N_{s1}$ and $N_{s2}$. The load is supplied by capacitor $C_o$ since the diode $D_3$ is reverse biased. The mode ends when the energy of the leakage inductor $L_{k2}$ is completely released. According

to the Fig. 4(c), the following relationships are given:

$$\begin{cases} i_{Lm1}(t) = i_{Lm1}(t_2) + \frac{kV_{i1}}{L_{m1}}(t-t_2) \\ i_{Lk1}(t) = i_{Lm1}(t) + \frac{2n_{s1}I_o}{D}(t-t_2) \\ i_{Lm2}(t) = i_{Lm2}(t_2) + \frac{kDV_{i2}}{(1-D)L_{m2}}(t-t_2) \\ i_{Lk2}(t) = i_{Lm2}(t) - \frac{2n_{s2}I_o}{1-D}(t-t_2) \end{cases}. \quad (3)$$

*Mode 4* $\{t_3 \le t \le t_4$, Fig. 4(d)$\}$: In this mode, the power switch $S_1$ remains ON-state and $S_2$ is OFF-state. The diodes $D_2$ and $D_4$ are forward biased, and the rest of diodes are reverse biased. The magnetizing inductors ($L_{m1}$, $L_{m2}$) are charged by the $V_{i1}$ and $V_{i2}$. The capacitor $C_2$ is charged by the secondary winding $N_{s1}$ and capacitor $C_1$. The capacitor $C_3$ is charged by the secondary winding $N_{s2}$ via the diode $D_4$. As the diode $D_3$ is reverse biased, the load is powered by capacitor $C_o$. This mode ends when the power switch $S_2$ starts to on-state. According to the Fig. 4(d), the following relationships can be achieved:

$$\begin{cases} i_{Lm1}(t) = i_{Lm1}(t_3) + \frac{kV_{i1}}{L_{m1}}(t-t_3) \\ i_{Lk1}(t) = i_{Lm1}(t) + \frac{2n_{s1}I_o}{D}(t-t_3) \\ i_{Lm2}(t) = i_{Lm2}(t_3) + \frac{kDV_{i2}}{(1-D)L_{m2}}(t-t_3) \\ i_{Lk2}(t) = i_{Lm2}(t) - \frac{2n_{s2}I_o}{1-D}(t-t_3) \end{cases}. \quad (4)$$

*Mode 5* $\{t_4 \le t \le t_5$, Fig. 4(e)$\}$: In this mode, the power switch $S_1$ keeps ON-state, and the power switch $S_2$ starts to ON-state. The power switch $S_2$ achieve the ZCS performance with the help of leakage inductor. The diodes $D_2$ and $D_4$ are forward biased, and the rest of diodes are reverse biased. This mode is a short transition mode, which ends when the power switch $S_2$ is completely turned ON.

*Mode 6* $\{t_5 \le t \le t_6$, Fig. 4(f)$\}$: The power switches $S_1$ and $S_2$ are ON-state and the diode $D_2$ is forward biased in this mode. The capacitor $C_2$ is charged by the secondary winding $N_{s1}$ and capacitor $C_1$ via diode $D_2$. Due to the reverse biased of diode $D_3$, the load is powered by capacitor $C_o$. This mode ends when the power switches $S_1$ is turned OFF.

*Mode 7* $\{t_6 \le t \le t_7$, Fig. 4(g)$\}$: In this mode, the power switch $S_1$ starts to OFF-state, while the power switch $S_1$ remains ON-state. The diodes $D_1$ and $D_3$ are forward biased, and the rest of diodes are reverse biased. The load is charged by the secondary windings $N_{s1}$, $N_{s2}$, capacitors $C_2$ and $C_3$ via the diode $D_3$. Because the power switch $S_1$ starts to OFF-state, the energy of the capacitor $C_1$ is charged by the leakage inductor $L_{k1}$. The mode ends when the energy of the leakage inductor $L_{k1}$ is completely released. According to the Fig. 4(g), the following relationship can be expressed as follows:

$$\begin{cases} i_{Lm1}(t) = i_{Lm1}(t_6) + \frac{kV_{i1}}{L_{m1}}(t-t_6) \\ i_{Lk1}(t) = i_{Lm1}(t) - \frac{2n_{s1}I_o}{1-D}(t-t_6) \\ i_{Lm2}(t) = i_{Lm2}(t_6) + \frac{kV_{i2}}{L_{m2}}(t-t_6) \\ i_{Lk2}(t) = i_{Lm2}(t) + \frac{2n_{s2}I_o}{1-D}(t-t_6) \end{cases}. \quad (5)$$

*Mode 8* $\{t_7 \le t \le t_8$, Fig. 4(h)$\}$: In this mode, the power switch $S_1$ is OFF-state, while the power switch $S_2$ remains ON-state. The diode $D_3$ is forward biased, and the rest of diodes are reverse biased. The energy of leakage inductor $L_{k1}$ is released through the $D_1$. The mode ends when power switch $S_1$ starts to ON-state. According to the Fig. 4(h), the following relationship can be achieved:

$$\begin{cases} i_{Lm1}(t) = i_{Lm1}(t_7) + \frac{kDV_{i1}}{(1-D)L_{m1}}(t-t_7) \\ i_{Lk1}(t) = i_{Lm1}(t) - \frac{2n_{s1}I_o}{1-D}(t-t_7) \\ i_{Lm2}(t) = i_{Lm2}(t_7) + \frac{kV_{i2}}{L_{m2}}(t-t_6) \\ i_{Lk2}(t) = i_{Lm2}(t) + \frac{2n_{s2}I_o}{1-D}(t-t_6) \end{cases}. \quad (6)$$

## III. Steady-State Analysis of the NI-DISO-CI

### A. Voltage Gain of the Proposed Converter

To simplify the theoretical analysis, the voltage expression for the secondary side of coupled inductor is given as follows:

$$\begin{cases} V_{Ns1} = kn_{s1}V_{Lm1} \\ V_{Ns2} = kn_{s2}V_{Lm2} \end{cases}. \quad (7)$$

In order to simple the steady-state analysis, the two short-time transition modes of modes 1 and 5 are ignored. According to Fig. 4(b), the relationships can be deduced as follows:

$$\begin{cases} V_{Lm1}^{(2)} = kV_{i1} \\ V_{Lm2}^{(2)} = kV_{i2} \\ V_{C2} = \mathrm{V}_{C1} + V_{Ns1} \end{cases}. \quad (8)$$

According to Fig. 4(c), the relationships can be deduced as follows:

$$\begin{cases} V_{Lm1}^{(3)} = kV_{i1} \\ V_{Lm2}^{(3)} = \frac{kDV_{i2}}{1-D} \\ V_{C1} = V_{C3} + V_{Ns2} \end{cases}. \quad (9)$$

According to Fig. 4(d), the relationships are given as follows:

$$\begin{cases} V_{Lm1}^{(4)} = kV_{i1} \\ V_{Lm2}^{(4)} = \frac{kDV_{i2}}{1-D} \\ V_{C2} = V_{C1} + V_{Ns1} \end{cases}. \quad (10)$$

According to Fig. 4(f), the relationships can be illustrated as follows:

$$\begin{cases} V_{Lm1}^{(6)} = kV_{i1} \\ V_{Lm2}^{(6)} = kV_{i2} \end{cases}. \quad (11)$$

According to Fig. 4(g), the relationships is given as follows:

$$\begin{cases} V_{Lm1}^{(7)} = \frac{kDV_{i1}}{1-D} \\ V_{Lm2}^{(7)} = kV_{i2} \end{cases}. \quad (12)$$

According to Fig. 4(h), the relationships are shown as follows:

$$\begin{cases} V_{Lm1}^{(8)} = \frac{kDV_{i1}}{1-D} \\ V_{Lm2}^{(8)} = kV_{i2} \\ V_o = \mathrm{V}_{i1} + \frac{DV_{i1}}{1-D} + n_{s1}V_{Lm1}^{(8)} + V_{C2} + V_{C3} + n_{s2}V_{Lm2}^{(8)} \end{cases}. \quad (13)$$

From the voltage-second balance principle of the magnetizing inductor $L_{m1}$ and $L_{m2}$, the follow relationships can be achieved

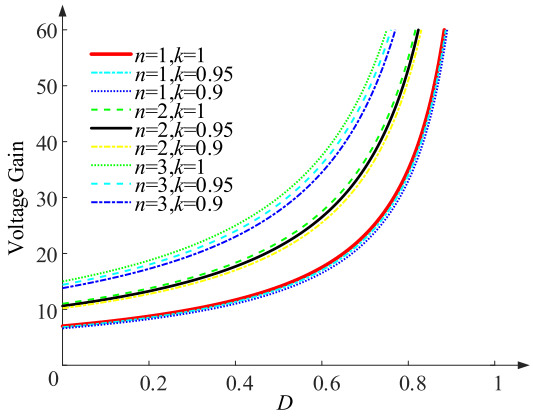


Fig. 5. Relationship between $k$, $n$, $D$ and voltage gain.

by solving the (8)–(13)

$$V_{C1} = \frac{1}{1-D}\max\{V_{i1}, V_{i2}\} \tag{14}$$

$$V_{C2} = kn_{s1}V_{i1} + \frac{1}{1-D}\max\{V_{i1}, V_{i2}\} \tag{15}$$

$$V_{C3} = \frac{1+kn_{s2}D}{1-D}V_{i2}. \tag{16}$$

The output voltage of the NI-DISO-CI is described as

$$V_o = \frac{(1+kn_{s1})V_{i1} + (1+kn_{s2})V_{i2} + \max\{V_{i1}, V_{i2}\}}{1-D}. \tag{17}$$

If the coupling coefficient $k = 1$, turns-ratio $n = n_{s1} = n_{s2}$, and the input voltage $V_{i1}$ and $V_{i2}$ are equal. The voltage gain of the NI-DISO-CI can be calculated as follows:

$$G = \frac{V_o}{V_{in}} = \frac{2n+3}{1-D}. \tag{18}$$

According to the (18), the output voltage is related to the input voltage $V_{i1}$, $V_{i2}$, turns-ratio $n_{s1}$, $n_{s2}$, and duty $D$. The output voltage curve of the NI-DISO-CI is shown in Fig. 5.

According to the Fig. 5, the output voltage of the NI-DISO-CI is proportional to the coupling coefficient $k$, turns-ratio $n_{s1}$, $n_{s2}$, and duty cycle $D$. Obviously, the voltage gain of NI-DISO-CI increases significantly as duty cycle $D$ or turns-ratio $n$ grows. The NI-DISO-CI achieves high voltage conversion ratio without an excessively duty.

### B. Voltage Stress of the Proposed Converter

When the coupling coefficient $k = 1$, the turns-ratio $n = n_{s1} = n_{s2}$, and the input voltage $V_{i1}$ and $V_{i2}$ are equal, the voltage stress on $C_1$, $C_2$, and $C_3$ are calculated as follows:

$$V_{VpsC1} = \frac{1}{2n+3}V_o \tag{19}$$

$$V_{VpsC2} = \frac{n(1-D)+1}{2n+3}V_o \tag{20}$$

$$V_{VpsC3} = \frac{1+nD}{2n+3}V_o. \tag{21}$$

From the (19)–(21), the voltage stress of $V_{C1}$, $V_{C2}$ and $V_{C3}$ are lower than the output voltage.

The voltage stress of the power switches and diodes can be calculated as follows:

$$V_{VpsS1} = \frac{V_{i1}}{1-D} \tag{22}$$

$$V_{VpsS2} = \frac{V_{i2}}{1-D} \tag{23}$$

$$V_{VpsD1} = V_{VpsD5} = \frac{1}{1-D}\max\{V_{i1}, V_{i2}\} \tag{24}$$

$$V_{VpsD2} = \frac{kn_{s1}V_{i1} + \max\{V_{i1}, V_{i2}\}}{1-D} \tag{25}$$

$$V_{VpsD3} = \frac{(1+kn_{s1})V_{i1} + (1+kn_{s2})V_{i2}}{1-D} \tag{26}$$

$$V_{VpsD4} = \frac{1+kn_{s2}}{1-D}V_{i2}. \tag{27}$$

According to the (22)–(27), the voltage stress across the semiconductors are lower than the output voltage.

When the coupling coefficient $k = 1$, $n = n_{s1} = n_{s2}$, $V_i = V_{i1} = V_{i2}$, the voltage stress of the switching components are calculated as follows:

$$V_{VpsS1(2)} = V_{VpsD1(5)} = \frac{1}{2n+3}V_o \tag{28}$$

$$V_{VpsD2} = V_{VpsD4} = \frac{n+1}{2n+3}V_o \tag{29}$$

$$V_{VpsD3} = \frac{2n+2}{2n+3}V_o. \tag{30}$$

According to the (28)–(30), it is possible to choose power switches with low on-resistance and diodes with low voltage drop, which significantly raise the overall performance of the NI-DISO-CI.

## IV. Efficiency and Loss Analysis of the NI-DISO-CI

By considering the parasitic elements of the components, the loss analysis of the NI-DISO-CI is considered as follows.

### A. Loss of Power Switches and Diodes

Since the ZCS performance is achieved for both power switches at the turn-ON instant. The losses of the power switches can be calculated as follows:

$$P_S = \sum_{i=1,2}\left(I_{rms\_Si}^2 R_{Si} + \frac{V_{Si}I_{Si\_on}t_{on} + V_{Si}I_{Si\_off}t_{off} + V_{Si}^2 C_r}{2}f_s\right) \tag{31}$$

where $V_{Si}$ is the voltage stress of the power switches, $I_{Si\_on}$, $I_{Si\_on}$ are the current stresses of ON-state and OFF-state, $t_{on}$ is the rising time, $t_{off}$ is the falling time, $C_r$ is the output capacitor, $f_s$ is the switching frequency, $I_{rms\_Si}$ is the rms current of the power switches, $R_{Si}$ is the on-resistance of the power switches. The rms current of power switches can be calculated as follows:

$$I_{rms\_S1} = \frac{\sqrt{3}I_o\sqrt{\frac{12nD(nD+D+2)+D(7D+4)+16}{D}}}{6(1-D)} \tag{32}$$

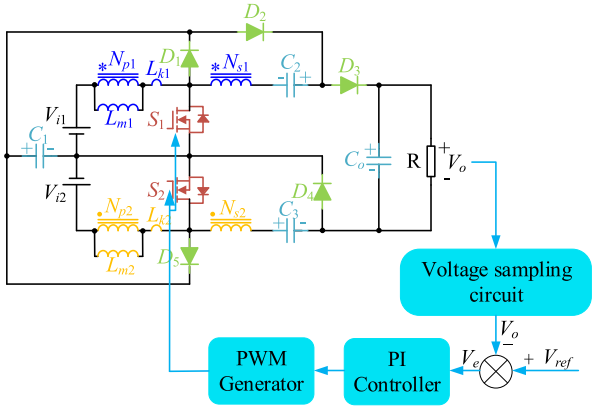


Fig. 6. Schematic of control circuit.

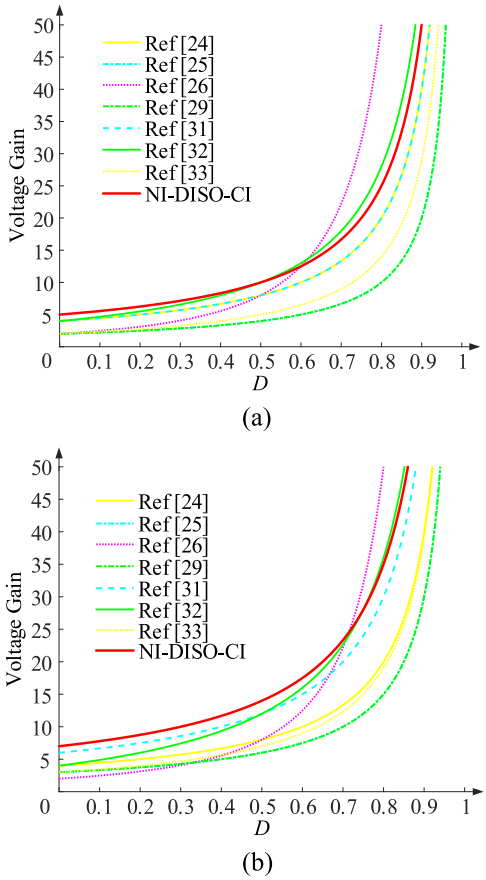


Fig. 7. Comparison of voltage gains versus duty cycle. (a) $n = 1$. (b) $n = 2$.

$$I_{\text{rms\_S2}} = \frac{\sqrt{12n(nD+D+2)+52-25D}}{2\sqrt{3}(1-D)} I_o. \tag{33}$$

The loss of the diodes can be calculated as follows:

$$P_D = \sum_{i=1,2,\ldots,5} (V_{Fi} I_o + I_{rms\_Di}^2 R_{Di}). \tag{34}$$

Where $V_{Fi}$ is the voltage drop of the diodes, and the rms current of the diodes is $I_{\text{rms\_}Di}$, and the on-resistance of the diodes is $R_{Di}$. The rms current of diodes can be calculated as

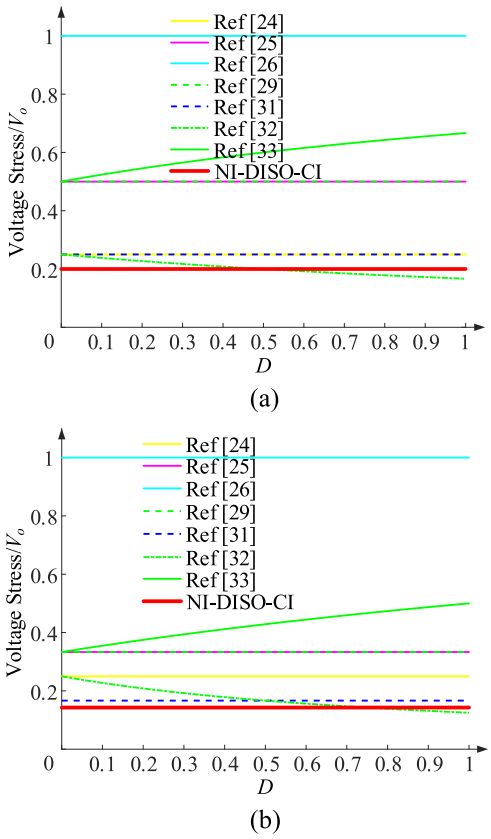


Fig. 8. Comparison of the maximum voltage stress versus duty cycle. (a) $n = 1$. (b) $n = 2$.

follows:

$$I_{rms\_D1} = I_{rms\_D5} = \frac{I_o}{2}\sqrt{\frac{12n(n+1)+7}{3(2n+1)(1-D)}} \tag{35}$$

$$I_{rms\_D2} = \frac{2I_o}{\sqrt{3D}} \tag{36}$$

$$I_{rms\_D3} = I_{rms\_D4} = \frac{2I_o}{\sqrt{3(1-D)}}. \tag{37}$$

### B. Capacitor and Magnetic Losses

The loss of the capacitors can be expressed as follows:

$$P_C = I_{rms\_Co}^2 R_{Co} + \sum_{i=1,2,3} I_{rms\_Ci}^2 R_{Ci}. \tag{38}$$

The rms currents of the capacitors are $I_{\text{rms\_}Co}$ and $I_{\text{rms\_}Ci}$. The on-resistance of the capacitors are $R_{Co}$ and $R_{Ci}$. The rms current of capacitors can be calculated as follows:

$$I_{rms\_C1} = I_o\sqrt{\frac{4n(3nD+2D+1)+D+6}{6D(2n+1)(1-D)}} \tag{39}$$

$$I_{rms\_C2} = \frac{2I_o}{\sqrt{3D(1-D)}} \tag{40}$$

$$I_{rms\_C3} = \frac{I_o}{1-D}\sqrt{\frac{2(3-2D)}{3}} \tag{41}$$

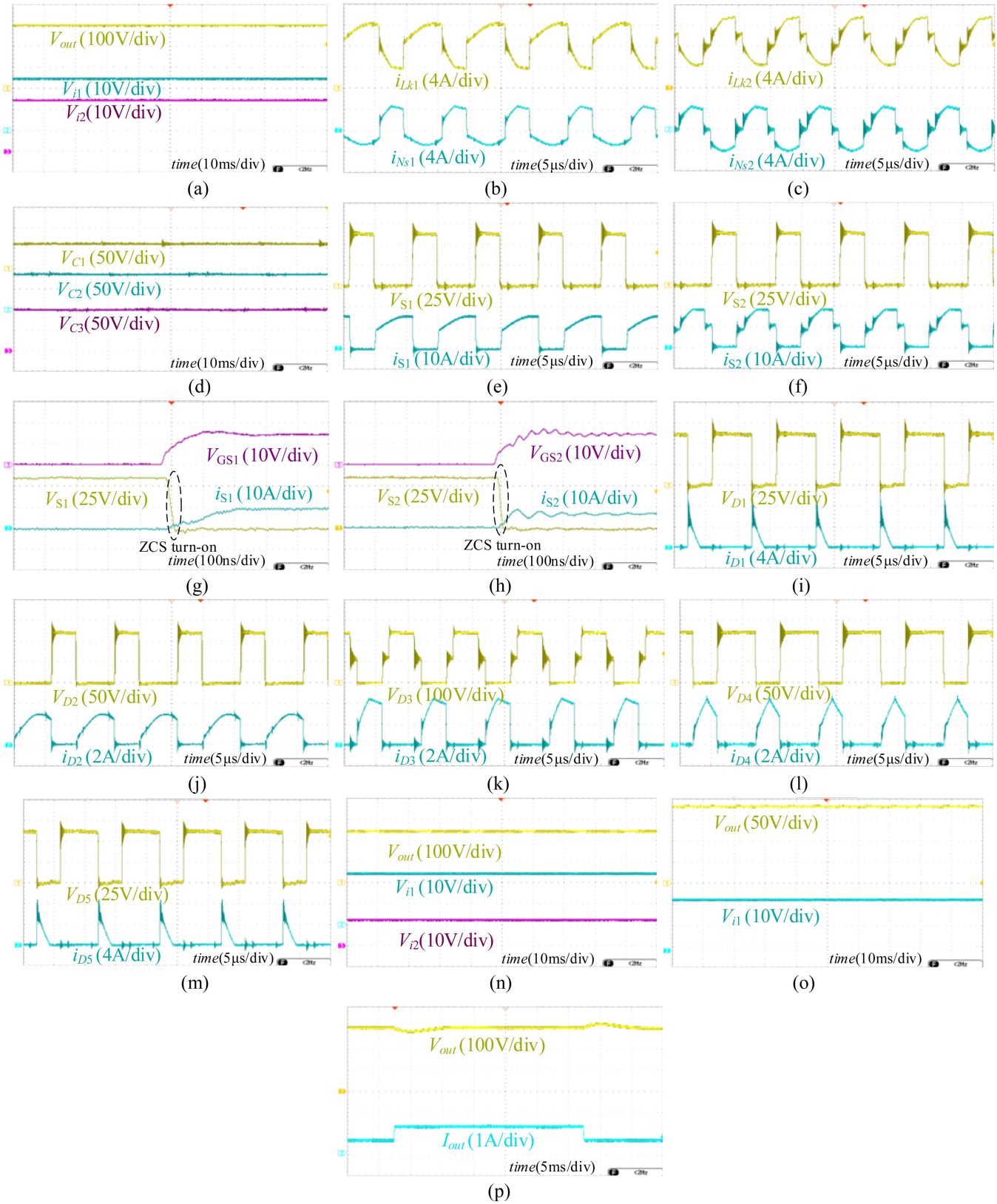


Fig. 9. Experimental waveforms of the NI-DISO-CI. (a) Input and output voltage waveforms. (b) Current waveforms of the CI 1. (c) Current waveforms of the CI 2. (d) Voltage across the capacitors. (e) Voltage and current waveforms of $S_1$. (f) Voltage and current waveforms of $S_2$. (g) ZCS turn-ON of $S_1$. (h) ZCS turn-ON of $S_2$. (i) Voltage and current stress of $D_1$. (j) Voltage and current stress of $D_2$. (k) Voltage and current stress of $D_3$. (l) Voltage and current stress of $D_4$. (m) Voltage and current stress of $D_5$. (n) Voltage waveforms under different input voltages $V_{i1} = 24$ V and $V_{i2} = 12$ V. (o) Voltage waveforms under single input voltage. (p) Dynamic response of the change in the load.

$$I_{rms\_Co} = I_o\sqrt{\frac{1+3D}{3(1-D)}}. \tag{42}$$

The loss of the CI includes the loss of copper and magnetic

$$P_{CI} = P_{cu,CI} + P_{core,CI} \tag{43}$$

$$P_{cu,CI} = \sum_{i=1,2} I^2_{rms-Lki} r_{pi} + \sum_{i=1,2} I^2_{rms-Lsi} r_{si} \tag{44}$$

where $I_{\text{rms-}Lki}$, and $I_{\text{rms-}Lsi}$ are the rms current of CI and $r_{pi}$, and $r_{si}$ are the resistance of CI.

$$I_{rms\_Lk1} = \frac{I_o}{2(1-D)}\sqrt{\frac{12nD(n+3)+11D+16}{3D}} \tag{45}$$

$$I_{rms\_Lk2} = \frac{\sqrt{\frac{12n^2(1-D)^2+4(21D^2-36D-15)+147D^2-210D+79}{3}}}{2(1-D)^2} I_o \tag{46}$$

$$I_{rms\_Ls1} = \frac{2I_o}{\sqrt{3D(1-D)}} \tag{47}$$

$$I_{rms\_Ls2} = \frac{2I_o}{(1-D)^2}\sqrt{\frac{3D^2-3D+1}{3}} \tag{48}$$

$$P_{core,CI} = V_e K_c f_s^{\delta} B_{\max}^{\beta} \tag{49}$$

where $V_e$ represents the volume of the magnet. $B_{\max}$ is the maximum magnetic flux of the magnetic component. The $K_c$, $\delta$, and $\beta$ are an empirical constant.

The overall loss of the converter is calculated as follows:

$$P_{\text{Loss}} = P_{\text{S}} + P_D + P_C + P_{\text{CI}}. \tag{50}$$

The theoretical efficiency is calculated as follows:

$$\eta = \frac{P}{P + P_{Loss}} \tag{51}$$

where $P$ represents the output power.

## V. Design Procedure of the NI-DISO-CI

In order to verify the theoretical analysis and performance of the NI-DISO-CI, a 400W experimental prototype with a 300 V output voltage and the switching frequency of 100 k is built.

### A. Design of Coupled Inductor

According to the (18), it can be seen that the voltage gain of NI-DISO-CI is related to the coupling coefficient $k$, turns-ratio $n_{s1}$, $n_{s2}$, duty cycle $D$, and input voltage $V_{i1}$, $V_{i2}$. For simplifying the design process, the coupling coefficient is taken as $k = 1$ and the turns-ratio is taken as $n_{s1} = n_{s2} = n$. The turns-ratio of the coupled inductor is calculated as follows:

$$n \geq \frac{\frac{1-D}{V_{in}}V_o - 3}{2}. \tag{52}$$

The duty cycle is initially chosen as $D = 0.6$, and the turns-ratio can be calculated by substituted into (52).

The ripple coefficient of the current is set as $\gamma$, the relationship between the current of the inductor and the ripple coefficient is given as follows:

$$\begin{cases} \text{I}_{Lm1} = \frac{\Delta i_{Lm1\_\max}}{\gamma} \\ \text{I}_{Lm2} = \frac{\Delta i_{Lm2\_\max}}{\gamma} \end{cases}. \tag{53}$$

The inductance of the coupled inductor is obtained as follows:

$$\begin{cases} L_{m1} \geq \frac{V_{i1}D}{\Delta i_{Lm1\_\max} f_s} = \frac{V_{i1}D}{\gamma I_{Lm1} f_s} \\ L_{m2} \geq \frac{V_{i2}D}{\Delta i_{Lm2\_\max} f_s} = \frac{V_{i2}D}{\gamma I_{Lm2} f_s} \end{cases}. \tag{54}$$

When the current ripple coefficient $\gamma = 0.4$, the inductance of the coupled inductors is calculated as $L_{m1} \geq 40.42$ $\mu$H and $L_{m2} \geq 43.79$ $\mu$H. The inductance of coupled inductor is selected as $L_{m1} = L_{m2} = 50$ $\mu$H in actual circuit. And the leakage inductance is controlled by adjusting the winding distribution and air gap.

### B. Design of the Capacitor

The rated voltage of the capacitor can be calculated by the (14)–(16). The capacitance is determined by the maximum ripple coefficient of the output voltage and the rated power, the ripple coefficient of the capacitor is assumed as $\alpha$. The capacitance can be calculated as follows:

$$C_{C1} \geq \frac{I_o}{\Delta V_{C1} f_s} = \frac{2n+3}{\alpha V_o^2 f_s} P_o \tag{55}$$

$$C_{C2} \geq \frac{I_o}{\Delta V_{C2} f_s} = \frac{2n+3}{(n(1-D)+1)\alpha V_o^2 f_s} P_o \tag{56}$$

$$C_{C3} \geq \frac{I_o}{\Delta V_{C3} f_s} = \frac{2n+3}{(1+nD)\alpha V_o^2 f_s} P_o \tag{57}$$

$$C_{Co} \geq \frac{I_o}{\Delta V_{Co} f_s} = \frac{P_o}{\alpha V_o^2 f_s}. \tag{58}$$

The voltage ripple coefficient is taken as $\alpha = 0.03$. According to the (55)–(58), the capacitance of $C_{C1}$ should be larger than 7.407 $\mu$F, the capacitance of $C_{C2}$ should be larger than 5.291 $\mu$F, the capacitance of $C_{C3}$ should be larger than 4.63 $\mu$F, and the capacitance of $C_{Co}$ should be larger than 1.481 $\mu$F. Considering the equivalent series resistance in the actual capacitor, the ripple of the output voltage will be larger than the theoretical value. Therefore, the capacitance of capacitors $C_1$, $C_2$, and $C_3$ is taken as 10 $\mu$F in the actual circuit. The capacitance of capacitor $C_o$ is selected as 7 $\mu$F in the actual circuit.

In summary, the key components of the NI-DISO-CI can be chosen as given in Table I.

### C. Schematic of Control Circuit

The schematic of control circuit is shown in Fig. 6. The output voltage $V_o$ of the proposed converter is obtained by the sampling circuit. The reference voltage is $V_{\text{ref}}$. And the $V_e$ is the error value of the target voltage $V_{\text{ref}}$ and the output voltage $V_o$. According to the $V_e$, PI controller adjust the duty cycle $D$ which ensures the reliability of the proposed converter. The pulsewidth

TABLE I
KEY COMPONENTS OF THE NI-DISO-CI

| Parameter/Component | Specification |
|---|---|
| Input Voltage $V_{in}$ | 12–24 V |
| Output Voltage $V_o$ | 300 V |
| Rated Power $P_o$ | 400 W |
| Magnetizing Inductance $L_{m1}$ | 50.31 $\mu$H |
| Magnetizing Inductance $L_{m2}$ | 50.73 $\mu$H |
| Leakage Inductance $L_{k1}$ | 1.53 $\mu$H |
| Leakage Inductance $L_{k2}$ | 1.59 $\mu$H |
| Turns Ratio | $N_p/N_s$=1:1 |
| Capacitor $C_1$, $C_2$, and $C_3$ | 10 $\mu$F/250 V |
| Capacitor $C_o$ | 7 $\mu$F/450 V |
| Diode $D_1$ and $D_5$ | MBR10100CT |
| Diode $D_2$ and $D_4$ | MBR10200CT |
| Diode $D_3$ | ASD265D |
| Power Switch $S_1$ and $S_2$ | IQE065N10NM5 |

modulation pulse signal of the power switches is obtained by the generator.

## VI. COMPARISON STUDY AND EXPERIMENTAL RESULTS ANALYSIS

### A. Comparison Study

In this section, the proposed NI-DISO-CI is compared to other similar converters. The voltage gain, voltage stress and the number of switches, diodes, capacitors, magnetic components are given in Table II. In order to make the comparison study as simple as possible, the duty cycle $D$, the turns-ratio $n$, and the input voltage $V_{i1}$&$V_{i2}$ are settled as equal.

An integrated dual-input converter is proposed with the switched-capacitor cell to further enhance the voltage gain in [24], [25], and [26]. The two Boost structures were integrated to obtain a dual-input converter in [29] and [33] and the coupled inductors were introduced to further increase the voltage gain. The input inductor of the dual-input converter was replaced by the coupled inductor in [31]. The energy of the leakage inductor was minimized by utilizing the switched capacitor cell, which had improved the voltage conversion ratio. And the coupled inductor was added in the switched capacitor cell in [32], which has low voltage spike in power switches and achieve a high voltage conversion ratio.

The NI-DISO-CI achieves higher voltage conversion ratio and lower switch voltage stress with fewer components when compared with the converters in [24], [25], [29], [31], and [33]. Compared with the [26] and [32], the NI-DISO-CI can achieve higher voltage conversion ratio with the lower duty cycle $D$. Moreover, the converters proposed in [26] have a higher voltage and current stress across semiconductors than the NI-DISO-CI. As shown in Fig. 7, the voltage gain of those converters is illustrated to compare the difference between the NI-DISO-CI and other similar converters. Fig. 8 compares the maximum voltage stress across the semiconductors between the NI-DISO-CI and other similar converters.

Compared to other converters, the NI-DISO-CI achieves the high voltage conversion ratio and reduces the voltage stress of the semiconductors. Therefore, it is possible to select the semiconductors with lower on-resistance, which significantly enhances the efficiency of the NI-DISO-CI.

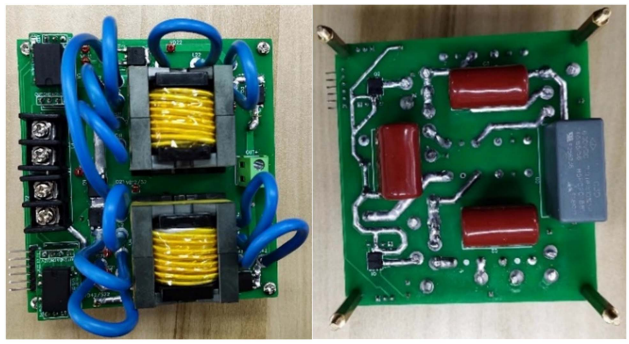


Fig. 10. Photograph of the experimental prototype. (a) Top. (b) Bottom.

### B. Experimental Results Analysis

A 400 W prototype is built to verify the accuracy of the NI-DISO-CI. The input and output voltage waveforms are shown in Fig. 9(a), which confirms the high voltage conversion ratio of the NI-DISO-CI. The current waveform of coupled inductors is shown in Fig. 9(b) and (c). As shown in Fig. 9(d), the voltage across the capacitors $C_1$, $C_2$, and $C_3$ are 60, 84, and 96 V respectively, which verifies the theoretical analysis. The voltage and current waveforms of power switches are illustrated in Fig. 9(e) and (f). The voltage stress across the power switches is about 60 V. The ZCS performance of the $S_1$ and $S_2$ is illustrated in Fig. 9(g) and (h), which significantly minimizes the switching loss. The voltage and current stress across the diodes are shown in Fig. 9(i)–(m). The measured voltage stress of the diodes $D_1$, and $D_5$ is about 60 V, which has confirmed the theoretical analysis. The measured voltage across the $D_2$, $D_3$, and $D_4$ is about 120, 240, and 120 V, respectively. Fig. 9(n) illustrates the input and output voltage waveforms for different input voltage. The input and output voltage waveforms under single input voltage are shown in Fig. 9(o). The dynamic response of the change in load are shown in Fig. 9(p). The experimental prototype is shown in Fig. 10.

The theoretical efficiency of NI-DISO-CI can be calculated by utilizing the (31)–(51). The highest efficiency of NI-DISO-CI at 360W is 97.472% in theory and 96.934% in reality. The efficiency of NI-DISO-CI at 400W is 97.46% in theory and 96.88% in reality. According to the loss analysis and measured results, Fig. 11 shows the efficiency curve of the NI-DISO-CI. Fig. 12 depicts the loss distribution of NI-DISO-CI at 400W with the components in Table I.

The loss can be further minimized by selecting the components with low parasitic parameters. The loss of magnetic

TABLE II
COMPARISON OF THE PROPOSED CONVERTER WITH OTHER SIMILAR CONVERTER

| Converter | Voltage Gain | Components S/D/C/CI+L/T | Voltage Stress on Switches | Soft Switching | Power | Input and Output | Efficiency | Common ground |
|---|---|---|---|---|---|---|---|---|
| [24] | $\frac{4}{1-D}$ | 2/8/6/2/18 | $\frac{V_{i1}}{1-D}, \frac{V_{i2}}{1-D}$ | ZVT | 800 W | 30V/40 V/ 400 V | 96.2% | No |
| [25] | $\frac{1+n}{1-D}$ | 2/8/5/2/17 | $\frac{V_{i1}}{1-D}, \frac{V_{i2}}{1-D}$ | ZVT | 800 W | 40 V/45 V/ 400 V | 93% | No |
| [26] | $\frac{2}{(1-D)^2}$ | 4/5/4/4/17 | $V_o, \frac{V_{i2}}{1-D_2}$ | – | 250 W | 20 V/24 V/ 400 V | 93.5% | Yes |
| [29] | $\frac{n+1}{1-D}$ | 2/6/4/2/14 | $\frac{V_{i1}}{1-D}, \frac{V_{i2}}{1-D}$ | ZCS | 800 W | 12 V/24 V/ 200 V | 91.28% | Yes |
| [31] | $\frac{2n+2}{1-D}$ | 2/4/4/2/12 | $\frac{V_o}{2n+2}$ | – | 200 W | 12 V/20/V 186 V | 95.4% | Yes |
| [32] | $\frac{2nD+4}{1-D}$ | 2/4/5/3/14 | $\frac{V_o}{2nD+4}$ | – | 350 W | 28 V/28 V/ 410 V | 96.35% | Yes |
| [33] | $\frac{1+n+D}{1-D}$ | 3/5/4/2/14 | $\frac{V_{i1}+DV_{i2}}{1-D}, V_{i2}, \frac{V_{i1}-(1-2D)V_{i2}}{1-D}$ | – | 100 W | 22 V/24 V/ 250 V | -- | Yes |
| NI-DISO-CI | $\frac{2n+3}{1-D}$ | 2/5/4/2/13 | $\frac{V_o}{2n+3}$ | ZCS | 400 W | 24/24 V/ 300 V | 97.46% | No |

S=Switch, D=Diode, C=Capacitor, CI=Coupled Inductor, L=Inductor, T=Total Components.

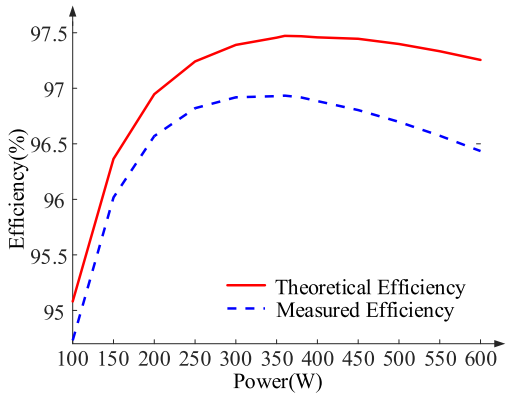


Fig. 11. Theoretical and measured efficiency of NI-DISO-CI.

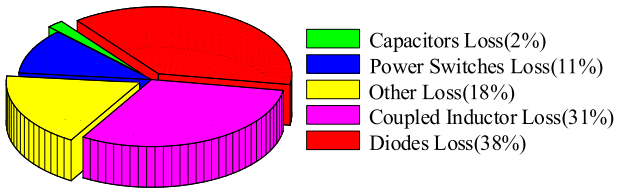


Fig. 12. Loss distribution when power is 400W.

component can be decreased for the coupled inductors by applying magnetic integration and increasing cross-sectional area of wires.

## VII. CONCLUSION

In this article, a novel NI-DISO-CI is proposed for the two different kinds of input source. By utilizing the coupled inductor in dual-input single-output dc/dc converter, a high voltage conversion ratio can be achieved without an extremely duty. The passive clamp circuit is integrated which has reduce the components and improve the overall performance of the NI-DISO-CI. Other merits of the NI-DISO-CI are low current and voltage stresses on semiconductors, simple topological structure and control method, and enhanced design flexibility. Furthermore, the leakage inductor from coupled inductor benefits the ZCS performance of the power switches. And the current falling rates of the most diodes are regulated by the leakage inductor, which significantly reduce the reverse-recovery losses. The operating principle and performance comparison against other similar converters have been explained in detail. A prototype with the characteristics of 24–24 V input, 300 V output, and 400 W was built, and the results of the experiments confirmed the accuracy of the theoretical analysis.

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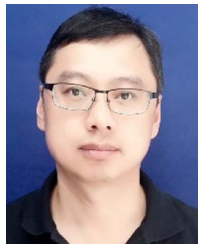

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