# Letters

## A Novel Driving Current Control Approach in Enhanced Current-Source Gate Driver

Qiaozhi Yue, Han Peng, Qiaoling Tong, and Yong Kang

***Abstract*—Active gate drivers (AGDs) are popular because of their capability to flexibly control the switching behavior of power transistors. State-of-the-art AGDs need to adopt extensive driving switches, resistors, or additional voltage or current sources, which significantly increase the cost, size, and complexity of gate drivers. To overcome this bottleneck, an enhanced inductor-based current-source gate driver (ECSGD) with well-controlled gate driving current and fast driving current transition is proposed in this letter. Driving current is controlled by switching between different resonant networks within a presettled hysteresis window to solve the poor gate driving current regulation limitation of conventional inductor-based current-source gate drivers. Driving current transition speed is also accelerated by the internal supply voltage boosting function. The design prototype demonstrates a driving current control of 2 A with a hysteresis window of 0.3 A. The driving current transition time is shortened by more than 30% with positive driving voltage boosted from 15 to 25 V. Hence, the ECSGD can be used as an AGD with a simple structure, high control accuracy, and fast response speed.**

***Index Terms*—Driving current control, driving voltage boosting, enhanced current-source gate driver.**

### I. Introduction

ACTIVE gate drivers (AGDs) have grown in popularity in recent years due to their controllability over the switching behavior of power transistors [1], [2]. AGDs adjust the gate voltage or current during the switching transient to optimize the switching losses, voltage or current overshoot, and electromagnetic interference. State-of-the-art AGDs can be roughly divided into three categories: variable gate resistance adjusted with resistor networks [3], [4], variable gate current by injecting or sinking with auxiliary current sources [5], and variable gate voltage using additional voltage sources [6]. All the abovementioned approaches require redundant components that severely increase the cost, size, and complexity of the gate driver. With the increasing demands of power density and compact module design, an AGD with a simple structure, strong driving capability, and flexible adjusting ability is urgently needed.

Current-source gate drivers (CSGDs) have the advantage of stronger driving capability and can be designed as either inductorless (by current mirror) or inductor-based CSGDs. An inductor-based full-bridge CSGD, also known as a resonant gate driver, drives the power transistor through an *LC* resonant circuit. It can also provide constant driving current by precharging the inductor [7], [8]. The inductor-based CSGD has the merits of ultra-low gate driver loss and high power density [9], [10]. However, to adopt the inductor-based CSGD as AGD, it suffers from a slow driving current adjustment rate due to the continuity of current in the inductor. In [11] and [12], the average driving current is adjusted in inductor-based CSGD during the power transistor's switching transient. But driving current had quite a long transition time with large current ripples, which led to a poor switching trajectory adjustment of the power transistor. An adaptive driving current adjustment was proposed in [13] using additional inductors, diodes, and driving switches for fast current injection and sinking, whereas the auxiliary inductors need to be carefully designed and precharged before current injection or sinking. Therefore, current approaches of inductor-based CSGDs using as AGDs have limited driving current control capability or require extra components.

To overcome the abovementioned limitations, an enhanced inductor-based CSGD (ECSGD) is proposed to realize fast and precise driving current adjustment with a simple structure. The main contributions are as follows.

1) The driving current is adjusted by switching between different resonant networks and stabilized to the required current level with hysteresis control. Precise driving current control in inductor-based CSGD can be achieved.
2) With the hysteresis-controlled driving current, a small driving inductor can be adopted for fast driving current transient speed and low driving current ripple, which improves the active controllability.

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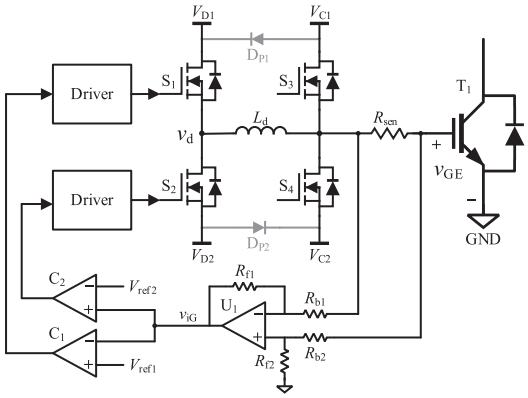


Fig. 1. Proposed enhanced CSGD.

3) To further accelerate the driving current transition speed and improve the overall driving capability, higher driving voltages than the gate clamping voltages are applied during the power transistor's switching transient, which forms a novel ECSGD.
4) Higher driving voltages are achieved by the full-bridge topology configured as a boost and inverting boost converter during the gate voltage clamping intervals. No additional power supply is required.

The rest of this letter is organized as follows. Section II discusses the topology, control approach, and working principle of the proposed ECSGD. Section III shows the designed ECSGD prototype and experimental results. Finally, Section IV concludes this letter.

## II. Proposed ECSGD and Driving Current Control Approach

Fig. 1 illustrates the schematic of the proposed ECSGD, where $T_1$ is the power transistor. ECSGD consists of four switches and a driving inductor $L_d$, where $S_1$ and $S_2$ form the driving arm and $S_3$ and $S_4$ form the clamping arm. $U_1$ is an operational amplifier, whereas $C_1$ and $C_2$ are hysteretic comparators with hysteresis voltage of $V_{hys}$. A small sensing resistor $R_{sen}$ is adopted to measure $i_G$.

### A. Driving Current Control Approach

Fig. 2 shows the key waveforms of the turn-ON transient to illustrate the proposed driving current control approach. $S_1$ in Fig. 2 refers to the driving voltage of switch $S_1$. $v_{GE}$ and $i_G$ are the gate voltage and current of $T_1$, respectively. $v_d$ is the switching node voltage of the driving arm. Fig. 3 illustrates the equivalent driving loops for turn-ON and turn-OFF transients, where $C_{ies}$ is the input capacitor of $T_1$. Basically, driving current of the proposed ECSGD is adjusted by switching between different resonant networks within the settled hysteresis window. A hysteresis control circuit is applied with driving current $i_G$ sampled by differential amplifier $U_1$. The output voltage of $U_1$ becomes $v_{iG} = k \times i_G$, where $k$ is expressed as $R_{sen} \times (R_{f1}/R_{b1})$. $v_{iG}$ is fed to $C_1$ and $C_2$ and compared to the reference voltages $V_{ref1}$ and $V_{ref2}$, to generate the driving signals of $S_1$ and $S_2$.

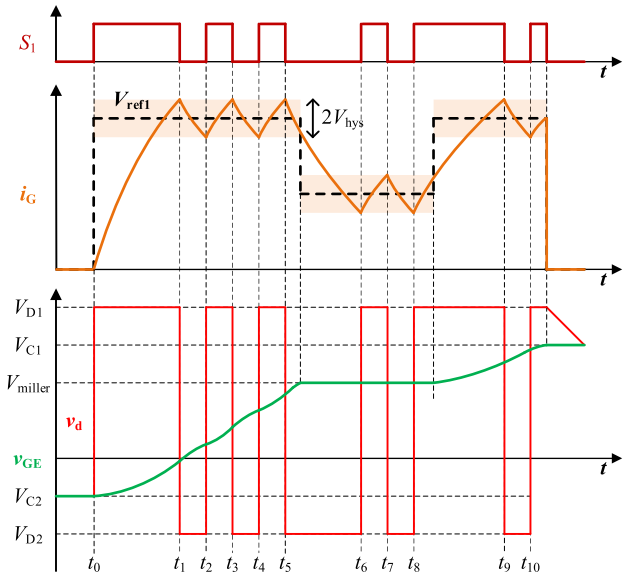


Fig. 2. Driving current control approach.

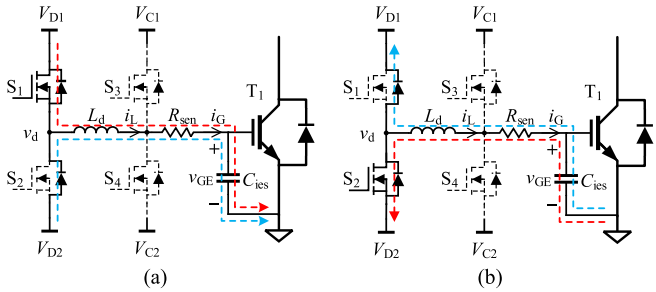


Fig. 3. Equivalent circuits of (a) turn-ON transient and (b) turn-OFF transient.

For the turn-ON transient, $S_1$ turns ON first, as depicted in Fig. 3(a) by the red dashed line, and $C_{ies}$ and $L_d$ resonant with $V_{D1}$. $v_{GE}$ and $i_G$ rise resonantly as shown in Fig. 2 for the $t_0$–$t_1$ stage. Once $v_{iG}$ is greater than $(V_{ref1} + V_{hys})$, $C_1$'s output turns low and $S_1$ turns OFF. As shown in Fig. 3(a) by the blue dashed line, $i_L$ freewheels through $D_2$. $C_{ies}$ and $L_d$ resonant with $V_{D2}$. $v_{GE}$ continues to increase while $i_G$ decreases resonantly in the $t_1$–$t_2$ stage, as shown in Fig. 2. ECSGD remains in this resonant loop until $v_{iG}$ drops below $(V_{ref1} - V_{hys})$. The output of $C_1$ will turn high again to turn ON $S_1$, and the resonant loop will be switched to the one with the red dashed line again. $i_G$ is kept within the hysteresis window of $2V_{ref1}$ by switching $S_1$ ON and OFF.

For the turn-OFF transient, a negative reference $V_{ref2}$ is provided to $C_2$ to control $i_G$ by switching $S_2$ ON and OFF, as shown in Fig. 3(b). By doing so, the proposed ECSGD can easily achieve active driving current control to meet the different switching transient requirements of $T_1$ by giving appropriate $V_{ref1}/V_{ref2}$.

### B. Active Controllability Enhancement

In order to achieve rapid current level adjustment, the driving current transition speed needs to be as fast as possible. However,

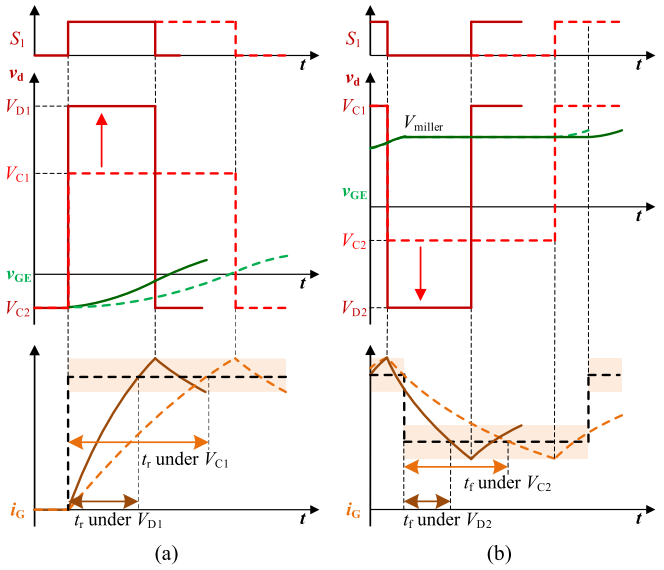


Fig. 4. Active controllability enhancement. (a) Driving current rising. (b) Driving current falling.

the current transition speed, expressed as $di_G/dt$ in the inductor-based CSGD, is limited by the value of the inductor and the driving voltage applied as $di_G/dt = (v_d - v_{GE})/L_d$. This letter proposes a novel method to achieve a boosted supply voltage for the driving arm to accelerate $di_G/dt$ by applying a higher $V_{D1}$ and a lower $V_{D2}$ at the switching transient. Fig. 4 shows the $v_{GE}$ and $i_G$ waveforms when $V_{ref1}$ changes during the turn-ON transient. The rising and falling speeds of $i_G$ are accelerated, as shown by the solid lines utilizing higher $V_{D1}$ and lower $V_{D2}$.

*1) Driving Voltage Boost Method:* In this design, one isolated power supply is required to provide $V_{C1}$ and $V_{C2}$, whereas $V_{D1}$ and $V_{D2}$ are obtained by internal boost and inverting boost functions formed by the full-bridge of the ECSGD without additional components.

*Boost mode:* During $T_1$'s ON-stage, $S_3$ remains ON to clamp $v_{GE}$ at $V_{C1}$, as shown in Fig. 5(a). $L_d$, switch $S_2$, and parasitic diode $D_1$ of $S_1$ will constitute a boost circuit as shown in Fig. 5(b). $L_d$ acts as the boost inductor here, and $V_{D1}$ can be boosted higher than $V_{C1}$. The ON–OFF control strategy is adopted to maintain $V_{D1}$ at the target value.

*Inverting boost mode:* During $T_1$'s OFF-stage, $S_4$ remains ON to clamp $v_{GE}$ at $V_{C2}$, as shown in Fig. 5(c). $L_d$, $S_1$, and parasitic diode $D_2$ of $S_2$ will constitute an inverting boost circuit, as shown in Fig. 5(d), and $V_{D2}$ will be inverted boosted lower than $V_{C2}$. Similar to the boost mode, ON–OFF control is adopted to control the switching of $S_1$.

With the internal driving voltage boosting approach, a much faster driving current transition speed can be achieved in the proposed ECSGD.

*2) Design Considerations:* The duty ratios $D_{S1}$ for $S_1$ and $D_{S2}$ for $S_2$ are selected to ensure that the equivalent boost circuit operates under discontinuous current mode for low switching losses.

The switching frequencies $f_{S1}$ for $S_1$ and $f_{S2}$ for $S_2$ are selected to limit the peak inductor current to avoid the saturation of driving inductor $L_d$.

TABLE I
DESIGN COMPONENTS OF ECSGD

| Components | Model | Parameters |
|---|---|---|
| Resonant switches, $S_1$/$S_2$ | EPC8009 | 65 V/4 A |
| $S_1$/$S_2$ gate driver | LMG1020 | 5 V/5 A |
| Signal transformer | 74930000 | 1:1, 350 $\mu$H |
| Clamping switches, $S_3$/$S_4$ | SH8K25 | 40 V/5.2 A |
| $S_3$/$S_4$ gate driver | LM5109 | 10 V/1 A |
| Driven IGBT, $T_1$ | FF300R17KE3 | 1700 V/300 A |
| Driven SiC MOSFET, $T_1$ | CAS300M12BM2 | 1200 V/300 A |
| Isolated power supply | MGJ6D121505LMC | +15 V/−5 V,6 W |
| Op Amp, $U_1$ | LT1809 | 180 MHz |
| Comparators, $C_1$/$C_2$ | TLV3601 | 325 MHz |

The driving voltage boost effect is also affected by the duration of clamping stages $T_{on\text{-}clamp}$ and $T_{off\text{-}clamp}$. Suppose the energy supplied to $V_{D1}$ and $V_{D2}$ in the ON- and OFF-clamping stages is $E_{VD1}$ and $E_{VD2}$, respectively. The energy released to $T_1$ at one switching transient is $E_{on} = E_{off} = C_{ies}(V_{C1} - V_{C2})^2/2$. If $T_{on\text{-}clamp}$ is short, making $E_{VD1} < E_{on}$, $V_{D1}$ will not be boosted and will be clamped by $V_{C1}$ through diode $D_{P1}$ eventually. The same happens to $V_{D2}$ when $T_{off\text{-}clamp}$ is very short. Under this scenario, the driving voltage is not boosted, but the ECSGD can still work properly.

### C. Whole Working Principle in Power Transistor's One Switching Period

Fig. 6 demonstrates the working principle of the whole switching period of ECSGD. $i_L$ is the current of driving inductor $L_d$. $v_{CE}$ and $i_C$ are the collector–emitter voltage and collector current of $T_1$, respectively. $S_1$–$S_4$ refer to the driving voltages of switches $S_1$–$S_4$.

In the power-up interval, $S_4$ is ON, and $S_1$, $S_2$, and $S_3$ are OFF. $C_{ies}$ is charged to $v_{GE} = V_{C2}$. Two diodes $D_{P1}$ and $D_{P2}$ are added, as shown in Fig. 1, to charge the driving voltages to $V_{D1} = V_{C1} - V_{Dp}$ and $V_{D2} = V_{C2} + V_{Dp}$, where $V_{Dp}$ is the voltage drop of diodes $D_{P1}$ and $D_{P2}$. The working principle of ECSGD can be divided into four subintervals.

*Interval I* [*prior* to $t_{on1}$] is the OFF-clamping state. $S_4$ remains ON. $v_{GE}$ is clamped at $V_{C2}$, and $T_1$ remains OFF. The ECSGD operates in the inverting boost mode until $t_{on1}$, and the $V_{D2}$ is charged lower than $V_{C2}$, as shown in Fig. 6.

*Interval II* [$t_{on1}$–$t_{on3}$] is the turn-ON transient. $S_4$ turns OFF. Different driving currents are applied to adjust the turn-ON behavior of $T_1$ by switching $S_1$ ON and OFF within the hysteresis window under $V_{ref1}$. Once $v_{GE}$ reaches $V_{C1}$ at $t_{on2}$, $S_1$ is turned OFF and $S_3$ is turned ON. $i_L$ commutates from the gate terminal of $T_1$ to $S_3$ and $i_G$ drops to 0 A, as depicted in Fig. 5(a). The energy stored in $L_d$ feeds back to the power supplies $V_{C1}$ and $V_{D2}$ at $t_{on3}$.

*Interval III* [$t_{on3}$–$t_{off1}$] is the ON-clamping state. $S_3$ remains ON. $v_{GE}$ is clamped at $V_{C1}$, and $T_1$ remains ON. The ECSGD operates in the boost mode at this interval, and $V_{D1}$ is charged higher than $V_{C1}$, as shown in Fig. 6 by the dashed line.

*Interval VI* [$t_{off1}$–$t_{off3}$] is the turn-OFF transient. $S_3$ turns OFF. Different driving currents are applied to adjust the turn-OFF

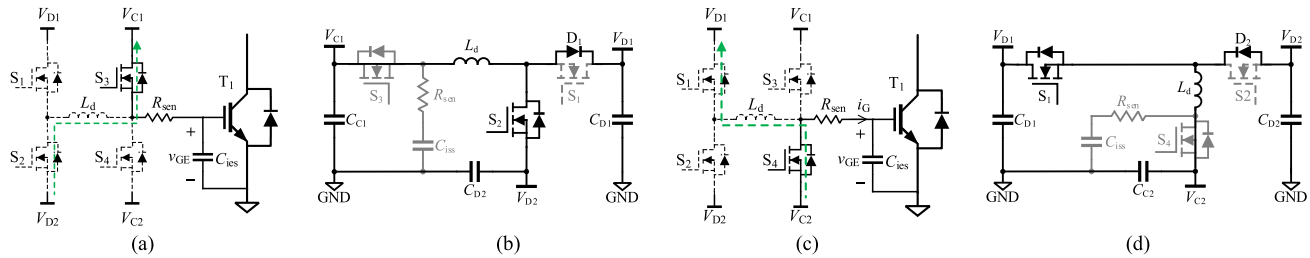


Fig. 5. Driving voltage boost equivalent circuits. (a) ON-clamping stage. (b) Boost mode. (c) OFF-clamping stage. (d) Inverting boost mode.

TABLE II
EXPERIMENTAL RESULTS OF THE ECSGD

| Experiments | IGBT working at 800V/300A | | | SiC MOSFET working at 800V/270A | | |
|---|---|---|---|---|---|---|
| | Case A | Case B | Case C | Case D | Case E | Case F |
| Driving inductance | 2400 nH | 2400 nH | 2400 nH | 1500 nH | 1500 nH | 1500 nH |
| Driving current | Constant at 2 A | Active controlled | Active controlled | Constant at 2 A | Active controlled | Active controlled |
| $V_{D1}$ boost | w/o | w/o | w/ | w/o | w/o | w/ |
| $dv/dt$ for turn-OFF | 3.27 V/ns | 2.83 V/ns | 2.08 V/ns | 9.73 V/ns | 8.92 V/ns | 8.47 V/ns |
| $V_{peak}$ for turn-OFF | 910.8 V | 893.2 V | 862.4 V | 1004 V | 978.8 V | 933.1 V |

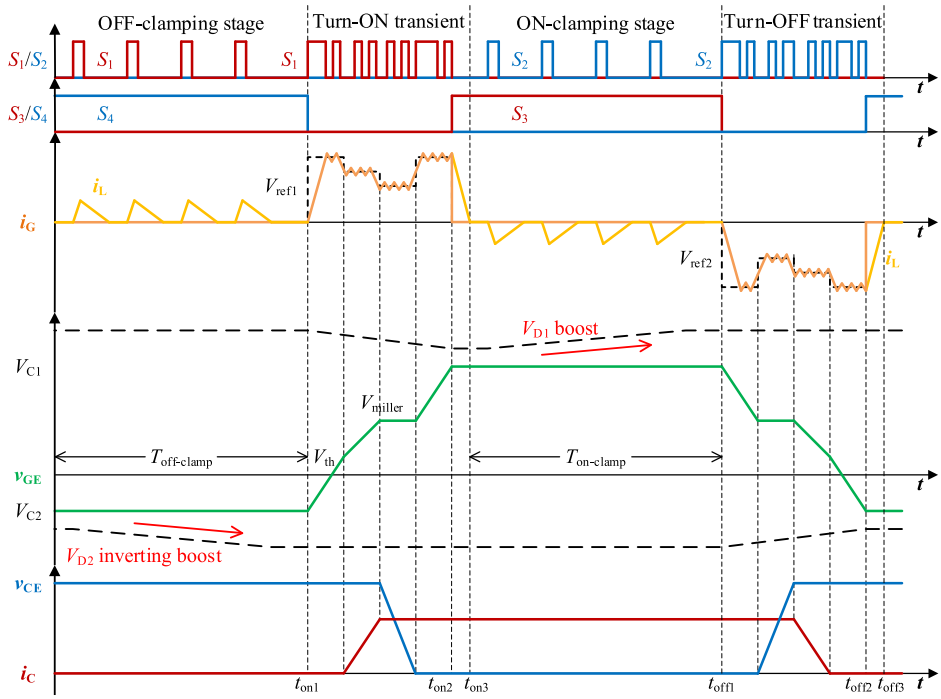


Fig. 6. Working principle of the ECSGD.

behavior of $T_1$ by switching $S_2$ ON and OFF within the hysteresis window under $V_{ref2}$. Once $v_{GE}$ reaches $V_{C2}$ at $t_{off2}$, $S_2$ is turned OFF, and $S_4$ is turned ON to clamp $v_{GE}$ at $V_{C2}$. Inductor current $i_L$ commutates from the gate terminal to $S_4$, and $i_G$ drops to 0 A, as depicted in Fig. 3(d). The energy stored in $L_d$ feeds back to $V_{D1}$ and $V_{C2}$ at $t_{off3}$.

## III. EXPERIMENTAL RESULTS

As shown in Fig. 7, the ECSGD prototype is built with the main components listed in Table I. The ECSGD is powered by an isolated power supply module MGJ6D121505LMC to provide $V_{C1}$ of 15 V and $V_{C2}$ of −5 V. GaN HEMTs of EPC8009 are chosen as the driving switches $S_1$ and $S_2$ for ultra-fast switching speed to achieve nanosecond resonant network alternating. To minimize the drive delay of $S_1$, a tiny signal transformer is used for isolated driving signal transmission, as shown in Fig. 8. The commercial low-side gate driver LMG1020 from TI is adopted. The total driving delay of $S_1$ is only about 5 ns, including the delay of the signal buffer, signal transformer, and drive IC. The clamping arm switches $S_3$ and $S_4$ do not need high-speed

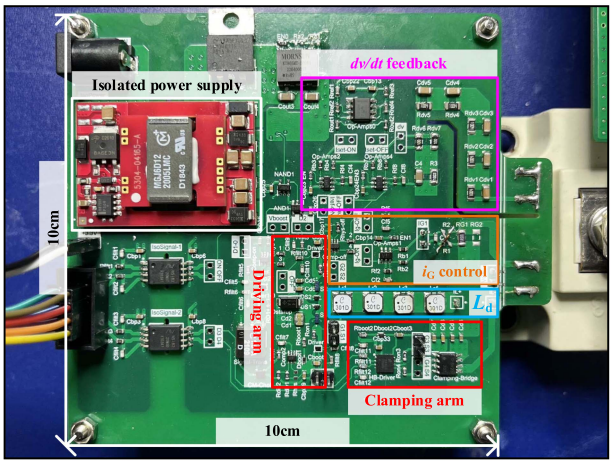


Fig. 7. ECSGD prototype.

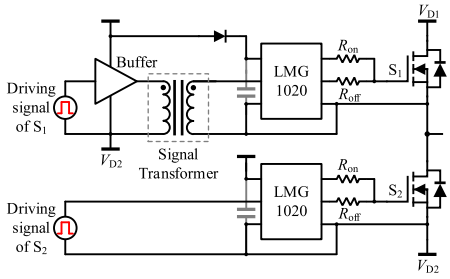


Fig. 8. Driving circuits of $S_1$ and $S_2$.

switching, so Si MOSFETs are used and driven by the half-bridge driver of LM5109.

First, the proposed ECSGD providing constant driving current is shown in Fig. 9 to demonstrate the capability of current control within the hysteresis window of 0.3 A. The switching frequency of the power device is set at 10 kHz. The turn-ON/OFF driving current is stabilized at 2 A/−2 A with a current ripple of 0.3 A. In the ON-clamping internal, the switching frequency $f_{S2}$ and duty ratio $D_{S2}$ of $S_2$ working in the boost mode are set to 2 MHz and 0.1, respectively. $V_{C1}$ is boosted from 15 to 25 V in the first period and then used in the subsequent switching periods. To verify the driving current regulation and enhanced driving voltage, a double pulse test circuit is built using an insulated-gate bipolar transistor (IGBT) module FF300R17KE3. The driving inductor is selected as $L_d = 2400$ nH with four inductors in series. Turn-OFF transients of the IGBT module are plotted in Fig. 10 under three different scenarios with results listed in Table II. The IGBT module operates at 800 V/300 A. ECSGD operates at a constant driving current mode of 2 A in Case A. However, in Case B and Case C, the driving current drops to 0.5 A by active feedback control in IGBT's *dv/dt* stage. The collector–emitter voltage transient rate is detected by the displacement current of the resistor–capacitor network connected at the collector of $T_1$. For Case C, $V_{D1}$ is boosted from 15 to 25 V while the negative driving voltage $V_{D2}$ is kept at −5 V. $i_G$ drops from 2 to 0.5 A in 267 ns in Case B, whereas it is

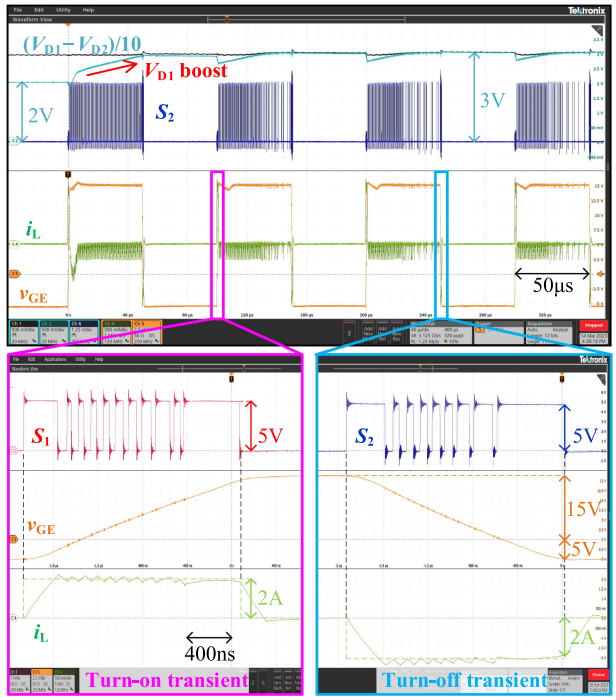


Fig. 9. Waveforms of ECSGD under constant driving current of 2 A/−2 A.

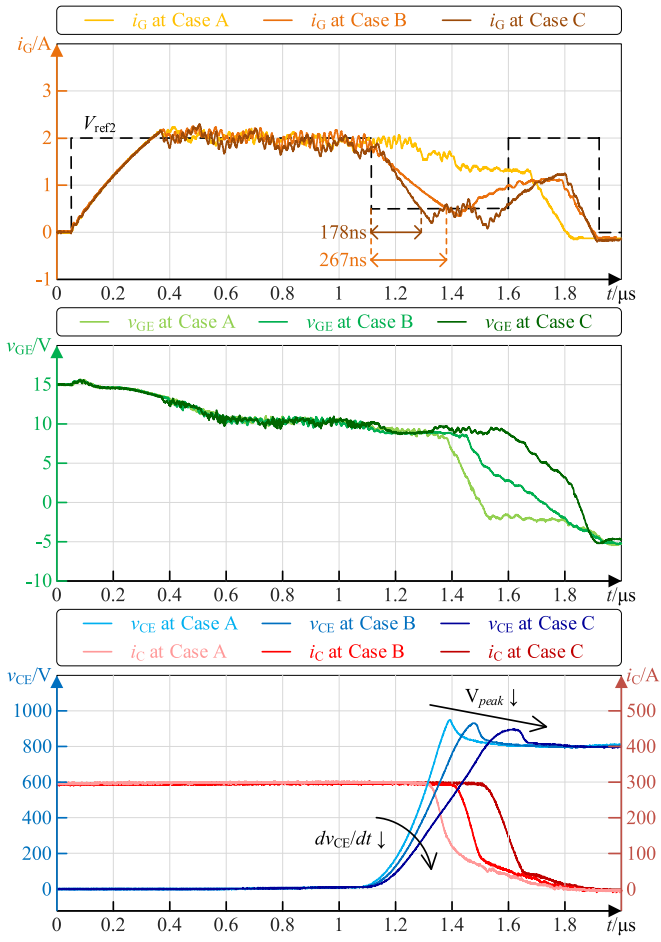


Fig. 10. Turn-OFF transient waveforms of ECSGD driving IGBT.

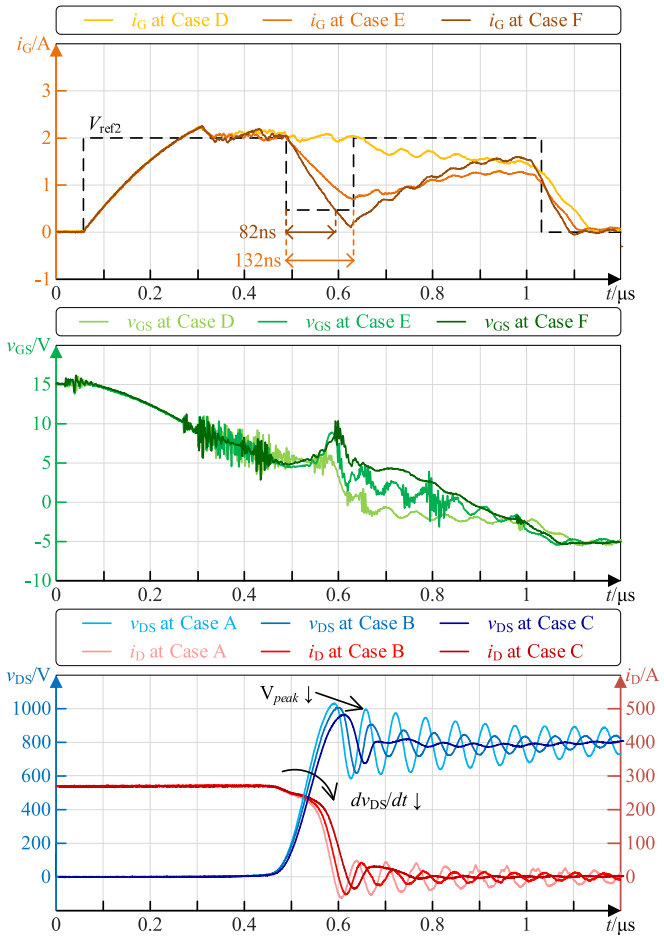


Fig. 11. Turn-OFF transient waveforms of ECSGD driving SiC MOSFET.

shortened to 178 ns in Case C. $dv_{CE}/dt$ is 3.27 V/ns for Case A, 2.83 V/ns for Case B, and 2.08 V/ns for Case C. The peak collector–emitter voltage is 910.8 V for Case A, 893.2 V for Case B, and 862.4 V for Case C. It can be clearly seen that with driving current adjustment and driving voltage boosting, the switching transients of the IGBT module can be well controlled.

The proposed ECSGD is also employed to drive the SiC MOSFET of CAS300M12BM2 under 800 V/270 A, with results listed in Table II. Driving inductance is adjusted to 1500 nH. Case D, Case E, and Case F have the same driving current control comments as Case A, Case B, and Case C, respectively. As plotted in Fig. 11, $i_G$ drops from 2 to 0.5 A within 132 ns in Case E and within 82 ns in Case F. $dv_{DS}/dt$ is 9.73 V/ns for Case D, 8.92 V/ns for Case E, and 8.47 V/ns for Case F. The peak drain–source voltage is 1004 V for Case D, 978.8 V for Case E, and 933.1 V for Case F. The $v_{DS}$ oscillation is suppressed in Case F. The whole turn-OFF transient lasts for 1.1 $\mu$s with $dv_{DS}/dt$ transient of about 100 ns. With the current transient reduced from 132 to 82 ns when $V_{ref2}$ drops, the peak drain–source voltage is reduced by 45.7 V, and the oscillation is well suppressed. The abovementioned experiments demonstrate the potential of ECSGD used in fast SiC devices. When applied to wide bandgap semiconductor devices with fast switching speed, small driving inductor is required for fast driving current slew rate. Furthermore, lower delay devices in a driving current control circuit are needed to keep the driving current fast and precisely controlled.

## IV. Conclusion

A driving current control approach is proposed in this letter for using inductor-based CSGD as an AGD with a simple structure, high control accuracy, and fast response speed. An ECSGD is introduced with boosted driving voltages to accelerate the driving current slew rate. The driving voltages are generated from the clamping voltages by the internal driving voltage boost function. The proposed solution enhances the active driving capability of inductor-based CSGD without additional components. The hysteresis current control approach is first demonstrated with 2 A/−2 A constant driving current control. Furthermore, turn-OFF transients of IGBT and SiC MOSFET are displayed to prove the driving current adjustment for different switching intervals and the benefit of driving voltage enhancement. The duration of the driving current adjustment is shortened by more than 30% when $V_{D1}$ is boosted from 15 to 25 V.

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