A New Predictive Current Control With Reduced Current Tracking Error and Switching Frequency for Multilevel Inverters

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***Abstract*—The forward Euler's integration method is widely used to compute the trajectories of the control variables in conventional predictive current control (PCC) techniques. However, the computational error caused by the forward Euler's method proportionally increases with the sampling time. Hence, the current tracking ability of conventional PCC techniques deteriorates when operating with a large sampling time. Furthermore, the conventional PCC methods produce more switching transitions to reduce the current tracking error, thereby leading to a high switching frequency operation. To overcome these problems, Heun's integration method is proposed for the PCC in this article. The proposed method has predictor and corrector stages to minimize the computational error caused by the large sampling time during the prediction process of the control variables. Thereby, the proposed Heun's method-based PCC techniques produce fewer switching transitions to minimize the current tracking error. Consequently, this results in a decrease in switching frequency. The proposed PCC method is applied to a four-level multilevel inverter (4L-MLI). The discrete-time system models are developed using Heun's integration method to implement the proposed PCC. The working philosophy of the proposed method is demonstrated through the dSPACE/DS1103 controlled 4L-MLI laboratory prototype. The experimental performance of the proposed PCC is compared with that of the conventional PCC in terms of average switching frequency, current tracking error, current harmonic distortion, and transient response time.**

***Index Terms*—Capacitor voltage control, current tracking error, multilevel inverter (MLI), numerical integration method, predictive current control (PCC), switching frequency, total harmonic distortion.**

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I. Introduction

MULTILEVEL inverters (MLIs) are considered the most promising solutions for industrial applications, thanks to their prominent features such as low common-mode voltage (CMV), low dv/dt, and power quality improvement without the need for additional filters [1], [2], [3]. In addition, MLIs offer higher power conversion efficiency due to a low switching frequency operation. However, MLIs require complex control methods to handle multiple control objectives, including the load currents, the dc-bus capacitor voltages, and the floating capacitor voltages [4], [5]. Linear control methods with pulsewidth modulation (PWM) techniques are widely used to handle the control objectives of MLIs [6]. These methods are designed with proportional-integral (PI) regulators in the synchronous dq-reference frame. Moreover, the PI-regulators are connected in a cascaded manner, which significantly affects the system's transient response [7], [8], [9].

Currently, the one-sample ahead prediction-based finite control set model predictive control (FCS-MPC) techniques have gained tremendous popularity owing to their ability to handle the multiple control objectives of the MLIs without compromising the system's transient response [10]. Furthermore, FCS-MPC techniques directly manipulate the device switching states to regulate the control variables along their reference trajectories in MLIs, making the design procedure fairly intuitive and straightforward [11]. In order to achieve low switching frequency (less than 1 kHz) operation, the FCS-MPC techniques need to be executed at a large sampling time [12], [13]. Additionally, the FCS-MPC uses all switching states/switching vectors of the MLI when computing the optimization problem in each sampling interval [14]. Therefore, the computational burden involved in solving the optimization problem exponentially increases with the output levels of the MLI. Hence, a large sampling time is necessary to implement the FCS-MPC in real-time controllers [15], [16].

In order to implement FCS-MPC, the required sampled-data system models are obtained from the discretization of continuous-time (CT) models at a fixed sampling interval [17]. Some of the popular discretization methods used in power electronic applications are zero-order hold (ZOH), matrix factorization, truncated Taylor series, bilinear transformation, backward Euler, and forward Euler methods [18]. The ZOH method

accurately represents the CT models in discrete-time (DT), leading to a superior accuracy level compared with other methods. This method involves the matrix exponential operations, and these matrices are time-varying in nature for linear-time variant (LTV) systems (e.g., electric drives) [19]. Also, the gain matrices have to be updated with their instantaneous values in each sampling interval, leading to a higher implementation complexity. Furthermore, the ZOH method is difficult to apply to higher-order systems due to the matrix exponential operations [20].

Alternatively, the simplified version of the ZOH method; known as matrix factorization, is used to develop the DT models of LTV systems. In this method, the gain matrices are factorized into two parts, one part contains constant parameters, and another part contains time-varying parameters [21]. This philosophy reduces implementation complexity but still has the same drawbacks as the ZOH method. On the contrary, the truncated Taylor series method without matrix exponential operations is developed for LTV systems. In this method, the second-order differential terms are considered along with the first-order terms during the discretization process, thereby the model accuracy can be improved significantly when compared with the matrix factorization method [22]. However, this process increases the complexity of the DT models and often presents nonlinear terms in the DT models, thus, affecting the real-time implementation of the FCS-MPC [23].

To develop DT models suitable for real-time implementation, approximate discretization methods such as bilinear transformation, backward Euler, and forward Euler methods are widely used in power electronic applications [24]. However, the bilinear transformation requires the past values of state variables, whereas the backward Euler method requires the future values of control input variables to discretize the CT models [25]. Thus, these methods are difficult to implement in real-time controllers due to the increase in memory requirements, and their performance is greatly affected by the large sampling time operation.

On the contrary, the forward Euler integration method requires only the present values of state and control input variables, leading to an ease of implementation in real-time controllers [26]. However, the computational error caused by the forward Euler's integration method in the FCS-MPC proportionally increases with the sampling time. Hence, the reference tracking ability of the FCS-MPC greatly deteriorates when operating with a large sampling time. This process also leads to a higher current harmonic distortion under a low switching frequency operation [27]. To overcome the aforementioned problems, the modified Euler's method; known as Heun's method, is highly recommended by Mathematicians and Engineers for the discretization of CT models. This method was first adopted in [28] to control a two-level inverter, in which only a single control objective is considered. However, the above article lacks in-depth information, such as the theoretical philosophy of Heun's method, detailed modeling of multiple objectives with Heun's method and its adoption for MLIs, as well as critical comparison analysis in terms of switching frequency, reference tracking error, and computational burden. Moreover, there are no such studies on Heun's method-based FCS-MPC for MLIs in the literature, which is the main focus of the present work.

Alternatively, the researchers have focused on executing the FCS-MPC techniques with a shorter sampling time to reduce the current tracking error. However, the shorter sampling time leads to a high switching frequency (5 kHz or above) operation of the MLIs [29], which is highly undesirable for high-power applications. Therefore, the objective of switching frequency reduction has been included in the cost function, and it is optimized along with the current control objective [30]. In this framework, the researchers have made a tradeoff between the current tracking error and switching frequency by utilizing weighting factors. Furthermore, it is difficult to achieve a significant reduction in the switching frequency without deteriorating the reference current tracking ability [31]. Also, the computational burden involved in the FCS-MPC optimization process needs to be reduced to achieve a shorter sampling time for the execution in real-time controllers.

To reduce the computational burden, the cascaded/sequential control structure is adopted in the implementation of the MPC algorithm [32], [33]. In this framework, the switching vectors and switching states used in the optimization process are reduced with the help of hysteresis comparators [34], the lowest common-mode voltage (CMV) criterion [35], and the reduction of harmonic voltage criterion [36]. This design process significantly reduces the computational burden, but it negatively affects the system's transient response [37]. However, the simplified MPC techniques can be executed in real-time controllers with a shorter sampling time, leading to a high switching frequency operation of the MLIs. Also, these methods cause large reference tracking errors when compared with the conventional FCS-MPC techniques [38].

From the above literature studies, it is observed that the tradeoffs have been made between the current tracking error, switching frequency, and transient response time when implementing the existing one-sample ahead prediction-based FCS-MPC and simplified MPC techniques. So far, there are no studies in the literature focusing on the improvement of current tracking ability without increasing the switching frequency. It is also identified that the FCS-MPC with a large sampling time is more suitable for high-power MLIs due to its low switching frequency operation and fast transient response. However, it is necessary to address the current tracking and harmonic distortion problems of FCS-MPC caused by a large sampling time.

Considering the aforementioned issues, this article introduces Heun's integration method for the one-sample ahead prediction-based FCS-MPC techniques. The proposed method is designed with predictor and corrector stages, and it takes the average of trajectories obtained in each stage to compute the final trajectory (prediction) of the control variables. Through this philosophy, the computational error in the prediction process of the control variables drastically decreases, leading to an improved reference tracking ability in comparison to Euler's method. Furthermore, the required number of switching transitions produced by Heun's method-based FCS-MPC is reduced, leading to a lower switching frequency.

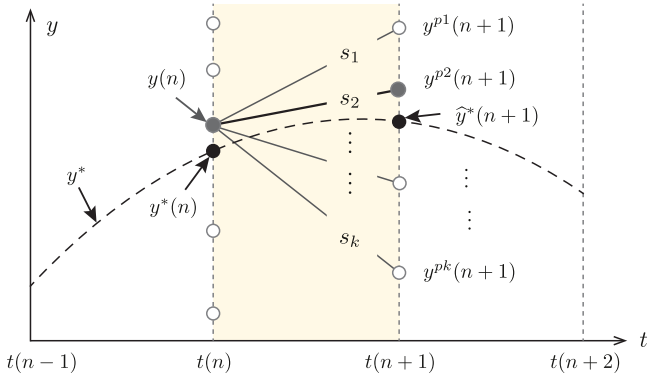

Fig. 1. Philosophy of the conventional PCC with Euler's method.

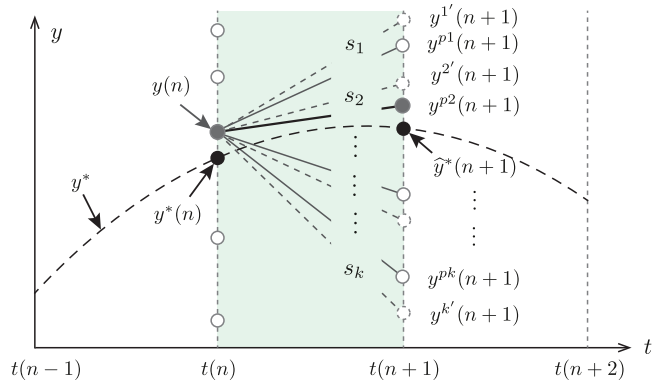

Fig. 2. Philosophy of the proposed PCC with Heun's method.

In this article, Heun's method is used to design the current control-based FCS-MPC [also known as predictive current control (PCC)]. In order to validate its performance, a four-level multilevel inverter (4L-MLI) is considered. To implement the proposed PCC, the DT models of a 4L-MLI are developed using Heun's integration method. These models are used to compute the control variable's trajectory for the finite number of switching states and are assessed based on the selected optimization criteria. Finally, the switching state which gives a favorable system response is chosen and directly applied to the 4L-MLI. The experimental studies are presented to validate the working principle of the proposed PCC. Furthermore, the performance of the proposed PCC is compared with the conventional PCC in terms of average switching frequency, current tracking error, current harmonic distortion, and transient response time.

II. Philosophy of the Proposed Heun's Method

In power electronic systems, the trajectory of the control variable (y) is expressed in CT as follows:

$$\frac{dy}{dt} = f(y(t), u(t)) \tag{1}$$

where u is the input variable.

As the PCC technique is a DT controller, the trajectory given in (1) must be computed in DT with a sampling time of T_s. Euler's integration method is widely used to compute the trajectory due to its simplicity and ease of implementation. According to Euler's method, the trajectory is computed using the known variables ($y(n)$ and $u(n)$) at the start of the sampling interval (n) as shown in Fig. 1 [22]. In power electronic systems, $u(n)$ is the function of switching states and the dc-bus/floating capacitor voltages. Hence, there will be h number of solutions for (1), where h is the number of switching states ($h = 1, 2, \ldots, k$). The general trajectory solution for h switching states at the nth sampling point is given as follows:

$$K_E^h(n) = f\left(y(n), u^h(n)\right). \tag{2}$$

From Fig. 1, the predicted state of the control variable (y^{ph}) at the $(n+1)$th sampling point is given as follows:

$$y^{ph}(n+1) = y(n) + T_s\, K_E^h(n). \tag{3}$$

The obtained predicted states from (3) are used in the PCC optimization problem to select an optimal switching state corresponding to the favorable system response. However, as the sampling time increases, the computed trajectory (K_E^h) at the nth sampling point may not remain constant until it reaches the $(n+1)$th sampling point. This process leads to an error in the computation of the predicted state, which consequently affects the reference tracking ability of the PCC with Euler's method. Furthermore, it requires more switching transitions to minimize the difference between the reference and the predicted variables, leading to a high switching frequency.

In order to address this problem, Heun's integration method is proposed for the PCC in this article and its philosophy is described in Fig. 2. The proposed Heun's method has an additional corrector stage along with a predictor stage to correct the error caused by the large sampling time during the prediction process of the control variables. Thereby, the predicted variables are extremely close to the reference variables, which significantly reduces the error compared with Euler's method. This error can be further minimized with the least number of switching transitions, allowing the proposed PCC to operate at a low switching frequency. According to the principle of Heun's method, the known values at the nth sampling point are used to compute the trajectory (K_H^h) for h switching states in the predictor stage as shown as follows:

$$K_H^h(n) = f\left(y(n), u^h(n)\right). \tag{4}$$

From the solution of trajectory in (4), the virtual state of the control variable ($y^{h'}$) at the $(n+1)$th sampling point is computed as follows:

$$y^{h'}(n+1) = y(n) + T_s\, K_H^h(n). \tag{5}$$

The implementation of the predictor stage follows the same design steps of Euler's method, and it can be seen in (2)–(5). On the other hand, the virtual variables at the $(n+1)$th are used to compute the trajectory in the corrector stage (K_C^h) as shown as follows:

$$K_C^h(n+1) = f\left(y^{h'}(n+1), u^{h'}(n+1)\right). \tag{6}$$

According to Heun's method, the average of trajectories in (4) and (6) is used in the prediction process of the control variable.

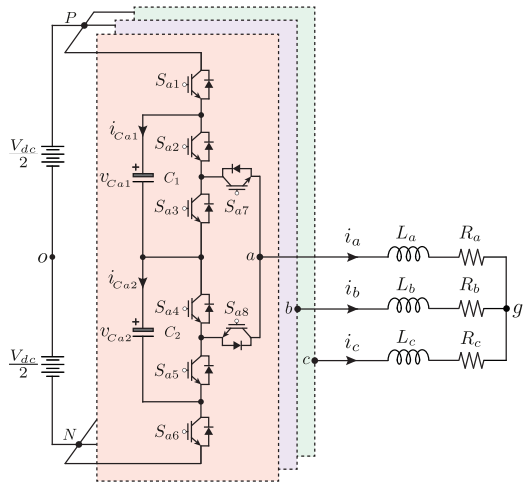

Fig. 3. Circuit configuration of the 4L-MLI.

As a result, the predicted state of the control variable at the $(n+1)$th sampling point is obtained as follows:

$$y^{ph}(n+1) = y(n) + \frac{T_s}{2}\left[K_H^h(n) + K_C^h(n+1)\right]. \tag{7}$$

The obtained predicted states from (7) are used in the optimization problem of the proposed PCC, thereby its reference tracking error will be reduced along with its switching frequency. Additionally, it should be noted that the number of predictions used in the optimization problem of the proposed PCC remains the same as that of the conventional PCC.

III. System Models Development With the Proposed Heun's Integration Method

In this article, a 4L-MLI is selected to study the performance of the proposed Heun's method-based PCC. The circuit configuration of the selected 4L-MLI is illustrated in Fig. 3 [39]. It has two floating capacitors (C_{z1} and C_{z2}) per phase, and their voltages v_{Cz1} and v_{Cz2} are regulated at one-third of the net dc-bus voltage (V_{dc}) under steady-state, where $z \in \{a, b, c\}$ represents the inverter ac terminal. Also, a three-phase passive load consisting of a resistor (R_z) and an inductor (L_z) is connected to the 4L-MLI ac terminals. In order to implement the proposed PCC, the control objectives of the 4L-MLI such as the floating capacitor voltages and the load currents are modeled in the DT domain using the proposed Heun's integration method.

A. Modeling of the Floating Capacitor Voltages

The trajectory of the jth floating capacitor voltage in phase-z is represented in the form of a first-order derivative as shown as follows:

$$\frac{dv_{Czj}}{dt} = \frac{i_{Czj}}{C_{zj}} \tag{8}$$

where $j \in \{1, 2\}$ is the floating capacitor index and C_{zj} is the capacitance value of the jth floating capacitor.

The trajectory given in (8) is solved to predict the floating capacitor voltage at the $(n+1)$th sampling point using the principle of the proposed Heun's integration method given in Section II. Based on this, the virtual state of the floating capacitor voltage at the $(n+1)$th sampling point is given as follows:

$$v'_{Czj}(n+1) = v_{Czj}(n) + T_s\,\frac{i_{Czj}(n)}{C_{zj}}. \tag{9}$$

To compute the virtual state of the capacitor voltage, the current flowing through the floating capacitors (C_{z1} and C_{z2}) at the nth sampling point is needed. From Table I, these currents are expressed in terms of the device switching states and the measured load currents i_z as follows:

$$\begin{aligned} i_{Cz1}(n) &= (S_{z1} - S_{z2})\, i_z(n) \\ i_{Cz2}(n) &= (S_{z5} - S_{z6})\, i_z(n). \end{aligned} \tag{10}$$

Similarly, the virtual state of the floating capacitor currents (i'_{Czj}) at the $(n+1)$th sampling point is expressed as follows:

$$\begin{aligned} i'_{Cz1}(n+1) &= (S_{z1} - S_{z2})\, i'_z(n+1) \\ i'_{Cz2}(n+1) &= (S_{z5} - S_{z6})\, i'_z(n+1) \end{aligned} \tag{11}$$

where i'_z is the virtual state of the load current at the $(n+1)$th sampling point.

According to the proposed Heun's method, the predicted value of the jth floating capacitor voltage (v^p_{Czj}) at the $(n+1)$th sampling point is computed as follows:

$$v^p_{Czj}(n+1) = v_{Czj}(n) + \frac{T_s}{2}\left[\frac{i_{Czj}(n)}{C_{zj}} + \frac{i'_{Czj}(n+1)}{C_{zj}}\right]. \tag{12}$$

B. Modeling of the Load Currents

From the circuit configuration shown in Fig. 3, the trajectory of the phase-z load current is expressed in terms of the load voltage (v_{zg}), the measured load current (i_z), and the load parameters as follows:

$$\frac{di_z}{dt} = \frac{1}{L_z}v_{zg} - \frac{R_z}{L_z}i_z. \tag{13}$$

The virtual state of the load current at the $(n+1)$th sampling point is given as follows:

$$i'_z(n+1) = i_z(n) + T_s\left[\frac{1}{L_z}v_{zg}(n) - \frac{R_z}{L_z}i_z(n)\right]. \tag{14}$$

From the 4L-MLI circuit shown in Fig. 3 and the switching states given in Table I, the load voltage (v_{zg}), the inverter voltage (v_{zo}), and the CMV (v_{go}) are defined at the nth sampling point as follows:

$$\begin{aligned} v_{zg}(n) &= v_{zo}(n) - v_{go}(n) \\ v_{zo}(n) &= S_{z1}V_{dc} + (S_{z2} - S_{z1})\, v_{Cz1}(n) \\ &\quad + (S_{z6} - S_{z5})\, v_{Cz2}(n) - \frac{V_{dc}}{2} \\ v_{go}(n) &= \frac{1}{3}\sum_{z=a,b,c} v_{zo}(n). \end{aligned} \tag{15}$$

TABLE I
4L-MLI SWITCHING STATES AND FLOATING CAPACITOR VOLTAGES VARIATION

S_{z1}	S_{z2}	S_{z3}	S_{z4}	S_{z5}	S_{z6}	S_{z7}	S_{z8}	v_{Cz1}	v_{Cz2}	v_{zN}
0	0	0	0	1	1	0	1	No Change	No Change	0
1	0	0	0	1	0	0	1	Discharge ($i_z \leq 0$) Charge ($i_z > 0$)	Discharge ($i_z \leq 0$) Charge ($i_z > 0$)	$V_{dc} - v_{Cz1} - v_{Cz2} = \frac{V_{dc}}{3}$
0	0	0	1	0	1	0	1	No Change	Charge ($i_z \leq 0$) Discharge ($i_z > 0$)	$v_{Cz2} = \frac{V_{dc}}{3}$
0	0	1	0	0	1	1	0	No Change	Charge ($i_z \leq 0$) Discharge ($i_z > 0$)	$v_{Cz2} = \frac{V_{dc}}{3}$
0	1	0	0	0	1	1	0	Charge ($i_z \leq 0$) Discharge ($i_z > 0$)	Charge ($i_z \leq 0$) Discharge ($i_z > 0$)	$v_{Cz1} + v_{Cz2} = \frac{2V_{dc}}{3}$
1	0	1	0	0	0	1	0	Discharge ($i_z \leq 0$) Charge ($i_z > 0$)	No Change	$V_{dc} - v_{Cz1} = \frac{2V_{dc}}{3}$
1	0	0	1	0	0	0	1	Discharge ($i_z \leq 0$) Charge ($i_z > 0$)	No Change	$V_{dc} - v_{Cz1} = \frac{2V_{dc}}{3}$
1	1	0	0	0	0	1	0	No Change	No Change	V_{dc}

Similarly, the virtual states of the load voltage (v'_{zg}), the inverter voltage (v'_{zo}), and the CMV (v'_{go}) are defined at the $(n+1)$th sampling point as follows:

$$\begin{aligned} v'_{zg}(n+1) &= v'_{zo}(n+1) - v'_{go}(n+1) \\ v'_{zo}(n+1) &= S_{z1}V_{dc} + (S_{z2} - S_{z1})\, v'_{Cz1}(n+1) \\ &\quad + (S_{z6} - S_{z5})\, v'_{Cz2}(n+1) - \frac{V_{dc}}{2} \\ v'_{go}(n+1) &= \frac{1}{3}\sum_{x=a,b,c} v'_{zo}(n+1). \end{aligned} \tag{16}$$

According to the proposed Heun's method, the predicted value of the phase-z load current (i_z^p) at the $(n+1)$th sampling point is computed as follows:

$$\begin{aligned} i_z^p(n+1) &= i_z(n) + \frac{T_s}{2}\left[\frac{1}{L_z}v_{zg}(n) - \frac{R_z}{L_z}i_z(n)\right] \\ &\quad + \frac{T_s}{2}\left[\frac{1}{L_z}v'_{zg}(n+1) - \frac{R_z}{L_z}i'_z(n+1)\right]. \end{aligned} \tag{17}$$

Based on the models given in (9)–(12) and (14)–(17), the proposed PCC can be realized by evaluating the models in each sampling interval.

IV. IMPLEMENTATION OF THE PROPOSED PCC

The design steps involved in the implementation of the proposed PCC are illustrated in Fig. 4, and they are further described as follows:

1) Measure the load currents ($i_z(n)$) and the floating capacitor voltages ($v_{Czj}(n)$) at the nth sampling point.
2) Calculate the reference load currents ($\widehat{i}_z^*(n+1)$) at the $(n+1)$th sampling point, which is obtained from the extrapolation of the reference load currents ($i_z^*(n)$) at the nth sampling point. In this study, the third-order Lagrange extrapolation is used to calculate the $\widehat{i}_z^*(n+1)$, and it is defined as follows [40]:

$$\begin{aligned} \widehat{i}_z^*(n+1) &= 4\, i_z^*(n) - 6\, i_z^*(n-1) + 4\, i_z^*(n-2) \\ &\quad - i_z^*(n-3). \end{aligned} \tag{18}$$

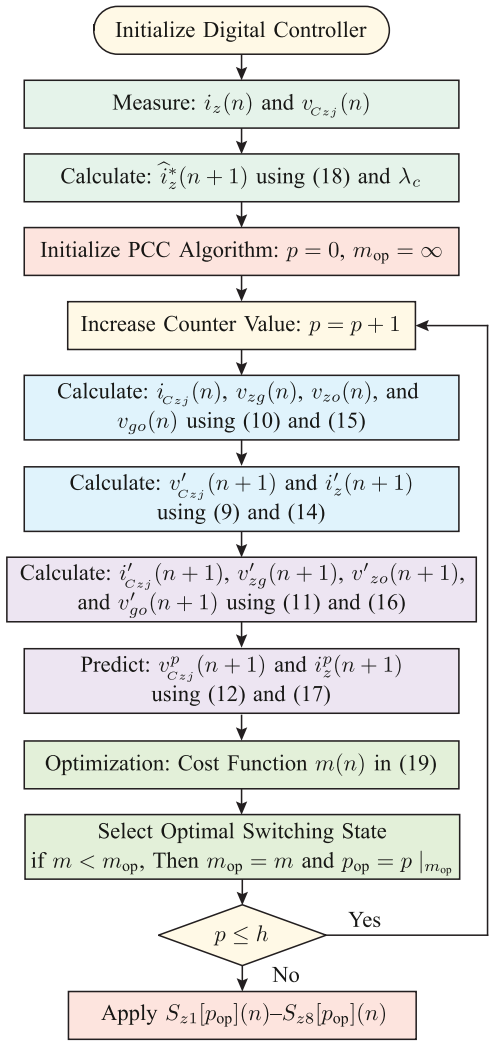

Fig. 4. Design steps of the proposed PCC.

3) Initialize the PCC algorithm with the switching states counter (p) and the optimal cost function value (m_{op}).
4) Calculate the floating capacitor currents ($i_{Czj}(n)$), the load voltage ($v_{zg}(n)$), the inverter voltage ($v_{zo}(n)$), and the CMV ($v_{go}(n)$) for each switching state using (10) and (15) at the nth sampling point.

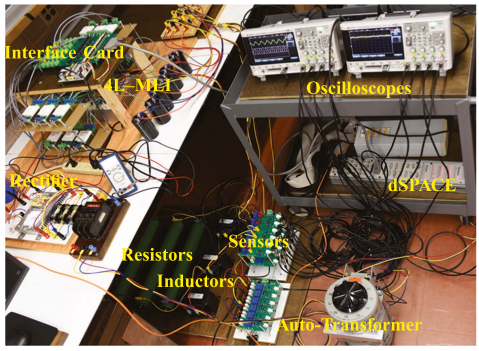

Fig. 5. Image of the 4L-MLI laboratory prototype.

TABLE II
SPECIFICATIONS OF THE LABORATORY PROTOTYPE

Variable Description	Value
Converter power (S_r)	6.5 kVA
Converter voltage (V_r)	208 V (L-L)
Converter current (I_r)	17.68 A (rms)
Rated frequency (f_o)	60 Hz
DC-bus voltage (V_{dc})	270 V
Floating capacitor voltage (V_C)	90 V
Floating capacitor capacitance (C)	2200 μF
Load inductance (L_z)	5 mH
Load resistance (R_z)	5 Ω
Load power factor (PF)	0.94 (lag)

5) Calculate the virtual state of the floating capacitor voltages ($v'_{Czj}(n+1)$) and the load currents ($i'_z(n+1)$) for each switching state using (9) and (14) at the $(n+1)$th sampling point.
6) Calculate the virtual state of the floating capacitor currents ($i'_{Czj}(n+1)$), the load voltage ($v'_{zg}(n+1)$), the inverter voltage ($v'_{zo}(n+1)$), and the CMV ($v'_{go}(n+1)$) for each switching state using (11) and (16) at the $(n+1)$th sampling point.
7) Predict the floating capacitor voltages ($v^p_{Czj}(n+1)$) and the load currents ($i^p_z(n+1)$) for each switching state using (12) and (17) at the $(n+1)$th sampling point.
8) The cost function ($m(n)$) is formulated with the reference and the predicted values of the control objectives such as the floating capacitor voltages and the load currents. The resultant cost function is defined as follows:

$$m(n) = \sum_{z=a,b,c} \left[\hat{i}^*_z(n+1) - i^p_z(n+1)\right]^2 + \lambda_c \sum_{z=a,b,c} \left\{\sum_{j=1}^{2} \left[v^*_{Czj}(n+1) - v_{Czj}(n+1)\right]^2\right\}. \quad (19)$$

In (19), the reference value of the floating capacitor voltage ($v^*_{Czj}(n+1)$) is set to $V_{dc}/3$, whereas λ_c is the weighting factor and its value is calculated using the per-unit method [40].
9) During the cost function optimization process, the redundancy switching states that have the same impact on the FC voltages are eliminated. Therefore, the cost function is evaluated for a total of 216 switching states (h) in the selected 4L-MLI. Finally, the proposed PCC directly selects an optimal switching state corresponding to the lowest cost value and applies it to the 4L-MLI. The optimal switching state ensures the reference current tracking with a reduced error while also regulating each floating capacitor voltage at its reference value.

V. EXPERIMENTAL STUDIES OF THE PROPOSED PCC

The experimental studies are conducted on a 6.5 kVA rated 4L-MLI laboratory prototype as shown in Fig. 5. The design specifications of the laboratory prototype are given in Table II. The 4L-MLI is constructed with Semikron SKM100GB12T4 devices, SKHI22B gate drivers, and EPCOS dc capacitors. The dc-bus of the 4L-MLI is designed with a voltage rating of 270 V, which is generated by using an auto-transformer and a diode-bridge rectifier as shown in Fig. 5. For four-level operation, each floating capacitor in the selected MLI is designed with a rated voltage of 90 V and a capacitance of 2200 μF. The ac terminals of the 4L-MLI are connected to a three-phase passive load, which is formed with a series connection of a 5 Ω resistance and a 5 mH inductance. The selected parameters lead to a load power factor (PF) of 0.94 (lag). The proposed Heun's method-based PCC algorithm is implemented in the dSPACE/DS1103 rapid control platform, and it is executed with a sampling time (T_s) of 200 μs. In this study, the performance of the proposed PCC is assessed in terms of the inverter average switching frequency (f_{sw}), current tracking error (e_i), current harmonic distortion (%THD$_i$), and voltage harmonic distortion (%THD$_v$).

A. Steady-State Operation At Different Power Factors

The proposed PCC performance with the load PFs of 0.94 (lag) and 0.60 (lag) is illustrated in Fig. 6(i) and (ii), respectively. In this study, the proposed PCC is designed with a reference current magnitude (I^*) of 15 A (peak) and a frequency (f_o) of 60 Hz, whereas the reference value of each floating capacitor voltage is set to 90 V. At PF = 0.94, the load is highly resistive, which leads to a higher current ripple as depicted in Fig. 6(i)–(a). These ripples cause an %e_i and %THD$_i$ of 6.02 and 7.60, respectively. Also, the highly resistive load causes a fast change in the load current trajectory and consequently increases the number of switching transitions in the load voltage as depicted in Fig. 6(i)–(b). This operation leads to a f_{sw} of 722 Hz and a %THD$_v$ of 53.43. At the same time, each floating capacitor voltage is regulated at 90 V.

At PF = 0.60, the load is highly inductive and has a filtering effect on the load currents as illustrated in Fig. 6(ii)–(a). Therefore, the load currents have a smaller ripple and are close to sinusoidal. Hence, the %e_i and %THD$_i$ are significantly reduced to 3.88 and 3.44, respectively, compared with that of the 0.94 PF operation. Also, the highly inductive load does not allow a fast change in the load current trajectory, which eliminates the unnecessary switching transitions from the load voltage as

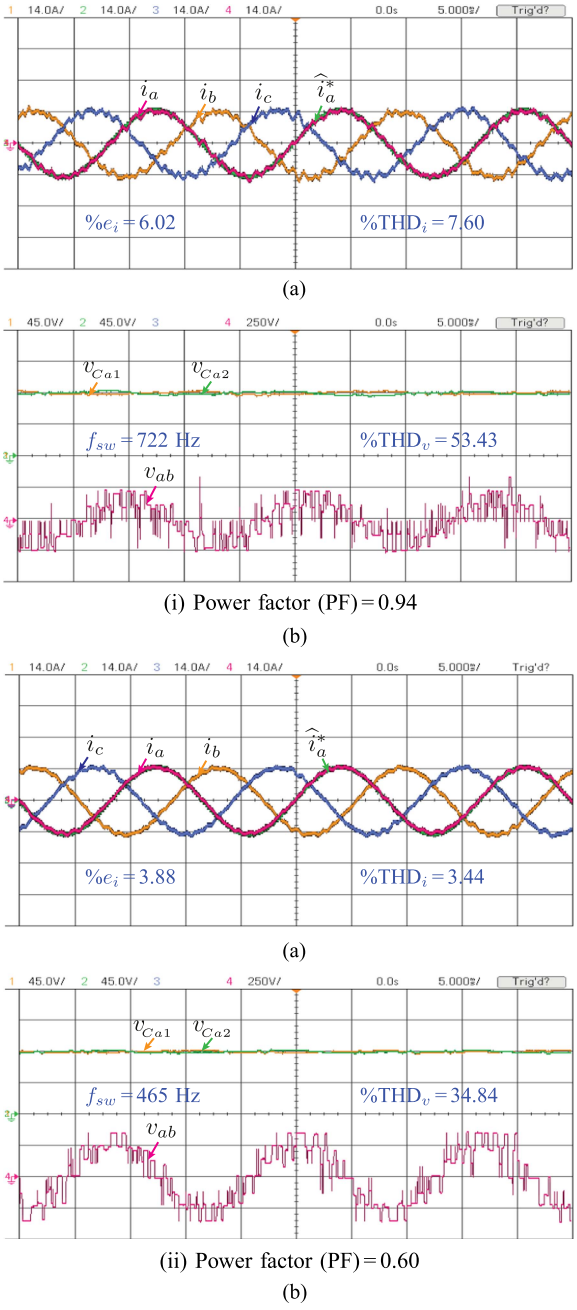

Fig. 6. Steady-state performance at $I^* = 15$ A and $f_o = 60$ Hz. (a) Extrapolated reference and actual load currents. (b) Phase-a floating capacitor voltages and line-line load voltage.

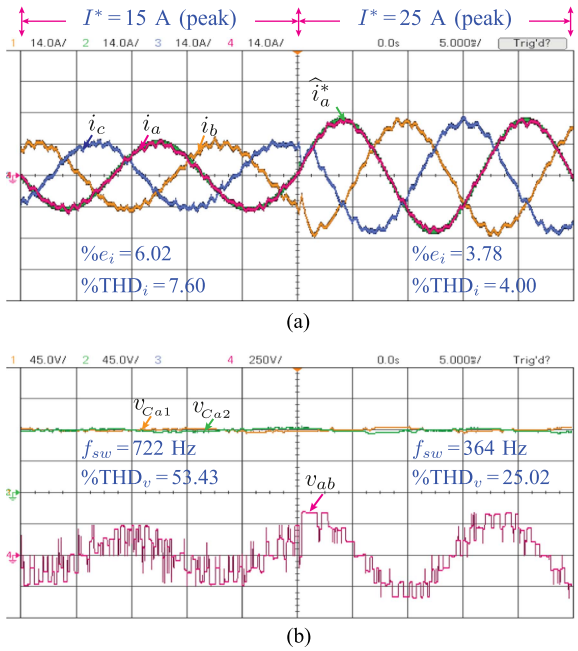

Fig. 7. Current magnitude step change performance at $f_o = 60$ Hz and PF = 0.94. (a) Extrapolated reference and actual load currents. (b) Phase-a floating capacitor voltages and line-line load voltage.

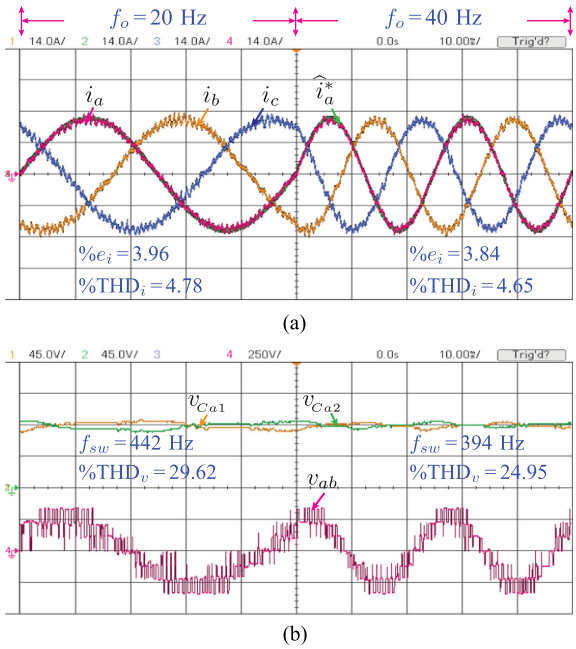

Fig. 8. Frequency magnitude step change performance at $I^* = 25$ A and PF = 0.94. (a) Extrapolated reference and actual load currents. (b) Phase-a floating capacitor voltages and line-line load voltage.

shown in Fig. 6(ii)–(b). Therefore, the f_{sw} and $\%\text{THD}_v$ are reduced to 465 Hz and 34.84, respectively, which are much lower compared with that of the 0.94 PF operation. Furthermore, the proposed PCC regulates the floating capacitor voltages at their rated value of 90 V irrespective of the load PF.

B. Step Change in the Current Magnitude

The proposed PCC performance with a step change in the current magnitude from 15 A (peak) to 25 A (peak) is illustrated in Fig. 7 . Initially, the proposed PCC is designed with a $I^* = 15$ A (peak) and a $f_o = 60$ Hz, whereas the reference value of each floating capacitor voltage is set to 90 V. With the help of the proposed PCC, the 4L-MLI produces three-phase load currents corresponding to their references as illustrated in Fig. 7(a). It is also observed that the actual load currents follow their reference currents with an $\%e_i = 6.02$ and a $\%\text{THD}_i = 7.60$. During this process, the 4L-MLI generates a line-to-line voltage with five steps across its load terminals as illustrated in Fig. 7(b), and it

has a %THD$_v$ = 53.43 and operates at a f_{sw} = 722 Hz. Also, each floating capacitor voltage is regulated at 90 V as depicted in Fig. 7(b).

At t = 25 ms, the step change is applied to the reference current magnitude from 15 (peak) to 25 A (peak). The 4L-MLI load currents (phase-b and -c) take a transient response time of 1.4 ms to reach their references as depicted in Fig. 7(a). Furthermore, the actual load currents track their respective reference currents with an $\%e_i$ = 3.78 at steady-state. These currents have less ripples compared to the measured currents at 15 A operation, leading to a %THD$_i$ = 4.00. During this process, the 4L-MLI produces a line-to-line voltage with seven steps while operating at f_{sw} = 364 Hz as illustrated in Fig. 7(b). The increase in the voltage steps leads to a %THD$_v$ = 25.02. Also, the floating capacitor voltages are tightly regulated at 90 V irrespective of the operating scenarios as depicted in Fig. 7(b). Overall, as the load current increases, the current tracking ability and harmonic performance of the 4L-MLI with the proposed PCC are improved significantly. On the other hand, the average switching frequency decreases, which leads to a large reduction in the switching power losses in the 4L-MLI.

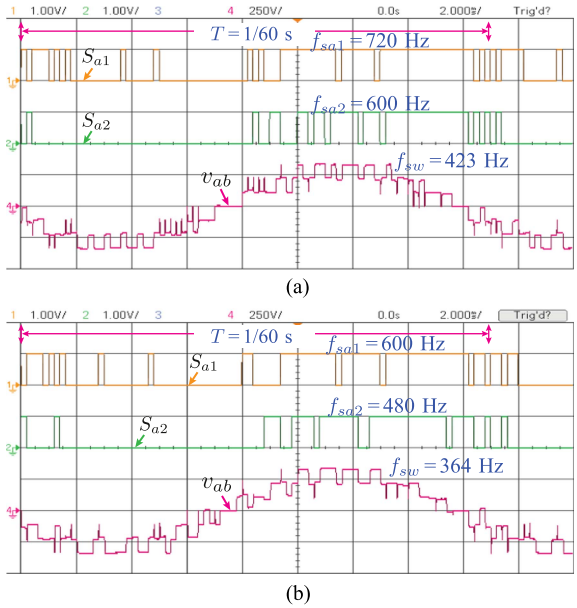

Fig. 9. Switching frequency comparison at I^* = 25 A and f_o = 60 Hz. (a) Conventional PCC. (b) Proposed PCC.

C. Step Change in the Frequency

The proposed PCC performance with a step change in the frequency of the reference current from 20 to 40 Hz is illustrated in Fig. 8. Initially, the proposed PCC is designed with a I^* = 25 A (peak) and a f_o = 20 Hz. The actual load currents follow their references with an $\%e_i$ = 3.96 and have a %THD$_i$ = 4.78 as illustrated in Fig. 8(a). During this process, the 4L-MLI generates a line-to-line voltage with seven steps while operating at a f_{sw} = 442 Hz as illustrated in Fig. 8(b). This operation leads to a %THD$_v$ = 29.62. Also, each floating capacitor voltage is regulated at 90 V with a peak-to-peak (p-p) ripple of 12 V as depicted in Fig. 8(b).

At t = 50 ms, the step change is applied to the frequency of the reference current from 20 to 40 Hz. The 4L-MLI load currents track their references without any time delay as depicted in Fig. 8(a). The $\%e_i$ and %THD$_i$ are reduced to 3.84 and 4.65, respectively, due to the significant reduction in the current ripple compared with the 20 Hz operation. On the other hand, the load voltage has the same number of steps (seven steps), but it has less PWM pulses, leading to a reduction in the f_{sw} to 394 Hz and %THD$_v$ to 24.95 as shown in Fig. 8(b). Furthermore, the floating capacitor voltage ripples are reduced to 8 V (p-p) while maintaining each capacitor average voltage at 90 V as shown in Fig. 8(b). Overall, the current tracking ability and harmonic performance of the 4L-MLI with the proposed PCC are improved along with the rise in the load current frequency. On the other hand, the average switching frequency and floating capacitor voltage ripples of 4L-MLI are decreased with the increase in operating frequency.

VI. Experimental Comparison With the Conventional PCC

The performance of the proposed PCC is compared with the conventional PCC in terms of average switching frequency (f_{sw}), current tracking error ($\%e_i$), current harmonic distortion (%THD$_i$), and transient response time under the identical operating scenarios.

A. Average Switching Frequency

The f_{sw} is an important operational parameter in high-power MLIs as it is an indicator of the switching losses and consequently the converter efficiency. The f_{sw} is estimated in real-time by measuring the switching transitions in the gating signals of all switching devices for 15 fundamental cycles [31], [41]. The f_{sw} performance of the 4L-MLI with the conventional and the proposed PCC at I^* = 25 A (peak) and f_o = 60 Hz is illustrated in Fig. 9(a) and (b), respectively. With the conventional PCC, the devices S_{a1} and S_{a2} gating signals have 12 and 10 switching transitions in one fundamental cycle, which leads to their switching frequencies of 720 and 600 Hz, respectively as illustrated in Fig. 9(a). These switching transitions are reflected in the load voltage resulting in a f_{sw} of 423 Hz.

On the other hand, the devices S_{a1} and S_{a2} are switched at frequencies of 600 and 480 Hz, respectively, with the proposed PCC as illustrated in Fig. 9(b). The reduced switching transitions are clearly reflected in the load voltage resulting in a f_{sw} of 364 Hz, which is 13.95% lower compared to the conventional PCC. The f_{sw} studies with the proposed and the conventional PCC are further conducted at different current magnitudes, and their performances are illustrated in Fig. 10(a). Irrespective of the PCC methods, the f_{sw} increases with the reduction in the current magnitude. However, the f_{sw} is much lower with the proposed PCC compared with the conventional PCC throughout the operating regions as shown in Fig. 10(a). Additionally, the proposed PCC can cause a maximum reduction of 20% in f_{sw} at I^* = 20 A. This reduction in f_{sw} indicates a reduction in switching power losses in the 4L-MLI. Furthermore, the proposed PCC

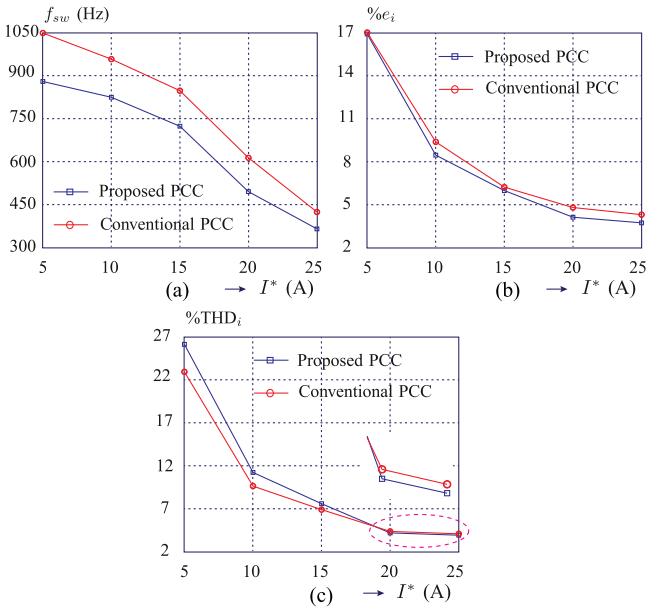

Fig. 10. Experimental performance assessment. (a) Average switching frequency (f_{sw}). (b) Current tracking error ($\%e_i$). (c) Current harmonic distortion ($\%\text{THD}_i$).

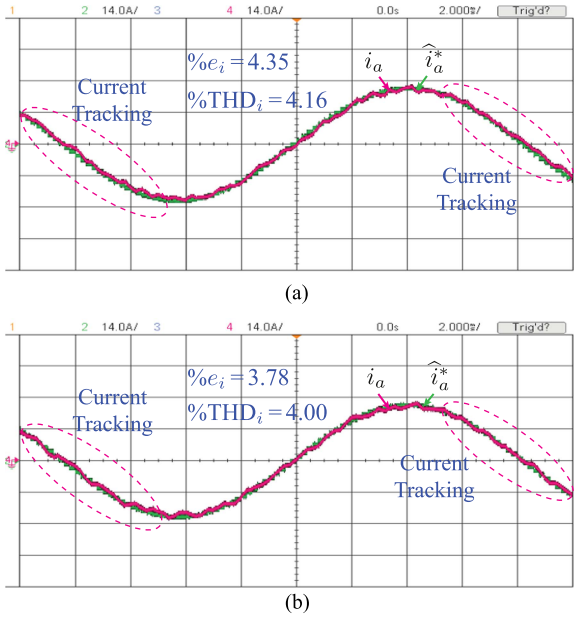

Fig. 11. Current tracking comparison at $I^* = 25$ A and $f_o = 60$ Hz. (a) Conventional PCC. (b) Proposed PCC.

keeps the f_{sw} below 1 kHz throughout the operating regions, making it highly suitable for high-power MLI applications.

B. Current Tracking Error

The $\%e_i$ symbolizes the current tracking performance of the PCC, and it is calculated as per the guidelines given in [31] and [41]. Fig. 11(a) and (b) show the current tracking performance of the conventional and the proposed PCC at $I^* = 25$ A (peak) and $f_o = 60$ Hz, respectively. It is observed that the conventional

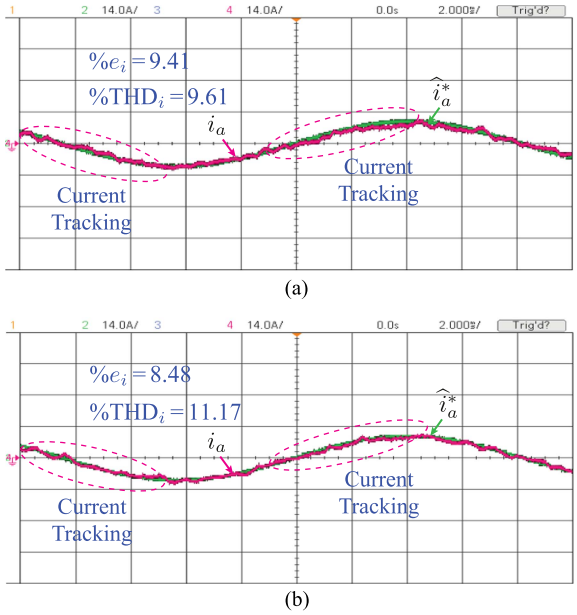

Fig. 12. Current tracking comparison at $I^* = 10$ A and $f_o = 60$ Hz. (a) Conventional PCC. (b) Proposed PCC.

PCC has a tracking problem during the rising and falling slope of the reference current compared with the proposed PCC. This is mainly due to the error caused by Euler's integration method during the prediction process of the control variables. On the contrary, the proposed Heun's integration method minimizes the prediction error, which is clearly reflected in the current tracking performance of the proposed PCC as shown in Fig. 11(b). At $I^* = 25$ A, the proposed PCC has an $\%e_i$ of 3.78, which is 13.10% lower compared with the conventional PCC. Similarly, the current tracking performance at $I^* = 10$ A is depicted in Fig. 12. The results show the proposed PCC reduces the $\%e_i$ by 9.88% compared with the conventional PCC.

The current tracking performance is further evaluated at different current magnitudes and is depicted in Fig. 10(b). The results show the proposed PCC has a lower $\%e_i$ compared with the conventional PCC throughout the operating regions. Also, the proposed PCC causes a maximum reduction of 14% in $\%e_i$ at $I^* = 20$ A. It is worth to note that the proposed PCC has reduced the switching frequency while improving the current tracking performance compared with the conventional PCC as shown in Fig. 10(a).

C. Current Harmonic Distortion

The $\%\text{THD}_i$ of the 4L-MLI with the conventional and the proposed PCC is investigated experimentally at different load current magnitudes, and their performances are depicted in Fig. 10(c). It is observed that the proposed PCC has a superior harmonic performance at higher current magnitudes ($I^* \geq 20$ A) as shown in Fig. 10(c). At $I^* = 20$ A, the proposed PCC has a $\%\text{THD}_i$ of 4.26, which is 3.84% lower compared with that of the conventional PCC. This improvement is obtained while operating at a low switching frequency as shown in Fig. 10(a).

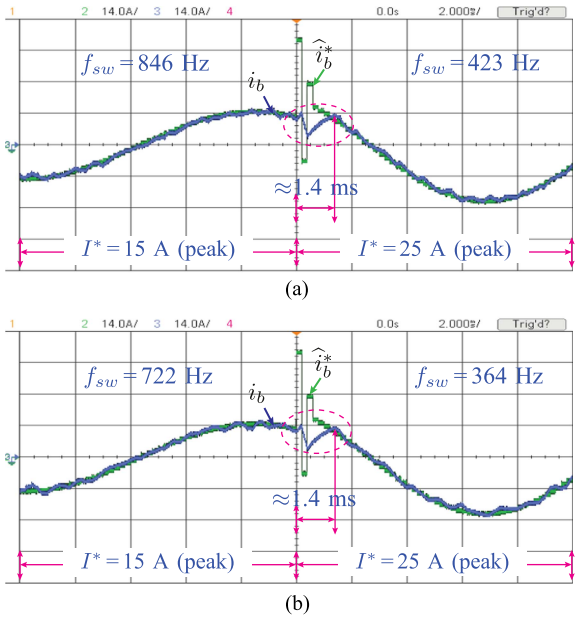

Fig. 13. Transient response comparison at $I^* = 15$ A to $I^* = 25$ A step change. (a) Conventional PCC. (b) Proposed PCC.

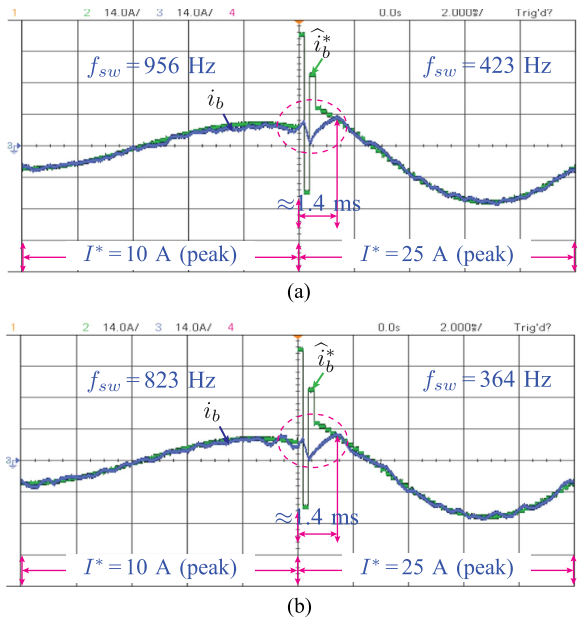

Fig. 14. Transient response comparison at $I^* = 10$ A to $I^* = 25$ A step change. (a) Conventional PCC. (b) Proposed PCC.

However, as the load current decreases ($I^* < 20$ A), the low switching frequency operation significantly affects the %THD$_i$, which leads to a deterioration in the harmonic performance of the proposed PCC as depicted in Fig. 10(c). At $I^* = 5$ A, the proposed PCC has a %THD$_i$ of 25.81, which is 13.85% higher compared with the conventional PCC. However, the increased %THD$_i$ will have a lower impact on the overall load performance due to the light loading conditions.

D. Transient Response Time

The proposed PCC is further compared with the conventional PCC in terms of the time required to reach steady-state operation when subjected to a step change. In this study, a step change of 15 to 25 A is applied in the reference current magnitude and the corresponding results are shown in Fig. 13. It is observed that both the conventional and the proposed PCC required approximately 1.4 ms to reach steady-state current during the step change process as shown in Fig. 13(a) and (b), respectively. However, it is worth to note that the proposed PCC operates at a lower switching frequency while maintaining the same transient response time of 1.4 ms compared with that of the conventional PCC. Similarly, the transient response comparison with the step change from 10 to 25 A is depicted in Fig. 14. The results show the proposed and the conventional PCC have identical response time of 1.4 ms (approx).

E. Computational Burden

In this study, the dSPACE/DS1103 control platform is used to implement the predictive algorithm. The computational burden comprises the time required to complete the ADC sampling, execution of the predictive algorithm, and gating signal generation. Furthermore, the redundancy switching states that gives the same output voltage and have the same impact on the FC voltages are eliminated during the experimental implementation. Thereby, the total number of predictions is limited to 216 only. To complete all tasks without overrun errors, the conventional PCC needs a minimum sampling time of 70 μs (approx), whereas the proposed PCC needs a minimum sampling time of 115 μs (approx). It is observed that the proposed PCC has a higher computational burden due to the additional computations related to the corrector stage. However, with the availability of advanced microcontrollers, it is feasible to handle the computational burden of the proposed PCC. Furthermore, the proposed PCC is targeted to achieve superior performance while operating at a large sampling time.

F. Summary of Relative Comparison

Considering various characteristics, the relative comparison between the conventional and the proposed PCC methods is summarized in Table III. It is observed that the proposed PCC has a low current tracking error and current THD while operating at a low switching frequency when compared with the conventional method. In addition, the proposed PCC maintains the same transient response as that of the conventional PCC, irrespective of the disturbance level. However, the major limitation of the proposed PCC is the computational burden, which is relatively higher compared with the conventional method. Furthermore, the minimization of the proposed PCC computational burden is an interesting research work and will be considered in future research studies.

VII. Conclusion

In this article, a new PCC technique based on Heun's integration method is proposed for high-power MLIs. Also, the

TABLE III
SUMMARY OF RELATIVE COMPARISON

Characteristics	Conventional PCC	Proposed PCC
Discretization method	Forward Euler	Heun's
Prediction horizon	one-sample	one-sample
Current tracking error	High	Low
Switching frequency	High	Low
Current THD	High (for higher values of I)	Low (for higher values of I)
Transient response time	Equal	Equal
Computational burden	Low	High

philosophy and the computational process of the control variables trajectory with the proposed Heun's integration method are introduced. A 4L-MLI is selected to validate the performance of the proposed PCC technique. Also, the DT models of the selected 4L-MLI are developed using Heun's integration method. To demonstrate the performance of the proposed PCC, the experimental studies are conducted on a scaled-down laboratory prototype under steady-state and transient operating conditions. Furthermore, the proposed PCC performance is compared with that of the conventional Euler's method-based PCC in terms of average switching frequency, current tracking error, current harmonic distortion, and transient response time. The results show the proposed PCC: 1) reduced the average switching frequency of the 4L-MLI, leading to a reduction in the switching losses; 2) has a superior current tracking performance (i.e., low current tracking error) while operating at a low switching frequency; 3) produces a less harmonic distortion in the load current (at higher current magnitudes); 4) maintains the same transient response time while operating at a low switching frequency; 5) has a higher computational burden compared with the conventional PCC. Overall, the proposed Heun method-based PCC has a superior performance and is a good fit for high-power MLIs.

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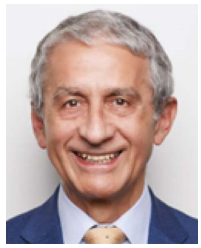

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