






A Multitime-Scale Analytical Model of ZVS Buck Converter

Mengjia Wei , Quanming Luo , *Member, IEEE*, Jian Chen , *Member, IEEE*, Xinyue Zhang, Lujing Xiong, Pengju Sun , *Member, IEEE*, and Xiong Du , *Member, IEEE*

Abstract—This article presents a modeling method to build a complete and accurate multitime-scale analytical model for low-voltage eGaN HEMTs-based zero-voltage switching buck converter with consideration of parasitic inductors, nonlinear junction capacitors, and nonlinear transconductance. The switching steady-state modes and switching transient modes are discussed in detail based on their corresponding equivalent circuits. The state equations of each mode are solved by MATLAB software to obtain the key operating waveforms throughout one switching cycle. Moreover, the established switching steady-state model and switching transient model are numerically merged together through continuous state variables, and then the multitime-scale model for stable operation is formed based on the iterative method. The waveforms and switching energy losses predicted by the model within one switching cycle are compared with the experimental results, respectively, to verify the accuracy of the model. In the end, the dead time is optimized based on the proposed model, and the optimization result is verified to be effective in reducing the switching energy loss through the experiment.

Index Terms—Dead time optimization, multitime-scale modeling method, synchronous buck converter, zero-voltage switching (ZVS).

I. INTRODUCTION

APPLICATIONS, such as data center power supply, battery fast charging, and point of load (POL) converters, require low-voltage and high-current output [1], [2], [3], [4]. The synchronous buck converter is a typical topology for low-voltage conversion, as shown in Fig. 1(a). GaN devices, the novel wide-bandgap semiconductor devices that have emerged in recent years, with low ON-resistance and fast switching speed, are excellent choices for power devices to improve the efficiency,

Manuscript received 31 January 2023; revised 16 April 2023; accepted 27 May 2023. Date of publication 6 June 2023; date of current version 28 July 2023. This work was supported in part by the Natural Science Foundation of China under Grant 52177170 and in part by Sichuan Science and Technology Program under Grant 2023YFH0050. Recommended for publication by Associate Editor M. Ferdowsi. (*Corresponding authors: Quanming Luo; Jian Chen.*)

Mengjia Wei, Quanming Luo, Lujing Xiong, Pengju Sun, and Xiong Du are with the State Key Laboratory of Power Transmission Equipment and System Security and New Technology, School of Electrical Engineering, Chongqing University, Chongqing 400044, China (e-mail: weimengjia1118@163.com; lgm394@cqu.edu.cn; 1093968141@qq.com; spengju@cqu.edu.cn; duxiong@cqu.edu.cn).

Jian Chen is with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu 611756, China (e-mail: chenjian@swjtu.edu.cn).

Xinyue Zhang is with the State Grid Sichuan Electric Power Company, Chengdu 611745, China (e-mail: 20181113088t@cqu.edu.cn).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TPEL.2023.3283294>.

Digital Object Identifier 10.1109/TPEL.2023.3283294

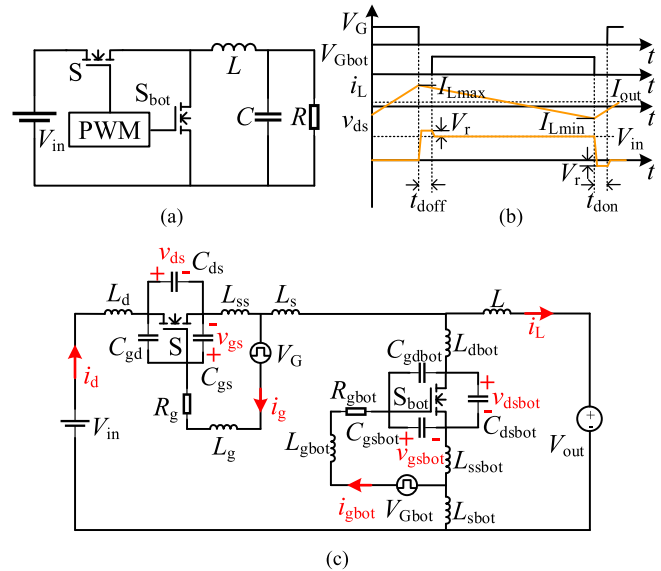


Fig. 1. (a) Single-phase synchronous buck converter. (b) Critical waveforms of the ZVS buck converter. (c) Equivalent circuit of the synchronous buck converter.

switching frequency, and power density of converters [5], [6], [7], [8]. Additionally, the zero-voltage switching (ZVS) of the power device can further reduce the turn-ON losses [9], [10], [11].

The influence of circuit parasitic parameters on switching performance is more and more significant because of the increasing switching frequency. The larger the parasitic inductor exists in the power circuit, the greater the oscillation will be generated, which leads to additional switching loss and impacts the reliability of the converter [12], [13], [14], [15]. Accordingly, the accurate time-domain analytical model is required to predict the losses and then optimize the parameters of the converter.

Existing time-domain models for converters, such as the articles presented in [16] and [17], generally treat the power switch as an ideal switch to simplify the analysis, which reflects significant merits in terms of computational speed. The model is established when the power switch is in ON-state or OFF-state; thus, it is called a switching steady-state model on microsecond time scale (μs time-scale). Based on the ideal model, approximate variation processes of periodic voltage and current can be acquired, and the operating principle of the converter can be analyzed. However, the model shows significant deviations in the

prediction of voltage and current during the switching transient process. Overvoltage and overcurrent protection as well as the precise efficiency optimization design cannot be achieved based on the model. Therefore, a more delicate model to describe the transient behavior of the power switch is indispensable.

In [18], an analytical model of low-voltage eGaN HEMTs with consideration of parasitic inductors of printed circuit board (PCB) traces, nonlinear junction capacitors of switches, and nonlinear transconductance is proposed. The model is established when the power switch is in the process of turning ON or turning OFF; thus, it is called a switching transient model on nanosecond time scale (ns time scale). The waveforms predicted by this model match well with the waveforms of simulation and experiment on ns time scale so that the switching losses can be predicted accurately.

However, the transient model in [18] is not available for operating modes other than continuous conduction mode. In [19], the triangular current-mode converter is modeled, but only the transient processes after the main switch is turned OFF are given, which lacks completeness.

Although the method in [18] and [19] is helpful for establishing the switching transient model in the buck converter, it is not useful to merge the switching steady-state and switching transient models. So far, we have not found any literature that presents a merging method.

Accordingly, a multitime-scale modeling method in the time domain is proposed in this article by taking the ZVS buck converter with low-voltage eGaN HEMTs as an example, which is also a good reference for other converters. The model provides the possibility to predict the converter losses and optimize the dead time accurately [18], [20]. And the primary contribution of this article is reflected in the following three aspects.

- 1) A complete and accurate multitime-scale modeling method is formed by merging the switching steady-state model and the switching transient model, which is different from the common steady-state converter model without considering the switching transient process.
- 2) The proposed analytical model can predict energy losses accurately; thus, the efficiency optimization design can be achieved. The dead time can be determined optimally according to the proposed model to further improve the efficiency.
- 3) Taking into account the variation of inductor current during the switching transition, a more accurate switching transient model is achieved for the ZVS buck converter, while the accurate switching transient models developed in previous articles are based on hard switching.

The rest of this article is organized as follows. Section II introduces the ZVS buck converter, the definition of parasitic parameters, and the method for obtaining parameters. In Section III, the switching steady-state model is developed and analyzed. In Section IV, the behaviors of the power switches during the turn-ON and turn-OFF transient processes are discussed in detail to derive the transient model. A complete multitime-scale modeling method is presented in Section V. The experimental results prove the accuracy of the proposed model in Section VI.

The dead time optimization based on the proposed model is performed in Section VII. Finally, Section VIII concludes this article.

II. BASIS OF THE ANALYTICAL MODEL

Fig. 1(a) shows the topology of the synchronous buck converter. The upper main switch S and the lower synchronous switch S_{bot} form a half-bridge structure with complementary conduction. It is worth noting that eGaN HEMTs have no p-n junctions, as distinguished from MOSFETs [6]. Nevertheless, eGaN HEMTs can conduct reverse current without gate voltage due to the symmetrical structure and bidirectional conducting channels, similar to the body diode of MOSFETs. To simplify the following analysis, we use the concept of a body diode without a reverse recovery process for eGaN HEMTs.

The critical waveforms of the ZVS buck converter are shown in Fig. 1(b). It is notable that the discussed ZVS is for S , as by default, the S_{bot} can definitely implement ZVS in the synchronous buck converter. The working principle of ZVS is described in [21] based on the switching waveforms, and the condition of complete ZVS is given in [4] based on the relationship between the energy stored in the output inductor and the energy required to discharge the output capacitors of the two switches.

Considering parasitic inductors and nonlinear capacitors, the equivalent circuit of the synchronous buck converter is shown in Fig. 1(c), where the directions of both voltage and current are the assumed reference directions. The output voltage can be regarded as a constant voltage source because the output voltage ripple is generally small enough. It can be seen that the drain inductors L_d and L_{dbot} , source inductors L_s and L_{sbot} , and common source inductors L_{ss} and L_{ssbot} form the power loop inductor L_{loop} , while the drive loop inductors consist of L_{ss} and L_{ssbot} together with gate inductors L_g and L_{gbot} . Notably, L_{ss} equals zero when the Kelvin connection of the device is applied, and the parasitic inductor of the Kelvin source is contained in L_g . The drain-source capacitor C_{ds} , gate-drain capacitor C_{gd} , and gate-source capacitor C_{gs} are the nonlinear junction capacitors of eGaN HEMTs.

Using Maxwell Q3D simulation, the parasitic inductors of a specific circuit can be extracted. And the nonlinear junction capacitors, the transfer characteristic between channel current i_{ch} and gate-source voltage v_{gs} , as well as the reverse conduction characteristic between i_{ch} and gate-drain voltage v_{gd} can be estimated from the datasheet with a curve fitting method [18].

III. SWITCHING STEADY-STATE MODEL

The switching steady states include the state of S ON and S_{bot} OFF and the state of S_{bot} ON and S OFF. The two steady states are modeled separately as follows.

A. State of S ON and S_{bot} OFF

The equivalent circuit for this steady-state mode is shown in Fig. 2(a). The conducted switch S is represented by the ON-resistance R_{dson} , and the nonconducted switch S_{bot} is represented by the output capacitor C_{ossbot} . During this period, the

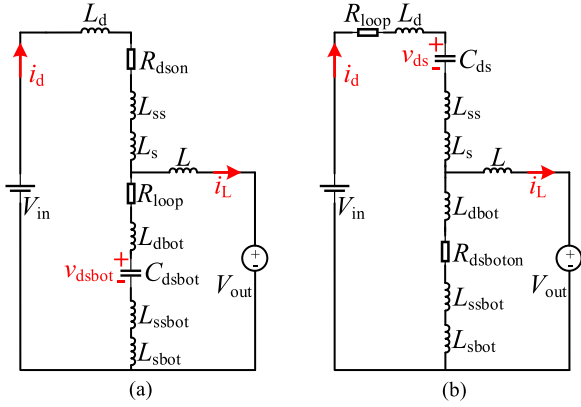


Fig. 2. (a) Equivalent circuit of the state of S ON and S_{bot} OFF. (b) Equivalent circuit of the state of S_{bot} ON and S OFF.

loop inductor L_{loop} resonates with the output capacitor C_{ossbot} , leading to a high-frequency damping resistor R_{loop} that can be extracted using Maxwell Q3D software.

The key to solving a circuit is to acquire the variation process of the independent state variables since all of the circuit variables can be expressed in terms of the state variables. As shown in Fig. 2(a), the independent state variables of this mode are the drain current i_d , drain-source voltage v_{dsbot} , and inductor current i_L , expressed in matrix format as $\mathbf{X} = [i_d \ v_{dsbot} \ i_L]^T$. Based on the equivalent circuit, the state equations can be obtained as follows:

$$C_{ossbot} \frac{dv_{dsbot}}{dt} = i_d - i_L \quad (1)$$

$$\begin{aligned} V_{in} &= (L_p + L_{ss}) \frac{di_d}{dt} + (L_{pbot} + L_{ssbot}) \frac{d(i_d - i_L)}{dt} \\ &\quad + (i_d - i_L) R_{loop} + i_d R_{ds(on)} + v_{dsbot} \\ &= L_{loop} \frac{di_d}{dt} - (L_{pbot} + L_{ssbot}) \frac{di_L}{dt} + (i_d - i_L) R_{loop} \\ &\quad + i_d R_{ds(on)} + v_{dsbot} \end{aligned} \quad (2)$$

$$\begin{aligned} V_{out} &= (L_{pbot} + L_{ssbot}) \frac{d(i_d - i_L)}{dt} - L \frac{di_L}{dt} + v_{dsbot} \\ &\quad + (i_d - i_L) R_{loop}. \end{aligned} \quad (3)$$

To simplify the state equations, set $L_p = L_d + L_s$, $L_{pbot} = L_{dbot} + L_{sbot}$, and $L_{loop} = L_p + L_{ss} + L_{pbot} + L_{ssbot}$. This steady-state mode ends when the drive voltage of S is removed.

B. State of S_{bot} ON and S OFF

The equivalent circuit for this steady-state mode is shown in Fig. 2(b). The independent state variables are $\mathbf{X} = [i_d \ v_{ds} \ i_L]^T$. Similar to the analysis of the state of S ON and S_{bot} OFF, the state equations can be obtained as follows:

$$C_{oss} \frac{dv_{ds}}{dt} = i_d \quad (4)$$

$$V_{in} = L_{loop} \frac{di_d}{dt} - (L_{pbot} + L_{ssbot}) \frac{di_L}{dt} + v_{ds}$$

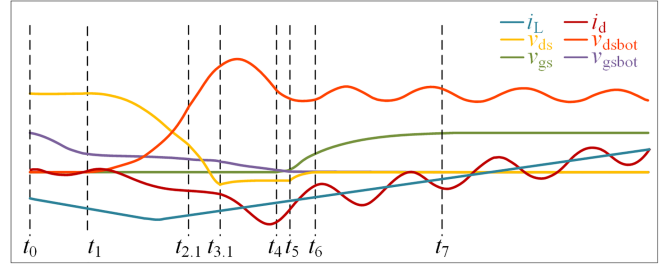


Fig. 3. Typical waveforms during the turn-ON transition of S .

$$+ (i_d - i_L) R_{dsbot(on)} + i_d R_{loop} \quad (5)$$

$$\begin{aligned} V_{out} &= (L_{pbot} + L_{ssbot}) \frac{d(i_d - i_L)}{dt} - L \frac{di_L}{dt} \\ &\quad + (i_d - i_L) R_{dsbot(on)}. \end{aligned} \quad (6)$$

This steady-state mode ends when the drive voltage of S_{bot} is removed.

IV. SWITCHING TRANSIENT MODEL

There are two parts to the switching transient processes. One is the turn-ON transient, that is, the transition process of S_{bot} turns OFF and S turns ON. The other is the turn-OFF transient, that is, the transition process of S turns OFF and S_{bot} turns ON. In this article, the two switching transient processes are divided into seven submodes, respectively, according to the variation of the critical circuit states. Based on the equivalent circuits of each submode, the state equations can be derived and solved to acquire the time-domain solutions of the state variables. It is worth noting that the final values of the state variables in the previous mode are used as the initial values of the next mode due to the continuity, and the boundary conditions between each submode depend on the variation of the state variables.

A. Transient Model During Turn-ON Transition

Typical waveforms during the turn-ON transition are shown in Fig. 3. It can be seen that the inductor current i_L is negative at the beginning of this process for the ZVS buck converter. Each submode is analyzed in detail below based on the equivalent circuits in Fig. 4.

1) *Mode I. S_{bot} Turn-OFF Delay Period [$t_0 \leq t \leq t_1$]:* Fig. 4(a) shows the equivalent circuit of this mode. At t_0 , the drive voltage V_{Gbot} is set to 0 V, and the gate current i_{gbot} starts to discharge C_{issbot} , which causes the gate-source voltage v_{gsbot} to drop. The independent state variables of this mode are $\mathbf{X} = [i_d \ v_{ds} \ v_{gsbot} \ i_{gbot} \ i_L]^T$. The state equations can be obtained from (4) and (7)–(10)

$$i_{gbot} = C_{issbot} \frac{dv_{gsbot}}{dt} \quad (7)$$

$$\begin{aligned} 0 &= (L_{gbot} + L_{ssbot}) \frac{di_{gbot}}{dt} + L_{ssbot} \frac{d(i_d - i_L)}{dt} \\ &\quad + v_{gsbot} + R_{gbot} i_{gbot} \end{aligned} \quad (8)$$

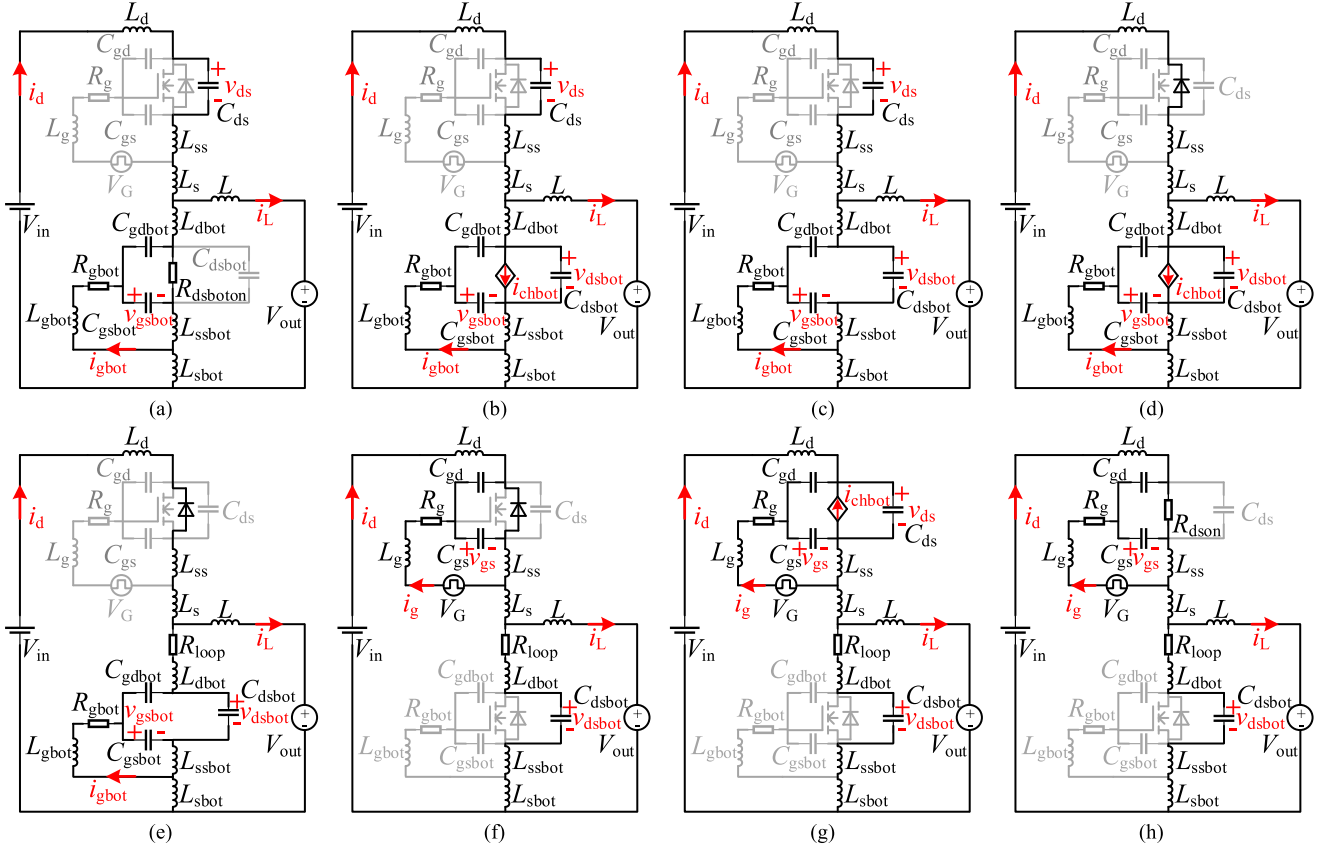


Fig. 4. Equivalent circuits during turn-ON transition of S . (a) Mode I. (b) Mode II. (c) Case 1 of mode III. (d) Case 2 of mode III. (e) Mode IV. (f) Mode V. (g) Mode VI. (h) Mode VII.

$$V_{in} = L_{loop} \frac{di_d}{dt} - (L_{pbot} + L_{ssbot}) \frac{di_L}{dt} + L_{ssbot} \frac{di_{gbot}}{dt} + v_{ds} + (i_d - i_L) R_{dsboton} \quad (9)$$

$$V_{out} = (L_{pbot} + L_{ssbot}) \frac{d(i_d - i_L)}{dt} + L_{ssbot} \frac{di_{gbot}}{dt} - L \frac{di_L}{dt} + (i_d - i_L) R_{dsboton}. \quad (10)$$

This mode ends when v_{gsbot} drops to the value

$$v_{gsbot} = V_{gsbotth} + \frac{i_d - i_L}{g_{fs}} \quad (11)$$

where g_{fs} is the slope of the transfer characteristic curve fitted from the datasheet, i.e., the nonlinear transconductance of eGaN HEMTs.

2) *Mode II. S_{bot} Turn-OFF Transition Period $[t_1 \leq t \leq t_{2.1}]$ or $[t_1 \leq t \leq t_{2.2}]$:* Fig. 4(b) shows the equivalent circuit of this mode. At t_1 , the channel current i_{chbot} begins to be controlled by v_{gsbot} as the transfer characteristic, and S_{bot} is regarded as voltage-controlled current source (VCCS). During this period, the difference between $i_d - i_L$ and i_{chbot} charges C_{ossbot} , leading to an increase of v_{dsbot} , and the current i_d discharges C_{oss} , leading to a decrease of v_{ds} . The independent state variables of this mode are $\mathbf{X} = [i_d \ v_{ds} \ v_{dsbot} \ v_{gsbot} \ i_{gbot} \ i_L]^T$. The state equations can be obtained from (4), (8)–(10), and (12)

and (13), where $(i_d - i_L)R_{dsboton}$ in (9) and (10) is replaced by v_{dsbot}

$$C_{ossbot} \frac{dv_{dsbot}}{dt} - C_{gdbot} \frac{dv_{gsbot}}{dt} + i_{chbot} = i_d - i_L \quad (12)$$

$$i_{gbot} = C_{issbot} \frac{dv_{gsbot}}{dt} - C_{gdbot} \frac{dv_{dsbot}}{dt}. \quad (13)$$

This mode ends when v_{gsbot} drops to $V_{gsbotth}$ or v_{ds} drops to $-V_r$ [22].

3) *Mode III. S_{bot} Turn-OFF Remaining Transition Period $[t_{2.1} \leq t \leq t_{3.1}]$ or $[t_{2.2} \leq t \leq t_{3.2}]$:*

Case 1 $[t_{2.1} \leq t \leq t_{3.1}]$: v_{gsbot} drops to $V_{gsbotth}$ before v_{ds} drops to $-V_r$. At $t_{2.1}$, the channel of S_{bot} stops conducting, as shown in Fig. 4(c). During this period, v_{dsbot} is rising and v_{ds} is falling. The independent state variables of this mode are the same as Mode II. The state equations can be obtained from (4), (8)–(10), and (12) and (13), where $(i_d - i_L) \cdot R_{dsboton}$ in (9) and (10) is replaced by v_{dsbot} and i_{chbot} in (12) equals zero.

This mode ends when v_{ds} drops to $-V_r$.

Case 2 $[t_{2.2} \leq t \leq t_{3.2}]$: v_{ds} drops to $-V_r$ before v_{gsbot} drops to $V_{gsbotth}$. At $t_{2.2}$, the equivalent diode of S starts to conduct, as shown in Fig. 4(d). The independent state variables of this mode are $\mathbf{X} = [i_d \ v_{dsbot} \ v_{gsbot} \ i_{gbot} \ i_L]^T$. The state equations can be obtained from (8), (10), and (12)–(14), where

$(i_d - i_L) \cdot R_{dsboton}$ in (10) is replaced by v_{dsbot}

$$V_{in} = L_{loop} \frac{di_d}{dt} - (L_{pbot} + L_{ssbot}) \frac{di_L}{dt} + L_{ssbot} \frac{di_{gbot}}{dt} - V_r + v_{dsbot}. \quad (14)$$

This mode ends when v_{gsbot} drops to $V_{gsbotth}$.

4) *Mode IV. Dead Time Duration Period* [$t_{3.1} \leq t \leq t_4$] or [$t_{3.2} \leq t \leq t_4$]: Fig. 4(e) shows the equivalent circuit of this mode. At $t_{3.1}$ or $t_{3.2}$, S_{bot} is entirely OFF and i_L flows through the equivalent diode of S . During this period, L_{loop} resonates with C_{ossbot} , leading to a high-frequency damping resistor R_{loop} . The independent state variables of this mode are the same as in case 2 of Mode III. The state equations can be obtained from (8), (12), (13), (15), and (16), where i_{chbot} in (12) equals zero

$$V_{in} = L_{loop} \frac{di_d}{dt} - (L_{pbot} + L_{ssbot}) \frac{di_L}{dt} + L_{ssbot} \frac{di_{gbot}}{dt} - V_r + v_{dsbot} + (i_d - i_L) R_{loop} \quad (15)$$

$$V_{out} = (L_{pbot} + L_{ssbot}) \frac{d(i_d - i_L)}{dt} + L_{ssbot} \frac{di_{gbot}}{dt} - L \frac{di_L}{dt} + v_{dsbot} + (i_d - i_L) R_{loop}. \quad (16)$$

This mode ends when the drive voltage V_G is applied.

5) *Mode V. S Turn-ON Delay Period* [$t_4 \leq t \leq t_5$]: Fig. 4(f) shows the equivalent circuit of this mode. At t_4 , V_G is applied and v_{gs} rises. And i_L still flows through the equivalent diode of S . The independent state variables of this mode are $\mathbf{X} = [i_d \ v_{dsbot} \ v_{gs} \ i_g \ i_L]^T$. The state equations can be obtained from (1), (3), and (17)–(19)

$$i_g = C_{iss} \frac{dv_{gs}}{dt} \quad (17)$$

$$V_G = (L_g + L_{ss}) \frac{di_g}{dt} + L_{ss} \frac{di_d}{dt} + v_{gs} + R_g i_g \quad (18)$$

$$V_{in} = L_{loop} \frac{di_d}{dt} + L_{ss} \frac{di_g}{dt} - (L_{pbot} + L_{ssbot}) \frac{di_L}{dt} - V_r + v_{dsbot} + (i_d - i_L) R_{loop}. \quad (19)$$

On account of the reverse conduction of S in this mode, eGaN HEMTs follow the reverse conduction characteristic. This mode ends when v_{gd} rises to the threshold voltage V_{gdth} .

6) *Mode VI. S Turn-ON Transition Period* [$t_5 \leq t \leq t_6$]: Fig. 4(g) shows the equivalent circuit of this mode. At t_5 , i_{ch} begins to be controlled by v_{gd} as the reverse conduction characteristic, and S is regarded as VCCS. During this period, the current $i_d + i_{ch}$ charges C_{oss} , leading to an increase in v_{ds} . The independent state variables of this mode are $\mathbf{X} = [i_d \ v_{ds} \ v_{dsbot} \ v_{gs} \ i_g \ i_L]^T$. The state equations can be obtained from (1), (3), and (18)–(21), where $-V_r$ in (19) is replaced by v_{ds}

$$C_{oss} \frac{dv_{ds}}{dt} - C_{gd} \frac{dv_{gs}}{dt} - i_{ch} = i_d \quad (20)$$

$$i_g = C_{iss} \frac{dv_{gs}}{dt} - C_{gd} \frac{dv_{ds}}{dt}. \quad (21)$$

This mode ends when v_{ds} rises from $-V_r$ to zero.

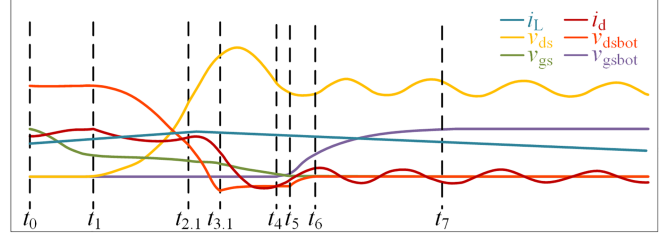


Fig. 5. Typical waveforms during the turn-OFF transition of S .

7) *Mode VII. Gate Charge Remaining Period* [$t_6 \leq t \leq t_7$]: Fig. 4(h) shows the equivalent circuit of this mode. At t_6 , S_{bot} is entirely ON. During this period, C_{iss} continues to be charged, leading to a rise in v_{gs} . The independent state variables of this mode are the same as Mode V. The state equations can be obtained from (1), (3), and (17)–(19), where $-V_r$ in (19) is replaced by $i_d \cdot R_{dson}$.

This mode ends when v_{gs} rises to V_G . After that, the steady state of S ON and S_{bot} OFF begins.

B. Transient Model During Turn-OFF Transition

Typical waveforms during the turn-OFF transition are shown in Fig. 5. Each submode is analyzed in detail below based on the equivalent circuits in Fig. 6.

1) *Mode I. S Turn-OFF Delay Period* [$\tau_0 \leq t \leq \tau_1$]: Fig. 6(a) shows the equivalent circuit of this mode. At τ_0 , V_G is set to 0 V, and v_{gs} is falling. The independent state variables of this mode are $\mathbf{X} = [i_d \ v_{dsbot} \ v_{gs} \ i_g \ i_L]^T$. The state equations can be obtained from (1), (17), and (22)–(24)

$$0 = v_{gs} + i_g R_g + (L_g + L_{ss}) \frac{di_g}{dt} + L_{ss} \frac{di_d}{dt} \quad (22)$$

$$V_{in} = L_{loop} \frac{di_d}{dt} + L_{ss} \frac{di_g}{dt} - (L_{pbot} + L_{ssbot}) \frac{di_L}{dt} + i_d R_{dson} + v_{dsbot} \quad (23)$$

$$V_{out} = (L_{pbot} + L_{ssbot}) \frac{d(i_d - i_L)}{dt} + v_{dsbot} - L \frac{di_L}{dt}. \quad (24)$$

This mode ends when v_{gs} drops to the value

$$v_{gs} = V_{gsth} + \frac{i_d}{g_{fs}}. \quad (25)$$

2) *Mode II. S Turn-OFF Transition Period* [$\tau_1 \leq t \leq \tau_2$]: Fig. 6(b) shows the equivalent circuit of this mode. During this period, v_{ds} is rising and v_{dsbot} is falling. The independent state variables of this mode are $\mathbf{X} = [i_d \ v_{ds} \ v_{dsbot} \ v_{gs} \ i_g \ i_L]^T$. The state equations can be obtained from (1), (21)–(24), and (26), where $i_d \cdot R_{dson}$ in (23) is replaced by v_{ds}

$$C_{oss} \frac{dv_{ds}}{dt} - C_{gd} \frac{dv_{gs}}{dt} + i_{ch} = i_d. \quad (26)$$

This mode ends when v_{gs} drops to V_{gsth} or v_{dsbot} drops to $-V_r$.

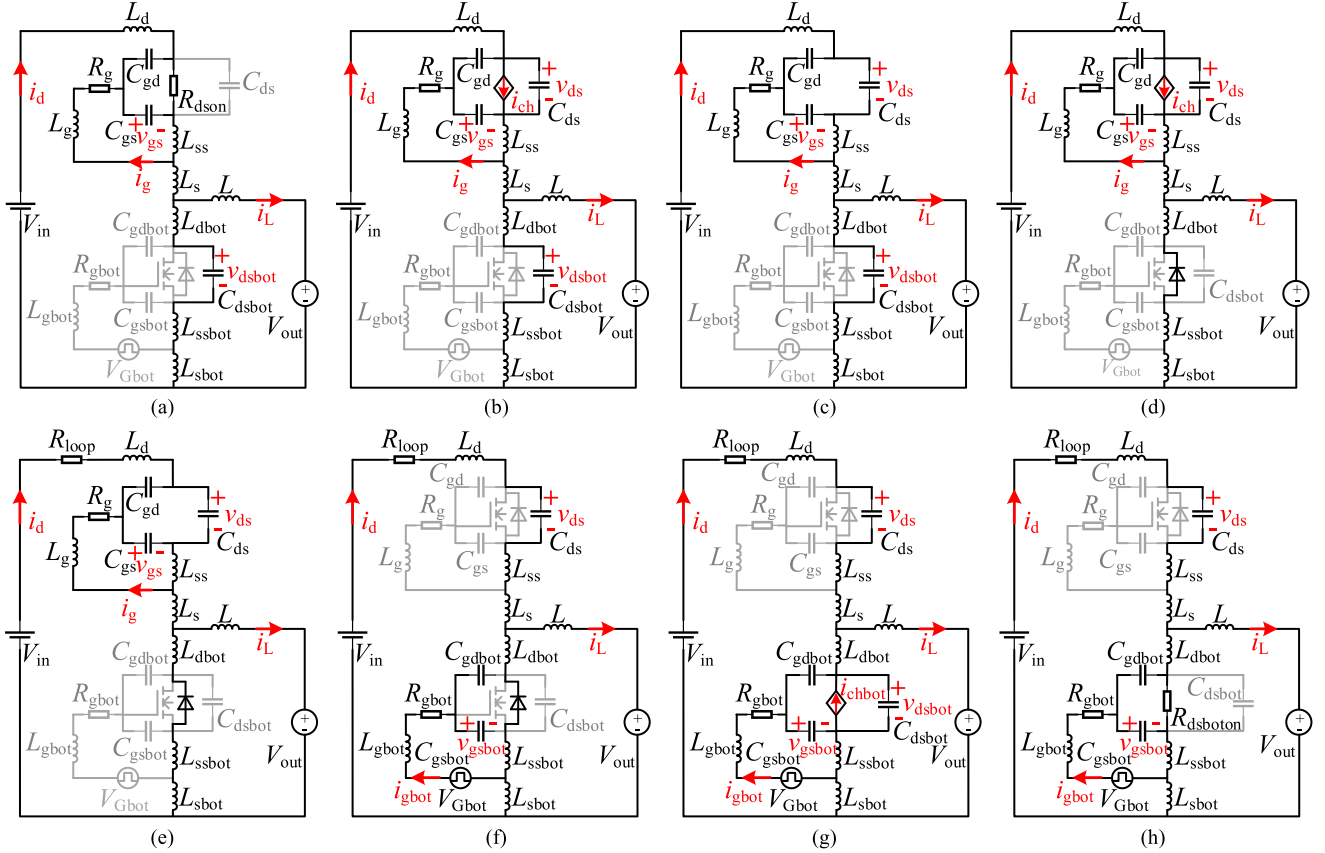


Fig. 6. Equivalent circuits during turn-OFF transition of S . (a) Mode I. (b) Mode II. (c) Case 1 of mode III. (d) Case 2 of mode III. (e) Mode IV. (f) Mode V. (g) Mode VI. (h) Mode VII.

3) *Mode III. S Turn-OFF Remaining Transition Period* $[\tau_{2.1} \leq t \leq \tau_{3.1}]$ or $[\tau_{2.2} \leq t \leq \tau_{3.2}]$:

Case 1 $[\tau_{2.1} \leq t \leq \tau_{3.1}]$: v_{gs} drops to V_{gsth} before v_{dsbot} drops to $-V_r$. At $\tau_{2.1}$, the channel of S stops conducting, as shown in Fig. 6(c). During this period, v_{ds} is rising and v_{dsbot} is falling. The independent state variables of this mode are the same as Mode II. The state equations can be obtained from (1), (21)–(24), and (26), where $i_d \cdot R_{dson}$ in (23) is replaced by v_{ds} and i_{ch} in (26) equals zero.

This mode ends when v_{dsbot} drops to $-V_r$.

Case 2 $[\tau_{2.2} \leq t \leq \tau_{3.2}]$: v_{dsbot} drops to $-V_r$ before v_{gs} drops to V_{gsth} . At $\tau_{2.2}$, the equivalent diode of S_{bot} starts to conduct, as shown in Fig. 7(d). The independent state variables of this mode are $\mathbf{X} = [i_d \ v_{ds} \ v_{gs} \ i_g \ i_L]^T$. The state equations can be obtained from (21), (22), (24), (26), and (27), where v_{dsbot} in (24) is replaced by $-V_r$

$$V_{in} = L_{loop} \frac{di_d}{dt} + L_{ss} \frac{di_g}{dt} - (L_{pbot} + L_{ssbot}) \frac{di_L}{dt} + v_{ds} - V_r. \quad (27)$$

This mode ends when v_{gs} drops to V_{gsth} .

4) *Mode IV. Dead Time Duration Period* $[\tau_{3.1} \leq t \leq \tau_4]$ or $[\tau_{3.2} \leq t \leq \tau_4]$: Fig. 6(e) shows the equivalent circuit of this

mode. At $\tau_{3.1}$ or $\tau_{3.2}$, S is entirely OFF and i_L flows through the equivalent diode of S_{bot} . During this period, L_{loop} resonates with C_{oss} , leading to a high-frequency damping resistor R_{loop} . The independent state variables of this mode are the same as in case 2 of Mode III. The state equations can be obtained from (21), (22), (24), (26), and (28), where v_{dsbot} in (24) is replaced by $-V_r$ and i_{ch} in (26) equals zero

$$V_{in} = L_{loop} \frac{di_d}{dt} + L_{ss} \frac{di_g}{dt} - (L_{pbot} + L_{ssbot}) \frac{di_L}{dt} + v_{ds} - V_r + i_d R_{loop}. \quad (28)$$

This mode ends when the drive voltage V_{Gbot} is applied.

5) *Mode V. S_{bot} Turn-ON Delay Period* $[\tau_4 \leq t \leq \tau_5]$: Fig. 6(f) shows the equivalent circuit of this mode. At τ_4 , V_{Gbot} is applied and v_{gsbot} rises. The independent state variables of this mode are $\mathbf{X} = [i_d \ v_{ds} \ v_{gsbot} \ i_{gbot} \ i_L]^T$. The state equations can be obtained from (4), (7), (10), (29), and (30), where $(i_d - i_L) \cdot R_{dsboton}$ in (10) is replaced by $-V_r$

$$V_{Gbot} = (L_{gbot} + L_{ssbot}) \frac{di_{gbot}}{dt} + L_{ssbot} \frac{d(i_d - i_L)}{dt} + v_{gsbot} + i_{gbot} R_{gbot} \quad (29)$$

$$V_{in} = L_{loop} \frac{di_d}{dt} + L_{ssbot} \frac{di_{gbot}}{dt} - (L_{pbot} + L_{ssbot}) \frac{di_L}{dt} + v_{ds} - V_r + i_d R_{loop}. \quad (30)$$

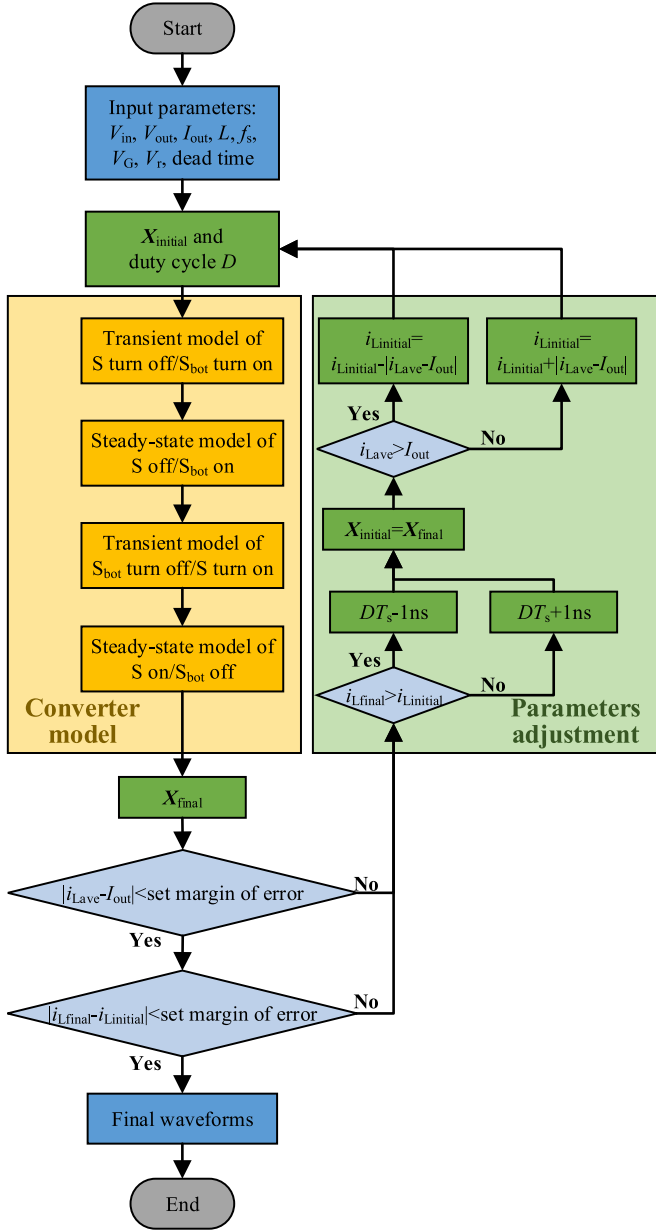


Fig. 7. Design flowchart of the proposed multitime-scale modeling method.

On account of the reverse conduction of S_{bot} in this mode, eGaN HEMTs follow the reverse conduction characteristic. This mode ends when v_{gdbot} rises to $V_{gdbotth}$.

6) *Mode VI. S_{bot} Turn-ON Transition Period* [$\tau_5 \leq t \leq \tau_6$]: Fig. 6(g) shows the equivalent circuit of this mode. During this period, v_{dsbot} is rising. The independent state variables of this mode are $\mathbf{X} = [i_d \ v_{ds} \ v_{dsbot} \ v_{gsbot} \ i_{gbot} \ i_L]^T$. The state equations can be obtained from (4), (10), (13), and (29)–(31), where $(i_d - i_L) \cdot R_{dsboton}$ in (10) is replaced by v_{dsbot} and $-V_r$ in (30) is replaced by v_{dsbot}

$$C_{ossbot} \frac{dv_{dsbot}}{dt} - C_{gdbot} \frac{dv_{gsbot}}{dt} - i_{chbot} = i_d - i_L. \quad (31)$$

This mode ends when v_{dsbot} rises from $-V_r$ to zero.

7) *Mode VII. Gate Charge Remaining Period* [$\tau_6 \leq t \leq \tau_7$]: Fig. 6(h) shows the equivalent circuit of this mode. At τ_6 , S is entirely ON. The independent state variables of this mode are the same as Mode V. The state equations can be obtained from (4), (7), (10), (29), and (30), where $-V_r$ in (30) is replaced by $(i_d - i_L) \cdot R_{dsboton}$.

This mode ends when v_{gsbot} rises to V_{Gbot} . After that, the steady state of S_{bot} ON and S OFF begins.

V. COMPLETE MULTITIME-SCALE ANALYTICAL MODEL

Through the above analysis, the switching steady-state model on μs time scale and the switching transient model on ns time scale are obtained. To fully describe the typical multitime-scale operation of synchronous buck converter, two models are merged in the following order.

Starting from the moment when the drive voltage V_G of S is removed, the model first proceeds to the transient process of S turning OFF and S_{bot} turning ON. At the end of this transient process, the model switches to the steady state of S OFF and S_{bot} ON. After this state, the model switches to the transient process of S_{bot} turning OFF and S turning ON. At the end of this transient process, the model switches to the steady state of S ON and S_{bot} OFF until the next time when the V_G is removed. By solving the state equations for each mode in turn based on the above sequence, a complete analytical model of the converter within one switching cycle is obtained.

The solving of the state equations and the switching of modes depend on the initial values of the state variables and duty cycle, which can be calculated as follows [23].

$$\mathbf{X}_{initial} = \begin{bmatrix} i_{d_{initial}} \\ v_{ds_{initial}} \\ v_{dsbot_{initial}} \\ v_{gs_{initial}} \\ i_{g_{initial}} \\ i_{L_{initial}} \end{bmatrix} = \begin{bmatrix} I_{out} + \frac{V_{in} - V_{out}}{2L} \cdot \frac{V_{out}}{V_{in}} \cdot T_s \\ 0 \\ V_{in} \\ V_G \\ 0 \\ I_{out} + \frac{V_{in} - V_{out}}{2L} \cdot \frac{V_{out}}{V_{in}} \cdot T_s \end{bmatrix} \quad (32)$$

$$D = \frac{V_{out}}{V_{in}}. \quad (33)$$

The final values of the state variables in the previous mode are used as the initial values of the next mode due to the continuity. Finally, the final values of the state variables in one cycle can be derived.

However, there are deviations between the waveform predicted by the model and the actual one in one cycle. The reason is the difference between the actual initial values of the state variables as well as the duty cycle and the theoretical values considering the losses of the converter. Therefore, the parameters are continuously adjusted in subsequent iterations to minimize the error with the actual values.

The converter is not yet stable when the error between the final values and the initial values of the state variables within one switching cycle is unacceptable. Assigning the final values in the previous cycle to the initial values in the next cycle, the basic periodic iteration is achieved. In addition, based on the steady-state analysis of the buck converter, it is known that the output capacitor follows the principle of amp-second balance, which means that the average value of the inductor current i_{Lave}

is equal to the load current I_{out} . Similarly, the output inductor follows the principle of volt-second balance, which means that the final value of the inductor current $i_{L_{final}}$ is equal to the initial value $i_{L_{initial}}$. The initial values of the inductor current and duty cycle need to be adjusted as follows.

- 1) The Initial Values of Inductor Current
 - a) When the average value of the inductor current is greater than the load current, indicating that the energy stored in the output capacitor is higher than the energy released in that cycle, the initial value of the inductor current for the next iteration is reduced.
 - b) When the average value of the inductor current is less than the load current, indicating that the energy stored in the output capacitor is lower than the energy released in that cycle, the initial value of the inductor current for the next iteration is increased.
- 2) Duty Cycle
 - a) When the final value of the inductor current is greater than the initial value, indicating that the energy stored in the output inductor is higher than the energy released in that cycle, the duty cycle for the next iteration is reduced.
 - b) When the final value of the inductor current is less than the initial value, indicating that the energy stored in the output inductor is lower than the energy released in that cycle, the duty cycle for the next iteration is increased.

The initial values of state variables and duty cycle are iterated repeatedly until the following two constraints are satisfied.

- 1) The difference between the average value of the inductor current and the load current is within the set margin of error.
- 2) The difference between the final value of the inductor current and the initial value is within the set margin of error.

Eventually, both constraints are satisfied simultaneously to acquire the stable state waveforms of the converter within one switching cycle. And the stricter the constraint is, the longer the iteration time and the closer the result to the actual situation will be.

The above merging and iterative methods for the multitime-scale model are summarized in a flowchart, as shown in Fig. 7. To begin with, the circuit parameters, including input voltage V_{in} , output voltage V_{out} , load current I_{out} , output inductor L , switching frequency f_s , drive voltage V_G , reverse conduction voltage V_r , and dead time, are inputs for the calculation of the initial values and duty cycle as well as the solving of the state equations. The parameters are adjusted during each iteration until the constraints are satisfied, and then the final waveforms are acquired. Moreover, when the difference between $i_{L_{final}}$ and $i_{L_{initial}}$ is large, the large adjustment step of duty cycle is given, and when the difference is small, the small step is given so that the iteration speed can be effectively improved.

VI. EXPERIMENTAL VALIDATION

In this article, a hardware prototype is built to verify the proposed multitime-scale analytical model, as shown in Fig. 8.

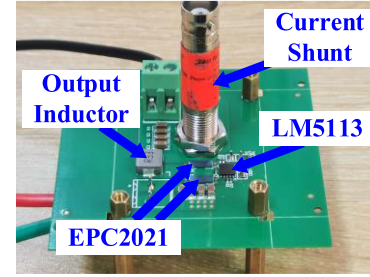


Fig. 8. Hardware prototype of the synchronous buck converter.

TABLE I
KEY CIRCUIT PARAMETERS

Parameters	Values
Input voltage V_{in}	12 V
Output voltage V_{out}	3.3 V
Output current I_{out}	1 A
Switching frequency f_s	1 MHz
Output inductor L	410 nH
Dead time of turn-off transition t_{doff}	43 ns
Dead time of turn-on transition t_{don}	82 ns

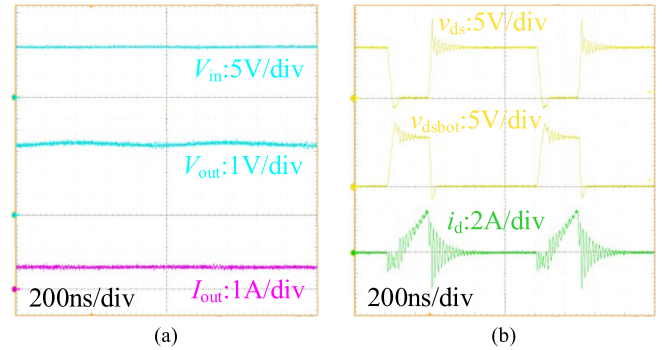


Fig. 9. Key experimental waveforms of the synchronous buck converter. (a) Input voltage V_{in} , the output voltage V_{out} , and the output current I_{out} . (b) Drain-source voltage v_{ds} of S , the drain-source voltage v_{dsbot} of S_{bot} , and the drain current i_d .

TABLE II
PARASITIC INDUCTORS OF PCB LAYOUT

Parasitic Inductors	Values
Drain inductor of S L_d	1.90 nH
Source inductor of S L_s	0.61 nH
Gate inductor of S L_g	4.29 nH
Drain inductor of S_{bot} L_{dbot}	0.61 nH
Source inductor of S_{bot} L_{sbot}	0.20 nH
Gate inductor of S_{bot} L_{gbot}	3.52 nH

The key circuit parameters are listed in Table I, the power device used in the experiment is EPC2021, and the driver chip is LM5113. The key steady-state experimental waveforms are measured with oscilloscope, as shown in Fig. 9. With Maxwell Q3D simulation, the parasitic inductors of the PCB layout for the power loop and drive loop can be extracted, as shown in Table II, and the waveforms predicted with the model are acquired by

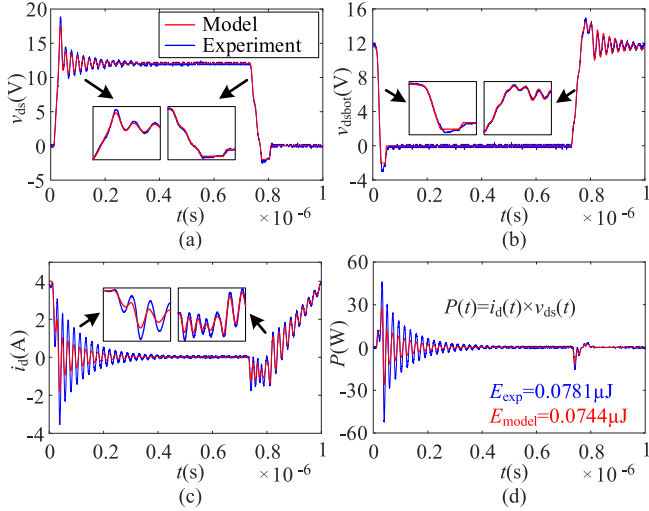


Fig. 10. Comparison of the critical waveforms obtained from the experiment and the proposed model within one switching cycle. (a) Drain–source voltage v_{ds} of S . (b) Drain–source voltage v_{dsbot} of S_{bot} . (c) Drain current i_d of S . (d) Power of S . (The red line is the model, and the blue line is the experiment).

TABLE III
PARAMETERS FOR EXPERIMENTAL AND MODEL RESULTS

Parameters	Experiment	Model	Error
Oscillation frequency	45.9 MHz	46.2 MHz	0.7%
Peak value of v_{ds}	18.8 V	17.6 V	6.4%
Peak value of v_{dsbot}	15.00 V	14.55 V	3.0%
Peak value of i_d	3.96 A	3.88 A	2.0%
Rise time of v_{ds}	17.5 ns	17.2 ns	1.7%
Fall time of v_{ds}	38.4 ns	38.3 ns	0.3%
Rise time of v_{dsbot}	36.3 ns	35.5 ns	2.2%
Fall time of v_{dsbot}	16.2 ns	15.9 ns	1.9%

solving the state equations in MATLAB software with the ode-45 function based on the Runge–Kutta methods.

The waveforms of v_{ds} , v_{dsbot} , and i_d obtained from the experiment and the proposed model within one switching cycle are shown in Fig. 10(a)–(c), which reflect the dynamic and steady-state characteristics of the converter. It can be seen that the steady-state waveforms of the model and experiment match very well. And the rising rate of drain current i_d predicted by the model in Fig. 10(c) is consistent with the experimental result. The oscillation frequencies measured and calculated with waveforms are 45.9 MHz and 46.2 MHz, respectively, as shown in Table III. And the oscillation amplitudes of voltage and current are slightly different. The inaccurate parasitic inductor induced by the coaxial shunt and the junction capacitor of the device from datasheet affect the frequency and amplitude of oscillation. Moreover, the initial energy in the resonant inductor and capacitor cannot be accurately determined, which also impacts the prediction accuracy of the oscillation amplitude. There is a slight deviation in the oscillation phase between the model and experiment, which is mainly caused by the deviation in switching speed.

The zoomed-in view in Fig. 10(a)–(c) shows the switching transient waveforms on the ns time scale. With the measurement, the peak values of the voltage and current in the experiment

and model waveforms are shown in Table III with acceptable errors. And the rise time and fall time of v_{ds} and v_{dsbot} in the experimental result and model result are shown in Table III with acceptable errors. Based on the comparison of the parameters, it can be concluded that the transient waveforms of the model and experiment match well. It is worth noting that the parameters of the power device, such as nonlinear junction capacitors and transconductance, are derived from the datasheet, which are tested under specific operating conditions. However, there are deviations between the parameters in the datasheet and the actual ones because the state of the circuit and the temperature of the device are constantly changing in practice. The deviations lead to errors in the predictions of the model for switching speed, oscillation frequency, and oscillation amplitude [24], [25], [26]. In future work, the parameters can be corrected by testing the circuit under different operating states and by considering temperature as a variable in the converter model.

Fig. 10(d) shows the power waveforms of the main switch S within one switching cycle obtained from the experiment and the proposed model, that is, the multiplication of the drain current i_d and the drain–source voltage v_{ds} . By integrating the waveform data, the energy losses of S can be found as $E_{exp} = 0.0781 \mu\text{J}$ and $E_{model} = 0.0744 \mu\text{J}$, respectively. It can be concluded that the proposed model can predict energy losses accurately.

VII. DEAD TIME OPTIMIZATION BASED ON THE CONVERTER MODEL

To avoid short circuits, the dead time is set between the drive signals of the main switch S and the synchronous switch S_{bot} , as shown in Fig. 1(b). However, the longer the dead time is, the higher the reverse conduction loss will be. The waveforms in Fig. 10(a) and (b) show that the reverse conduction voltage of the GaN device is around 2 V, which is a large value and leads to a more significant reverse conduction loss. Therefore, dead time optimization is essential to enhance the efficiency of the converter.

The accurate initial values of the state variables in a stable state can be obtained from the proposed converter model with repeated iterations, which is beneficial for reliable calculation of optimal dead time. At t_0 , the drive voltage V_{Gbot} is removed. At $t_{3.1}$ or $t_{3.2}$, v_{gsbot} drops to $V_{gsbotth}$ and v_{ds} drops to $-V_r$, which means S_{bot} is completely turned OFF. At t_4 , the drive voltage V_G is applied. At t_5 , v_{gd} rises to v_{gdth} , which means S starts to turn ON. If S immediately starts to turn ON when S_{bot} is fully turned OFF, it is possible to avoid straight-through and additional reverse conduction losses. The optimal dead time $t_{odt'on}$ during the turn-ON transition can be obtained from (34). Likewise, the optimal dead time $t_{odt'off}$ during the turn-OFF transition can be obtained from (35)

$$t_{odt'on} = t_{3.1or3.2} - t_0 - (t_5 - t_4) \quad (34)$$

$$t_{odt'off} = \tau_{3.1or3.2} - \tau_0 - (\tau_5 - \tau_4). \quad (35)$$

These times can be obtained by solving the model in MATLAB software. The optimal dead time is derived as $(t_{odt'on}, t_{odt'off}) = (52.9 \text{ ns}, 27.1 \text{ ns})$ under the operating condition in Section VI. The experiment is performed with the dead time

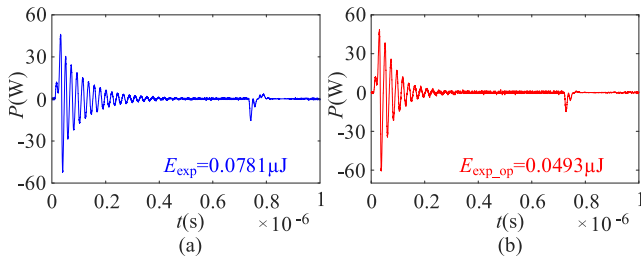


Fig. 11. Power waveforms of S within one switching cycle obtained from the experiments. (a) Before the dead time optimization ($t_{don} = 82$ ns and $t_{doff} = 43$ ns). (b) After the dead time optimization ($t_{don} = 56$ ns and $t_{doff} = 30$ ns).

optimized to $(t_{don}, t_{doff}) = (56$ ns, 30 ns). Fig. 11 shows the power waveforms of S within one switching cycle obtained from the experiments before and after the dead time optimization. By integrating the waveform data, the switching energy losses of S can be found as $E_{exp} = 0.0781$ μ J and $E_{exp_op} = 0.0493$ μ J. It can be concluded that the dead time optimization based on the proposed model can reduce the energy loss of the device effectively. Furthermore, the efficiency of the converter measured is improved from 83.9% to 86.0%.

VIII. CONCLUSION

In this article, a multitime-scale converter modeling method is proposed based on the analysis of the switching steady-state process on μ s time scale and the switching transient process on ns time scale within one switching cycle, taking into account the effects of parasitic parameters, nonlinear junction capacitors, and nonlinear transconductance of the power device. At the methodological level, the switching cycle is divided into multiple modes based on the circuit state, and the numerical model is given in the form of the state equations of each mode. To obtain the time-domain steady-state analytical model of the ZVS buck converter, different time-scale models are merged based on the iterative idea according to the continuous state variables and the boundary conditions of each mode. This modeling method is also applicable to other converters. At the effect level, the switching waveforms on μ s time scale and ns time scale as well as the switching energy loss derived by solving the state equations in MATLAB software are in good agreement with the experimental results, which validates the accuracy of the proposed model.

The multitime-scale analytical model can be applied to the ZVS buck converter with specific parameters to obtain the numerical solution for the state variables and the duration of the states during the switching cycle. Based on the proposed model, dead time optimization is achieved, which effectively reduces the switching energy loss of the power device. In the future, the model can be used to optimize the efficiency of the converter in the circuit parameter design stage.

REFERENCES

- [1] L. Yu, L. Wang, W. Mu, and C. Yang, "An ultrahigh step-down DC-DC converter based on switched-capacitor and coupled inductor techniques," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11221–11230, Nov. 2022, doi: [10.1109/TIE.2021.3118368](https://doi.org/10.1109/TIE.2021.3118368).
- [2] L. Yu, L. Wang, C. Yang, and M. Wu, "Analysis and implementation of a single-stage transformer-less converter with high step-down voltage gain for voltage regulator modules," *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 12239–12249, Dec. 2021, doi: [10.1109/TIE.2020.3045592](https://doi.org/10.1109/TIE.2020.3045592).
- [3] M. Hajiheidari, H. Farzanehfard, and M. Esteki, "Asymmetric ZVS buck converters with high-step-down conversion ratio," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 7957–7964, Sep. 2021, doi: [10.1109/TIE.2020.3013538](https://doi.org/10.1109/TIE.2020.3013538).
- [4] B. N. Sanusi and Z. Ouyang, "Integrated inductor design for a highly compact embedded battery charger," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 8873–8885, Aug. 2022, doi: [10.1109/TPEL.2022.3156372](https://doi.org/10.1109/TPEL.2022.3156372).
- [5] R. Ramachandran and M. Nymand, "Experimental demonstration of a 98.8% efficient isolated DC-DC GaN converter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9104–9113, Nov. 2017, doi: [10.1109/TIE.2016.2613930](https://doi.org/10.1109/TIE.2016.2613930).
- [6] A. Lidow, M. de Rooij, J. Strydom, D. Reusch, and J. Glaser, *GaN Transistors for Efficient Power Conversion*, 3rd ed. Hoboken, NJ, USA: Wiley, 2019.
- [7] K. Wang, B. Li, H. Li, X. Yang, and A. Qiu, "Characterization and modeling of frequency-dependent on-resistance for GaN devices at high frequencies," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4925–4933, May 2020, doi: [10.1109/TPEL.2019.2947075](https://doi.org/10.1109/TPEL.2019.2947075).
- [8] Y. Shen, L. Shillaber, H. Zhao, Y. Jiang, and T. Long, "Desynchronizing paralleled GaN HEMTs to reduce light-load switching loss," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9151–9170, Sep. 2020, doi: [10.1109/TPEL.2020.2970240](https://doi.org/10.1109/TPEL.2020.2970240).
- [9] Z. Yao and S. Lu, "A simple approach to enhance the effectiveness of passive currents balancing in an interleaved multiphase bidirectional DC-DC converter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7242–7255, Aug. 2019, doi: [10.1109/TPEL.2018.2881058](https://doi.org/10.1109/TPEL.2018.2881058).
- [10] L. Zhou and M. Preindl, "Variable-switching constant-sampling frequency critical soft switching MPC for DC/DC converters," *IEEE Trans. Energy Convers.*, vol. 36, no. 2, pp. 1548–1561, Jun. 2021, doi: [10.1109/TEC.2021.3058306](https://doi.org/10.1109/TEC.2021.3058306).
- [11] Z. Yao and S. Lu, "Voltage self-balance mechanism based on zero-voltage switching for three-level DC-DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10078–10087, Oct. 2020, doi: [10.1109/TPEL.2020.2977881](https://doi.org/10.1109/TPEL.2020.2977881).
- [12] K. Wang, L. Wang, X. Yang, X. Zeng, W. Chen, and H. Li, "A multiloop method for minimization of parasitic inductance in GaN-based high-frequency DC-DC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4728–4740, Jun. 2017, doi: [10.1109/TPEL.2016.2597183](https://doi.org/10.1109/TPEL.2016.2597183).
- [13] A. Letellier, M. R. Dubois, J. P. F. Trovão, and H. Maher, "Calculation of printed circuit board power-loop stray inductance in GaN or high di/dt applications," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 612–623, Jan. 2019, doi: [10.1109/TPEL.2018.2826920](https://doi.org/10.1109/TPEL.2018.2826920).
- [14] Z. Qi, Y. Pei, L. Wang, Q. Yang, and K. Wang, "A highly integrated PCB embedded GaN full-bridge module with ultralow parasitic inductance," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4161–4173, Apr. 2022, doi: [10.1109/TPEL.2021.3128694](https://doi.org/10.1109/TPEL.2021.3128694).
- [15] J. Chen, X. Du, Q. Luo, X. Zhang, P. Sun, and L. Zhou, "A review of switching oscillations of wide bandgap semiconductor devices," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13182–13199, Dec. 2020, doi: [10.1109/TPEL.2020.2995778](https://doi.org/10.1109/TPEL.2020.2995778).
- [16] J. Sun, L. Yuan, Q. Gu, R. Duan, Z. Lu, and Z. Zhao, "Design-oriented comprehensive time-domain model for CLLC class isolated bidirectional DC-DC converter for various operation modes," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3491–3505, Apr. 2020, doi: [10.1109/TPEL.2019.2938312](https://doi.org/10.1109/TPEL.2019.2938312).
- [17] O. M. Hebala, A. A. Aboushady, K. H. Ahmed, and I. Abdel-salam, "Generic closed-loop controller for power regulation in dual active bridge DC-DC converter with current stress minimization," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4468–4478, Jun. 2019, doi: [10.1109/TIE.2018.2860535](https://doi.org/10.1109/TIE.2018.2860535).
- [18] J. Chen, Q. Luo, J. Huang, Q. He, and X. Du, "A complete switching analytical model of low-voltage eGaN HEMTs and its application in loss analysis," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1615–1625, Feb. 2020, doi: [10.1109/TIE.2019.2891466](https://doi.org/10.1109/TIE.2019.2891466).
- [19] Y. Zhang et al., "Analysis of dead-time energy loss in GaN-based TCM converters with an improved GaN HEMT model," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1806–1818, Feb. 2023, doi: [10.1109/TPEL.2022.3217456](https://doi.org/10.1109/TPEL.2022.3217456).
- [20] Y. Zhang, C. Chen, Y. Xie, T. Liu, Y. Kang, and H. Peng, "A high-efficiency dynamic inverter dead-time adjustment method based on an improved GaN HEMTs switching model," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2667–2683, Mar. 2022, doi: [10.1109/TPEL.2021.3112694](https://doi.org/10.1109/TPEL.2021.3112694).

- [21] K. Wang, H. Zhu, J. Wu, X. Yang, and L. Wang, "Adaptive driving scheme for ZVS and minimizing circulating current in MHz CRM converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3633–3637, Apr. 2021, doi: [10.1109/TPEL.2020.3025810](https://doi.org/10.1109/TPEL.2020.3025810).
- [22] K. Wang, X. Yang, H. Li, H. Ma, X. Zeng, and W. Chen, "An analytical switching process model of low-voltage eGaN HEMTs for loss calculation," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 635–647, Jan. 2016, doi: [10.1109/TPEL.2015.2409977](https://doi.org/10.1109/TPEL.2015.2409977).
- [23] R.W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Kluwer, 2001.
- [24] S. Li, S. Yang, S. Han, and K. Sheng, "Investigation of temperature-dependent dynamic R_{ON} of GaN HEMT with hybrid-drain under hard and soft switching," in *Proc. 32nd Int. Symp. Power Semicond. Devices ICs*, 2020, pp. 306–309, doi: [10.1109/ISPSD46842.2020.9170048](https://doi.org/10.1109/ISPSD46842.2020.9170048).
- [25] S. Shamsir, F. Garcia, and S. K. Islam, "Modeling of enhancement-mode GaN-GIT for high-power and high-temperature application," *IEEE Trans. Electron Devices*, vol. 67, no. 2, pp. 588–594, Feb. 2020, doi: [10.1109/TED.2019.2961908](https://doi.org/10.1109/TED.2019.2961908).
- [26] S. Ji, S. Zheng, F. Wang, and L. M. Tolbert, "Temperature-dependent characterization, modeling, and switching speed-limitation analysis of third-generation 10-kV SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4317–4327, May 2018, doi: [10.1109/TPEL.2017.2723601](https://doi.org/10.1109/TPEL.2017.2723601).



Mengjia Wei was born in Anhui Province, China, in 1998. She received the B.S. degree in electrical engineering from Anhui University, Hefei, China, in 2020. She is currently working toward the master's degree in electrical engineering with Chongqing University, Chongqing, China.

Her current research interests include the analytical modeling and efficiency optimization of converters with wide bandgap devices.



Quanming Luo (Member, IEEE) was born in Chongqing, China, in 1976. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Chongqing University, Chongqing, China, in 1999, 2002, and 2008, respectively.

He was with Emerson Network Power Company, Ltd., Shenzhen, China, as a Research and Development Engineer from 2002 to 2005. Since 2005, he has been with the College of Electrical Engineering, Chongqing University, where he is currently a Professor. He is the author or coauthor of more than

80 papers in journal or conference proceedings. His current research interests include LED driving systems, communication power systems, power harmonic suppression, and power conversion systems in electrical vehicles.



Jian Chen (Member, IEEE) was born in Hubei Province, China, in 1993. He received the B.S. degree from Qinghai University, Xining, China, in 2016, and the Ph.D. degree from Chongqing University, Chongqing, China, in 2021, both in electrical engineering.

He is currently an Assistant Professor with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu, China. His current research interests include wide bandgap device characteristics and models, active gate drivers, and power electronic integration.



Xinyue Zhang was born in Sichuan Province, China, in 1996. She received the B.S. degree from the Harbin Institute of Technology, Weihai, China, in 2018, and the master's degree from Chongqing University, Chongqing, China, in 2021, both in electrical engineering.

She is currently an employee of State Grid Sichuan Electric Power Company, Chengdu, China. Her current research interests include the analytical modeling and the loss calculation of wide bandgap devices.



Lujing Xiong was born in Chongqing, China. She received the B.E. degree in electrical engineering in 2020 from Chongqing University, Chongqing, China, where she is currently working toward the master's degree in electrical engineering.

Her current research interests include analytical, electrothermal modeling of wide bandgap devices, and thermal design of converter.



Pengju Sun (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Chongqing University, Chongqing, China, in 2005 and 2011, respectively.

Between September 2009 and August 2010, she was a Visiting Student with the University of California, Irvine, CA, USA. Since 2011, she has been with the College of Electrical Engineering, Chongqing University, where she is currently an Associate Professor. Her research interests include switching power converters, power quality control, and reliability of power converter.



Xiong Du (Member, IEEE) received the B.S., M.S., and Ph.D. degrees from Chongqing University, Chongqing, China, in 2000, 2002, and 2005, respectively, all in electrical engineering.

Since 2002, he has been with Chongqing University, where he is currently a Full Professor with the School of Electrical Engineering. He was a Visiting Scholar with Rensselaer Polytechnic Institute, Troy, NY, USA, from July 2007 to July 2008. His research interests include power electronics system reliability and stability.

Dr. Du was a recipient of the National Excellent Doctoral Dissertation of P.R. China in 2008.