A Cascaded Modular Isolated Back-to-Back Solid State Transformer Scheme for AC/DC/AC Interconnection With Improved Performance and Simple Control

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***Abstract*—This article proposes a cascaded modular isolated back-to-back solid-state transformer (CMIB-SST) for electrical isolated interconnection of two distribution ac grids, which consists of modular multilevel converter stage, cascaded H bridge (CHB)-stage, and six-terminal active bridge-stage. A switching synchronization hybrid phase-shift modulation (SSHPSM) for the STAB-stage is utilized to suppress the low-frequency voltage ripple of submodule (SM) both in CHB-stage and MMC-stage to reduce the SM capacitance significantly with a simple control scheme of the CMIB-SST. The proposed CMIB-SST is friendly to the cost under the new capacitance constraint, and the big size electrolytic capacitor could be replaced by film capacitor, which is beneficial to security and life of the SST module. The voltage gain, mathematical model of the proposed SST is analyzed to illustrate the principle of SM low-frequency ripple-current decoupling with the SM capacitor and cancellation mechanism in STAB-stage. The corresponding transformer design is carried out under considering the parasitic leakage inductance value and the constraints of its magnetic fields, thermal, electric field strength and insulation. The scheme is evaluated by cost and volume of switches, SM capacitors and magnetic unit. Finally, the processed topology and SSHPSM method are verified by simulation and experimental results.**

***Index Terms*—Cascaded H-bridge (CHB), modular multilevel converter (MMC), six-terminal active bridge (STAB), solid state transformer (SST).**

NOMENCLATURE

CMIB-SST	Cascaded modular isolated back to back solid state transformer.
CHB	Cascaded H bridge.
MMC	Modular multilevel converter.
DAB	Dual active bridge.
STAB	Six-terminal active bridge.
HFT	High-frequency transformer.
SSHPSM	Switching synchronization hybrid phase-shift modulation.
VAC1	AC port 1.
VAC2	AC port 2.
VDC	DC bus.
SM	Sub-module.
FB_C	STAB full bridge connecting the SM of CHB-stage.
FB_M	STAB full bridge connecting the SM of MMC-stage.
$u_{\mathrm{VAC1,2}x}(x = a,b,c)$	VAC1,2 voltage.
$i_{\mathrm{VAC1,2}x}(x = a,b,c)$	VAC1,2 current.
$U_{\mathrm{VAC1,2}}$	Amplitude of VAC1,2 voltage.
$I_{\mathrm{VAC1,2}}$	Amplitude of VAC1,2 current.
U_{VDC}	VDC voltage.
I_{VDC}	VDC current.
$I_{2\mathrm{VAC2}}$	Amplitude of the second-order-frequency circulating current of the MMC-stage bridge arm.
i_{ux}	Upper arm current of MMC-stage.
$i_{\mathrm{SM}x\text{-C}}$	SM charging current of phase-x of CHB-stage.
$i_{\mathrm{SM}x\text{-Mu}}$	SM charging current of phase-x of MMC-stage upper arm.
$i_{\mathrm{SM\text{-}CDC}}$, $i_{\mathrm{SM\text{-}MDC}}$	DC comment of $i_{\mathrm{SM}x\text{-}C}$ and $i_{\mathrm{SMx\text{-}Mu}}$.
$i_{\mathrm{SM}x\text{-CAC}}$	Second-order-frequency comment of $i_{\mathrm{SMx\text{-}C}}$.
$i_{\mathrm{SM}x\text{-MuAC}}$	AC comment of $i_{\mathrm{SM}x\text{-Mu}}$.
$i_{\mathrm{SM}x\text{-MuAC1}}$	Fundamental frequency component of $i_{\mathrm{SM}x\text{-Mu}}$.
$i_{\mathrm{SM}x\text{-MuAC2}}$	Second-order-frequency component of $i_{\mathrm{SM}x\text{-Mu}}$.
$i_{Cx\text{-}CAC}$	Current of $i_{\mathrm{SM}x\text{-CAC}}$ flowing into the SM capacitor of CHB-stage.
$i_{Sx\text{-}CAC}$	Current of $i_{\mathrm{SM}x\text{-CAC}}$ flowing into the STAB primary side port $\mathrm{FB_C}$.

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$i_{Sx\text{-}CACy}$	Current of $i_{Sx\text{-CAC}}$ flowing into other two phases.
$i_{Cx\text{-}C}$	Incompletely coupled ripple current of SM capacitor current of CHB-stage stimulated by three current sources.
$C_{x\text{-}C}$, $C_{x\text{-}M}$	SM capacitance of phase-x of CHB-stage and MMC-stage of CMIB-SST scheme interconnected by DAB.
$C_{Lx\text{-}C}$, $C_{Lx\text{-}M}$	New SM capacitance of phase-x of CHB-stage and MMC-stage of CMIB-SST interconnected by STAB.
$U_{\text{SM-}C}$, $U_{\text{SM-Mu}}$	Stable voltage of CHB-stage and MMC-stage SM capacitors.
$u_{\text{SM-}C}$, $u_{\text{SM-Mu}}$	SM capacitor ripple voltages of CHB-stage and MMC-stage.
$u_{\text{SM-}C\text{avg}}$	Average voltage of CHB-stage three-phase SM capacitor.
$u_{\text{SM}x\text{-}C\text{avg}}$	Average voltage of CHB-stage phase-x SM capacitor.
$u_{\text{ref}}*$	SM capacitor reference voltage of CHB-stage.
$u_{\text{FBM}}*$	FB_M port reference voltage.
u_{FBM}	FB_M port voltage.
P_{VAC1}	VAC1 active power.
P_{VAC2}	VAC2 active power.
P_{VDC}	VDC power.
$P_{\text{SM-}C}$, $P_{\text{SM-}M}$	SM active power of CHB-stage and MMC-stage.
T_{DAB}	Two-winding transformer of DAB.
T_C, T_M	Four-winding transformers of STAB.
N	Transformer turns ratio of T_{DAB}.
N_C, N_M	Transformer turns ratio T_C and T_M.
$u_{px\text{-}C}$, $u_{px\text{-}M}$	HFT primary side voltage of T_C and T_M.
$i_{px\text{-}C}$, $i_{px\text{-}M}$	HFT primary side current of T_C and T_M.
L	DAB inductor.
L_S	STAB inductor
i_{Ls}	STAB inductor current.
I_{Ls}	Maximum value of STAB inductor current.
I_{PM}, I_{SM}	Maximum value of the primary and secondary side currents of T_{DAB}.
$L_{Tx\text{-}C}$, $L_{Tx\text{-}M}$	HFT leakage inductance of primary side of T_C and T_M.
ΔL_{T1}	Difference between L_{Ta} and L_{Tb}.
ΔL_{T2}	Difference between L_{Ta} and L_{Tc}.
ϕ_{FBC}, ϕ_{FBM}	Phase angle of FB_C and FB_M of STAB.
m_C, m_M	Voltage modulation ratio of CHB-stage and MMC-stage.
ω	Any angular frequency.
ω_{F}	Fundamental angular frequency.
$\omega_{2\text{nd}}$	Second-order angular frequency.
f_F	Fundamental frequency.
f_C, f_M	Switching frequency of CHB-stage and MMC stage.
f_D	Switching frequency of DAB.
f_S	Switching frequency of STAB.
φ_C, φ_M	Power factor angle of CHB-stage and MMC-stage.
θ_{Cx}, θ_{Mx}	Initial phase angle of phase-x of CHB-stage and MMC-stage.
θ_{2Mx}	Initial phase angle of the Second-order-frequency circulating current.
ε	SM capacitor voltage ripple coefficient.
$Z_{CLx\text{-}C}$, $Z_{CLx\text{-}M}$	SM capacitance impedance of CHB-stage and MMC-stage.
$Z_{LTx\text{-}C}$, $Z_{LTx\text{-}M}$	HFT leakage inductance impedance of primary side of T_C and T_M.
$Z_{ex\text{-}C}$, $Z_{ex\text{-}M}$	Equivalent input impedance of phase-x of CHB-stage and MMC-stage.
n	Number of SM in one arm of MMC-stage.

I. Introduction

LINE frequency transformers are one of the key element for ac grids interconnection with different voltage levels as electricity grids around the world worked with alternating current in the past years. [1]. Now the application of high-voltage dc (HVdc) transmission has been increasing based on the ac/ac or ac/dc conversion with voltage source converter (VSC) [2], [3]. Modular multilevel converter is one kind of the VSC with characteristics of low-voltage modularity, strong expansibility and low harmonic injection [4], [5], [6].

As MMC has independent common dc bus, it fits for implementation of back-to-back no isolated ac/ac conversion [4], [5], [6]. [7], [8] discussed an isolated back-to-back scheme based on two CHBs (BTB-CHBs), by interconnecting their SMs with dual active bridge (DAB) conversion unit. This scheme is suitable for the medium- and high-voltage ac grids interconnection with the advantages of electrical isolation and wide range of voltage magnitude. Both the SMs of CHB or MMC require large size capacitance to suppress the low-frequency voltage ripple [9], [10], so the SM capacitance has a high impact on cost and power density. A third harmonic injection modulation of CHB/MMC-stage was proposed [11], [12] to minimize the SM capacitance voltage ripple which will increase conduction losses and controller resources. Zhang et al. [13] and Zhou et al. [14] proposed a ripple power control loop of dc/dc isolation-stage to suppress SM capacitor voltage ripple, the regulator should be designed carefully.

A cascaded modular isolated back-to-back solid state transformer (CMIB-SST) is demonstrated in Fig. 1(a), by replacing one CHB by MMC in isolated CHBs based back-to-back scheme, and replacing DAB by a six-terminal active bridge (STAB) to provide galvanic isolation between the interconnected systems as shown in Fig. 1(b). Switching synchronization hybrid phase-shift modulation (SSHPSM) method is proposed for the STAB to achieve low-frequency ripple component decoupling with CHB-stage and MMC-stage SMs, thus SM capacitance size can be reduced significantly as the ripple power on SM capacitors are cancelled without the circulating current injection strategy for the MMC-stage and the third harmonic voltage injection strategy of both two ac/dc-stages.

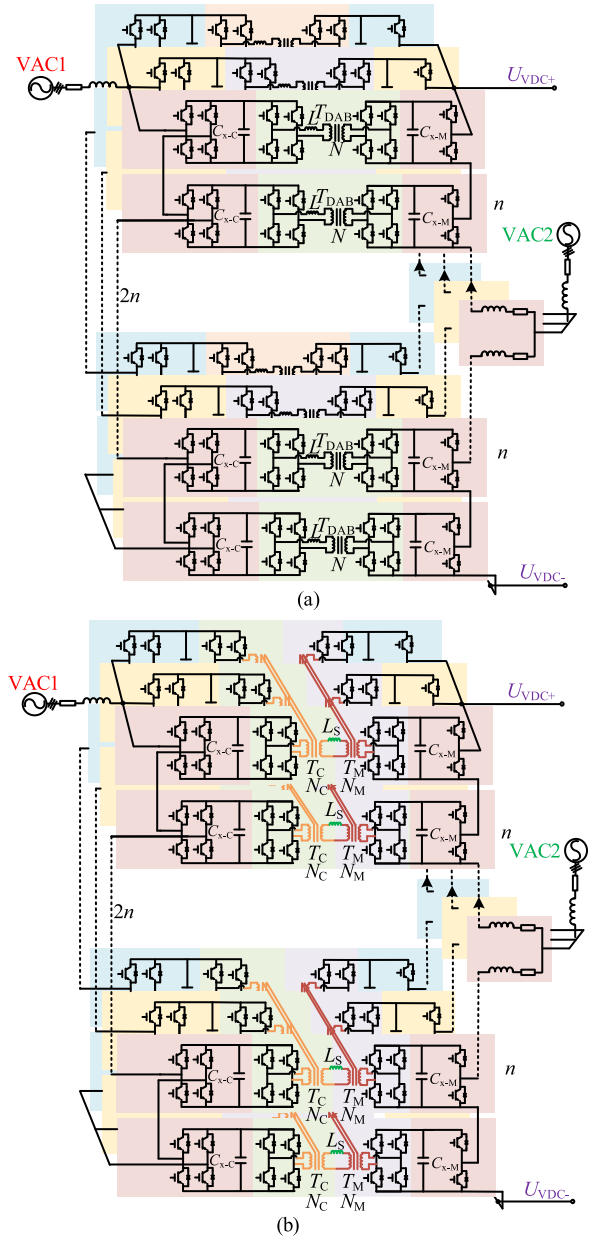

Fig. 1. CMIB-SST scheme. (a) CMIB-SST scheme interconnected by DAB. (b) CMIB-SST scheme interconnected by STAB.

The rest of this article is organized as follows: In Section II, the topology of CMIB-SST is illustrated, the voltage gain, power flow and the ripple current mathematic model are analyzed. In Section III, the CMIB-SST scheme interconnected by STAB and the SSHPSM method of STAB are proposed, and the principle of ripple current cancellation is also introduced. In Section IV, the current stress of the switch is compared and the model selection is carried out, the new capacitance constraints are given and isolation-stage magnetic elements are designed, and the system control strategy is demonstrated. In Sections V and VI, simulation and experimental results are provided to validate the theoretical analysis and the SSHPSM method. Finally, Section VII concludes this article.

II. CMIB-SST Scheme Interconnected By DAB

A. Topology Configuration of CMIB-SST

The CMIB-SST consists of CHB-stage, DAB-stage and MMC-stage is shown in Fig. 1(a) with two ac ports and a dc port for distribution grid interconnection. The galvanic isolation and interconnection between CHB-stage and MMC-stage are realized by DAB and the number of DAB and SM in both the CHB-stage and MMC-Stage are same. Each port of the power distribution interface can implement bidirectional power flow.

B. AC/AC Voltage Magnitude Conversion Gain

The relationship between the voltage amplitude U_{VAC2} and U_{VDC} of VAC2 grid and Vdc bus can be expressed as

$$U_{\mathrm{VAC2}} = \frac{U_{\mathrm{VDC}} m_M}{2} \tag{1}$$

where m_M is the voltage modulation ratio of MMC-stage. Based on the configure of MMC-stage, the voltage of VDC bus is $nU_{\mathrm{SM}\text{-}M}$, then the voltage of VAC2 can also be expressed as (2), where n is the number of SM in one arm of MMC-stage, $U_{\mathrm{SM}\text{-}M}$ is the stable voltage of MMC-stage SM capacitor

$$U_{\mathrm{VAC2}} = \frac{nU_{\mathrm{SM}-M} m_M}{2}. \tag{2}$$

The voltage of VAC1 can be expressed as

$$U_{\mathrm{VAC1}} = 2nU_{\mathrm{SM}-C} m_C = 2nNU_{\mathrm{SM-M}} m_C \tag{3}$$

where N is the DAB transformer turns ratio, m_C is the voltage modulation ratio of CHB-stage, $U_{\mathrm{SM}\text{-}C}$ is the voltage magnitude of CHB-stage SM capacitor. According to (2) and (3), the relation between voltage of VAC1 and VAC2 can be expressed as

$$\frac{U_{\mathrm{VAC2}}}{U_{\mathrm{VAC1}}} = \frac{m_M}{4Nm_C}. \tag{4}$$

Defining $K = m_M/(4Nm_C)$ as the voltage conversion gain of grid interconnection in Fig. 1, which is controlled by the voltage modulation ratio of CHB-stage, MMC-stage and the transformer turns ratio. If the transformer turns ratio of isolation-stage is 1 and the modulation ratio of the two ac/dc-stages is the same, the scheme has at least four times ac voltage conversion capability which could be used for 10 and 35 kV distribution grid interconnection for example. Furthermore, the proposed scheme could implement a wide voltage regulation by adjusting the modulation or turn ratio parameters.

C. Power Flow

All the three ports of the CMIB-SST have the ability of bilateral power control. The voltage and current of VAC1 and VAC2 are shown in (5) and (6), where I_{VAC1}, I_{VAC2} are the current amplitude of VAC1 and VAC2 ports, ω_{F} is the fundamental angular frequency, φ_C and φ_M are the CHB-stage and MMC-stage power factor angles, respectively,

$$\begin{cases} u_{\mathrm{VAC1}x}(t) = U_{\mathrm{VAC1}} \cdot \sin(\omega_F t) \\ i_{\mathrm{VAC1}x}(t) = I_{\mathrm{VAC1}} \cdot \sin(\omega_F t + \varphi_C) \end{cases} \tag{5}$$

$$\begin{cases} u_{\mathrm{VAC2}x}(t) = U_{\mathrm{VAC2}} \cdot \cos(\omega_F t) \\ i_{\mathrm{VAC2}x}(t) = I_{\mathrm{VAC2}} \cdot \cos(\omega_F t + \varphi_M) \end{cases}. \tag{6}$$

The power of CHB-stage and MMC-stage is shown in (7) and (8), where P_{VAC1}, P_{VAC2} and P_{VDC} are the power of VAC1, VAC2 and Vdc bus, respectively, $P_{\mathrm{SM}\text{-}C}$ and $P_{\mathrm{SM}\text{-}M}$ are the SM active power

$$\begin{aligned} P_{\mathrm{VAC1}} &= (3/2)U_{\mathrm{VAC1}}I_{\mathrm{VAC1}}\cos\varphi_C \\ &= 6n \cdot P_{\mathrm{SM}-C} = 6n \cdot P_{\mathrm{SM}-M} \end{aligned} \tag{7}$$

$$P_{\mathrm{VAC2}} = (3/2)U_{\mathrm{VAC2}}I_{\mathrm{VAC2}}\cos\varphi_M = 6n \cdot P_{\mathrm{SM-M}} - P_{\mathrm{VDC}}. \tag{8}$$

The power between the SMs of CHB-stage and MMC-stage is regulated by the phase-shift angle ϕ between the primary and secondary ports of DAB, as shown in (9) [15], where f_{D} is the switching frequency of DAB, L is the DAB inductor

$$P_{\mathrm{SM}-C} = P_{\mathrm{SM}-M} = \frac{NU_{\mathrm{SM}-C}U_{\mathrm{SM}-M}}{2\pi^2 f_D L}\phi(\pi-\phi). \tag{9}$$

D. Mathematical Model of Ripple Current

The phase current $i_{\mathrm{VAC1}x}$ of CHB-stage and the upper arm current i_{ux} of MMC-stage can be expressed, respectively, as

$$i_{\mathrm{VAC1}x} = I_{\mathrm{VAC1}}\sin(\omega_F t + \varphi_C + \theta_{Cx}) \tag{10}$$

$$\begin{aligned} i_{ux} = {} & \frac{I_{\mathrm{VDC}}}{3} + \frac{I_{\mathrm{VAC2}}}{2}\cos(\omega_F t + \varphi_M + \theta_{Mx}) \\ & + I_{2\mathrm{VAC2}}\cos(2\omega_F t + \varphi_M + \theta_{2Mx}) \end{aligned} \tag{11}$$

where I_{VDC} is the current of VDC bus, $I_{2\mathrm{VAC2}}$ is the amplitude of the second-order-frequency ripple current component. θ_{Cx} and θ_{Mx} are the initial phase angles of phase-x of CHB-stage and MMC-stage, respectively, (x stands for phase-a, b, and c), $\theta_{Ca} = \theta_C$, $\theta_{Cb} = \theta_C$-2π/3, $\theta_{Cc} = \theta_C$+2π/3, and $\theta_{Ma} = \theta_M$, $\theta_{Mb} = \theta_M$-2π/3 $\theta_{Mc} = \theta_M$+2π/3, θ_{2Mx} is the initial phase angle of the second-order-frequency circulating current, where $\theta_{2Ma} = \theta_{2M}$, $\theta_{2Mb} = \theta_{2M}$+2π/3 and $\theta_{2Mc} = \theta_{2M}$-2π/3. According to (10), the charging current of the CHB-stage SM capacitor $i_{\mathrm{SMx\text{-}C}}$ can be expressed as (12) [13], where $i_{\mathrm{SM\text{-}CDC}}$ is the dc component, $i_{\mathrm{SM}x\text{-}\mathrm{CAC}}$ is the second-order-frequency component

$$\begin{cases} i_{\mathrm{SM}x-C} = i_{\mathrm{SM-CDC}} + i_{\mathrm{SM}x-\mathrm{CAC}} \\ i_{\mathrm{SM-CDC}} = I_{\mathrm{VAC1}}m_C \cdot \cos\varphi_C/2 \\ i_{\mathrm{SM}x-\mathrm{CAC}} = -I_{\mathrm{VAC1}}m_C \cdot \cos(2\omega_F t + \varphi_C + 2\theta_{Cx})/2 \end{cases}. \tag{12}$$

Take the upper arm of MMC-stage for example, according to (11) the charging current of SM capacitor of MMC-stage can be expressed as (13) shown at the bottom of this page, [14], where $i_{\mathrm{SM\text{-}MuDC}}$, $i_{\mathrm{SMx\text{-}MuAC}}$ are the dc and ac components of $i_{\mathrm{SMx\text{-}Mu}}$ respectively, $i_{\mathrm{SMx\text{-}MuAC1}}$ and $i_{\mathrm{SMx\text{-}MuAC2}}$ are the fundamental frequency and second-order-frequency components

The ac component in (12) and (13) will flow into the SM capacitor thus voltage ripple is generated as shown in (14) and (15), refer to [13] and [14], where, $u_{\mathrm{SM}\text{-}C}$ is the SM capacitor ripple voltage of CHB-stage. $u_{\mathrm{SM\text{-}Mu}}$ is SM capacitor ripple voltage of MMC-stage upper arm, $C_{x\text{-}C}$ and $C_{x\text{-}M}$ are the SM capacitance of CHB-stage and MMC-stage

$$u_{\mathrm{SM}-C} = U_{\mathrm{SM}-C} + \frac{m_C I\mathrm{VAC1}\sin(2\omega_F t + \varphi_C + \theta_{Cx})}{4\omega_F C_{x-C}} \tag{14}$$

$$\begin{aligned} u_{\mathrm{SM-Mu}} = {} & U_{\mathrm{SM}-M} + \frac{1}{C_{x-M}} \\ & \times \begin{bmatrix} \frac{I_{\mathrm{VAC2}}}{4\omega_F}\sin(\omega_F t + \varphi_M + \theta_{Mx}) \\ -\frac{m_M I_{\mathrm{VDC}}}{6\omega_F}\sin(\omega_F t + \theta_{Mx}) \\ -\frac{m_M I_{2\mathrm{VAC2}}}{4\omega}\sin(\omega_F t - \theta_{\mathrm{Mx}} + \theta_{2Mx}) \end{bmatrix} \\ & + \frac{1}{C_{x-M}}\Big[-\frac{m_M I_{\mathrm{VAC2}}}{16\omega}\sin(2\omega_F t + \varphi_M + 2\theta Mx) \\ & + \frac{I_{2\mathrm{VAC2}}}{4\omega_F}\sin(2\omega_F t + \theta_{2Mx})\Big]. \end{aligned} \tag{15}$$

E. SM Ripple Current Characteristics

According to (12) and (13), the vector diagrams of each frequency ripple current component of CHB-stage and MMC-stage is shown in Fig. 2. The second-order-frequency component of the SM charging current of CHB-stage and the fundamental frequency and second-order-frequency components of the SM charging current of MMC-stage show three-phase symmetry. In the CMIB-SST scheme shown in Fig. 1(a), the SM of CHB-stage and MMC-stage are interconnected by DAB and there is no connection between the three-phase SM, hence the capacitor voltage ripple caused by the ac current components of SM shown in Fig. 2 needs to be filtered by the large size capacitance as shown in Fig. 3. Alternatively, the appropriate control strategies strategy can be used to suppress the SM capacitor voltage

$$\begin{cases} i_{\mathrm{SM-Mux}} = i_{\mathrm{SM-MuDC}} + i_{\mathrm{SM-MuAC}} = \underbrace{\frac{I_{\mathrm{VDC}}}{6} - \frac{I_{\mathrm{VAC2}}m_M}{8}\cos\varphi_M}_{i_{\mathrm{SM-MDC}}} \\ + \frac{I_{\mathrm{VAC2}}}{4}\cos(\omega_F t + \varphi_M + \theta_{Mx}) - \frac{I_{\mathrm{VDC}}m_{\mathrm{M}}}{6}\cos(\omega_{\mathrm{F}} t + \theta_{Mx}) \\ \underbrace{-\frac{I_{2\mathrm{VAC2}}m_M}{4}\cos(\omega_F t - \theta_x + \theta_{2\mathrm{Mx}})}_{i_{\mathrm{SMx-MuAC1}}} \\ \underbrace{+\frac{I_{2\mathrm{VAC2}}}{2}\cos(2\omega_F t + \theta_{2\mathrm{Mx}}) - \frac{I_{\mathrm{VAC2}}m_{\mathrm{M}}}{8}\cos(2\omega_F t + \varphi_M + 2\theta_{Mx})}_{i_{\mathrm{SMx-MuAC2}}} \end{cases}. \tag{13}$$

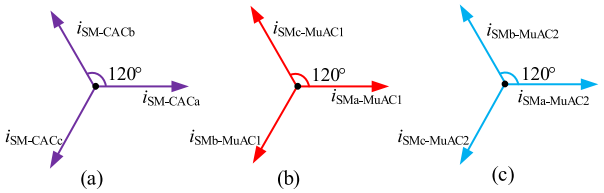

Fig. 2. Vector diagram of each-frequency AC component. (a) Second-order-frequency of CHB-stage SM. (b) Fundamental frequency comment of MMC-stage SM. (c) Second-order-frequency of MMC-stage SM.

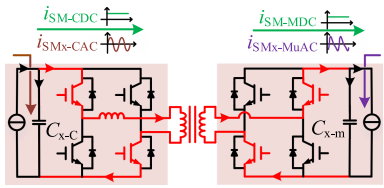

Fig. 3. SM charging current distribution between CHB-stage and MMC-stage of the CMIB-SST scheme interconnected by DAB.

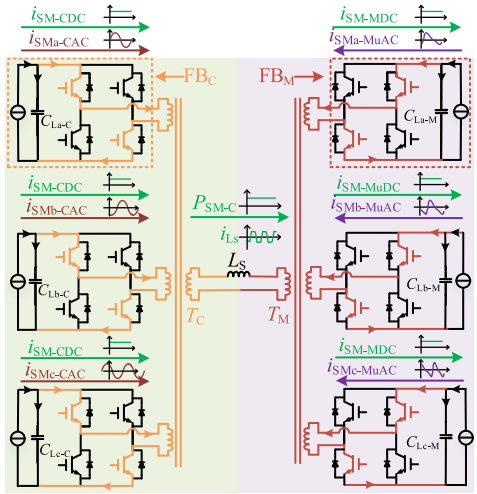

Fig. 4. STAB-stage topology and SM charging current transfer process.

ripple [12], [13] but it is usually complicated and has limited suppression effects.

III. CMIB-SST Scheme Interconnected by STAB

A. Topology Configuration of STAB

This article proposed the CMIB-SST with a STAB based isolation-stage is shown in Fig. 4 to improve performance of scheme in Fig. 1(a). The primary side of T_C and T_M is connected to FB_C and FB_M, respectively, and the secondary side is connected to the STAB inductor L_S. Full bridges FB_Cs with their high-frequency transformer (HFT) T_C are defined as the primary side of STAB-stage and full bridges FB_Ms with their HFT T_M are defined as the secondary side of STAB-stage. The CMIB-SST scheme interconnected by STAB is shown in Fig. 1(b), the three-phase SMs of CHB-stage and MMC-stage are respectively connected to the full-bridge FB_C and FB_M.

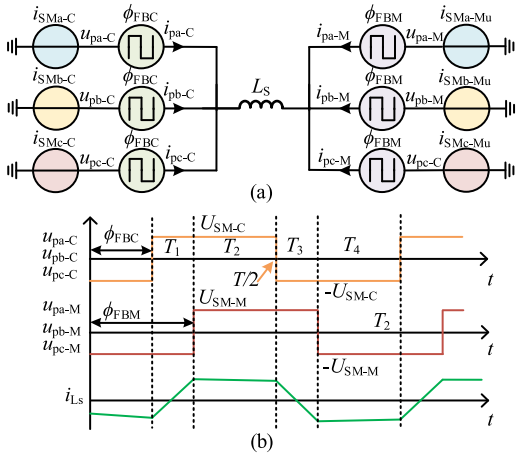

Fig. 5. Equivalent model and modulation waveforms of FB_C and FB_M under SSHPSM method. (a) Equivalent model of STAB. (b) Equivalent modulation waveforms of SSHPSM method.

For the purpose of SM capacitance minimization design of CMIB-SST scheme, the SSHPSM method is proposed in this article. Under the SSHPSM method of the STAB, the low-frequency ripple currents between the three-phase SMs of CHB-stage and MMC-stage will be decoupled with the SM capacitors and transfer to the primary sides of transformers T_C and T_M which will be cancelled based on the three-phase symmetry, so as to reduce the SM capacitance of both AC/DC-stages. The SSHPSM method is studied in Section III-B, and the transmission and cancellation process of low-frequency ripple current are also analyzed in Section III-C.

B. Modulation Method of STAB

Neglecting the switching-frequency components of $i_{SM\text{-}Cx}$ and $i_{SM\text{-}Mux}$, the CHB-stage and the MMC-stage both can be equivalent to a current source which is composed of a dc current source superimposed with a low frequency AC current source. Then the equivalent model of STAB-stage is shown as Fig. 5(a), where $u_{px\text{-}C}$ and $i_{px\text{-}C}$ are the equivalent modulation voltages and currents of the FB_Cs, $u_{px\text{-}M}$ and $i_{px\text{-}M}$ are the equivalent modulation voltages and currents of the FB_Ms. The SSHPSM method is shown in Fig. 5(b), the phase-angles of three FB_Cs are all ϕ_{FBC}, the phase-angles of three FB_Ms are all ϕ_{FBM}. All the duty ratio of six gate signals is 0.5.

With the proposed SSHPSM method, in a switching cycle, the STAB has four phases $T_1 \sim T_4$, and $T_1+T_2 = T_3+T_4$. In T_1, as shown in Fig. 6(a), all the three FB_Cs are equivalent connected in parallel and the terminal voltage of T_C is $U_{SM\text{-}C}$, all the three FB_Ms are equivalent connected in parallel and the terminal voltage of T_M is $-U_{SM\text{-}M}$; In other phases, the equivalent parallel characteristics are still satisfied, and the transformer terminal voltage is summarized as follows: In T_2, the terminal voltage of T_C is $U_{SM\text{-}C}$, the terminal voltage of T_M is $U_{SM\text{-}M}$; In T_3, the terminal voltage of T_C is $-U_{SM\text{-}C}$, the terminal voltage of T_M is $U_{SM\text{-}M}$; In T_4, the terminal voltage of T_C is $-U_{SM\text{-}C}$, the terminal voltage of T_M is $-U_{SM\text{-}M}$. The equivalent model of

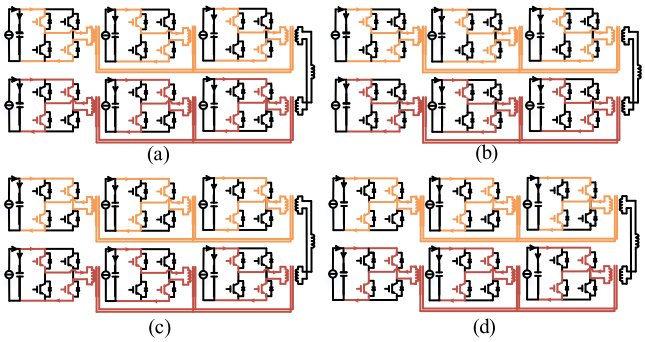

Fig. 6. Equivalent models of HFL of STAB-stage primary and secondary sides. (a) T_1. (b) T_2. (c) T_3. (d) T_4.

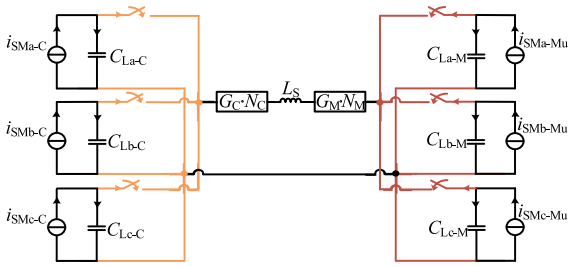

Fig. 7. Equivalent model of switched-capacitor circuits.

high frequency link (HFL) established by the three-phase SM capacitors of CHB and MMC-stages and primary and secondary side H-bridges of STAB-stage is shown in Fig. 6.

The phase-shift angle between FB$_C$ and FB$_M$ is $\phi = \phi_{\mathrm{FBC}} - \phi_{\mathrm{FBM}}$, the active power transfer between the primary and secondary sides of STAB-stage is controlled by the phase shift modulation and the inductor current i_{Ls} is shown as Fig. 5(b).

It can be seen from Fig. 6 that the three-phase SM capacitors are interconnected by the full bridges with their transformer primary windings of T_C and T_M of STAB-stage in each half duty cycle and form the switched-capacitor circuits, so the FB$_C$s and FB$_M$s of STAB-stage operate in switched-capacitor mode as shown in Fig. 7, where N_C and N_M are the transformer turns ratio of the T_C and T_M. G_C and G_M are voltage conversion gains in different time periods, in T_1, G_C is 1, G_M is -1; in T_2, G_C is 1, G_M is 1; in T_3, G_C is -1, G_M is 1; in T_4, G_C is -1, G_M is -1. In Fig. 7, the three-phase SMs are equivalent connected in parallel and their voltages are same at the steady-state stage of the half duty cycle.

C. Ripple Current Elimination by STAB

In the switched-capacitor circuits equivalent model as shown in Fig. 7, the SM charging currents $i_{\mathrm{SM}x\text{-}C}$ and $i_{\mathrm{SM}x\text{-}Mu}$ consist of the dc component $i_{\mathrm{SM\text{-}CDC}}$, $i_{\mathrm{SM\text{-}MuDC}}$ and ac component $i_{\mathrm{SMx\text{-}CAC}}$, $i_{\mathrm{SM}x\text{-}\mathrm{MuAC}}$. For the dc component, the SM capacitance impedance tends to infinity, so the dc power is transferred between the primary and secondary sides of STAB-stage.

For the ac component, the analysis of the ripple current transmission process is as follows. Considering the influence of leakage impedance, the equivalented circuit of Fig. 7 is shown in

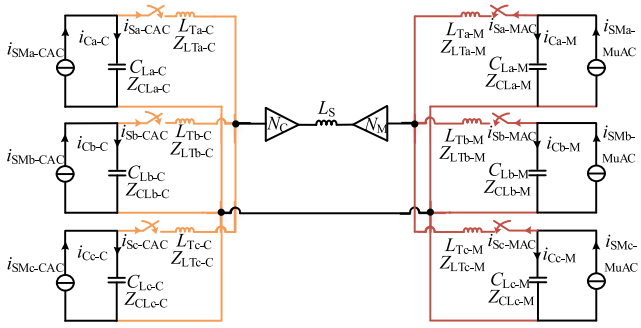

Fig. 8. Equivalent model of switched-capacitor circuits considering leakage inductance.

Fig. 8, where $L_{Tx\text{-}C}$, $Z_{Tx\text{-}C}$, and $L_{Tx\text{-}M}$, $Z_{Tx\text{-}M}$ are the leakage inductance and the leakage inductance impedance of the T_C and T_M primary sides, respectively, and $Z_{Tx\text{-}C} = j\omega L_{Tx\text{-}C}$, $Z_{Tx\text{-}M} = j\omega L_{Tx\text{-}M}$. $C_{Lx\text{-}C}$, $Z_{CLx\text{-}C}$ and $C_{Lx\text{-}M}$, $Z_{CLx\text{-}M}$ are the SM capacitance and the capacitance impedance of the CHB-stage and MMC-stage respectively, and $Z_{CLx\text{-}C} = 1/j\omega C_{Lx\text{-}C}$, $Z_{CLx\text{-}M} = 1/j\omega C_{Lx\text{-}M}$, ω is any angular frequency.

Take the phase-x SM of CHB-stage as an example, defining set $P = \{a, b, c\}$ and $x, y, z \in P$, then the equivalent input impedance of the phase-x of STAB-stage primary side is defined as Z_{ex} shown in (16), at the bottom of the next page, which includes the $Z_{\mathrm{LT}x\text{-}C}$ of phase-x and $Z_{CLy\text{-}C}$ and $Z_{\mathrm{LT}y\text{-}C}$ of the other two phases. The ripple-current $i_{\mathrm{SM}x\text{-CAC}}$ flowing into the SM capacitor and STAB-stage primary side are defined as $i_{Cx\text{-CAC}}$ and $i_{Sx\text{-CAC}}$, respectively. According to the relationship between Z_{Cx} and Z_{ex}, $i_{\mathrm{C}x\text{-CAC}}$ and $i_{\mathrm{S}x\text{-CAC}}$ can be expressed as (17)

$$\begin{cases} i_{SMx-CAC} = i_{Cx-CAC} + i_{Sx-CAC} \\ i_{Cx-CAC} = i_{SMx-CAC} \times Z_{ex} / \left(Z_{CLx-C} + Z_{ex}\right) \\ i_{Sx-CAC} = i_{SMx-CAC} \times Z_{CLx-C} / \left(Z_{CLx-C} + Z_{ex}\right) \end{cases} . \tag{17}$$

For Fig. 8, taking phase-x as an example, $i_{\mathrm{SM}x\text{-CAC}}$ of the other two-phases is set to be open circuits, $i_{Sx\text{-CAC}y}$ is the currents flowing into other two phases from the equivalent ac current source $i_{\mathrm{Sx\text{-}CAC}}$, which can be expressed as

$$\begin{cases} i_{Sx-CAC} = \sum_{y \in P, y \neq x} i_{Sx-CACy} \\ i_{Sx-CACy} = \frac{i_{Sx-CAC} \times \left(Z_{LTz-C} + Z_{CLz-C}\right)}{Z_{LTy-C} + Z_{LTz-C} + Z_{CLy-C} + Z_{CLz-C}}, z \neq y \neq x \end{cases} . \tag{18}$$

Taking phase-a as an example, according to the superposition theorem, the response of $i_{\mathrm{Ca\text{-}C}}$ is equal to the algebraic sum of the response of $i_{\mathrm{Ca\text{-}CAC}}$, $i_{\mathrm{Sb\text{-}CACa}}$ and $i_{\mathrm{Sc\text{-}CACa}}$ by considering the equivalent ac current sources of phase-a, b and c which can be expressed as

$$\begin{aligned} i_{Ca-C} &= i_{Ca-CAC} + i_{Sb-CACa} + i_{Sc-CACa} \\ &= \frac{i_{SMa-CAC} Z_{ea}}{Z_{CLa-C} + Z_{ea}} + \frac{i_{SMb-CAC} Z_{CLb-C}}{Z_{CLb-C} + Z_{eb}} \\ &\quad \cdot \frac{Z_{LTc-C} + Z_{CLc-C}}{Z_{LTa-C} + Z_{LTc-C} + Z_{CLa-C} + Z_{CLc-C}} \end{aligned}$$

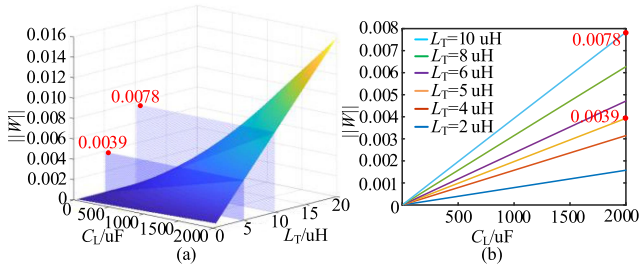

Fig. 9. Proportion of ripple current flowing into the SM capacitor in SM ripple current varies with C_L and L_T. (a) Three-dimensional view. (b) Two-dimensional view.

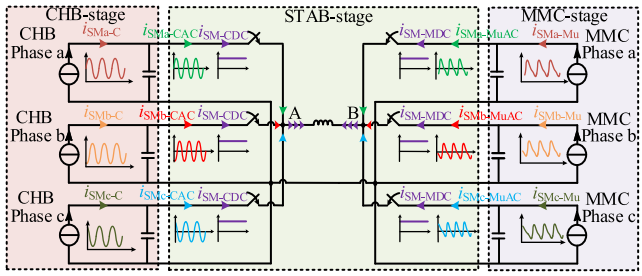

Fig. 10. Transfer process of ripple current based on switched-capacitor circuits.

$$+\frac{i_{SMc-CAC}Z_{CLc-C}}{Z_{CLc-C}+Z_{ec}}\cdot\frac{Z_{LTb-C}+Z_{CLb-C}}{Z_{LTa-C}+Z_{LTb-C}+Z_{CLa-C}+Z_{CLb-C}} \quad (19)$$

Assuming the parameters of the SM capacitance and leakage inductance of HFT are consistent, that are, $Z_{CLa\text{-}C}=Z_{CLb\text{-}C}=Z_{CLc\text{-}C}=1/j\omega_{2nd}C_L$, $Z_{LTa\text{-}C}=Z_{LTb\text{-}C}=Z_{LTc\text{-}C}=j\omega_{2\mathrm{nd}}L_T$, $\omega_{2\mathrm{nd}}$ is the second-order angular frequency. To focus the second-order-frequency ripple voltage depression, $i_{Ca\text{-}C}$ in (19) can be rewritten as (20) combined with (12) considering second-order-frequency component, the definition W represents the gain factor of the second-order-frequency ripple current flowing into the SM capacitor

$$\begin{aligned} i_{Ca-C}&=i_{Ca-CAC}+i_{Sb-CACa}+i_{Sc-CACa}\\ &=i_{SMa-CAC}\cdot\frac{1}{1+\frac{1}{w_{2nd}^2L_TC_L}}=i_{SMa-CAC}\times W. \end{aligned} \quad (20)$$

According to (20), the $\|W\|$ varies with C_L and L_T is shown in Fig. 9. It can be seen that the ripple current cannot completely decouple with the SM capacitor indeed, but it might be very small or even the impact can be neglected considering the value of the leakage inductance parameter. For example, $\|W\|$ is less than 0.008 when L_T is less than 10 uH, and $\|W\|$ is less than 0.004 when L_T is less than 5uH as shown in Fig. 9(b). Therefore, the leakage inductance of the HFT of STAB-stage is need to be designed as small as possible so that the $i_{Ca\text{-}C}$ approaches zero which means that the ripple current $i_{\mathrm{SM}x\text{-}\mathrm{CAC}}$ is completely decoupled with the SM capacitor and transferred to the primary side of T_C of STAB-stage based on the low impedance characteristics of equivalent connected in parallel without the additional ripple power transfer control.

The SM low-frequency ripple current of MMC-stage is transmitted to the primary side of T_M based on the same principle. Low-frequency AC component $i_{\mathrm{SM}x\text{-}\mathrm{CAC}}$ flows into point "A" and $i_{\mathrm{SM}x\text{-}\mathrm{MuAC}}$ flows into point "B" in the switched-capacitor circuits and are both cancelled based on the three-phase symmetry, therefore, only active power is transferred between the primary and secondary sides of STAB-stage as shown in Fig. 10.

D. Influence of the Primary Side Leakage Inductance Inconsistency in HFT

Generally, assuming the parameters of the SM capacitance are consistent, that is, $Z_{CLa\text{-}C}=Z_{CLb\text{-}C}=Z_{CLc\text{-}C}=1/j\omega_{2nd}C_L$ considering second-order-frequency component. But the leakage inductance of each winding cannot be exactly the same in practical. Supposing that $\Delta L_{\mathrm{T}1}$ is the difference value between $L_{Ta\text{-}C}$ and $L_{Tb\text{-}C}$, and ΔL_{T2} is the difference value between $L_{Ta\text{-}C}$ and $L_{Tc\text{-}C}$, then the leakage inductance impedance of the CHB-stage transformer can be rewritten as $Z_{LTa\text{-}C}=j\omega_{2\mathrm{nd}}L_{Ta}$, $Z_{LTb\text{-}C}=j\omega_{2\mathrm{nd}}(L_{Ta}+\Delta L_{\mathrm{T}1})$, $Z_{LTc\text{-}C}=j\omega_{2\mathrm{nd}}(L_{Ta}+\Delta L_{\mathrm{T}2})$, $i_{\mathrm{Ca\text{-}CAC}}$ and $i_{\mathrm{Sa\text{-}CAC}}$ in (17) can be further expressed as (21), shown at the bottom of the next page, and the ripple currents $i_{Sb\text{-}CACa}$ and $i_{Sc\text{-}CACa}$ from phase-b and phase-c to phase-a respectively can be written as (22):

$$\begin{cases} i_{Sb-CACa}=i_{Sb-CAC}\frac{\omega_{2nd}^2C_L(L_{Ta}+\Delta L_{T2})+1}{\omega_{2nd}^2C_L(2L_{Ta}+\Delta L_{T2})+2}\\ i_{Sc-CACa}=i_{Sc-CAC}\frac{\omega_{2nd}^2C_L(L_{Ta}+\Delta L_{T1})+1}{\omega_{2nd}^2C_L(2L_{Ta}+\Delta L_{T1})+2} \end{cases}. \quad (22)$$

The above analysis is also applied to MMC-stage. According to the small leakage design requirement in Section III-C and manufacturing technique of the transformer in practical high-power application [16], the range of L_{Ta} is set as 1∼10 uH, the maximum value of ΔL_{T1} and ΔL_{T2} are set to 50% of the L_{Ta}. In order to simplify the analysis of the influence of inconsistent primary leakage inductance of the transformer on ripple current

$$Z_{\mathrm{ex}}=\frac{\left[\begin{array}{l} Z_{\mathrm{LT}x-C}\sum\limits_{y\in P,y\neq x}(Z_{\mathrm{LT}y-C}+Z_{\mathrm{CL}y-C})+\\ \sum_{y,z\in P,z\neq y\neq x}(Z_{\mathrm{LT}y-C}Z_{\mathrm{CLz}-C})+\prod_{y\in P,y\neq x}Z_{\mathrm{LT}y-C}+\prod_{y\in P,y\neq x}Z_{\mathrm{CL}y-C} \end{array}\right]}{\sum_{y\in \mathrm{P},y\neq x}(Z_{\mathrm{LT}y-C}+Z_{\mathrm{CL}y-C})} \quad (16)$$

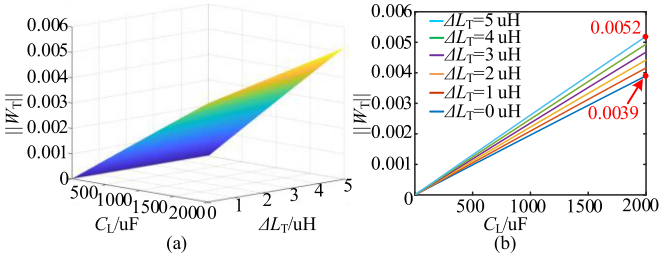

Fig. 11. Proportion of ripple current flowing into the SM capacitor in SM ripple current varies with C_L and ΔL_T. (a) Three-dimensional view. (b) Two-dimensional view.

decoupling, L_{Ta} is set as 5uH, $\Delta L_{T1} = \Delta L_{T2} = \Delta L_T$ and the maximum value is 5uH which means the maximum value of L_{Tb} and L_{Tc} is 10 uH. The $i_{Ca\text{-}C}$ in (19) can be rewritten as (23) combined with (12), (21) and (22), the definition W_T represents the gain factor of the second-order-frequency ripple current flowing into the SM capacitor considering the leakage inductance inconsistency

$$\begin{aligned} i_{Ca-C} &= i_{Ca-CAC} + i_{Sb-CACa} + i_{Sc-CACa} \\ &= i_{\mathrm{SM}a-CAC} \cdot \frac{1}{1 + \frac{3}{\omega_{2\mathrm{nd}}^2 C_L (3L_{Ta} + \Delta L_T)}} \\ &= i_{\mathrm{SMa-CAC}} \cdot W_T. \end{aligned} \tag{23}$$

According to (23), the $\|W_T\|$ varies with C_L and ΔL_T is shown in Fig. 11. It can be seen that when the primary side leakage inductance of the transformer is consistent, that is, $\Delta L_T = 0$, the gain factor $\|W_{\mathrm{T}}\| = \|W\| = 0.0039$ corresponding to L_T of 5 uH as shown in Fig. 9. When the leakage inductance difference between the primary side windings increases to 5 uH, $\|W_T\|$ increases from 0.0039 to 0.0052 as shown in Fig. 11(b), the variation trend is consistent with Fig. 9, and the impact of leakage inductance inconsistency can be neglected when the leakage inductance is reduced as small as possible in design.

IV. Parameter Constraint and Performance Evaluation of Two Schemes

The performance of the CMIB-SST scheme interconnected by DAB and the CMIB-SST scheme interconnected by STAB are compared from the evaluated units shown in Fig. 12, including three-phase SMs, DAB and STAB switches, inductors and transformers which account for the largest proportion of the system volume. The variables and components parameters given in Table I.

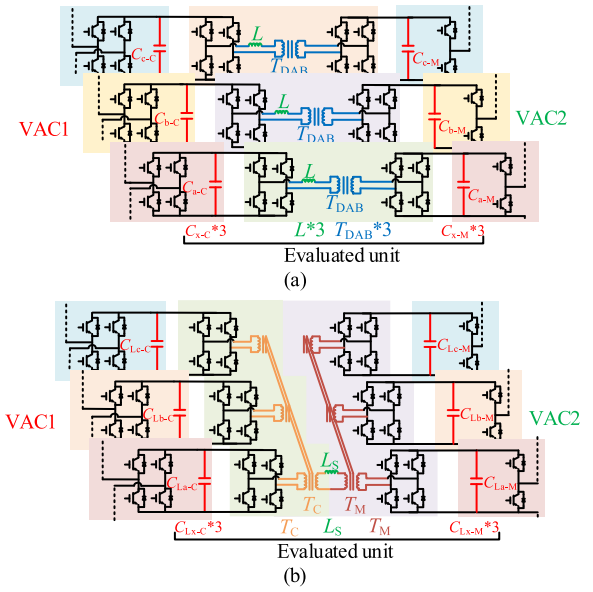

Fig. 12. The comparison of evaluated units of two schemes. (a) CMIB-SST scheme interconnected by DAB. (b) CMIB-SST scheme interconnected by STAB.

A. Current Stress Assessment and Switch Selection

In the evaluated units as shown in Fig. 12, the current stresses of CHB-stage and MMC-stage SM under the two schemes are consistent and can be evaluated according to (12) and (13). The DAB-stage and STAB-stage current stresses can be evaluated by the transformer peak current. The CMIB-SST scheme interconnected by STAB transfers the SM ripple current from the CHB and MMC-stages to the primary side of the HFT of STAB-stage, so that the transformer suffers a larger peak current compared with the CMIB-SST scheme interconnected by DAB.

$$\begin{cases} i_{Ca-CAC} \\ = i_{\mathrm{SM}a-CAC} \left(\dfrac{\left[\begin{array}{l} \omega_{2nd}^4 C_L^2 \left(3L_{Ta}^2 + 2L_{Ta}\Delta L_{T1} + 2L_{Ta}\Delta L_{T2} + \Delta L_{T1}\Delta L_{T2}\right) \\ + \omega_{2nd}^2 C_L \left(4L_{Ta} + \Delta L_{T1} + \Delta L_{T2}\right) + 1 \end{array} \right]}{\left[\begin{array}{l} \omega_{2nd}^4 C_L^2 \left(3L_{Ta}^2 + 2L_{Ta}\Delta L_{T1} + 2L_{Ta}\Delta L_{T2} + \Delta L_{T1}\Delta L_{T2}\right) \\ + 2\omega_{2nd}^2 C_L \left(3L_{Ta} + \Delta L_{T1} + \Delta L_{T2}\right) + 3 \end{array} \right]} \right) \\ i_{Sa-CAC} \\ = i_{\mathrm{SM}a-CAC} \left(\dfrac{\omega_{2nd}^2 C_{\mathrm{L}} (2L_{Ta} + \Delta L_{T1} + \Delta L_{T2}) + 2}{\left[\begin{array}{l} \omega_{2nd}^4 C_L^2 \left(3L_{Ta}^2 + 2L_{Ta}\Delta L_{T1} + 2L_{Ta}\Delta L_{T2} + \Delta L_{T1}\Delta L_{T2}\right) \\ + 2\omega_{2nd}^2 C_L \left(3L_{Ta} + \Delta L_{T1} + \Delta L_{T2}\right) + 3 \end{array} \right]} \right) \end{cases} \tag{21}$$

TABLE I
PARAMETERS

Parameters	CMIB-SST
CHB-stage	
VAC1 rated active power/P_{VAC1}	12 MW
RMS of line voltage/$U_{\mathrm{Lrms\text{-}C}}$	35 kV
SM capacitor voltage/$U_{\mathrm{SM\text{-}C}}$	750 V
PWM carrier frequency/f_{C}	2 kHz
SM capacitance/$C_{\mathrm{x\text{-}C}}$, $C_{\mathrm{Lx\text{-}C}}$	10 mF, 1.2 mF
MMC-stage	
VAC2 rated active power/P_{VAC2}	10 MW
VDC power/P_{VDC}	2 MW
RMS of line voltage/$U_{\mathrm{Lrms\text{-}M}}$	10 kV
VDC voltage/U_{VDC}	18 kV
Number of SM of per arm/n	24
SM capacitor voltage/$U_{\mathrm{SM\text{-}M}}$	750 V
PWM carrier frequency/f_{M}	2 kHz
SM capacitance/$C_{\mathrm{x\text{-}M}}$, $C_{\mathrm{Lx\text{-}M}}$	16 mF, 1.8 mF
Isolation-stage	
Active power/P_{DAB}, P_{STAB}	0.08 MW, 0.25 MW
Transformer turns ratio/N, $N_{\mathrm{C,M}}$	1:1, 1:1:1:1
Inductance /L, L_{S}	56.25 uH, 18.75 uH
Switching frequency/f_{D}, f_{S}	10 kHz

TABLE II
SWITCHING CURRENT STRESS EVALUATION AND DEVICE SELECTION UNDER DIFFERENT SCHEMES

Switch position	CMIB-SST (DAB)	CMIB-SST (STAB)
CHB-stage switching current stress	250A	
Switch model	FF400R12KT3	
Volume	0.2dm^3	
Cost	$260	
MMC-stage switching current stress	500A	
Switch model	FF800R12KE7	
Volume	0.2dm^3	
Cost	$358	
DC/DC-stage primary side switching current stress	150A	400A
Switch model	FF300R12KE4	FF600R12KE4
Volume	0.2dm^3	0.2dm^3
Cost	$193	$314
DC/DC-stage secondary side switching current stress	150A	500A
Switch model	FF300R12KE4	FF800R12KE7
Volume	0.2dm^3	0.2dm^3
Cost	$193	$358

Under the parameters in Table I, the primary and secondary side currents of the DAB transformer are shown in (24), the capacitor voltage $U_{\mathrm{SM\text{-}C}}$ and $U_{\mathrm{SM\text{-}M}}$ of CHB and MMC stages are equal and defined as U_{SM}, and the maximum value of the primary and secondary side transformer currents I_{PM} and I_{SM} are expressed as (25) [17]

$$i_{px-C(\mathrm{DAB})} = i_{px-M(\mathrm{DAB})} = \frac{NU_{\mathrm{SM}}}{2\pi^2 f_D L}\phi\left(\pi-\phi\right) \tag{24}$$

$$I_{\mathrm{PM}} = I_{\mathrm{SM}} = \frac{nU_{\mathrm{SM}} - U_{\mathrm{SM}}\left(1-2\phi/\pi\right)}{4f_D L}. \tag{25}$$

The transformer current at the primary and secondary sides of STAB-stage is shown in (26) at the bottom of this page, based on double Fourier transformation and Taylor expansion, where ω_S is switching angular frequency of STAB-stage, I_{Ls} is the maximum value of STAB inductor current, which can also be evaluated according to (25). The low-frequency components exist with the form of sideband harmonics in the primary side high-frequency modulation currents of HFT which leads to the increasement of the STAB switching current stress

The SM switches are evaluated according to (12) and (13), and DAB-stage and STAB-stage switches are evaluated according to (25) and (26). The switch current stress, switch model, and specification parameters in the evaluated units of Fig. 12 are given in Table II, the switch selection is based on Infineon's IGBT for high-power and current applications, the cost data of the switch comes from Digi-Key Electronics. The current stress of the CHB and MMC-stages switches in the CMIB-SST scheme interconnected by STAB are consistent with the CMIB-SST scheme interconnected by DAB, so the same model of switch is adopted. The current stress of primary and secondary side switches of STAB-stage is larger than that of DAB-stage, therefore, switches with higher current stress should be adopted in STAB-stage, but the volume of switches with higher current stress does not change and the switch volume accounts for

$$\begin{cases} i_{px-C(\mathrm{STAB})} = \underbrace{\dfrac{2I_{\mathrm{VAC1}}m_C}{\pi}\sum_{j=1}^{\infty}\dfrac{\sin\left[\left(2j-1\right)\omega_S t\right]}{2j-1}}_{\mathrm{Activecurrent}} \\ \quad + \underbrace{\dfrac{I_{\mathrm{VAC1}}m_C}{\pi}\sum_{j=1}^{\infty}\dfrac{\cos\left[\left[\left(2j-1\right)\omega_S \pm 2\omega_F\right]t+\theta_x\right]}{2j-1}}_{2^{\mathrm{nd}}-\mathrm{order}-\mathrm{frequency sideband harmonics}} \\ i_{\mathrm{px-M(STAB)}} = \underbrace{\dfrac{4I_{\mathrm{Ls}}}{3\pi}\sum_{j=1}^{\infty}\dfrac{\sin\left[\left(2j-1\right)\omega_S t\right]}{2j-1}}_{\mathrm{Activecurrent}} \\ \quad + \underbrace{\left(\dfrac{I_{\mathrm{VAC2}}m_M}{2\pi}-\dfrac{I_{\mathrm{VDC}}m_M}{3\pi}\right)\sum_{j=1}^{\infty}\dfrac{\cos\left[\left[\left(2j-1\right)\omega_S \pm \omega_F\right]t+\theta_x\right]}{2j-1}}_{\mathrm{Fundamental sideband harmonics}} \\ \quad + \underbrace{\dfrac{I_{\mathrm{VAC2}}m_M}{4\pi}\sum_{j=1}^{\infty}\dfrac{\cos\left[\left[\left(2j-1\right)\omega_S \pm 2\omega_F\right]t+\theta_x\right]}{2j-1}}_{2^{\mathrm{nd}}-\mathrm{order}-\mathrm{frequency sideband harmonics}} \end{cases}. \tag{26}$$

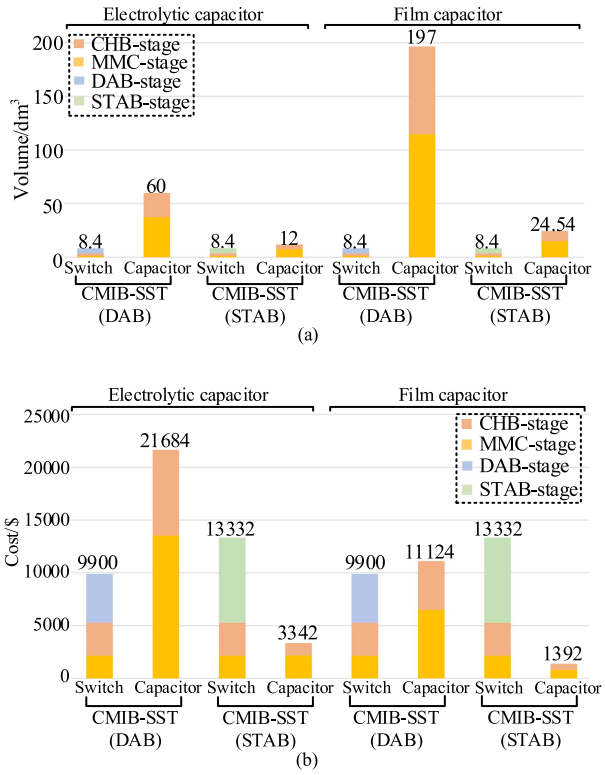

Fig. 13. Comparison of switch and SM capacitor volume and cost of two schemes. (a) Volume. (b) Cost.

a relatively small proportion in the total system volume as shown in Fig. 13(a), and the cost only increases by 26% as shown in Fig. 13(b) in the evaluated units as shown in Fig. 12. However, combined with the subsequent SM capacitor design of Section IV-B, the capacitance minimizing brings significant advantages to the system. As shown in Fig. 13(a) and (b), when electrolytic capacitor is adopted, the volume and cost of the SM capacitors are reduced by 80% and 85%. When film capacitor is adopted the cost and volume of the SM capacitors are reduced by 87.5% and 87.5% as shown in Fig. 13(a) and (b). The proposed CMIB-SST scheme interconnected by STAB still has great advantages.

B. Constraints of SM Capacitors

Large capacitance is required for the SM of the CMIB-SST scheme interconnected by DAB shown in Fig. 1(a) to suppress the low-frequency voltage ripple of CHB-stage and MMC-stage shown in (14) and (15), the capacitance constraint of CHB-stage can be derived from [13] as

$$C_{x-C} \geq \frac{m_C I_{\mathrm{VAC1}}}{4\varepsilon U_{\mathrm{SM}-C}\pi f_F} \tag{27}$$

where $C_{x\text{-}C}$ is the SM capacitance constraint of the CHB-stage of the CMIB-SST scheme interconnected by DAB, f_F is the fundamental frequency, ε is the voltage ripple coefficient. The SM capacitor of the MMC-stage needs to smooth the DC voltage and absorb the fundamental-frequency and second-order-frequency voltage ripple. The capacitance constraint of MMC-stage can be obtained according to [18] as

$$C_{x-M} \geq \frac{P\left(1-\left(\frac{m_M\cos\varphi_M}{2}\right)^2\right)^{\frac{3}{2}}}{6nm_M U^2_{\mathrm{SM}-M}\varepsilon\pi f_F\cos\varphi_M} \tag{28}$$

where $C_{x\text{-}M}$ is the SM capacitance constraint of MMC-stage of the CMIB-SST scheme interconnected by DAB, P is the real power transferred.

According to the analysis in Section III-C, after the low frequency ripple current is eliminated, the SM capacitors of the CMIB-SST scheme interconnected by STAB shown in Fig. 1(b) only need to absorb the switching harmonics generated by the SMs of CHB-stage and MMC-stage and the full bridges of STAB-stage during the pulse width modulation process. Since the switching frequency of the STAB-stage is much higher than that of the CHB-stage and MMC-stage, the harmonic current need to be handled by the SM capacitor mainly comes from the latter. Taking the CHB-stage as an example, the charging energy of the SM capacitor in a switching cycle is

$$\Delta E_{\mathrm{SM}} = \frac{i_{\mathrm{SMx-CACmax}} D_{\mathrm{SM}}}{f_C} \tag{29}$$

where D_{SM} is the duty ratio of the switches in the SM full-bridge which maximum value is equal to m_C and less than 1, f_C is the switching frequency of CHB-stage. And the capacitance voltage ripple caused by ΔE_{SM} is (30), where the $C_{Lx\text{-}C}$ is the small capacitance of CHB-stage:

$$\varepsilon U_{\mathrm{SM}-C} = \frac{\Delta E_{\mathrm{SM}}}{C_{Lx-C}} = \frac{m_C i_{SMx-\mathrm{Cmax}}}{C_{Lx-C} f_C}. \tag{30}$$

Therefore, the new capacitance constraint of CHB-stage SM is

$$C_{Lx-C} \geq \frac{I_{\mathrm{VAC1}} m_C^2}{2\varepsilon U_{\mathrm{SM}-C} f_C}. \tag{31}$$

And similarly, the new capacitance constraint of MMC-stage SM can be similarly obtained as

$$C_{Lx-M} \geq \frac{m_M i_{\mathrm{SMx-MuACmax}}}{\varepsilon U_{\mathrm{SM}-M} f_M} = \frac{(1+2m_M^2) I_{\mathrm{VAC2}}}{16\varepsilon U_{\mathrm{SM}-M} f_M} \tag{32}$$

where when the low-frequency ripple is suppressed and the influence of $I_{2\mathrm{VAC2}}$ is neglected, according to [19], the $\theta_{2\mathrm{Mx}}$ tends to zero when φ_{Mx} tends to zero, considering the maximum current condition, that is the I_{VDC} is equal to zero, $i_{\mathrm{SMx\text{-}MuACmax}}$ can be calculated by taking the extreme value of (13).

In conclusion, the SM capacitance constraints of the CHB-stage and MMC-stage of the CMIB-SST scheme interconnected by DAB are in (27) and (28) respectively, the SM capacitance constraints of the CHB-stage and MMC-stage of the CMIB-SST scheme interconnected by STAB are in (31) and (32).

Based on the parameters in Table I and the constrains of SM capacitance under two schemes, the SM capacitor specifications are given in Table III, the parameter of capacitor is based on TDK's electrolytic capacitor and film capacitor, the cost data of capacitor comes from Mouser Electronics. The volume and cost of the capacitors in evaluated units are compared as shown in Fig. 14. It can be seen that when electrolytic capacitors are used, the volume of SM capacitors in the CMIB-SST scheme

TABLE III
SM CAPACITOR PARAMENTS AND SPECIFICATIONS

		CMIB-SST (DAB)	CMIB-SST (STAB)
Electrolytic capacitor			
CHB-stage	SM voltage	750 V	750 V
	$C_{x\text{-}C}$, $C_{Lx\text{-}C}$	10 mF	1.2 mF
	Model	B43720B8688M000	B43700B8278M000
	Specification	6.8 mF/600 V	2.7 mF/600 V
	Composition	Two in series form a group, three groups in parallel	Two in series
	Volume	1.25dm^3*6=7.5dm^3	0.76dm^3*2=1.52dm^3
	Cost	\$451*6=\$2706	\$193*2=\$386
MMC-stage	$C_{x\text{-}C}$, $C_{Lx\text{-}C}$	16 mF	1.8 mF
	Model	B43720B8688M000	B43700B8228M000
	Specification	6.8 mF/600 V	2.2 mF/600 V
	Composition	Two in series form a group, five groups in parallel	Two in series form a group, two groups in parallel
	Volume	1.25 dm^3*10=12.5 dm^3	0.62 dm^3*4=2.48 dm^3
	Cost	\$451*10=\$4510	\$182*4=\$728
Film capacitor			
CHB-stage	Model	B25690C1248K203	A: B25690A1108K203 B: B25690A1307K201
	Specification	2.4mF/1200V	A:1mF/1200V B:0.3mF/1200V
	Composition	Five in parallel	A and B are in parallel
	Volume	5.46 dm^3*5=27.3 dm^3	2.49 dm^3+0.71dm^3=3.2 dm^3
	Cost	\$309*5=\$1545	\$134+\$62=\$196
MMC-stage	Model	B25690C1248K203	B25690A1108K203
	Specification	2.4mF/1200V	1mF/1200V
	Composition	Seven in parallel	Two in parallel
	Volume	5.46 dm^3*7=38.22 dm^3	2.49 dm^3*2=4.98 dm^3
	Cost	\$309*7=\$2163	\$134*2=\$268

TABLE IV
MAGNETIC CORE SPECIFICATION OF TRANSFORMERS

	T_{DAB}*3	T_C, T_M
Single specification	CN-200*100*60*35	CN-305*130*40*60
Staking thickness/A[mm]	60	40
Window width/B[mm]	100	130
Window length/C[mm]	200	305
Height/D[mm]	35	60
Mean path length/Le[cm]	78.9	99.5
Iron cross section/Ae[cm^2]	16.8	19.2

interconnected by STAB is reduced by 80% compared with the CMIB-SST scheme interconnected by DAB, and the cost is reduced by 85%. When the film capacitors are used, the volume of SM capacitors in the CMIB-SST scheme interconnected by STAB is reduced by 87.5% compared with the CMIB-SST scheme interconnected by DAB and the cost is reduced by 87.5%.

C. Design of Magnetic Elements

The transformer structure and isolation structure of two-winding transformer T_{DAB} of DAB and the four-winding transformers T_C and T_M of STAB are shown in Fig. 15. The specifications of magnetic cores are given in Table IV.

The winding configure of DAB transformer and STAB are shown in in Fig. 15. The gap from shell to the surface of the magnetic core is defined as d_{shell} and d_{shell1} is named for the VAC1 side and d_{shell2} is named for the VAC2 side; d_{cw} is the insulation distance between the iron yoke and the winding;

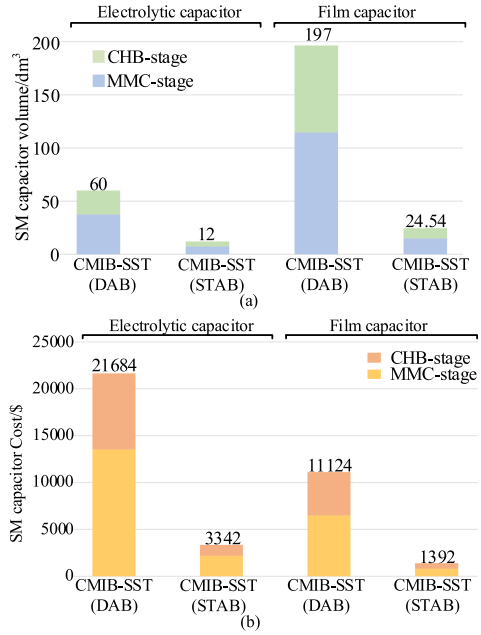

Fig. 14. Histogram of the SM capacitor volume and cost comparison. (a) Volume. (b) Cost.

TABLE V
ISOLATION VOLTAGE LEVEL AND INSULATION DISTANCE

	T_{DAB}	T_C	T_M
d_{shell1}	70 kV/6 mm	70 kV/6 mm	—
d_{shell2}	35 kV/3 mm	—	35 kV/3 mm
d_{ps}	70 kV/6 mm	70 kV/6 mm	35 kV/3 mm
d_{pp}	—	70 kV/6 mm	35 kV/3 mm
d_{cw}	70 kV/6 mm	70 kV/6 mm	35 kV/3 mm

d_{gap} and d_{cp} can be set as the minimum which are limited by the skeleton of the transformer in practice; d_{ps} is the insulation distance between the primary and secondary side windings of T_{DAB}, T_C and T_M; d_{pp} is the insulation distance between the adjacent primary side windings of T_C and T_M; The insulation distance can be calculated as

$$d_{\mathrm{ins}} = \frac{V_{\mathrm{ref}}}{K_{\mathrm{ins}} E_{\mathrm{ins}}} \tag{33}$$

where V_{ref} is low-frequency voltage isolation level in the transformer design considering the long-term operation of the transformer, refer to IEEE Std. C57.12.01[20]. E_{ins} is the dielectric constant of the insulation material which is 23.8 kV/mm in the case of epoxy resin, k_{ins} is a coefficient representing the insulation margin which is 0–1. The isolation voltage level and insulation distance of each transformer are given in Table V.

Finite-element method (FEM) simulations are carried out to verify the insulation distance design of the T_{DAB}, T_C, and T_M. The distribution of the electric field is presented in Fig. 16 with the applied voltages in Table V. The maximum dielectric strength in the insulation layer is 8.79, 12.2, and 11.3 kV/mm, respectively, which are less than the dielectric strength of the epoxy resin, so the insulation distance satisfies the requirements.

In the T_C and T_M in STAB-stage of the CMIB-SST scheme interconnected by STAB, the primary side windings completely

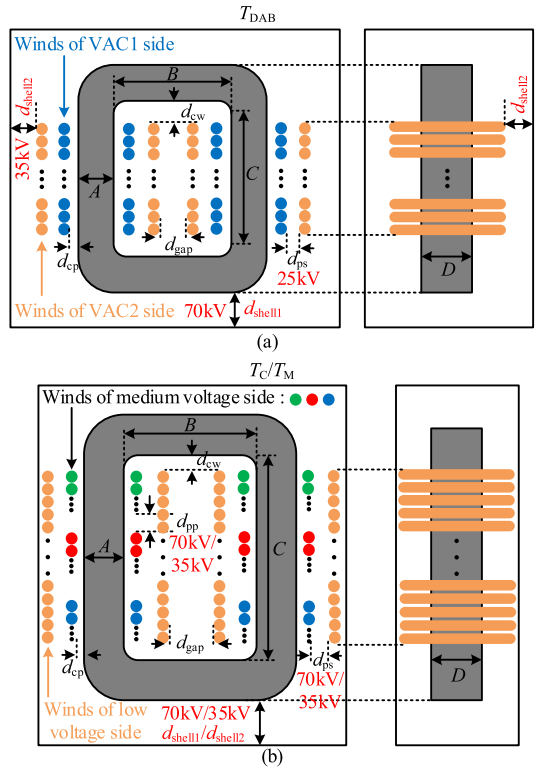

Fig. 15. Transformer and isolation structures of two schemes. (a) Two-winding transformer of DAB. (b) Four-winding transformers of STAB.

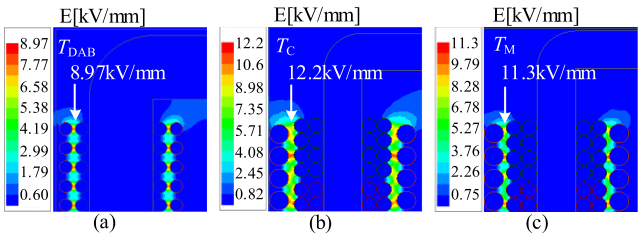

Fig. 16. FEM simulation results of electric field in the transformer (1/4 region) of two schemes. (a) T_{DAB} of the DAB-stage. (b) T_{C} of the primary side of the STAB-stage. (c) T_M of the secondary side of the STAB-stage.

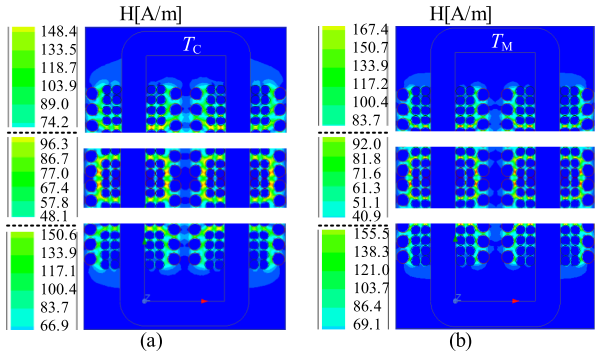

Fig. 17. Magnetic field strength distribution of two transformers of STAB. (a) T_C. (b) T_M.

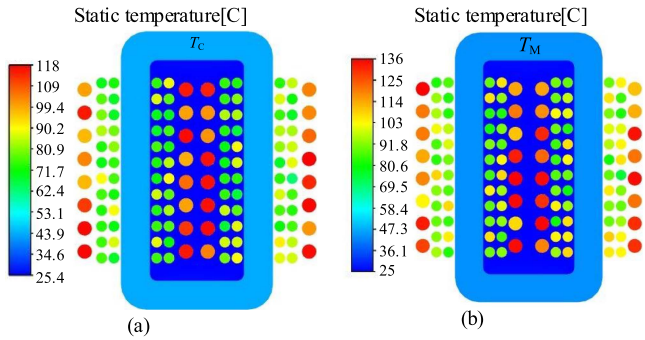

Fig. 18. Temperature distribution of two transformers of STAB. (a) T_C. (b) T_M.

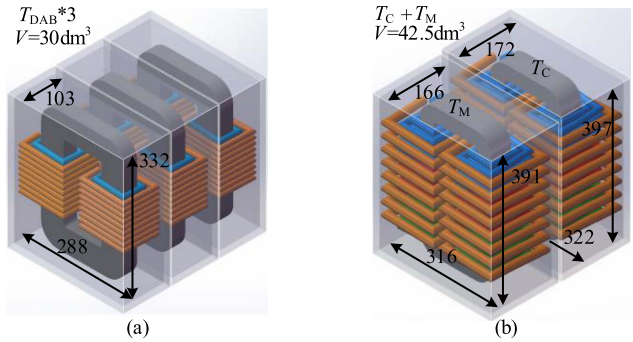

Fig. 19. Comparison of transformers in evaluated units of two schemes. (a) Transformers in the evaluated unit of the CMIB-SST scheme interconnected by DAB. (b) Transformers in the evaluated unit of the CMIB-SST scheme interconnected by STAB.

cover the core and are covered by the secondary side winding to reduce the leakage inductance of the HFT and satisfy the requirement that the leakage inductance is designed to be as small as possible in Section III-C. The magnetic field strength distribution of T_C and T_M is shown in Fig. 17(a) and (b).

The leakage inductance is about 10.8, 6.0, and 10.8 uH of the primary side of T_{C} and the leakage inductance is about 8.8, 4.4, and 8.8 uH of the primary side of T_M. The influence of transformer leakage inductance on the decoupling of ripple current can be ignored as shown in Fig. 9. The leakage magnetic path between the primary and secondary side windings close to the upper and lower yoke is symmetric, and the leakage inductance of the winding is approximately equal, the leakage inductance of the winding is negatively correlated with the minimum distance from the upper and lower yoke, and the leakage inductance of the winding far away from the yoke is smaller, the difference between the primary side leakage inductance of the transformer is less than 4.8uH, and its impact can also be neglected as shown in Fig. 11.

The temperature distribution of T_C and T_M is shown in Fig. 18(a) and (b). The core temperature of T_{C} is about 53 °C, the maximum winding temperature is about 118 °C, the core temperature of T_M is about 58 °C, and the maximum winding temperature is about 136 °C.

The overall structure of the transformers under the two schemes are shown in Fig. 19. The volumes of T_{DAB}, T_C, and T_M

TABLE VI
MAGNETIC CORE SPECIFICATION OF INDUCTORS

	L*3, L_S
Single specification	NPH500060
Outer diameter/d_o[mm]	134.2
Inner diameter/d_i[mm]	77
Height/h[mm]	21.7
Inductance/A_L[uH]	0.124
Mean path length/Le[cm]	34.42
Iron cross section/Ae[cm^2]	5.347
Saturated flux density/B[T]	1.2

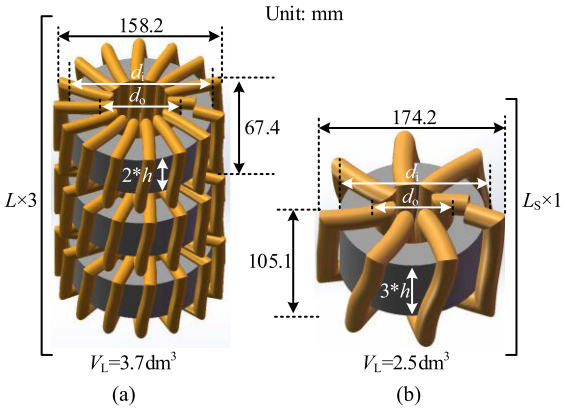

Fig. 20. Comparison of inductors in evaluated units of two schemes. (a) Three inductors in the evaluated unit of the CMIB-SST scheme interconnected by DAB. (b) One inductor in the evaluated unit of the CMIB-SST scheme interconnected by STAB.

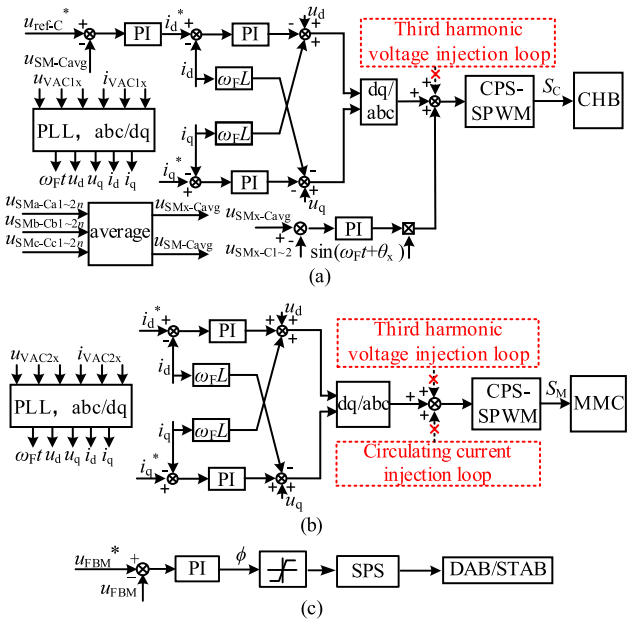

Fig. 21. Each stage control strategy of CMIB-SST schemes. (a) CHB-stage. (b) MMC-stage. (c) Voltage control of DAB/STAB.

are 10, 22, and 20.5 dm^3, respectively. In the evaluated unit of the CMIB-SST scheme interconnected by DAB, the total volume of three transformers is 30 dm^3. In the evaluated unit of the CMIB-SST scheme interconnected by STAB, the total volume of transformers T_C and T_M is 42.5 dm^3, which increases by 29%.

Two magnetic particle cores with model NPH500060 are used in parallel for the inductor in DAB, and three magnetic cores with the same model in parallel are used for the inductor in STAB. The magnetic specifications are given in Table VI.

In the two evaluated units shown in Fig. 12, the overall structure of the inductors is compared as shown in Fig. 20. The total volume of the three inductors in the evaluated unit of the CMIB-SST scheme interconnected by DAB is 3.97 dm^3, and the volume of one inductor in the evaluated unit of the CMIB-SST scheme interconnected by STAB is 2.5dm^3, reducing by 37%.

D. Control Diagram

The control strategy of the CMIB-SST scheme is shown in Fig. 21. In the CMIB-SST scheme interconnected by DAB, control loops within dotted rectangle are required to realize the low frequency voltage ripple suppression of SM in both ac/dc-stages, which is not needed in the proposed CMIB-SST scheme interconnected by STAB, and the system control is simple.

Fig. 21(a) shows the control strategy of CHB-stage, the average value $u_{\mathrm{SM}\text{-}C\mathrm{avg}}$ of all the SM capacitor voltages is taken as the feedback of the voltage loop to stabilize the SM capacitor voltage. Besides, the SM capacitance voltage $u_{\mathrm{SM}x\text{-}C}$ is controlled to balance the SM capacitance voltage. Fig. 21(b) shows the MMC-stage control strategy which adopts a single current close loop control under the synchronous reference frame to realize the unit power factor. Fig. 21(c) shows the DAB/STAB control strategies, the secondary side port voltage u_{FBM} of DAB/STAB-stage serves as the feedback of the external voltage loop to stabilize STAB-stage port voltage and realize the SM capacitor voltage balanced of the MMC-stage, so the SM capacitor voltage balance strategy of MMC-stage can be neglected. The power control between the primary and secondary sides of DAB/STAB-stage is realized by single phase shift modulation.

When the STAB-stage of the CMIB-SST scheme interconnected by STAB adopts the proposed SSHPSM method as shown in Fig. 21(c). The power flowing between the FB_C and FB_M is achieved by the phase-shift modulation, and under SSHPSM method, the three-phase SM capacitors of MMC-stage and CHB-stage show equivalent connected in parallel characteristics, respectively, that is the switched-capacitor characteristics which allowing the ripple current flow freely between SMs, and be cancelled based on three-phase symmetry, and for MMC-stage the circulating current will not appear due to the suppression of the second-order-frequency ripple current. Therefore, compared with the CMIB-SST scheme interconnected by DAB with capacitors size reduced by proper control strategies, the third harmonic voltage injection strategy is not needed for CHB-stage and MMC-stage, and the circulating current injection strategy is not needed for MMC-stage which simplifies the control strategy.

E. Performance Evaluation Summary

Comparing the two evaluated units in Fig. 12, the CMIB-SST scheme shown in Fig. 1(b) is optimized in terms of topology,

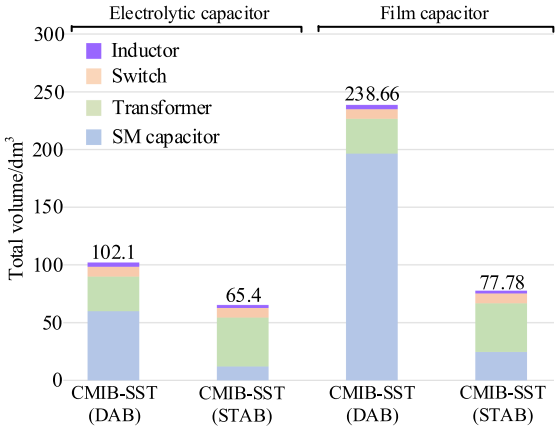

Fig. 22. Evaluated unit volume comparison of two schemes.

TABLE VII
MULTIFACETED EVALUATION OF DIFFERENT SCHEMES

Features	BTB-CHB [7]-[8]	CMIB-SST (DAB)	CMIB-SST (STAB)
Number of SMs	$6n$	$6n$	$6n$
Number of inductors	$6n$	$6n$	$2n$
Number of transformers	$6n$	$6n$	$2n$
Number of switches	$96n$	$84n$	$84n$
SM capacitance of VAC1 side converter	10 mF	10 mF	1.2 mF
SM capacitance of VAC2 side converter	10 mF	16 mF	1.6 mF
Inductance	56.25 uH	56.25 uH	18.75 uH
SM capacitor volume of electrolytic capacitor or film capacitor	45 dm^3/ 164 dm^3	60 dm^3/ 197 dm^3	12 dm^3/ 24.54 dm^3
SM capacitor cost of electrolytic capacitor or film capacitor	16236\$/ 9270\$	21648\$/ 11124\$	3342\$/ 1392\$
Transformer volume	30 dm^3	30 dm^3	42.34 dm^3
Inductor volume	3.7 dm^3	3.7 dm^3	2.5 dm^3
Circulating current injection strategy	×	√	×
Third harmonic voltage injection strategy	√	√	×

control strategy, system volume and cost. Under the evaluated units in Fig. 12, the significant advantages of the CMIB-SST scheme interconnected by STAB include that:

1) When the SM capacitors of CMIB-SST schemes use electrolytic capacitors, compared with CMIB-SST scheme interconnected by DAB, the total volume in evaluated units is reduced by 36%, and when the film capacitors are used, the total volume is reduced by 67% as shown in Fig. 22.
2) The control strategies of CHB-stage and MMC-stage are also simple, the circulating current injection strategy is not essential for the MMC-stage, and neither the third harmonic voltage injection strategy of the two ac/dc-stages.

The specific comparison of different schemes is given in Table VII.

V. SIMULATION RESULTS

In order to verify the effectiveness of the proposed power distribution interface, a simulation platform of the CMIB-SST scheme interconnected by STAB is built in PLECS which simulation platform parameters are given in Table VIII, and the SM capacitance of the CHB-stage and MMC-stage are given according to (31) and (32).

TABLE VIII
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters	Simulation	Experimental
CHB-stage		
VAC1 rated active power/P_{VAC1}	12 MW	1k W
RMS of line voltage/$U_{Lrms\text{-}C}$	35 kV	152 V
Fundamental-frequency/f_F	50 Hz	50 Hz
PWM carrier frequency/f_C	2k Hz	5k Hz
SM capacitance voltage/$U_{SM\text{-}C}$	3k V	40 V
SM capacitance/$C_{Lx\text{-}C}$	300 uF	160 uF
MMC-stage		
VAC2 rated active power/P_{VAC2}	10 MW	0.9 kw
VDC power/P_{VDC}	2 MW	0.1 kw
RMS of line voltage/$U_{Lrms\text{-}M}$	10 kV	38 V
VDC voltage/U_{VDC}	18 kV	80 V
Fundamental-frequency/f_F	50 Hz	50 Hz
PWM carrier frequency/f_M	2 kHz	5 kHz
Number of SM of per arm/n	6	2
SM capacitance voltage/$U_{SM\text{-}M}$	3 kV	40 V
SM capacitance/$C_{Lx\text{-}M}$	400 uF	270 uF
	STAB-stage	
Power/P_{STAB}	1 MW	250 W
Transformer turns ratio of T_C and T_M/N_C, N_M	1:1:1:1	1:1:1:1
Switching frequency/f_S	10 kHz	20 kHz
STAB Inductance/L_S	75 uH	36 uH

A. AC Power and DC Voltage Control

Fig. 23 is the voltages and currents of VAC1 grid, VAC2 grid, and Vdc bus.

Before $t = 1$s, VAC1 grid feeds VAC2 grid 10 MW and VDC bus 2 MW. When $t = 1$ s, the power of VAC2 grid switches to 5 MW, and the power of VAC1 grid responds to the power demand of the system and outputs 7 MW under the control strategy shown in Fig. 21.

B. Ripple Current Decoupling and Cancellation

Fig. 24 is the HFT voltage and current waveforms of T_C and T_M of STAB-stage corresponding to the SSHPSM method shown in Fig. 5(b). The FB$_C$ and FB$_M$ adopt SSHPSM method and the power flow is realized by phase-shift modulation.

Fig. 25 is the SM ripple current transfer of the CHB and MMC-stages under the proposed SSHPSM method. Fig. 25(a) is the SM charging current of CHB-stage in (12) and the SM charging current of MMC-stage in (13), under SSHPSM method, the dc component of SM charging current transfer between the primary and secondary sides of STAB-stage by phase-shift modulation, the second-order-frequency component of the CHB-stage SM charging current, the fundamental frequency and second-order-frequency components of the MMC-stage SM charging current are transmitted to the FB$_C$ and FB$_M$ based on the low impedance characteristic of equivalent connected in parallel of switched-capacitor circuits under synchronization modulation as shown in Fig. 25(c). Therefore, the SM capacitor currents of CHB and MMC-stages mainly contain the switching harmonics generated by the SM of CHB-stage and MMC-stage during the pulse width modulation process as shown in Fig. 25(b).

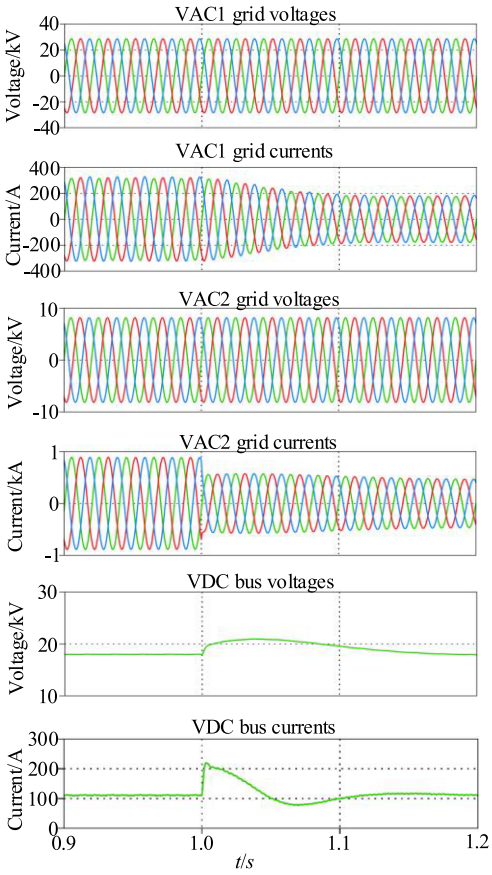

Fig. 23. System AC power flow and DC voltage waveforms of the CMIB-SST scheme interconnected by STAB.

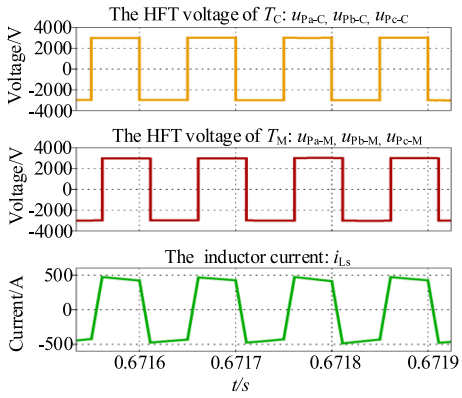

Fig. 24. Waveforms of modulation voltage and current of SSHPSM method.

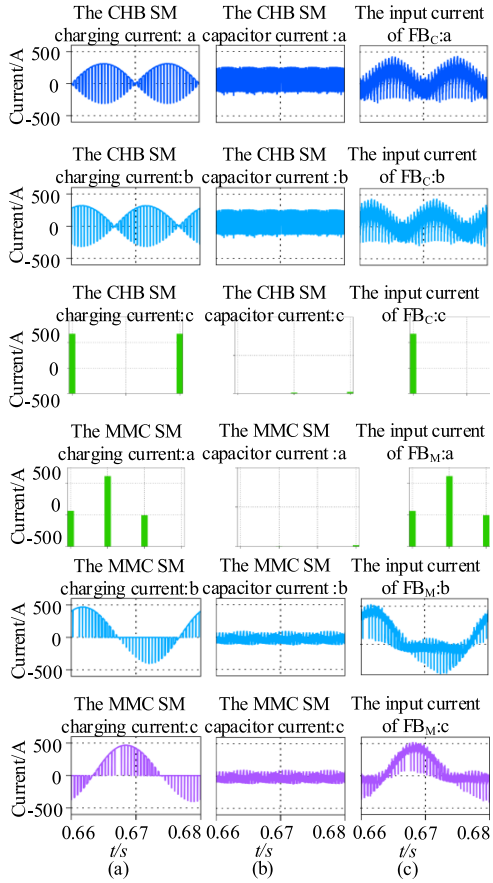

Fig. 25. Waveforms of SM ripple current transfer of CHB and MMC-stages. (a) Waveforms of the SM charging current. (b) Waveforms of the SM capacitor current. (c) Waveforms of the input current of full bridges of primary and secondary sides of STAB-stage.

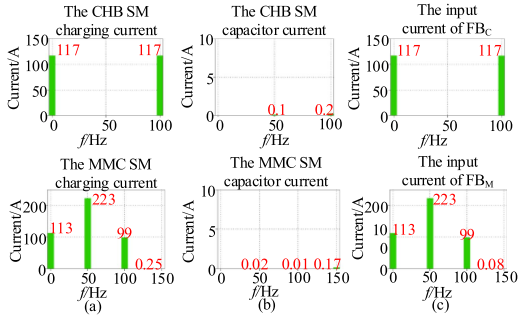

Fig. 26. FFT analysis results of SM low-frequency ripple current of CHB and MMC-stages. (a) SM charging current. (b) Capacitance current. (c) FB_C and FB_M input current of STAB-stage.

Fig. 26(a) is the FFT analysis results in Figs. 25(a), 26(b), and (c) correspond to Fig. 24(b) and (c), respectively. The SM capacitor currents of the two ac/dc-stages hardly contain low-frequency ripple current components which mainly flow into the STAB-stage and further realize decoupling between three-phase SMs. Therefore, the SM capacitor only needs to deal with the high-frequency switching harmonics.

Fig. 27 shows the HFT primary side currents of T_C and T_M of STAB-stage, the low-frequency components exist with the form of sideband harmonics in the primary side high-frequency modulation currents of HFT as shown in (26). The $i_{px\text{-}C}$ is the primary side modulation current of T_C which ripples in the form of the second-order-frequency, $i_{px\text{-}M}$ is the primary side modulation current of T_M which ripples in the form of the fundamental frequency superposed by the second-order-frequency, and i_{Ls} is the STAB inductor current. The above current waveforms indicate that, under SSHPSM method, the dc

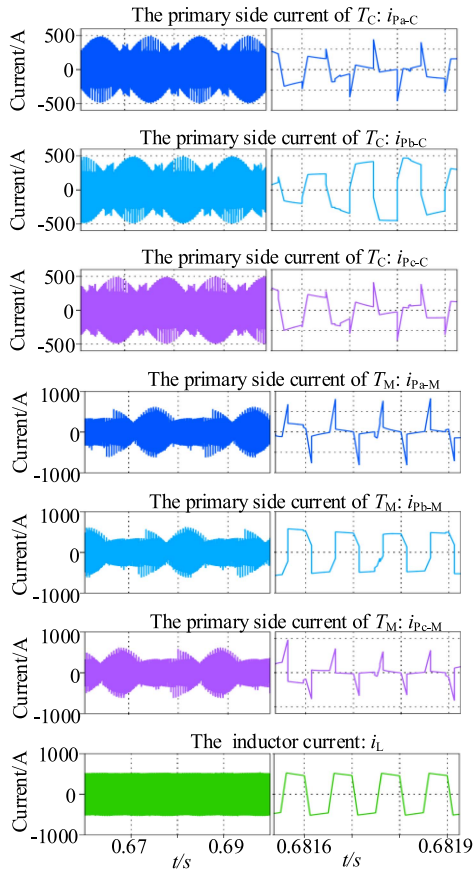

Fig. 27. Waveforms of HFT primary side currents of T_C and T_M and the inductor current of STAB.

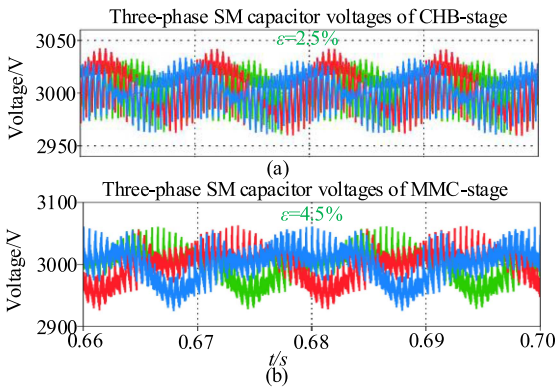

Fig. 28. SM capacitor voltages of CHB and MMC-stages. (a) CHB-stage. (b) MMC-stage.

power and low-frequency ripple power can flow to the primary sides of the transformers T_C and T_M through FB$_C$s and FB$_M$s. After the ripple power decoupling with the SM capacitors and cancelling at the primary sides of T_C and T_M based on the three-phase symmetry, as analyzed in Section III-C, only dc power is transferred between the primary and secondary sides of the STAB through the inductor.

Fig. 28 is the SM capacitor voltages of CHB and MMC-stages. Under the small capacitance constraint of (31) and (32), the SM

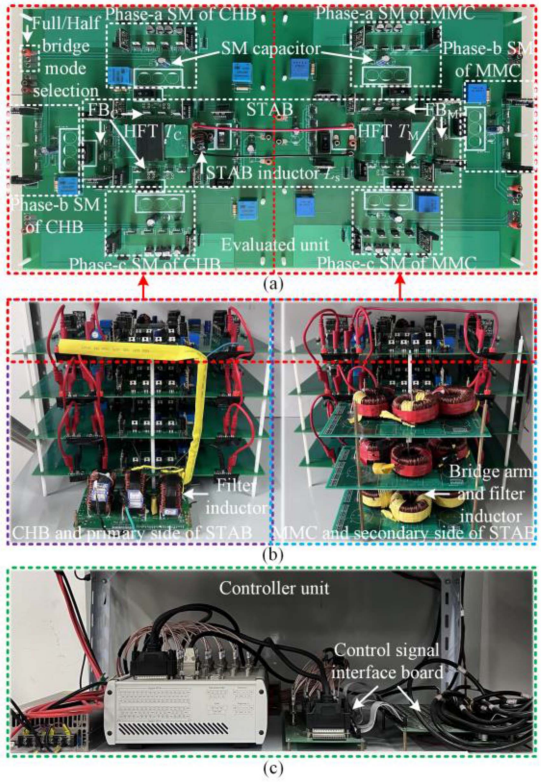

Fig. 29. Scaling down experimental prototype of CMIB-SST system interconnected by STAB. (a) Evaluated unit. (b) Overall structure of the main power circuit. (c) Controller unit.

capacitance of CHB-stage is 300uF and the capacitor voltage ripple is 2.5%, as shown in Fig. 27(a), the SM capacitance of MMC-stage is 400 uF and the capacitor voltage ripple is 4.5%, as shown in Fig. 27(b). It can be seen that the CMIB-SST scheme interconnected by STAB under SSHPSM method can suppress the SM capacitor voltage ripple under the new small capacitance constraint. Therefore, film capacitor with small capacitance can be used, which is beneficial to security and life of the module of the SST.

VI. Experimental Results

A 1 kW small-scale test prototype of the CMIB-SST scheme interconnected by STAB is built in this article, the experimental parameters are given in Table VIII and the experimental prototype is shown in Fig. 29. Fig. 29(a) corresponds to the evaluated unit shown in Fig. 12(b), which is composed of two parts; one is the CHB three-phase SM and STAB primary side full bridge and transformer T_C, and the other is the MMC three-phase SM and STAB secondary side full bridge and transformer T_M. The STAB primary and secondary sides are connected through STAB inductor L_s. Fig. 29(b) shows the overall structure of the main power circuit composed of $2n$ ($n = 2$) evaluated units. Fig. 29(c) is the dSPACE based controller unit. The SM capacitance is 160 uF of CHB-stage and 270 uF of MMC-stage according to (31) and (32), and 220 and 330 uF capacitor are used in experiments.

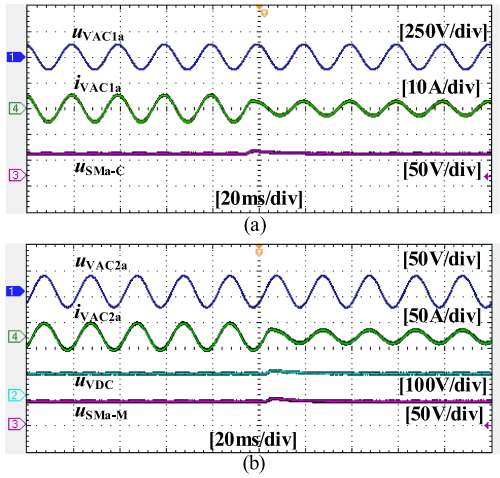

Fig. 30. Waveforms of power flow of three ports. (a) CHB-stage port. (b) MMC-stage port.

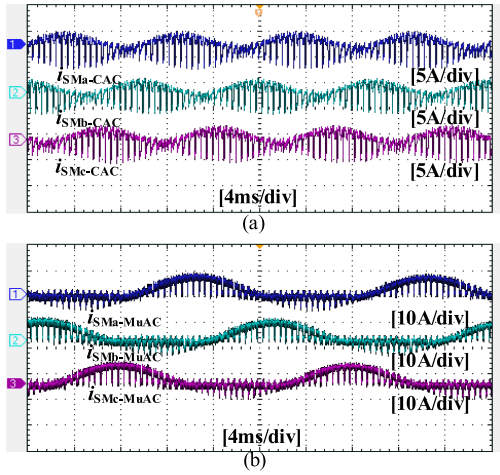

Fig. 31. Waveforms of input current of FB_C and FB_M of STAB-stage. (a) Waveforms of the input current of FB_C. (b) Waveforms of the input current of FB_M.

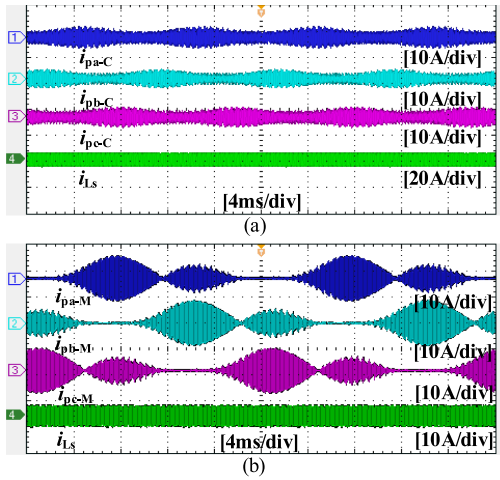

Fig. 32. Waveforms of HFT currents of STAB-stage. (a) Primary side. (b) Secondary side.

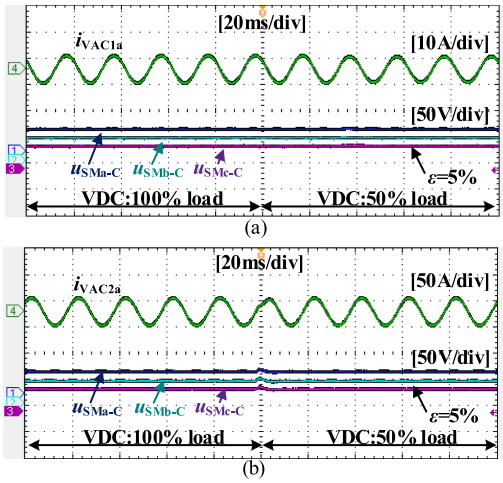

Fig. 33. Waveforms of phase-a current and SM capacitor voltage of (a) CHB-stage and (b) MMC-stage.

Fig. 30 is the three ports power flow waveforms, Fig. 30(a) shows the VAC1 grid voltage and current and the SM capacitor voltage of CHB-stage, and Fig. 30(b) shows the VAC2 grid voltage and current, the Vdc bus voltage and the SM capacitor voltage of MMC-stage. When the power of VAC2 grid switches to 50% of the original, under the control strategy in Fig. 21, the VAC1 grid responds to the power demand and the Vdc port voltage and SM capacitor voltage in both ac/dc stages is stable.

Under the SSHPSM method, the second-order-frequency ripple currents of CHB-stage SM are decoupled with the SM capacitors and transfer to the FB_Cs of the primary sides of STAB-stage as shown in Fig. 31(a), the fundamental frequency and second-order-frequency ripple currents of MMC-stage SM are decoupled with the SM capacitors and transfer to the FB_Ms of the secondary sides of STAB-stage as shown in Fig. 31(b), the above process corresponds to the simulation results in Fig. 25.

The low-frequency ripple power of CHB-stage is cancelled in the primary sides of T_C based on the three-phase symmetry as shown in Fig. 32(a), and the low-frequency ripple power of MMC-stage are also cancelled in the primary sides of T_M based on the three-phase symmetry as shown in Fig. 32(b), therefore, only active power is transferred between the primary and secondary sides of the STAB. The above process corresponds to the simulation results in Fig. 27.

Fig. 33 shows SM capacitor voltages of CHB-stage and MMC-stage under the small capacitance constraint. Fig. 33(a) shows the phase-a current $i_{\mathrm{VAC1}\,a}$ and the three-phase SM capacitor voltages of CHB-stage, when the Vdc bus load is switched from full load to 50% load, $i_{\mathrm{VAC1}\,a}$ decreases in response to system power demand, the SM capacitor voltage ripple of CHB-stage is only 5%. Fig. 32(b) shows the phase-a current $i_{\mathrm{VAC2}\,a}$ and the three-phase SM capacitor voltages of MMC-stage, $i_{\mathrm{VAC2}\,a}$ remains unchanged under constant reference and the SM capacitor voltage ripple of MMC-stage is only 5%. It verifies that the effectiveness of the capacitance minimization strategy based on SSHPSM method and the new capacitance constraint.

VII. Conclusion

A STAB with SSHPSM method-based galvanic isolation CMIB-SST is studied for interconnection of ac distribution grids. The low-frequency ripple currents of the both ac side SMs are decoupled with SM capacitors and transferred to the primary sides of HFT for cancellation. The SM capacitor cost and the total volume are significantly reduced under the utilization of both electrolytic capacitor or film capacitor but the current stress of STAB is increased.

According to the impact analysis of the STAB leakage inductance on the decoupling of the ripple current, the reasonable leakage inductance parameters and their inconsistency will not affect the normal operation and the detailed transformer design process of the proposed CMIB-SST scheme is demonstrated. By the help of SSHPSM modulation, the system control is simple as the circulating current injection strategy is not essential for the MMC-stage, and neither the third harmonic voltage injection strategy of the two ac/dc-stages.

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