# SiC Three-Level Neutral-Point-Clamped Converter With Clamping Diode Volume Reduction Using Quasi-Two-Level Operation

Xiang Lin, *Student Member, IEEE*, and Dong Dong, *Senior Member, IEEE*

***Abstract*—Medium voltage SiC MOSFETs have recently garnered considerable attention in the medium-voltage high-power areas like high-frequency solid-state transformers and multilevel converters. While direct series connection of these MOSFETs is an option for higher voltage levels, it requires complex voltage balancing approaches for device voltage balancing during fast switching transients. Alternatively, converter-level solutions such as the three-level (3L) neutral-point-potential converter can be used. This article proposes a new modulation strategy, combining 3L, and Quasi-two-level modulations, to minimize the rating and volume of clamping diodes by tightly controlling the thermal stress on the diodes. This approach achieves better efficiency, higher power density, and a simpler converter bus-structure to stack two SiC MOSFETs effectively in series. We present a real-time clamping diode loss estimation to improve the effectiveness of the proposed modulation strategy. To verify the proposed converter-level approach and modulation strategy, we test a 20 kV rated phase-leg with two 10 kV SiC MOSFETs and 3.3 kV SiC diodes.**

***Index Terms*—Diode clamped converter, efficiency improvement, series connected SiC MOSFETs.**

## I. Introduction

In RECENT years, there has been a growing interest in medium-voltage (MV) SiC MOSFETs with rated voltages of 6.5, 10, and 15 kV for MV power conversion applications due to their potential to improve efficiency and power density by using simpler topologies and fewer conversion stages. For designing a phase-leg with a higher blocking voltage requirement, a switching unit realized by series-connected SiC MOSFETs is desirable and suitable for certain applications, such as the following.

1) Isolated dc–dc converter: Phase-legs in isolated dc–dc converters need to generate high-frequency two-level PWM voltage for the high-frequency transformer. When the blocking voltage requirement is higher than the blocking voltage of a single device, the two-level phase-leg with series-connected devices is a better solution compared to a multilevel structure because it eliminates the need for extra passive components.
2) Solid-state transformer or modular multilevel converter (MMC): For converters required to interface with the ac grid, multiple ac–dc converter cells need to be cascaded to meet the voltage requirement. Because of the blocking voltage limit of the device, too many cells may be required. The two-level phase-leg with series-connected SiC MOSFETs can help improve the blocking voltage for each cell, reducing the number of cells needed and simplifying the control complexity of the entire system. Additionally, the interleaved operation of different cells can maintain low current harmonics.

TABLE I
Comparison of Different Approaches for Voltage Balancing Control of Series-Connected SiC MOSFETs

| Solutions | Robust voltage balance control | Extra switching loss | Extra component volume |
|---|---|---|---|
| Passive device-level solution | Easy | **Large** | Small |
| Active device level solution | **Difficult** | Small | Small |
| Converter-level solution | Easy | Small | **Large** |

The series-connected SiC MOSFETs are attractive for their requirement of fewer extra components, but under high switching speed conditions, severe voltage sharing issues exist. In the literature [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], three types of solutions have been proposed to address the voltage imbalance issue, which are summarized as follows (also presented in Table I).

1) Passive device-level solution [9], [10]: This solution involves the use of passive components for direct series connection. Passive snubber is one of the typical solutions that applies extra passive components to slow down the switching speed of devices and reduce the turn-OFF dv/dt difference. However, this method increases the switching loss, making it unattractive for SiC MOSFET with a higher switching frequency.

Manuscript received 18 September 2022; revised 27 December 2022 and 10 March 2023; accepted 11 April 2023. Date of publication 25 April 2023; date of current version 21 June 2023. Recommended for publication by Associate Editor Y. Siwakoti. *(Corresponding author: Xiang Lin.)*

Xiang Lin is with the Tesla, Palo Alto, CA 94304 USA (e-mail: xianglin18@vt.edu).

Dong Dong is with the Center for Power Electronics System, Virginia Tech, Blacksburg, VA 24060 USA (e-mail: dongd@vt.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3270370.

Digital Object Identifier 10.1109/TPEL.2023.3270370

2) Active device-level solution: This solution adds extra controls to the device gate drivers to actively control the voltage sharing. The main benefit of this method is its low extra switching loss compared to the passive device-level solution. Several different approaches have been developed to affect voltage sharing. Some approaches [11], [12], [13], [14], [15], [16], [17] propose to control the turn-OFF *dv/dt* to affect the voltage sharing, while others [18], [19], [20], [21] propose to control the turn-OFF time. However, the fast-switching speed of SiC MOSFETs and the impact of parasitic capacitors on voltage sharing require careful and complicated design of the active voltage balancing method [22], [23].
3) Converter-level solution: This solution involves the addition of extra components to form a multilevel converter structure to avoid the direct series connection of SiC MOSFETs. The modulation strategy is adjusted to two-level modulation or quasi-2-level (Q2L) modulation, which helps limit the volume of extra components. In the literature, this type of solution prefers the capacitor-based multilevel converter structure like MMC [24], [25], [26], [27], [28], [29], [30], [31], [32] or flying-capacitor (FC) converter [33], [34], [35], [36]. However, for MV applications, the capacitor volume cannot be ignored even with a small capacitor value. Therefore, this type of solution with a capacitor-based multilevel converter structure usually results in a significant volume increase, making it unattractive.

The capacitor-based multilevel structure is not the only solution for the converter-level approach, and it is important to explore other suitable converter topologies that can minimize the volume of extra components. One such topology is the diode-clamped converter, which has been discussed in some literature [37], [38] in the context of Q2L modulation to avoid complex dc-link capacitor balancing issues. In [39], the Q2L modulation was first applied to series-connected SiC MOSFETs in a medium voltage half-bridge module design. The designed half-bridge module showed a small extra volume of clamping diodes, indicating that the diode-clamped converter topology is more suitable as a converter-level solution. However, no detailed comparison between the diode-clamped and capacitor-based converter topologies has been reported in the literature. Therefore, this article focuses on evaluating the volume reduction potential of clamping diodes with the existing Q2L modulation and compares it to the capacitor-based multilevel converter topology. The comparison is limited to a three-level (3L) multilevel converter structure, as shown in Fig. 1.

Moreover, this article investigates whether the Q2L modulation is the most suitable modulation strategy for the dc–ac inverter/rectifier applications. Compared to the traditional 3L modulation, the Q2L modulation causes more switching losses on the main switches ($S_1$–$S_4$ in Fig. 1) to limit the losses on the clamping diodes. However, the analysis also shows that the Q2L modulation does not fully utilize the clamping diode thermal capability. More loss on the clamping diode could be desirable if it helps save the switching loss of main switches. Therefore, this article proposes a new modulation strategy for the 3L NPC converter that can maintain the benefits of the Q2L modulation on clamping diode volume reduction while achieving better efficiency with controlled losses on the clamping diode. The proposed modulation strategy includes both 3L modulation and Q2L modulation during operation, and the details will be explained in this article.

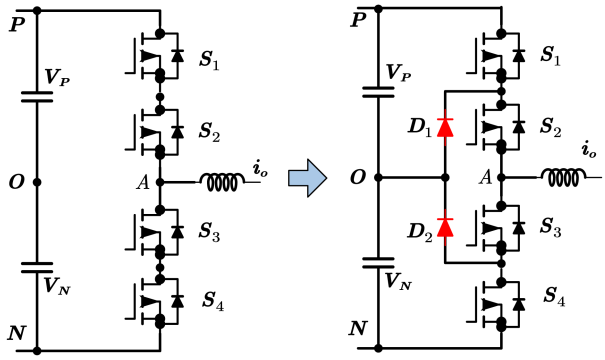



Fig. 1. 3L NPC converter structure for voltage balancing of series-connected SiC MOSFETs.

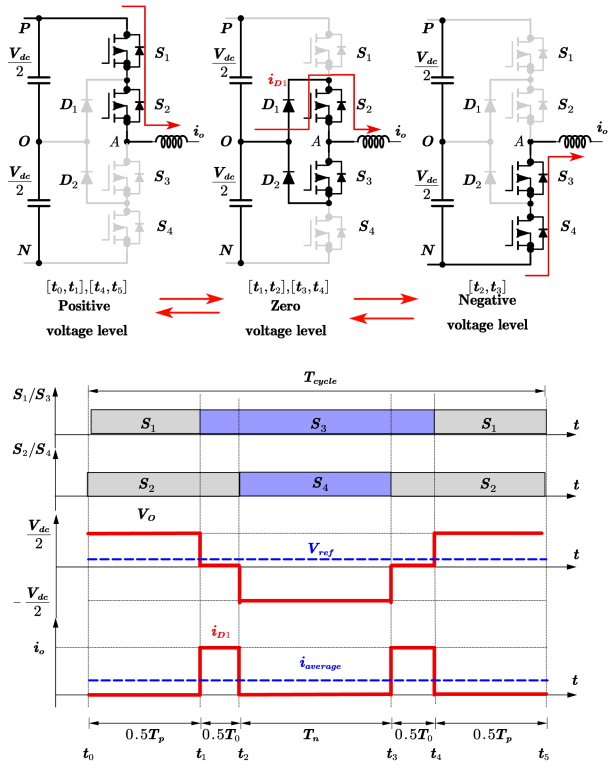



Fig. 2. Q2L operation principle of 3L NPC converter.

## II. Analysis of 3L NPC Converter With Q2L Modulation

### A. Q2L Modulation of 3L NPC Converter

In Fig. 2, the Q2L modulation strategy is illustrated. As a result of the inclusion of two extra clamping diodes $D_1$ and $D_2$, the series-connected devices do not need to switch simultaneously,

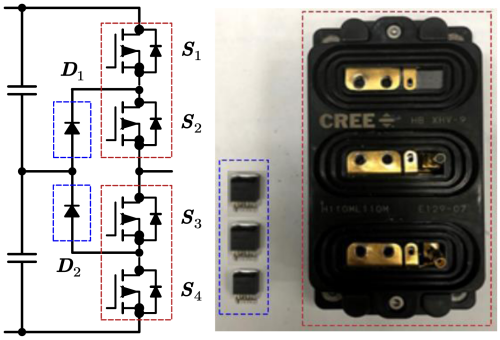



Fig. 3. Clamping diode selection for 10 kV/16 A SiC MOSFETs.

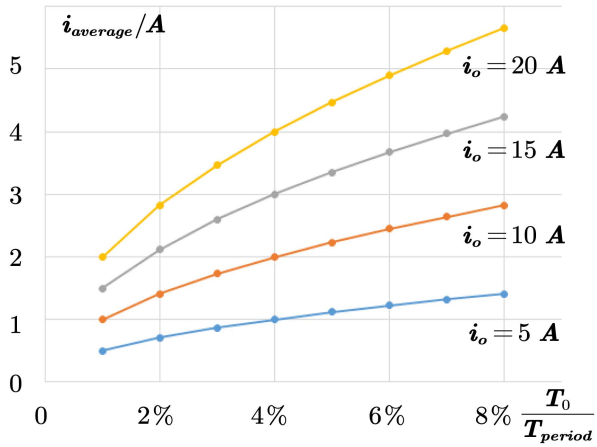



Fig. 4. Calculation of $i_{\text{average}}$ under different conditions.

and the turn-OFF voltage of each device is clamped by dc-link capacitors. Unlike the traditional 3L modulation, the zero-voltage level is used only for transient, and the voltage waveform is similar to the voltage waveform with 2L modulation. The output voltage maintains the voltage-second balance with the voltage reference, as listed in

$$\begin{cases} V_{\text{ref}}\ T_{\text{period}} = \ 0.5V_{\text{dc}}T_p - 0.5V_{\text{dc}}T_n \\ T_{\text{period}} - \ T_0 = T_p \ + T_n \end{cases}. \tag{1}$$

The Q2L modulation strategy offers control freedom over the conduction time $T_0$ of $D_1$ and $D_2$, which is independent of the voltage reference $V_{ref}$. With $T_0$ determined, $T_p$ and $T_n$ can be calculated using (1). By restricting the clamping diodes' conduction time, their loss can be minimized, leading to a significant reduction in their volume. To demonstrate the benefits of clamping diode selection, we present an example in Fig. 3, where the switches $S_1$–$S_4$ are 10 kV/16 A SiC MOSFETs and the clamping diode is a "10 kV" SiC Schottky diode without a heatsink, realized by three 3.3 kV/5 A SiC Schottky diodes [40] in series connection. Fig. 4 shows that by keeping $T_0$ much smaller than the switching period (<10%), the average diode conduction current $i_{\text{average}}$ is much smaller than the actual load current $i_o$. Moreover, the volume comparison in Fig. 3 indicates that the clamping diodes' volume is negligible compared to the 10 kV SiC MOSFETs. Note that the diode selection in Fig. 3 is not the only choice, and a 10 kV SiC Schottky diode could also be adopted if available.

TABLE II
SIMULATION PARAMETERS

| Parameters | Value |
|---|---|
| Dc-link Voltage | 11 kV |
| Line-to-line grid voltage | 6.06 kV |
| Output current | 0-10 A (rms) |
| Fundamental frequency | 60 Hz |
| Switching frequency | 10 kHz |
| Zero-voltage-level length $T_0$ | 5 $\mu$s |

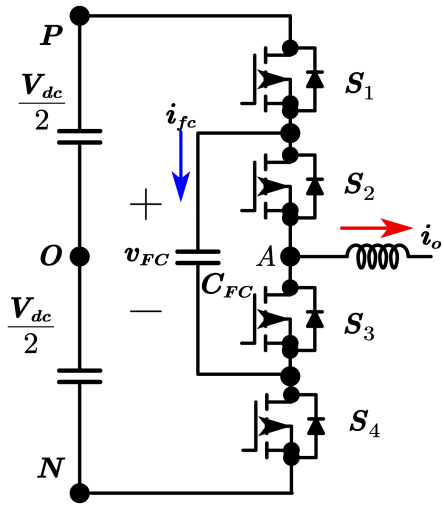



Fig. 5. 3L FC converter structure.

## B. Comparison of 3L NPC Converter and 3L FC Converter in Q2L Modulation

This section presents a comparison between the 3L NPC converter structure and the 3L FC converter structure for the Q2L modulation. The comparison is carried out on an ac–dc converter designed with 10 kV/ 16 A SiC MOSFET, as depicted in Fig. 3, and the relevant parameters are listed in Table II.

In this section, we compare the 3L NPC converter structure with the 3L FC converter structure for the Q2L modulation. The 3L FC converter structure is illustrated in Fig. 5. In a 3L FC converter, the capacitance of the FC must be sufficiently large to keep the maximum voltage ripple of FC below a predetermined limit. However, the Q2L modulation can help limit the charge/discharge time of the clamping diodes, thereby significantly reducing the required capacitance of FC. Moreover, the Q2L modulation also affects the self-balance of the FC voltage. Fig. 6 shows the two switching sequences for the Q2L modulation based on [36]. The switching sequence in Fig. 6(a) does not balance the charge and discharge currents of the FC when considering the current ripple, which makes it difficult to control the FC voltage. Thus, the switching sequence in Fig. 6(b) is proposed in [36]. However, this sequence causes a larger FC voltage ripple because the charge and discharge of the FC occur over two switching cycles. To calculate the flying-capacitance based on (2), we set the maximum voltage ripple $V_{pp,Q2L}$ as

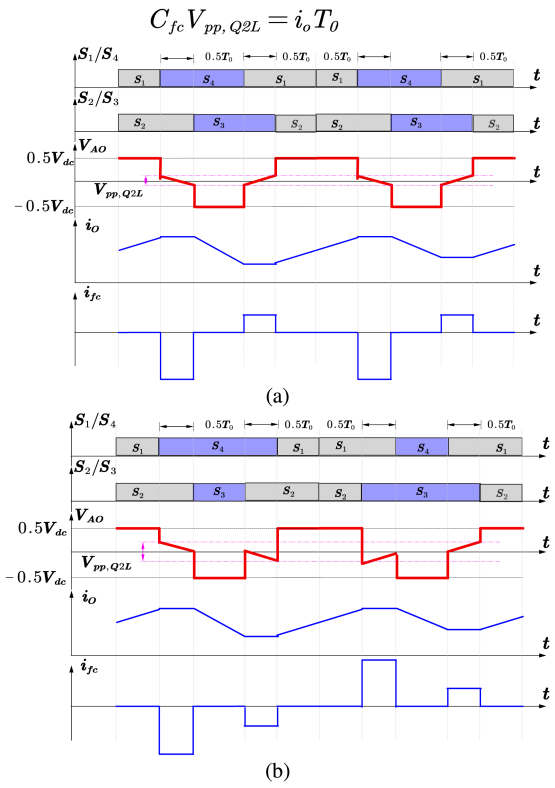



Fig. 6. Two switching sequence of Q2L modulation of 3L FC converter.

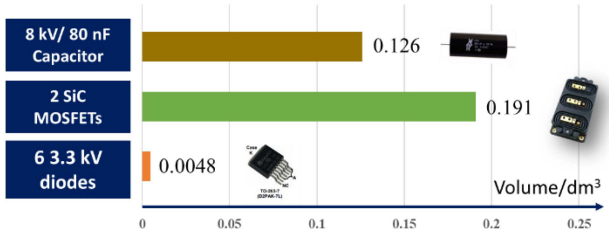



Fig. 7. Volume comparison of components.

1 kV, which is approximately 10% of the dc link voltage. Based on this calculation, we select an 80 nF capacitance and use eight 8 kV/10 nF capacitors from [41] in parallel for the FC. The total volume is 0.126 dm$^3$, which is larger than the total volume of six MV diodes and becomes comparable to the volume of the SiC MOSFET module based on Fig. 7

$$C_{fc}\, V_{pp,Q2L} = i_o\, T_0. \tag{2}$$

In conclusion, the 3L NPC converter structure is a more suitable converter-level approach than the 3L FC converter structure based on volume comparison. In addition to the volume benefit, the analysis also shows that the Q2L modulation provides further benefits with the 3L NPC converter structure.

First, the FC voltage in the 3L FC converter affects the blocking voltage of $S_1$–$S_4$. Fig. 8 shows that due to the FC voltage ripple, one of $S_1$ and $S_2$ turns OFF at a voltage lower than 0.5 $V_{dc}$ and turns on at a voltage higher than 0.5 $V_{dc}$.

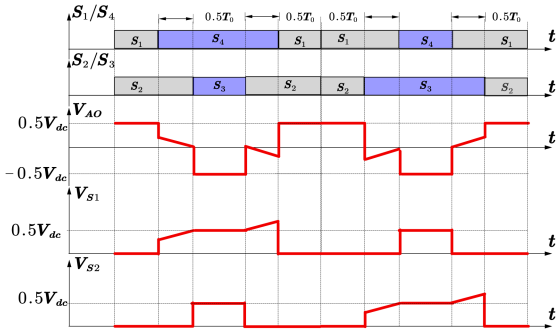


Fig. 8. Device blocking voltage in 3L FC converter.

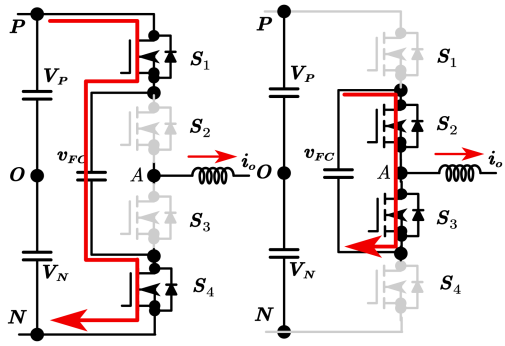


Fig. 9. Fault conditions that the fault current charges/discharges FC.

Since the switching loss of SiC MOSFET is proportional to the blocking voltage and the turn-ON loss is usually much higher than the turn-OFF loss, the switching loss of devices increases with smaller FCs and higher FC voltage ripple. On the contrary, for the 3L NPC converter structure, the blocking voltage of $S_1$–$S_4$ is clamped at 0.5 $V_{dc}$ with two dc-link capacitors. Therefore, the FC 3L converter with Q2L modulation will have more switching loss on MOSFETs, and the increase of switching loss is determined by the voltage ripple of the FC.

Second, the reduced FC value of FC 3L converter is not desirable for converter protection. Fig. 9 shows that during some fault conditions, such as direct parallel with dc-link capacitor or shorting, the FC could be directly charged and discharged by a large fault current instead of normal operation current. The fault current will result in a much larger voltage ripple on the FC and corresponding high blocking voltage on $S_1$–$S_4$. On the contrary, considering the fault current during very short periods of time, the clamping diodes will not be damaged because the actual power loss is small.

## III. Modulation Strategy to Fully Utilize the Clamping Diode Loss Capability

### A. Proposed Modulation Strategy

In Section II, we evaluated the use of a diode with a small volume to solve the voltage imbalance of two series-connected SiC MOSFETs with the existing Q2L modulation. However, Q2L modulation has not yet been approved as the optimized modulation strategy, particularly for low-frequency ac current

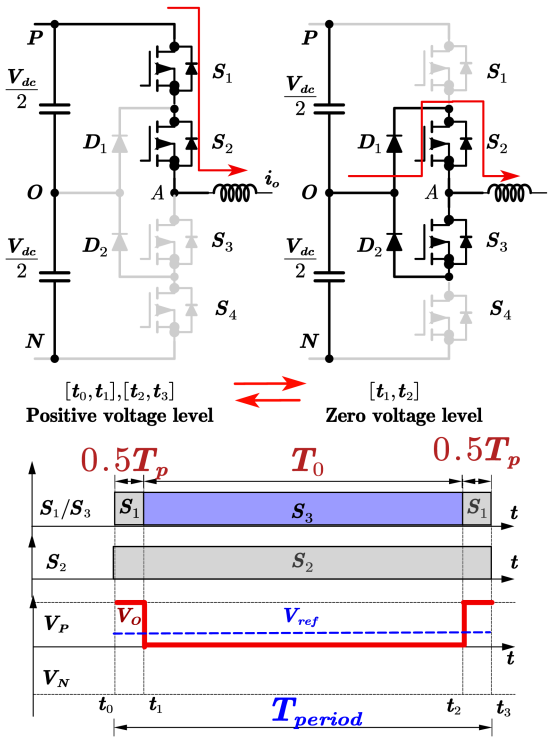



Fig. 10. 3L operation principle of 3L NPC converter.

(50 or 60 Hz), which was mentioned in the introduction. In addition to Q2L modulation, the 3L NPC phase-leg could also operate in 3L modulation (as shown in Fig. 10). In 3L PWM modulation, two voltage levels are used for each switching cycle. Unlike in 3L modulation, all switches $S_1$–$S_4$ switch once in the switching cycle in Q2L modulation to limit the conduction time $T_0$. This leads to an increase in the switching loss of $S_1$–$S_4$ with Q2L modulation. Therefore, it is desirable to evaluate a new modulation technique that could achieve less total loss compared to Q2L modulation while maintaining the benefit of diode volume reduction provided by the Q2L modulation.

This article presents a novel modulation strategy aimed at maximizing the thermal capacity of clamping diodes and minimizing the switching loss of $S_1$–$S_4$ in comparison to Q2L modulation. The proposed method is outlined in detail in Fig. 11. Our approach involves incorporating an open-loop conduction loss estimation of the clamping diode, allowing for the selection of either Q2L modulation or 3L modulation in each switching cycle. In this way, we can achieve less total loss while preserving the diode volume reduction benefits of Q2L modulation. It is worth noting that our approach disregards reverse recovery loss since the SiC Schottky diode structure, which is typically adopted, has negligible reverse recovery loss.

$$P_{ave,3\mathrm{L}} = \frac{V_f\left(i_o\right) i_o T_o}{T_{\text{period}}} \tag{3}$$

$$\begin{cases} V_{ref}\, T_{\text{period}} = 0.5 V_{\text{dc}} T_p \\ T_0 = T_{\text{period}} - T_p = T_{\text{period}} \left(1 - \frac{V_{ref}}{0.5 \text{V}_{\text{dc}}}\right). \end{cases} \tag{4}$$

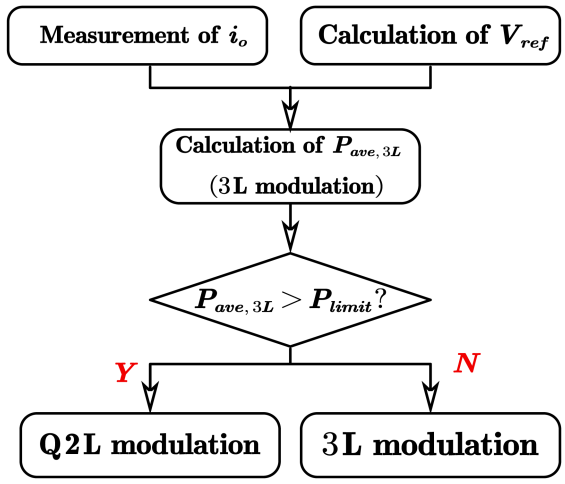



Fig. 11. Flowchart of proposed modulation strategy in each switching cycle.

The proposed modulation strategy includes an evaluation of the estimated clamping diode average conduction loss $P_{ave,3\mathrm{L}}$, which is further discussed in detail. Equation (3) shows that $P_{ave,3\mathrm{L}}$ is estimated using the forward voltage $V_f(i_o)$ and conduction time $T_0$ of the clamping diode, which can be calculated using the ac current $i_0$ and voltage reference $V_{ref}$, respectively. The forward voltage $V_f(i_o)$ can be obtained from the clamping diode's datasheet using curve fitting once the diode is selected. The conduction time $T_0$ for the zero-voltage level is determined using (4), as illustrated in Fig. 10.

After the estimated loss is calculated, the proposed modulation strategy compares $P_{ave,3\mathrm{L}}$ with the pre-set limit $P_{\text{limit}}$ to determine the conduction time of different voltage levels. If $P_{ave,3\mathrm{L}}$ is less than $P_{\text{limit}}$, 3L modulation is selected to save the switching loss of $S_1$–$S_4$. If $P_{ave,3\mathrm{L}}$ exceeds $P_{\text{limit}}$, Q2L modulation is selected to limit the conduction loss of clamping diodes. In this case, the conduction time $T_0$ for the zero-voltage level is chosen to achieve clamping diode loss equal to $P_{\text{limit}}$, as shown in (5). The maximum conduction time of clamping diodes is used when the conduction loss does not exceed $P_{\text{limit}}$, as expressed in (6). Fig. 12 shows that a larger zero voltage level conduction time helps reduce current ripple. The conduction time for the other voltage level can be calculated using (1)

$$P_{ave,Q2L} = \frac{V_f\left(i_o\right) i_o T_o}{T_{\text{period}}} = P_{\text{limit}} \tag{5}$$

$$T_o = \frac{P_{\text{limit}} T_{\text{period}}}{V_f\left(i_o\right) i_o}. \tag{6}$$

Fig. 13 illustrates the carrier-based modulation used to generate the PWM control signals. This type of modulation was chosen as it can be applied to both single-phase and three-phase operation. Switching cycle #1 depicts Q2L modulation, while switching cycle #2 shows 3L modulation. The selection of Q2L modulation or 3L modulation can be achieved by controlling the difference between the voltage references $V_{ref1}$ of $S_1$ and $V_{ref2}$ of $S_2$.

With the proposed modulation strategy, the average conduction loss of the clamping diodes in every switching cycle is

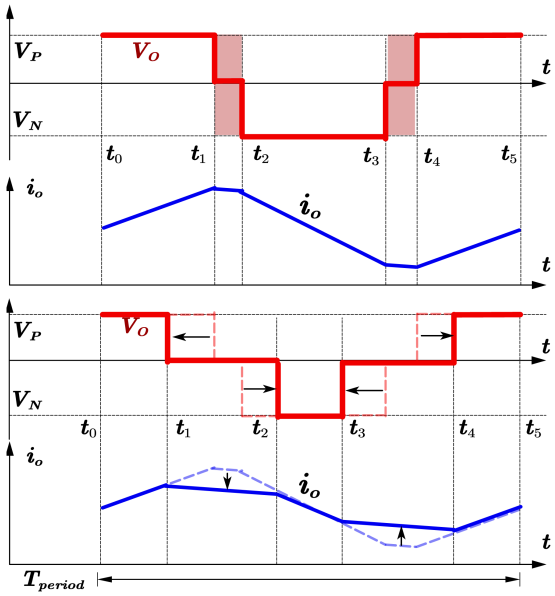



Fig. 12. Illustration of relation between the load current ripple and zero voltage level conduction time in Q2L modulation.

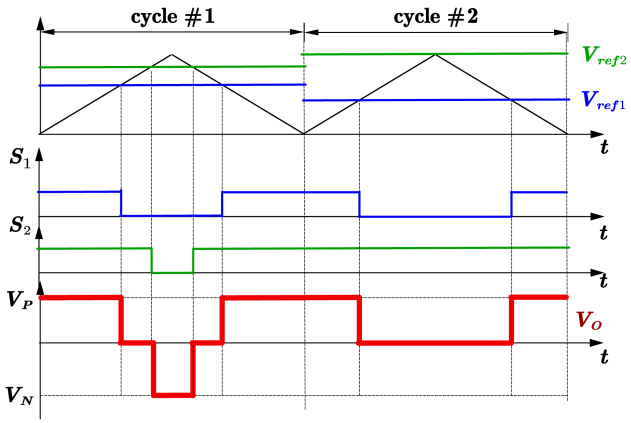



Fig. 13. Carrier-based modulation to generate the PWM control signals.

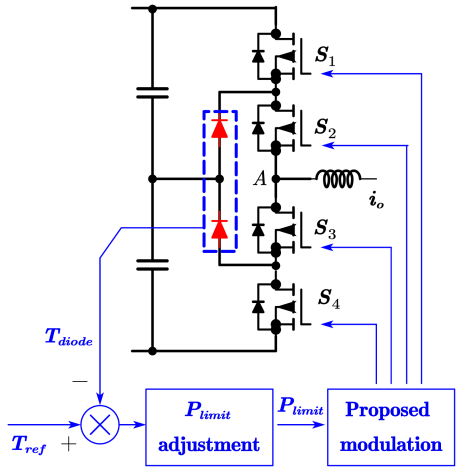



Fig. 14. Closed-loop control diagram for clamping diode temperature.

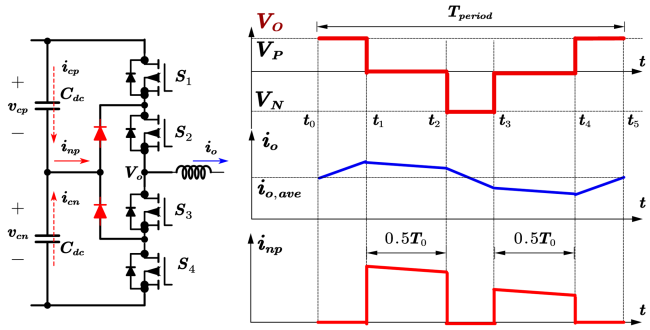



Fig. 15. Illustration of $i_{np}$ impact on DC-link neutral-point voltage.

less than $P_{\text{limit}}$, ensuring that the actual conduction loss is also less than $P_{\text{limit}}$. By properly selecting $P_{\text{limit}}$, the proposed modulation strategy does not cause any thermal issues with the clamping diodes. Additionally, the proposed modulation strategy allows for the use of 3L modulation in some switching cycles, which reduces the switching loss of MOSFETs.

In implementing the proposed modulation strategy, there are different approaches to determining $P_{\text{limit}}$. One solution is to estimate the maximum allowable loss of the clamping diodes based on thermal resistances or experimental measurements. However, there may be estimation errors that could affect the actual temperature of the diodes. Closed-loop control on the temperature of the clamping diode could also be introduced. As shown in Fig. 14, the temperature of the clamping diode $T_{\text{diode}}$ could be continuously measured and used to determine $P_{\text{limit}}$. When $T_{\text{diode}}$ exceeds the reference, $P_{\text{limit}}$ could be reduced to lower the clamping diode loss, or vice versa. Since clamping diodes usually take at least tens of seconds to significantly change temperature, the frequency of the temperature sensor does not need to be close to the switching frequency of the SiC MOSFETs.

In addition to the impact on clamping diode conduction loss, it is also important to evaluate the effect of the proposed modulation on neutral point potential balancing. The charge and discharge of two dc-link capacitors caused by the current $i_{np}$ are depicted in Fig. 15 and can be expressed in (7), while the change in voltage difference $\Delta(V_{cp}\text{-}V_{cn})$ during each switching cycle is given in (8). The term $i_{o,ave}T_0$ in (4) and (5) is related to the conduction loss, and as such, the relation between clamping diode conduction loss and $\Delta(V_{cp}\text{-}V_{cn})$ can be expressed in (9) and (10). Notably, by controlling $P_{\text{limit}}$, the dc capacitor voltage ripple can also be regulated, as shown in (10)

$$i_{np} = C_{\text{dc}} \frac{dv_{cp}}{dt} - C_{\text{dc}} \frac{dv_{cn}}{dt} \tag{7}$$

$$\Delta\ (V_{cp} - V_{cn}) = \frac{1}{C_{\text{dc}}} \int_0^{T_{\text{period}}} i_{np} dt \tag{8}$$

$$P_{\text{limit}} \geq \frac{V_f\,(i_{o,ave})\, i_{o,ave} T_o}{T_{\text{period}}}$$

$$= \frac{V_f\,(i_{o,ave})\, C_{dc}}{T_{\text{period}}}\, \Delta\,(V_{cp} - V_{cn}) \tag{9}$$

$$\Delta\,(V_{cp} - V_{cn}) \leq P_{\text{limit}} \frac{T_{\text{period}}}{V_f\,(i_{o,ave})\, C_{\text{dc}}}. \tag{10}$$

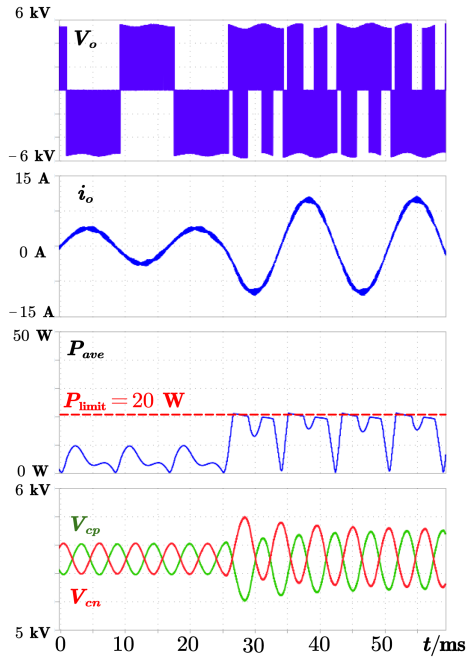



Fig. 16. Simulation of proposed modulation under load current transient.

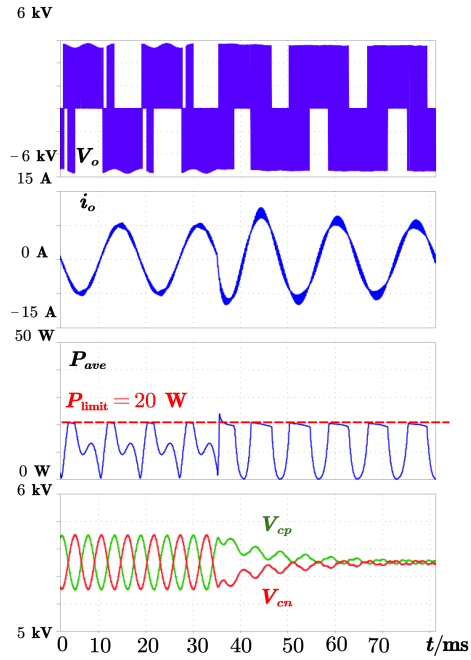



Fig. 17. Simulation of proposed modulation under power factor change.

### *B. Simulation Verification*

To verify the proposed modulation strategy, simulations are first conducted. The simulation condition is a three-phase 3L NPC converter connected with the grid with an L filter. The simulation parameters are shown in Table II. The dc-link capacitor $C_{\text{dc}}$ is 10 $\mu$F.

Fig. 16 shows the simulation results for the proposed modulation strategy under load transient. The waveform demonstrates that the strategy can automatically adjust the 3L modulation to Q2L modulation while estimating the loss of every switching cycle. Similarly, Fig. 17 depicts the simulation results under power factor change. Here, $P_{ave}$ represents the average conduction loss on the clamping diodes in each switching cycle, while $V_o$, $i_o$, $V_{cp}$, and $V_{cn}$ denote the output voltage, output current, and two dc-link capacitor voltages, respectively (as shown in Fig. 15). As can be seen from the simulation results in Figs. 16 and 17, the proposed modulation strategy effectively limits the conduction loss of clamping diodes under all conditions. To evaluate the strategy's performance, we selected 20 W for $P_{\text{limit}}$, which represents the maximum loss of clamping diodes with Q2L modulation in the simulation. Under this condition, the phase-leg current is 10 A (rms), and clamping diodes conduct 10 $\mu$s in each switching cycle with Q2L modulation. Overall, our proposed modulation strategy ensures that clamping diode loss does not exceed the maximum loss in Q2L modulation while reducing the switching loss of SiC MOSFETs with 3L modulation.

Fig. 18 shows the simulation waveform of the proposed modulation strategy with different $P_{\text{limit}}$ values. With a smaller $P_{\text{limit}}$, the period with Q2L modulation is increased to limit the conduction loss on clamping diodes. Additionally, the waveform shows that the maximum voltage difference $\Delta V_{np,\max}$ between the dc capacitors is reduced when the $P_{\text{limit}}$ is lowered.

To further demonstrate the effectiveness of the proposed modulation strategy, we conducted simulations for total device loss $P_{\text{device}}$ (including clamping diodes and SiC MOSFETs), clamping diode loss $P_{\text{diode}}$, and maximum voltage difference $\Delta V_{np,\max}$ under different ac load current conditions. The simulations were conducted for two power factors: 1 and 0. $P_{\text{diode}}$ and $P_{\text{device}}$ were calculated for a single phase leg, and $\Delta V_{np,\max}$ was simulated with three-phase operation. The results are presented in Fig. 19.

As shown in Fig. 19, under light load conditions, the proposed modulation strategy behaves similarly to 3L modulation due to the small clamping diode loss, resulting in reduced total device loss compared to Q2L modulation. However, for the rest of the load current conditions, the proposed modulation strategy automatically switches between 3L modulation and Q2L modulation to control the clamping diode loss. Furthermore, the switching loss of MOSFETs remains lower than Q2L modulation. Notably, the proposed modulation strategy also helps limit $\Delta V_{np,\max}$.

Overall, Fig. 19 demonstrates two significant benefits of the proposed modulation strategy. First, it can maintain more efficient 3L modulation when the clamping diode loss is acceptable. Second, it can limit the peak clamping diode loss when the 3L modulation causes large losses on the clamping diodes.

### *C. Proposed Modulation Strategy for Single Converter in DC–AC Application*

The preceding analysis demonstrates that the proposed modulation strategy is a superior alternative to the Q2L modulation strategy for the specific applications discussed in the introduction. As single NPC converters are widely employed in dc–ac applications, the proposed modulation strategy must also be

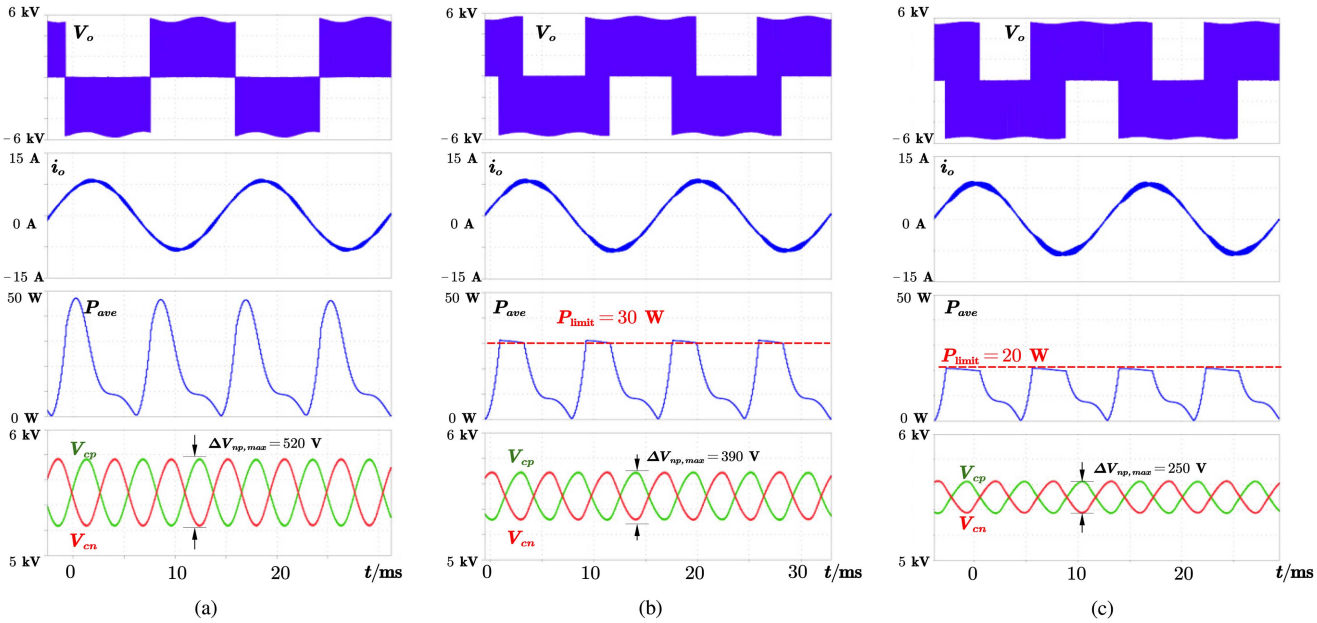



Fig. 18. Simulation of proposed modulation with different $P_{\text{limit}}$. (a) 3L modulation. (b) $P_{\text{limit}} = 30$ W. (c) $P_{\text{limit}} = 20$ W.

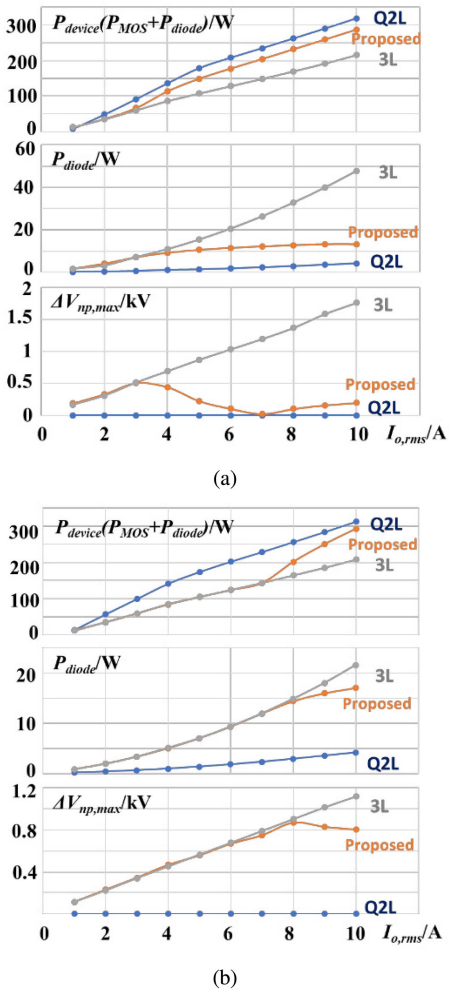



Fig. 19. Loss comparison of different modulation strategies under different power factors. (a) PF = 0. (b) PF = 1.

evaluated for such applications. In contrast to the Q2L modulation strategy, which leads to increased volume of the ac filter and reduced power density, the proposed modulation strategy is appropriate for the NPC converter in dc–ac applications with a different $P_{\text{limit}}$ for clamping diode loss.

In most dc–ac applications, the converter's power factor is usually near 1 during normal operation. By selecting $P_{\text{limit}}$ slightly higher than the maximum diode loss during normal operation, the proposed modulation strategy becomes equivalent to 3L modulation during such periods. With this $P_{\text{limit}}$ selection, the proposed modulation strategy can limit the diode conduction loss only under abnormal operating conditions, unlike the 3L modulation strategy, where diode conduction loss under abnormal conditions may be much higher than the loss under normal operating conditions.

Moreover, the proposed modulation strategy's more flexible clamping diode selection facilitates the commutation loop design of the NPC converter [42], [43]. The commutation loop inductance is a crucial design challenge for the circuit layout of the NPC converter. For high-power SiC MOSFET-based NPC converters, replacing clamping diodes with active switches is a practical solution to reducing the commutation loop inductance, but it incurs extra costs related to additional switches and gate drivers. The smaller clamping diode volume enabled by the proposed modulation strategy offers an alternative means of reducing the commutation loop inductance, as it allows for more flexible placement of clamping diodes in the converter design.

In summary, the proposed modulation strategy may also be appealing for single NPC converters in dc–ac applications. However, its impact on the converter design with various $P_{\text{limit}}$ values requires further detailed research. This article should involve a comparison of detailed converter designs and consider the converter's power rating and voltage rating, which are outside the scope of this article. This article primarily focuses on a better

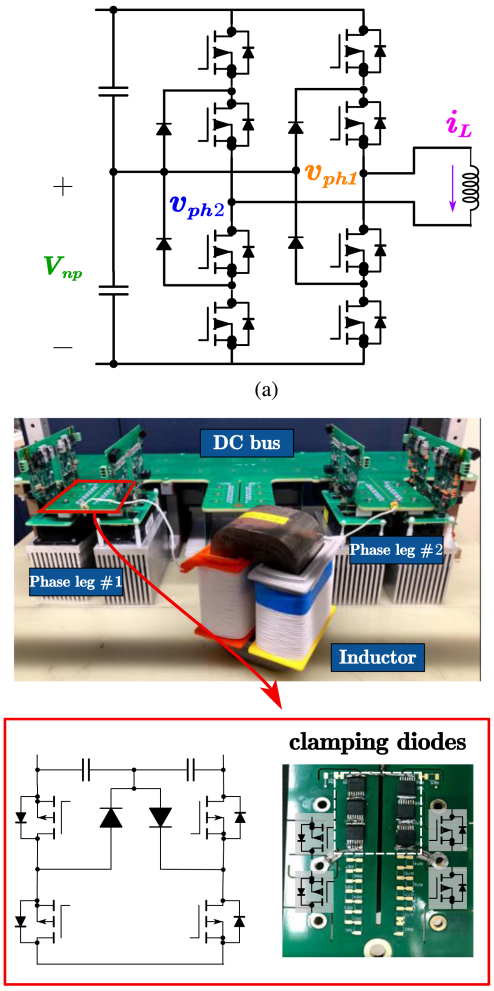



Fig. 20. Test setup for verifying the proposed modulation strategy. (a) Configuration. (b) Actual prototype.

alternative approach to the two-level converter structure with series-connected switches.

## IV. Experiment Verification

Fig. 20 illustrates an NPC 3L phase-leg design using the proposed modulation strategy, where the extra clamping diodes are implemented with diodes from Fig. 3, without requiring an external heatsink. This phase leg is a modification of the 2L phase leg with series-connected SiC MOSFETs, as described in [23]. The small volume of the clamping diodes is negligible compared to the overall power stage design and facilitates the phase-leg design. In traditional 3L NPC phase-leg designs, careful placement of both SiC MOSFETs and diodes is required to reduce switching loop inductance, as the high *dv/dt* of SiC MOSFETs can result in a large voltage spike during the switching transient. However, in the proposed design, the layout of the phase-leg mainly needs to consider the SiC MOSFETs, while the small volume diodes can be easily integrated with the bus-bar, simplifying the layout design and reducing switching loop inductance.

TABLE III
Experiment Parameters

| Parameters | Value |
|---|---|
| Dc-link voltage | 2 kV |
| Dc-link capacitor | 3 $\mu$F |
| Switching frequency | 10 kHz |
| Load Inductor | 8 mH |

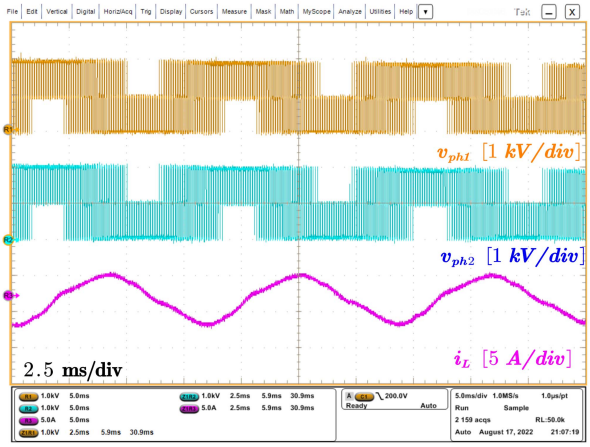
The experiments are conducted to verify: 1) the phase leg could operate without direct series connection of SiC MOSFETs; 2) the clamping diode temperature could be controlled with the proposed modulation strategy. The test parameters are shown in Table III.

Fig. 21 presents the waveform of the proposed modulation strategy, where a 2 kV dc bus voltage is used to demonstrate the modulation. During the open-loop control test, the power factor was close to 0. The experiment shows that the modulation switches between Q2L and 3L depending on the current. When the current is close to 0, the modulation is kept as 3L to minimize the number of switching events. As the current increases, the modulation is switched to Q2L to limit the conduction loss on the clamping diodes during the switching cycle. These results confirm that the proposed modulation strategy can be effectively implemented during operation.

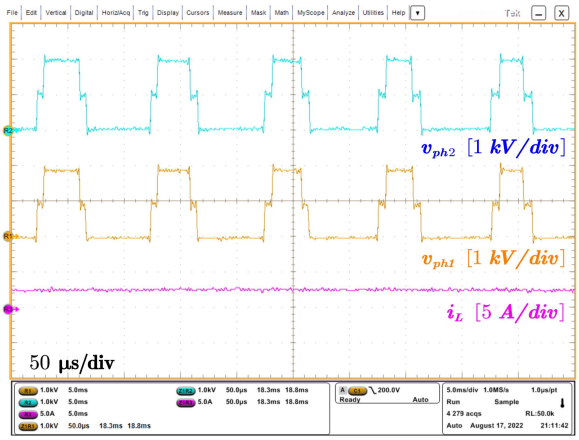
Fig. 21 demonstrates the application of the proposed modulation strategy to both phase-legs, which cancels out its impact on the dc neutral point voltage. To highlight the modulation's impact on the dc neutral point voltage, one of the phase-legs was switched to 2L modulation, where the zero-voltage level is not used for modulation, and only one phase leg affects the dc capacitor voltages. The resulting waveform is shown in Fig. 22. Fig. 22(a) shows that $v_{np}$ has small ripples when only one phase-leg is controlled with the proposed modulation strategy. As discussed in Section III, the $v_{np}$ ripple is affected by the 3L modulation operation time, which is determined by $P_{\text{limit}}$. Fig. 22(b) shows the $v_{np}$ waveform under larger 3L modulation operation time, indicating that the voltage ripple on the dc neutral point increases with more switching cycles in 3L modulation, which matches the simulation waveform in Fig. 17.

Although there is some current distortion in Figs. 21 and 22 due to open-loop modulation, the experiment is sufficient to verify the proposed modulation strategy. It is important to note that no closed-loop control was applied to the current to compensate for the impact of nonideal MOSFET switching and dc neutral point voltage ripple.

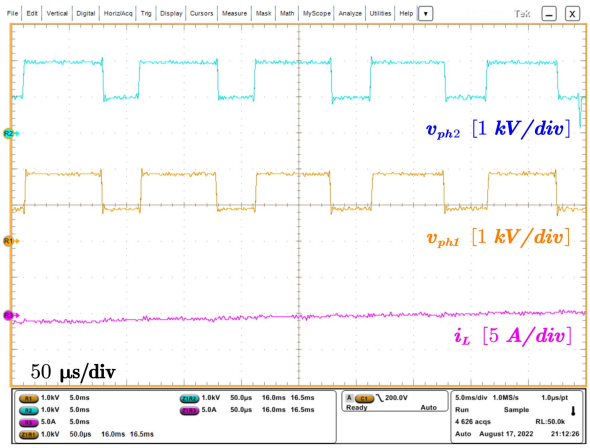
To investigate the impact of modulation on clamping diode loss, a phase-leg with different modulation strategies but the same output current (2 A rms) was tested. The dc bus voltage was set at around 500 V, and SiC MOSFETs did not face any thermal problems. The modulation index was 0.7, the switching frequency was 10 kHz, and the power factor was 0. For the experiments in Figs. 23–25, the phase-leg was controlled with the same power factor and current (with the same voltage reference in open-loop control), and only the modulation strategy was varied. The test results are shown in Figs. 23–25, and the temperature of clamping diodes under different modulation strategies is summarized in Table IV.




(a)




(b)

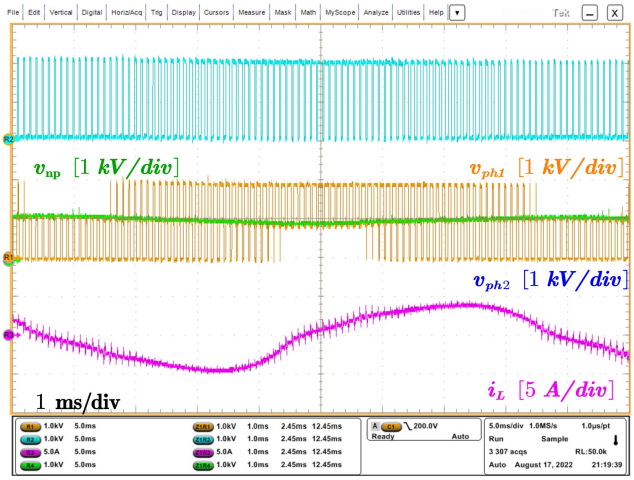



(c)

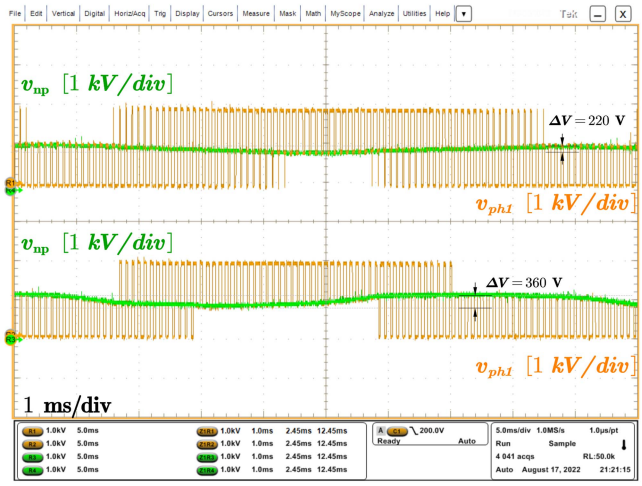
Fig. 21. Experiment result with proposed modulation. (a) Line frequency waveform. (b) Zoom-in waveform of Q2L modulation period. (c) Zoom-in waveform of 3L modulation period.

TABLE IV
CLAMPING DIODE TEMPERATURE IN DIFFERENT MODULATION STRATEGIES

| Modulation strategy | 3L modulation (see Fig. 23) | Proposed modulation (see Fig. 25) | Q2L modulation (see Fig. 24) |
|---|---|---|---|
| Maximum temperature of diodes | 90 °C | 61.4 °C | 40.5 °C |




(a)




(b)

Fig. 22. DC neutral point voltage ripple with proposed modulation. (a) Experiment waveform of one $P_{\text{limit}}$. (b) Comparison with different $P_{\text{limit}}$.

Fig. 23 shows the temperature of the clamping diode with a 3L modulation strategy. The 3L modulation strategy cannot control the conduction time of the clamping diodes, and as a result, when the power factor is close to 0 in Fig. 23, the clamping diodes have a long conduction time in the switching cycles when the current is close to the peak value. Although the current is only 2A (rms), the clamping diodes reach 90 °C in less than 10 min, indicating thermal problems with the diode selection. In contrast, Fig. 24 shows the temperature of the clamping diode with the Q2L modulation strategy, indicating that changing the modulation strategy can reduce the loss of clamping diodes. The diode temperature is less than 50 °C. However, this result also indicates that the Q2L modulation is not an optimal modulation strategy at the tested load current because the diode temperature is very low, requiring a new modulation strategy.

Fig. 25 shows the temperature of the clamping diode with the proposed modulation strategy in Section III. The experiment shows that with the proposed modulation strategy, the temperature can be controlled to better utilize the thermal capability

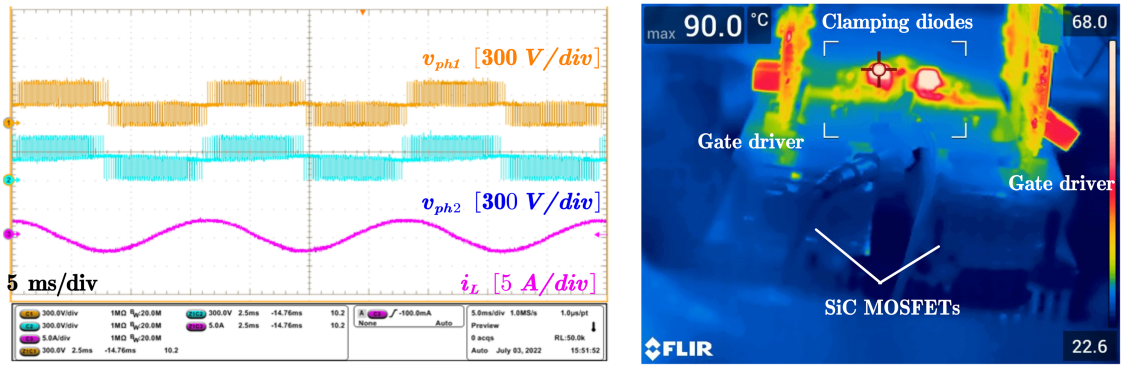



Fig. 23. Clamping diodes temperature with 3L modulation in less than 10 min of operation.

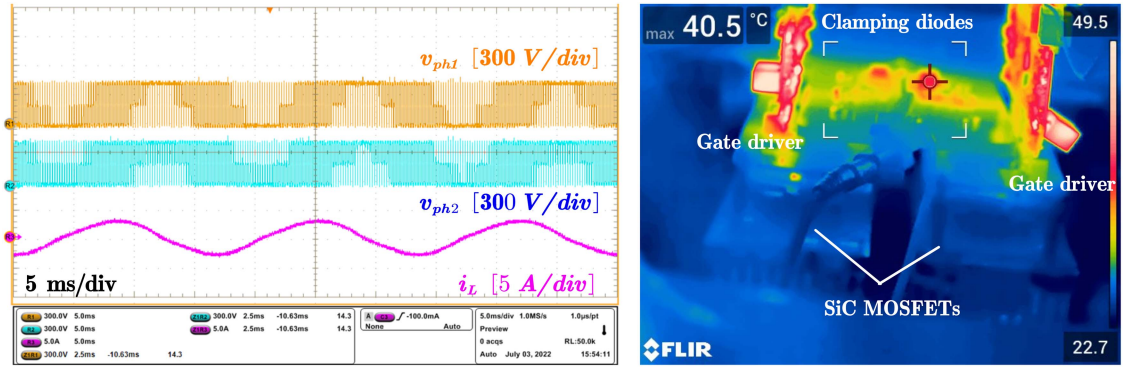



Fig. 24. Clamping diodes temperature with Q2L modulation after 10 min of operation.

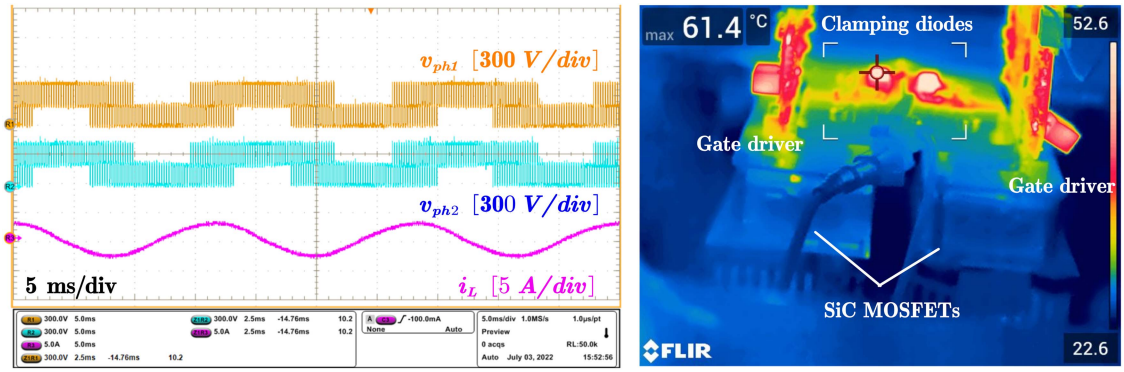



Fig. 25. Clamping diodes temperature with proposed modulation strategy after 10 min of operation.

of the clamping diodes. In addition, the Q2L modulation is not required for all the switching cycles, helping to reduce the switching loss of the SiC MOSFETs. Although the experiments in Figs. 23–25 have some distortion in current due to open-loop modulation, the results confirm the impact of the proposed modulation strategy on clamping diode loss and its effectiveness in controlling the temperature of clamping diodes.

## V. Conclusion

In conclusion, this article presents a 3L NPC converter-level approach to connect SiC MOSFETs in series, with a focus on reducing the loss on clamping diodes. The 3L NPC converter structure can avoid direct series connection of SiC MOSFETs without significantly increasing the converter volume, by changing the modulation strategy. Furthermore, the NPC structure is shown to be a better option than the capacitor-based multilevel structure as the converter-level approach for series-connected SiC MOSFETs. This article also proposes a new modulation strategy for the 3L NPC converter structure by adopting the combination of 3L modulation and Q2L modulation based on loss estimation. Compared to the Q2L modulation, the proposed modulation strategy achieves better loss control of clamping diodes and improves overall efficiency. Therefore, the 3L NPC converter structure with the proposed modulation strategy is a better option in applications where the 2L converter structure

with series-connected SiC MOSFETs is suitable. The experiment results presented in this article validate the proposed modulation strategy.

## REFERENCES


[1] D. Dong, X. Lin, L. Ravi, N. Yan, and R. Burgos, "Advancement of SiC high-frequency power conversion systems for medium-voltage high-power applications," in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf.*, 2020, pp. 717–724, doi: 10.1109/IPEMC-ECCEAsia48364.2020.9367948.

[2] D. Dong, M. Agamy, J. Z. Bebic, Q. Chen, and G. Mandrusiak, "A modular SiC high-frequency solid-state transformer for medium-voltage applications: Design, implementation, and testing," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 768–778, Jun. 2019, doi: 10.1109/JESTPE.2019.2896046.

[3] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99.1% efficient 10 kV SiC-based medium-voltage ZVS bidirectional single-phase PFC AC/DC stage," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 779–797, Jun. 2019.

[4] S. Ji et al., "Medium voltage (13.8 kV) transformer-less grid-connected DC/AC converter design and demonstration using 10 kV SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 1953–1959.

[5] J. Pan et al., "7-kV, 1-MVA SiC-based modular multilevel converter prototype for medium-voltage electric machine drives," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10137–10149, Oct. 2020.

[6] S. Mocevic et al., "Power cell design and assessment methodology based on a high-current 10-kV SiC MOSFET half-bridge module," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 3916–3935, Aug. 2021, doi: 10.1109/JESTPE.2020.2995386.

[7] J. Wang, S. Mocevic, R. Burgos, and D. Boroyevich, "High-scalability enhanced gate drivers for SiC MOSFET modules with transient immunity beyond 100 V/ns," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10180–10199, Oct. 2020.

[8] J. Wang, R. Burgos, D. Boroyevich, and Z. Liu, "Design and testing of 6 kV H-bridge power electronics building block based on 10 kV SiC MOSFET module," in *Proc. Int. Power Electron. Conf.*, 2018, pp. 3749–3756.

[9] K. Vechalapu and S. Bhattacharya, "Performance comparison of 10 kV# x2013; 15 kV high voltage SiC modules and high voltage switch using series connected 1.7 kV LV SiC MOSFET devices," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8.

[10] C. Li, S. Chen, H. Luo, C. Li, W. Li, and X. He, "A modified RC snubber with coupled inductor for active voltage balancing of series-connected SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11208–11220, Oct. 2021.

[11] S. Parashar and S. Bhattacharya, "A novel gate driver for active voltage balancing in 1.7 kV series connected SiC MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 2773–2779.

[12] V. K. Miryala, S. Dhanasekaran, P. Ganesan, K. Hatua, and S. Bhattacharya, "Active gate driving technique for series connecting SiC MOSFETs in the presence of gate pulse delay mismatch," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12402–12413, Dec. 2022.

[13] I. Lee and X. Yao, "Active gate control for series connected SiC MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 453–457.

[14] A. Marzoughi, R. Burgos, and D. Boroyevich, "Active gate-driver with dv/dt controller for dynamic voltage balancing in series-connected SiC MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2488–2498, Apr. 2019.

[15] E. Raszmann, K. Sun, R. Burgos, I. Cvetkovic, J. Wang, and D. Boroyevich, "Voltage balancing of four series-connected SiC MOSFETs under 2 kV bus voltage using active dv/dt control," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 6666–6672.

[16] Y. Zhou, L. Xian, and X. Wang, "Variable turn-OFF gate voltage drive for voltage balancing of high-speed SiC MOSFETs in series-connection," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9285–9297, Aug. 2022.

[17] Y. Zhou, X. Wang, L. Xian, and D. Yang, "Active gate drive with gate–drain discharge compensation for voltage balancing in series-connected SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5858–5873, May 2021.

[18] T. Wang, H. Lin, and S. Liu, "An active voltage balancing control based on adjusting driving signals time delay for series-connected SiC MOSFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 454–464, Mar. 2020.

[19] P. Wang, F. Gao, Y. Jing, Q. Hao, K. Li, and H. Zhao, "An integrated gate driver with active delay control method for series connected SiC MOSFETs," in *Proc. IEEE 19th Workshop Control Model. Power Electron.*, 2018, pp. 1–6.

[20] K. Shingu and K. Wada, "Digital control based voltage balancing for series connected SiC MOSFETs under switching operations," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 5495–5500.

[21] Z. Zhang et al., "High precision gate signal timing control based active voltage balancing scheme for series-connected fast switching field-effect transistors," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 925–930.

[22] X. Lin, L. Ravi, Y. Zhang, R. Burgos, and D. Dong, "Analysis of voltage sharing of series-connected SiC MOSFETs and body-diodes," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7612–7624, Jul. 2021.

[23] X. Lin, L. Ravi, R. Burgos, and D. Dong, "Hybrid voltage balancing approach for series-connected SiC MOSFETs for DC–AC medium-voltage power conversion applications," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8104–8117, Jul. 2022, doi: 10.1109/TPEL.2022.3149146.

[24] J. Zhang, S. Shao, Y. Li, J. Zhang, and K. Sheng, "A voltage balancing method for series-connected power devices in an LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3628–3632, Apr. 2021, doi: 10.1109/TPEL.2020.3025595.

[25] I. Lee and X. Yao, "Active voltage balancing of series connected SiC MOSFET submodules using pulsewidth modulation," *IEEE Open J. Power Electron.*, vol. 2, pp. 43–55, 2021, doi: 10.1109/OJPEL.2021.3054310.

[26] J. Yu and R. Burgos, "Operation and control of converters having integrated capacitor blocked transistor cells," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 2625–2632, doi: 10.1109/ECCE44975.2020.9235414.

[27] S. Milovanovic and D. Dujic, "Comprehensive analysis and design of a quasi two-level converter leg," *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 3, pp. 181–196, 2019.

[28] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams, "Quasi two-level operation of modular multilevel converter for use in a high-power DC transformer with DC fault isolation capability," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 108–123, Jan. 2015.

[29] A. Mertens and J. Kucka, "Quasi two-level PWM operation of an MMC phase leg with reduced module capacitance," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6765–6769, Oct. 2016.

[30] Y. Wang, Q. Song, B. Zhao, J. Li, Q. Sun, and W. Liu, "Quasi-square-wave modulation of modular multilevel high-frequency DC converter for medium-voltage DC distribution application," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7480–7495, Sep. 2018.

[31] H. You and X. Cai, "Stepped two-level operation of nonisolated modular DC/DC converter applied in high-voltage DC grid," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1540–1552, Sep. 2018.

[32] C. Wang, K. Wang, Z. Zheng, and Y. Li, "A new control strategy for modular multilevel converter operating in quasi two-level PWM mode," in *Proc. Int. Power Electron. Conf.*, 2018, pp. 2386–2392.

[33] M. Schweizer and T. B. Soeiro, "Heatsink-less Quasi 3-level flying capacitor inverter based on low voltage SMD MOSFETs," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. P1–P10.

[34] S. Mersche, D. Bernet, and M. Hiller, "Quasi-two-level flying-capacitor-converter for medium voltage grid applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 3666–3673.

[35] S. Gierschner, Y. Hein, M. Gierschner, A. Sajid, and H.-G. Eckel, "Quasi-two-level operation of a five-level flying-capacitor converter," in *Proc. 21st Eur. Conf. Power Electron. Appl.*, 2019, pp. P.1–P.9.

[36] P. Czyz, P. Papamanolis, T. Guillod, F. Krismer, and J. W. Kolar, "New 40kV/300kVA quasi-2-level operated 5-level flying capacitor SiC 'Super-Switch' IPM," in *Proc. 10th Int. Conf. Power Electron. ECCE Asia*, 2019, pp. 813–820.

[37] G. P. Adam, S. J. Finney, A. M. Massoud, and B. W. Williams, "Capacitor balance issues of the diode-clamped multilevel inverter operated in a quasi two-state mode," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 3088–3099, Aug. 2008.

[38] C. Lu, W. Hu, H. Wu, and F. C. Lee, "Quasi-two-level bridgeless PFC rectifier for cascaded unidirectional solid state transformer," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 12033–12044, Oct. 2021.

[39] J. Liu, C. Li, Z. Zheng, K. Wang, and Y. Li, "A quasi-two-level medium-voltage SiC MOSFET power module with low loss and voltage self-balance," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 519–533, Jan. 2022, doi: 10.1109/TPEL.2021.3098536.

[40] GeneSiC 3300V/5 A SiC Schottky Diode, GB05MPS33-263, 2020. [Online]. Available: https://genesicsemi.com/sic-schottky-mps/GB05MPS33-263/GB05MPS33-263.pdf

[41] FTCAP high voltage capacitors, HA10n8kd020050. [Online]. Available: https://www.ftcap.de/en/downloads/

[42] D. Zhang, J. He, and D. Pan, "A megawatt-scale medium-voltage high-efficiency high power density 'SiC+ Si' hybrid three-level ANPC inverter for aircraft hybrid-electric propulsion systems," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 5971–5980, Nov./Dec. 2019.

[43] H. Gui et al., "Modeling and mitigation of multiloops related device overvoltage in three-level active neutral point clamped converter," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7947–7959, Aug. 2020.

**Xiang Lin** (Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2015 and 2018, respectively, and the Ph.D. degree in power electronics from Center for Power Electronics Systems, Virginia Tech Blacksburg, VA, USA, in 2022.

After graduation, he was with the Tesla as an Electronics Design Engineer. His research interests include gate driver of 10 kV SiC MOSFET, series connection of SiC MOSFET, and multilevel converter.

**Dong Dong** (Senior Member, IEEE) received the B.S. degree from Tsinghua University, Beijing, China, in 2007, and the M.S. and Ph.D. degrees from Virginia Tech, Blacksburg, VA, USA, in 2009 and 2012, respectively, all in electrical engineering .

From 2012 to 2018, he was with GE Global Research Center, Niskayuna, NY, USA, as an Electrical Engineer. Since 2018, he has been an Assistant Professor with the Bradley Department of Electrical and Computer Engineering, Virginia Tech. He has authored and coauthored more than 20 referred journal publications and more than 50 IEEE conference publications. He currently holds 28 granted US patents. His research interests include modeling and design of single-phase to multiphase power converters, wide-band-gap power semiconductor-based high frequency power conversion, and power conversion system for grid, renewable, and transportation applications.

Dr. Dong is currently an Associate Editor for IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. He was the recipient of two Prize Paper Awards from the IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS.