O Splines-Based Fixed-Frequency Integral Sliding-Mode Controller for PFC Rectifier

Gabriel E. Mejia-Ruiz, *Student Member, IEEE*, Mario R. Arrieta Paternina, *Member, IEEE*,
José Antonio de la O Serna, *Senior Member, IEEE*, and Alejandro Zamora-Mendez, *Member, IEEE*

***Abstract*—This article proposes a fast-response sliding mode controller for a semibridgeless boost converter under large and quick load fluctuations to ensure tight output voltage regulation and unity power factor correction at the line side. In this sense, a novel approach for estimating the reference current profile is presented focusing on the real-time phasor estimation via the O-splines of the discrete-time Taylor-Fourier transform. This method allows for improving the computational efficiency and dynamic performance of the estimations of amplitude, frequency, and phase of the network voltage used for the generation of the reference current profile. Several aspects of the controller design are discussed, including the choice of the sliding surface, the existence and stability conditions, and the implementation of an adaptive hysteresis band to fix the switching frequency and reduce zero-crossing distortion. Experimental results of a GaN-based prototype validate the theoretical predictions, exhibiting a power factor close to 1 and a total harmonic distortion lower than 3.2% in presence of load changes of up to 50% and changes in the output voltage set point. Several comprehensive experimental comparisons between the proposed framework and the most widely used methods recently reported in the literature are accomplished in terms of transitory and steady-state responses. The robustness of the proposed control approach is experimentally demonstrated under sag conditions and a wide operating range of the input voltage.**

***Index Terms*—Active rectifier, adaptive hysteresis band (AHB), discrete-time Taylor-Fourier transform (DTTFT), GaN switches, nonlinear control, O-splines, power factor correction (PFC), sliding mode control (SMC).**

I. INTRODUCTION

IN RECENT years, many countries, policymakers, and research centers have recognized the growing need to develop more efficient and safe electrical systems, making them more reliable and environmentally friendly [1], [2]. In this scenario, circuits with automatic power factor correction (PFC) are one of the key technologies to reduce harmonic distortion and optimize the efficiency of the network infrastructure [3], [4], [5].

Currently, grid-connected equipment must guarantee a high power factor (PF) and low harmonic content according to the limits established by the IEEE 519 and IEC/EN 61000 standards [6], [7]. A comparison of different PFC boost converters is summarized in Table I.

The control targets in PFC rectifiers are emphasized to achieve a sinusoidal input current in phase with the network voltage and precisely regulate the dc output voltage. Although the development of PFC rectifier control systems has been extensively covered in previous studies [8], [9], [10], [11], two research gaps still remain: 1) the development of robust control systems with wide operational range; and 2) improving the synchronization methods to reduce the harmonic content, zero-crossing noise, and computational burden.

The sliding mode controller (SMC) grants stability and robustness to the PFC circuit against parameter, line voltage, and load uncertainties over a wide operating range and can be implemented with a straightforward control rule [2], [12], [13], [14]. However, the practical application of SMC in PFC converters is limited by the nonconstant switching frequency [15], [16], [17], [18], [19]. Variable operating frequency increases the size and cost of filters, inductors and heat sinks, as well as increases power losses.

To deal with the adverse variable switching frequency, several possible solutions have been proposed. These include the incorporation of constant timing functions or circuitries, increasing the complexity and cost of the overall system [20], [21]. The SMC with fixed frequency can also be implemented indirectly using pulse width modulation (PWM), but this approach reduces the robustness of the closed-loop system [4], [17], [22]. This work applies an adaptive hysteresis band (AHB) that allows operation with a fixed switching frequency without affecting the robustness of the SMC and without adding complexity to the system [16].

Aiming to synchronize the active rectifiers with the network voltage, the converter controller often embeds an active synchronization algorithm such as the phase-locked loop

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Gabriel E. Mejia-Ruiz is with the Graduated program in Electrical Engineering-Power Systems, National Autonomous University of Mexico (UNAM), Mexico City 04510, Mexico (e-mail: gabriel.mejia.ruiz@comunidad.unam.mx).

Mario R. Arrieta Paternina is with the Department of Electrical Engineering, National Autonomous University of Mexico (UNAM), Mexico City 04510, Mexico (e-mail: mra.paternina@fi-b.unam.mx).

José Antonio de la O Serna is with the Department of Electrical Engineering, Autonomous University of Nuevo Leon, Monterrey, NL 66450, Mexico (e-mail: delao@ieee.org).

Alejandro Zamora-Mendez is with the Electrical Engineering Faculty, Michoacan University of Saint Nicholas of Hidalgo (UMSNH), Michoacan 58030, Mexico (e-mail: azamoram@umich.mx).

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TABLE I
COMPARISON OF DIFFERENT PFC BOOST CONVERTERS

Reference	***Topology***	***Synchronization method***	***Fixed switching frequency***	***Controller***	***Computational requirements***	***validation by***
[25]	Conventional boost with diode bridge	The normalized measurement of the input voltage	No	Two loops, inner with hysteresis and external with linear controller	Medium	Experimental tests
[26]	Conventional interleaved boost with diode bridge	synchronized-OFF voltage-mode	No	Two loops with linear controllers	Medium	Experimental tests
[10]	Conventional interleaved boost with diode bridge	PLL	No	Linear controllers	High	Experimental tests
[9]	Conventional interleaved boost with diode bridge	The normalized measurement of the input voltage	No	Linear controllers	Medium	Experimental tests
[27]	Conventional boost with diode bridge	The normalized measurement of the input voltage	No	Two loops, inner with SMC and external with PI	Medium	Experimental tests
[4]	Conventional boost with diode bridge	The normalized measurement of the input voltage	Yes	Two loops, inner with SMC-PWM and external with PI	Medium	Simulations and experimental tests
[5]	ZVS hybrid resonant pulse-width modulated	The normalized measurement of the input voltage	Yes	Linear cascade controllers	Medium	Simulations and experimental tests
[19]	Interleaved Totem-Pole	The normalized measurement of the input voltage	Yes	SMC-PWM	Medium	Experimental tests
[23]	Totem-pole bridgeless	PLL	Yes	PR and PI linear controllers	Very high	Experimental tests
[11]	Semibridgeless with active virtual ground	PLL	Yes	Boundary and deadbeat	Very high	Experimental tests
Proposed controller	Semibridgeless with clamped diodes	O-splines-based estimations	Yes	Integral SMC	Low	Experimental tests

The bold entities highlight the column headings and the most significant results.

(PLL) [1], [23], [24]. PLLs work under harmonic distortion and voltage dips; nonetheless, their sophisticated algorithms require complex and large software routines to implement operations with high-resolution signals, preventing their implementation with low-cost platform processors and increasing the computational burden on the controller [1], [11], [23].

To effectively address the aforementioned issues, this article proposes a fixed switching frequency integral SMC with a sophisticated algorithm known as the O-splines of the discrete-time Taylor-Fourier transform (DTTFT) to precisely and timely estimate the amplitude, frequency and phase of the input voltage with low computational burden, even under transient conditions. The additional integral term in the sliding surface contributes to effectively reducing the steady-state error of the dc voltage. A GaN-based prototype of the PFC rectifier circuit was implemented to verify the control scheme. Experimental results are in close agreement with theoretical predictions.

Specifically, the primary contributions of the article are as follows.

1) This article presents a practical application of a SM controller with the O splines-based synchronization method (OSM) and an adaptive hysteresis band. The proposed approach reduces the execution time by 80.3% and exhibits an improved dynamic performance compared to the PI-based controller with PLL.
2) A procedure to calculate the AHB based on the dynamic states of the boost converter PFC is presented. The AHB allows for reducing the total harmonic distortion, ripple, and deformation at the zero crossing of the input current of the PFC rectifier circuit. Besides, this approach allows for fixing the switching frequency.
3) A new sliding surface with fast dynamic responses, inherent robust characteristics, and a wide operating range is proposed for application to the PFC rectifiers.

II. SYNTHESIS OF INTEGRAL SLIDING MODE CONTROLLER

Several converters with PFC have been proposed [3], [5], [8], [28], [29]. Among these, the semibridgeless boost converter (SBBC) stands out for reducing the number of semiconductor devices in the current path from the source to the load compared to the traditional input diode bridge boost converter. This results in a notable reduction in conduction losses, increasing its power density [4].

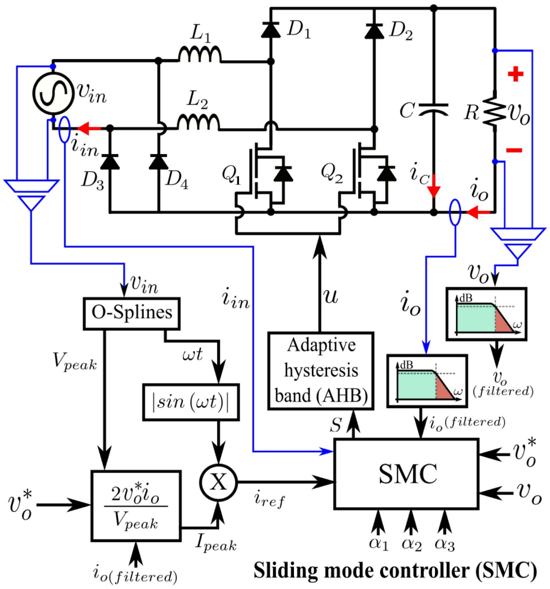


Fig. 1. Semibridgeless boost converter (SBBC) circuit and diagram of the proposed sliding mode controller for single-phase PFC applications.

The topology and the proposed controller of the SBBC are depicted in Fig. 1. This PFC converter has two inductors L_1 and L_2, four diodes D_1–D_4, two power switches Q_1 and Q_2, and a capacitor bank C. The SBBC can be modeled as a boost converter for each half cycle; where L_1, Q_1, D_1, and D_3 operate on the positive half cycle, whereas L_2, Q_2, D_2, and D_4 operate on the negative half cycle. The switches are activated with the control signal u ($u = 1$ ON-state and $u = 0$ OFF-state). Based on circuit analysis, the nonlinear model of the SBBC is given by

$$\frac{dv_o}{dt} = -\frac{v_o}{RC} + \frac{i_{in}}{C}(1-u) \tag{1}$$

$$\frac{di_{in}}{dt} = \frac{v_{in}}{L} - \frac{v_o}{L}(1-u) \tag{2}$$

where $L_1 = L_2 = L$, v_o and i_o are the voltage and current over the load, and the current and voltage at the line side are expressed as $i_{in} = I_{\text{peak}}\sin(\omega t)$ and $v_{in} = V_{\text{peak}}\sin(\omega t)$, respectively.

A. Architecture of the Proposed Controller

Two state variables such as input current (i_{in}) and v_o are selected to control the PFC-SBBC. This control structure has the following goals: 1) to control the waveform of i_{in}, keeping it sinusoidal and in phase with v_{in} to gain a unity PF; and 2) to regulate v_o with precision, low overvoltage, and fast response. In this scheme, the O-splines estimator provides the peak amplitude (V_{peak}) and frequency (ω) of v_{in} with high computational efficiency and low sampling rate. The amplitude (I_{peak}) of the reference current (i_{ref}) is calculated based on the power balance. The rectified sinusoidal waveform in phase with v_{in} is obtained from the estimated ω. v_o and i_o signals are filtered to remove high-frequency noise components. Finally, the AHB generates the trigger signal u from the sliding surface (s) and the dynamic model of the converter to set the fixed switching frequency.

B. Proposed Sliding Surface

The sliding surface ($S = 0$) is the core of the sliding mode control, driving the behavior of the controlled variables [13]. Then, the control law is constrained to the trajectory of the state variables, which is described by

$$S = \alpha_1(i_{\text{ref}} - i_{in}) + \alpha_2(v_o^* - v_o) + \alpha_3 \int (v_o^* - v_o)dt \tag{3}$$

where α_1, α_2, and α_3 represent the sliding coefficients and v_o^* is the reference value of v_o.

C. Generating a Suitable Reference-Current Profile

The reference current i_{ref} must have the suitable amplitude for providing the power required by the load and the sinusoidal waveform to reach a unity PF with low total harmonic distortion. Meanwhile, its amplitude, I_{peak}, is estimated using the power balance ($P = V_{\text{peak}}I_{\text{peak}}/2 = v_o^* i_o$), neglecting the converter's losses. The phase synchronization is obtained employing the ω estimated by the O-splines. Thus, i_{ref} can be represented by

$$i_{\text{ref}} = I_{\text{peak}}|\sin(\omega t)| = \frac{2 i_o v_o^*}{V_{\text{peak}}}|\sin(\omega t)|. \tag{4}$$

D. Transversality Condition

The transversality condition evaluates the ability of the controller to modify the system dynamics with the proposed switching surface, verifying that u is present in the derivative of the switching function, according to $\frac{d}{du}(\frac{dS}{dt}) \neq 0$ [12]. Thus, the time derivative of the switching function is expressed as follows:

$$\begin{aligned}\dot{S} = \alpha_1 &\left(\frac{2v_o^* i_o \omega}{V_{\text{peak}}}\text{sign}(\sin(\omega t))\cos(\omega t) - \frac{v_{in}}{L} + \frac{v_o}{L}(1-u)\right)\\ &+ \alpha_2\left(\frac{i_{in}}{C}(1-u) - \frac{v_o}{RC}\right) + \alpha_3(v_o^* - v_o).\end{aligned} \tag{5}$$

According to (6), the fulfillment of the transversality condition is given when $\frac{\alpha_2}{\alpha_1} \neq \frac{Cv_o}{Li_{in}}$

$$\frac{d}{du}\left(\frac{dS}{dt}\right) = \frac{\alpha_2 i_{in}}{C} - \frac{\alpha_1 v_o}{L} \neq 0. \tag{6}$$

E. Reachability and Existence Conditions

The selected switching surface must guarantee that the control action redirects the system trajectories to approach and eventually reach the sliding surface ($s = 0$), independent of the initial conditions of the system. To ensure the reachability condition, the necessary and sufficient condition ($s\dot{s} < 0$) must be satisfied [13]. Compliance with the reachability condition is achieved with the following control function:

$$u = \begin{cases} 1 & \text{if } S > 0 \text{ and } \dot{S} < 0 \\ 0 & \text{if } S < 0 \text{ and } \dot{S} > 0. \end{cases} \tag{7}$$

When the sliding surface is reached, it must be guaranteed that the system trajectories remain in the vicinity of the surface $S = 0$, ensuring the existence condition of the sliding mode. This condition can be determined by local inspection of the reachability condition, as follows:

$$\lim_{S\to 0^-} \frac{dS}{dt}\bigg|_{u=0} > 0 \quad \text{and} \quad \lim_{S\to 0^+} \frac{dS}{dt}\bigg|_{u=1} < 0. \tag{8}$$

The substitution of (5) and (7) into the previous conditions gives

$$\begin{aligned} 0 &> \alpha_1\left(K_1 - \frac{v_{in}}{L}\right) + \alpha_2\frac{v_o}{RC} + \alpha_3(V_{\text{ref}} - v_o)\\ &> \alpha_2\left(\frac{i_{in}}{C}\right) - \alpha_1\frac{v_o}{L} \end{aligned} \tag{9}$$

where K_1 is defined as $\frac{2V_{\text{ref}} i_o \omega}{V_{\text{peak}}}\text{sign}(\sin(\omega t))\cos(\omega t)$, and L, C, and V_{ref} are known parameters of the system and their values can be substituted directly into the inequality for inspection. v_{in}, i_{in}, and v_o represent the range of input and output operating conditions to comply with the existence condition.

F. Equivalent Dynamics and Control

The equivalent-control signal of the proposed SM controller applied to the SBBC is obtained by solving $dS/dt = 0$, which gives

$$u_{eq} = \frac{\alpha_1\left(K_1 - \frac{v_{in}}{L} + \frac{v_o}{L}\right) - \alpha_2\left(\frac{i_{in}}{C} - \frac{v_o}{RC}\right) + \alpha_3(V_{\text{ref}} - v_o)}{\frac{v_o \alpha_1}{L} - \frac{\alpha_2 i_{in}}{C}} \tag{10}$$

where u_{eq} is a control law that leads the system to slide over the surface in an ideal way, neglecting the high-frequency ripple [13]. The verification of u_{eq} within the operating limits of u $(0 < u_{eq} < 1)$ determines the region in the state-space, thereby the sliding regime can be created. In this case, the evaluation of u at its operational limits corroborates the inequality (9) where the sliding regime exists. The corresponding ideal sliding dynamics are given by (11) and (12), respectively, as follows:

$$\frac{di_{in}}{dt} = \frac{v_{in}}{L} - \frac{v_0}{L}K_2 \tag{11}$$

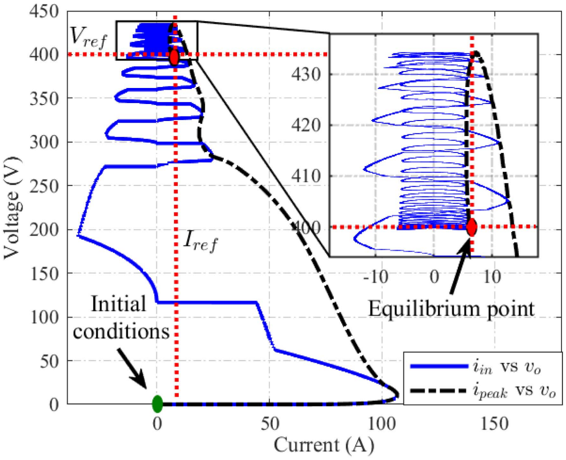


Fig. 2. Trajectories obtained from the ideal sliding dynamics model.

$$\frac{dv_0}{dt} = \frac{i_{in}}{C} K_2 - \frac{v_0}{RC} \tag{12}$$

where K_2 is given by

$$K_2 = \frac{\alpha_1\left(\frac{v_0 - v_{in}}{L} - K_1\right) - \alpha_2\left(\frac{i_{in}}{C} - \frac{v_0}{RC}\right) + \alpha_3(v_{\text{ref}} - v_0)}{\alpha_2 \frac{i_L}{C} - \alpha_1 \frac{v_0}{L}}. \tag{13}$$

Fig. 2 shows the trajectories obtained from the ideal sliding dynamics model during startup. The converter trajectories slide from the initial conditions (0,0) until reaching the equilibrium point given by (I_{ref}, V_{ref}).

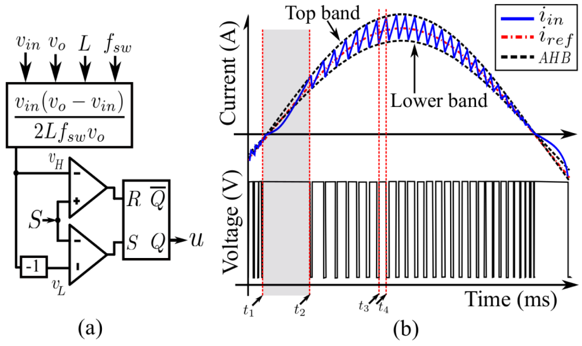
G. Stability Analysis of Ideal Sliding-Mode Dynamic Model

The stability of equivalent dynamic model (11) and (12) in steady state ($\frac{di_{in}}{dt} = 0$; $\frac{dv_0}{dt} = 0$) can be studied by using the linearized system around the equilibrium point $\mathbf{X}^* = [I_{in} \quad V_{\text{ref}}]$ [4], with $I_{in} = v_{\text{ref}}^2 / Rv_{in(\text{RMS})}$. It should be noted that the equilibrium point represents the root mean square (RMS) value of the variables in steady state. The evaluation of the Jacobian matrix $\mathbf{J}$ from (11) and (12) in $\mathbf{X}^*$ leads to define the characteristic polynomial of the system given by $P(s) = det(\mathbf{J} - s\mathbf{I}) = s^2 + a_1 s + a_2$. The linearized system is stable if $a_1 < 0$ and $a_2 > 0$, then the maximum value of a_1 is obtained when $\text{sign}(\sin(\omega t))\cos(\omega t) = 1$; under this condition, $a_1 < 0$ while the inequality (14) is satisfied.

$$\begin{aligned}\alpha_3 < {} & (v_{in}(C\alpha_2 v_{\text{peak}} R^2 v_{in}^2 \alpha_1 + 2Cv_{\text{ref}} v_{\text{peak}} Rv_{in}\alpha_2^2) \\ & - 2v_{in}(2v_{ref}^2 \alpha_1 \alpha_2 v_{\text{peak}} + 2Cv_{\text{ref}}^3 \alpha_1^2 \omega \\ & + Rv_{in} v_{\text{ref}} \alpha_2^2 v_{\text{peak}} + 2CRv_{in} v_{\text{ref}}^2 \alpha_1 \alpha_2 \omega))/Lv_{\text{ref}}^2 v_{\text{peak}} \\ & \times (Lv_{\text{ref}}\alpha_2 - CRv_{in}\alpha_2). \end{aligned} \tag{14}$$

The minimum value of a_2 is obtained when $\text{sign}(\sin(\omega t))\cos(\omega t) = -1$, then with the previous assertion, a_2 becomes greater than zero when

$$\alpha_2 > \frac{\alpha_2 L v_{\text{peak}} v_{\text{ref}}}{C v_{\text{peak}} R v_{in} + 2CL\omega v_{\text{ref}}^2}. \tag{15}$$



(a) (b)

Fig. 3. Adaptive hysteresis band (AHB). (a) Algorithm implementation. (b) AHB, input current (i_{in}) and control signal waveforms (u).

The proper selection of α_1, α_2, and α_3 will allow fulfilling the condition of stability around the operating point.

H. Adaptative Hysteresis Band

The detailed analysis of the mathematical model and the geometry of the current ripple (i_{in}) enables defining the hysteresis band of the modulator with a fixed frequency, as expressed in (16). An AHB also mitigates the harmonic distortion of i_{in} at the zero crossing, increasing the PF.

$$\text{AHB} = \frac{v_s(v_o - v_s)}{2Lf_{sw}v_o}. \tag{16}$$

The AHB is calculated in each sampling cycle and it is compared with the actual sample of S. The result of the comparison is stored in the RS flip-flop which generates the switching signal u, as shown in Fig. 3(a). The operation of the hysteresis band is illustrated in Fig. 3(b). When i_{in} crosses zero (at t_1), L is completely discharged, Q_1 closes allowing L to charge, and consequently, i_{in} increases exponentially until reaching the upper limit of AHB ($i_{in} \geq (i_{\text{ref}} + \text{AHB}/2)$). At t_2, Q_1 opens reducing i_{in} until it meets the condition $i_{in} \leq (i_{\text{ref}} - \text{AHB}/2)$. This technique allows that i_{in} remains within the hysteresis band, as detailed between t_3 and t_4.

III. O-SPLINES: FUNDAMENTALS

For network synchronization purposes, the fundamentals of the O-splines, obtained in closed form in [30] from the DTTFT, are described as follows. The DTTFT expands the Fourier subspace by incorporating Taylor terms greater than zero. As a consequence, a new Taylor-Fourier subspace is derived by including in the basis vectors of the Fourier matrix the Taylor terms of a Kth Taylor polynomial.

A. O-Splines Implementation

Since a specific finite impulse response (FIR) filter is required to deal with the phasor estimation process, this is designed by employing the lowpass O-splines in $\tilde{\mathbf{\Phi}}_0$ by solving in closed form the inverse of the Taylor matrix $\mathbf{\Upsilon}$ [30]. Thus, each vector in $\tilde{\mathbf{\Phi}}_0$ corresponds to the concatenation of the diagonals in each row of diagonal submatrices in $\mathbf{\Upsilon^{-1}}$. These vectors contain the

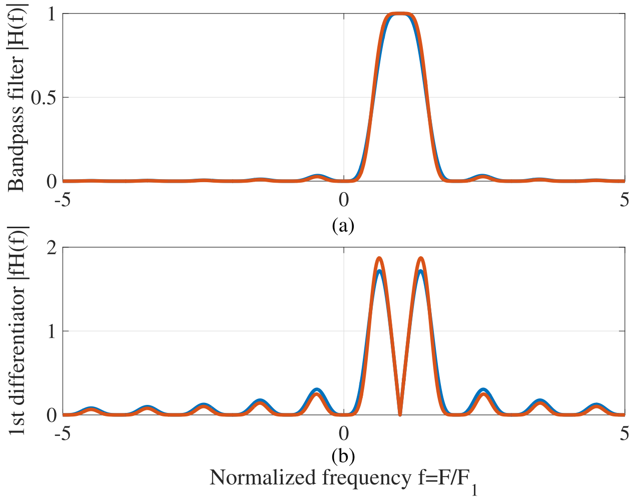


Fig. 4. Bandpass and first differentiator frequency response.

successive derivatives of the O-spline, which are the envelopes of the impulse responses of the bandpass filters at each harmonic frequency. Therefore, implementing the O-splines and their derivatives as lowpass filters, the computational complexity of the DTTFT is ostensibly decreased, since it is reduced to a small number of FIR filters [30]. In this work, only the phasor and its first derivative are needed at the nominal fundamental frequency. Fig. 4(a) shows the frequency responses of the DTTFT bandpass filters used in this article to extract the phasor of the measured signal for $K = 3$ and $K = 5$. While Fig. 4(b) depicts the frequency responses of the first differentiators for $K = 3$ and $K = 5$, respectively, at the nominal fundamental frequency. These FIR filters have a length of $(K + 1)N$, where K is the order of the O-spline, and N is the number of samples per fundamental period.

Thereby, the successive polynomial cyclic pieces of the Kth lowpass O-spline are given by [30]

$$\tilde{\varphi}_{1p}^{(K)}(u) = \frac{1}{D_p}\prod_{\substack{m=1,\\ m\neq p}}^{K+1}(u+m-p)\, p = 1, 2, \ldots, K+1 \tag{17}$$

where the constant D_c guarantees a unit value at $u = 0$ for each polynomial piece. Thus, the polynomial pieces for $p = 1, \ldots, K + 1$ of the O-spline of order $K = 3$ are given by

$$\tilde{\varphi}_{11}^{(3)}(u) = \frac{1}{6}(u+1)(u+2)(u+3), \qquad u \in [-2, -1); \tag{18}$$

$$\tilde{\varphi}_{12}^{(3)}(u) = -\frac{1}{2}(u-1)(u+1)(u+2), \quad u \in [-1, 0); \tag{19}$$

$$\tilde{\varphi}_{13}^{(3)}(u) = \frac{1}{2}(u-2)(u-1)(u+1), \qquad u \in [0, 1); \tag{20}$$

$$\tilde{\varphi}_{14}^{(3)}(u) = -\frac{1}{6}(u-3)(u-2)(u-1), \quad u \in [1, 2). \tag{21}$$

TABLE II

FREQUENCY SPECIFICATION OF THE BANDPASS FILTER

Filter No.	F_{min}(Hz)	F_c (Hz)	F_{max} (Hz)
1	30	60	90

The bold entities highlight the column headings and the most significant results.

Finally, the O-spline is given by the concatenation of the former cyclic pieces, in their corresponding domains

$$\tilde{\varphi}_{1}^{(3)}(u) = [\tilde{\varphi}_{11}^{(3)}(u), \tilde{\varphi}_{12}^{(3)}(u), \tilde{\varphi}_{13}^{(3)}(u), \tilde{\varphi}_{14}^{(3)}(u)]^T \tag{22}$$

$u \in [-2, 2)$.

B. Phasor Estimates by the DTTFT's O-Splines

For phasor estimation, the DTTFT bandpass filter for extracting the phasor is a simply modulated version of the O-spline at the nominal fundamental frequency. Thus, one FIR filter as specified in Table II is designed, where F_c corresponds to the central frequency (nominal fundamental frequency) and $[F_{\min}, F_{\max}]$ are the bounds for the desired passband, and the sampling rate (F_s) is equal to 1.92 KHz. The filter impulse response for processing voltage and current phasors is denoted as $\mathbf{h}_1$. Thereby, the impulse response for a phasor estimation is given by

$$\mathbf{h}_1(u) = \tilde{\varphi}_1^{(3)}(u)e^{j2\pi u}. \tag{23}$$

Finally, by taking N samples per fundamental cycle, we obtain the discrete-time impulse response of the bandpass filter as follows:

$$\mathbf{h}_1(n) = \tilde{\varphi}_1^{(3)}(n)e^{j\frac{2\pi}{N}n} \tag{24}$$

where $n = -\frac{(K+1)N}{2}, -\frac{(K+1)N}{2} + 1, \ldots, \frac{(K+1)N}{2} - 1$, for odd K.

By using the first differentiator at the fundamental frequency, the phasor derivative is estimated, and in turn, the frequency of voltage and current signals is also estimated. It should be noted that the first derivative of the O-spline is modulated at the fundamental frequency, as for the bandpass filter. Thus, the first differentiator is given by

$$\mathbf{h}_2(u) = F_c\tilde{\varphi}_2^{(3)}(u)e^{j2\pi u} \tag{25}$$

and its discrete-time version is given by

$$\mathbf{h}_2(n) = F_c\tilde{\varphi}_2^{(3)}(n)e^{j\frac{2\pi}{N}n}. \tag{26}$$

Once the FIR filters are designed by the O-splines in [30], the best Taylor-Fourier (TF) coefficients are provided by the following equation:

$$\hat{\boldsymbol{\xi}} = [\mathbf{h}_1\ \mathbf{h}_2]^H\mathbf{s}_n \tag{27}$$

where vector $\hat{\boldsymbol{\xi}}$ contains the estimated TF coefficients, in this case, the phasor and its first derivative, $\mathbf{s}_n$ is a vector array of the measured signal (voltage or current), and $[\mathbf{h}_1\ \mathbf{h}_{1\text{freq}}]$ are vectors of the corresponding dual matrix that carry the bandpass O-spline and its first derivative centered at

TABLE III
EXPERIMENTAL PARAMETERS

System ratings	**Specification**
Rated grid voltage (v_{in}), grid frequency	120 V_{RMS}, 60 Hz
Rated output voltage (v_o)	400 V
Rated power (P), rated load (R)	1 kW, 160 Ω
Switching frequency	50 kHz
Power converter components	
Digital signal processor	TMS320F28379D
Regular diodes (D_3,D_4)	GBJ2506
GaNs switches (Q_1,Q_2)	TP65H050WSQA
Fast diodes (D_1,D_2)	FFSP3065B
Current sensor, voltage sensor	CQ3202, AMC3330
Power converter parameters	
Boost inductances (L_1, L_2), DC link capacitance (C)	1.6 mH, 1.36 mF
Controllers' parameters	
α_1, α_2, α_3	1.2, 0.03, 0.005
PI voltage loop k_{PV}, k_{IV}	1.5, 5
PI current loop k_{PI}, k_{II}	0.5, 2

The bold entities highlight the column headings and the most significant results.

the fundamental frequency. Thus, the vector $\hat{\boldsymbol{\xi}}$ is defined, as follows:

$$\hat{\boldsymbol{\xi}} = [\hat{\xi}_c \quad \dot{\hat{\xi}}_c]^T. \tag{28}$$

Finally, the estimates of amplitude and phase angle, as well as their first derivatives are obtained as follows [31]:

$$\hat{a}(t_0) = 2|\hat{\xi}_c| \qquad \hat{\varphi}(t_0) = \angle\hat{\xi}_c \tag{29}$$

$$\dot{\hat{a}}(t_0) = \mathrm{Re}\{2\dot{\hat{\xi}}_c e^{-j\hat{\varphi}}\} \qquad \dot{\hat{\varphi}}(t_0) = \frac{\mathrm{Im}\{2\dot{\hat{\xi}} e^{-j\hat{\varphi}}\}}{\hat{a}} \tag{30}$$

where the derivative of the phase angle estimates the instantaneous frequency of the waveforms, being given by

$$\hat{f} = f_1 + \frac{\dot{\hat{\varphi}}}{2\pi} \tag{31}$$

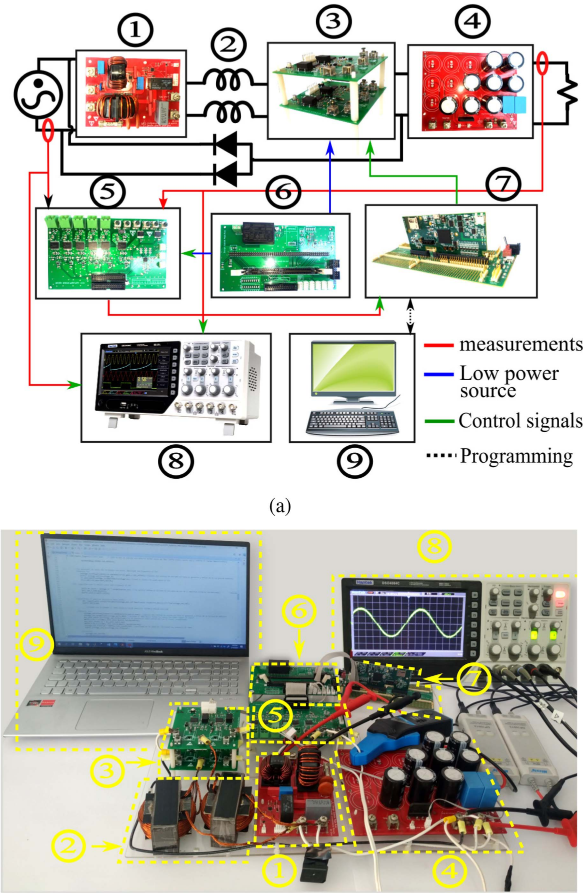
where f_1 stands for the fundamental frequency. It is worth noting that no preprocessing and postprocessing stages are needed when using the dynamic phasor model powered by the O-splines.

In the following section, the O-splines of the DTTFT are used to estimate dynamic phasors in power systems.

IV. EXPERIMENTAL RESULTS

This section encloses the experimental results of the proposed fixed frequency integral SMC with the O-splines estimator applied to the PFC rectifier. The report of the experimental results is split into the following subsections: Section IV-A presents the dynamic performance of the proposed control approach at steady-state and under significant load and output voltage changes. In Section IV-B, a comprehensive experimental comparison between the proposed framework and the most widely used methods recently reported in the scientific literature is conducted. The results under fault conditions are also presented in this section. Finally, in Section IV-C, an exhaustive comparison between the PLL and the proposed O-spline synchronization method is carried out under steady-state and transient conditions.

The power electronic converter and experimental parameters in Fig. 5 are summarized in Table III. The sliding mode controllers, PLL, and the O-spline-based estimator were implemented in a digital signal processor (TMS320F28379D) from the manufacturer Texas Instruments. Meanwhile, the control algorithms were generated using the Simulink Coder.



(a)

(b)

Fig. 5. Experimental setup 1) EMI filter, 2) boost inductors, 3) power stage, 4) capacitors bank, 5) measurement board, 6) low power supply, 7) DSP, 8) oscilloscope and 9) human–machine interface. (a) Diagram of connections. (b) Prototype of the experimental setup.

A. *SMC Performance With Adaptive Hysteresis Band and O-Splines Synchronization Method*

1) PF Correction and Adaptive Hysteresis Band Test: For this test, the experimental waveforms of i_{in} and v_{in} are illustrated in Fig. 6 when the system's operating power is about 1 kW. If the controller is working in closed-loop operation, the input current has a sinusoidal waveform with low harmonic distortion ($THD_i = 3.2\%$) and is in phase with the input voltage. The adaptive hysteresis band reduces the amplitude of the current ripple at the zero crossing, significantly mitigating the harmonic distortion. Likewise, the input of the system has a near unity power factor (PF $=$ 0.9987) under the operating conditions imposed by the SM controller.

2) Load Change Test: Figs. 7 and 8 show the results when a 50% load change occurs. With the proposed controller, the reference current changes its amplitude in the shortest possible time, showing the load change in a single switching cycle. The zoomed output voltage shows the 120 Hz ripple

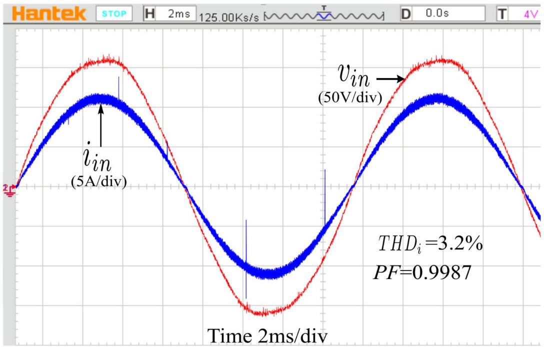


Fig. 6. Steady-state input side voltage and current.

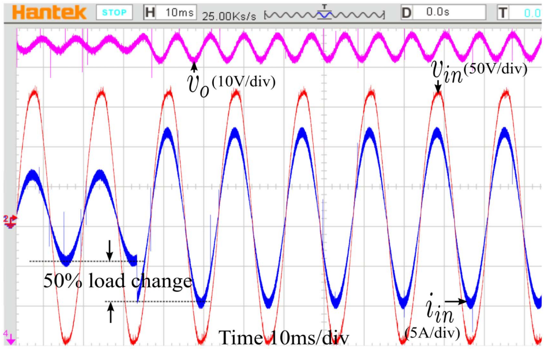


Fig. 7. Experimental results when the load is increased by 50%.

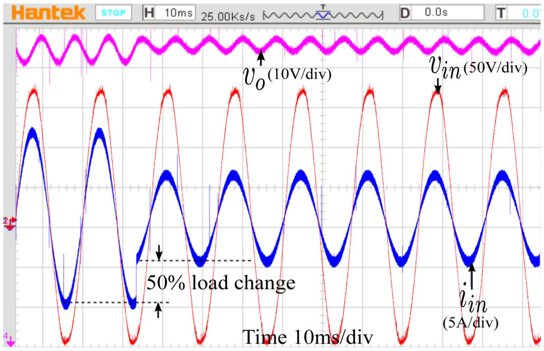


Fig. 8. Experimental results when the load is reduced by 50%.

caused by the rectifying action. The amplitude of this ripple changes in direct proportion to the load change; however, the output voltage does not exhibit overvoltages or undervoltages when the operational change takes place, avoiding load disturbances.

3) Output Voltage Set Point Change Test: Fig. 9 shows the response of the state variables when the set-point of the dc voltage is reduced from 400 to 375 V. Under these conditions, the dc voltage exhibits a stabilization time of 275 ms and the change is completed without any undervoltage around the stabilization point. In addition, the current amplitude is reduced to reflect the change of power over the load. In the whole test, the proposed controller keeps the ac current and voltage in phase, ensuring a PF close to 1.

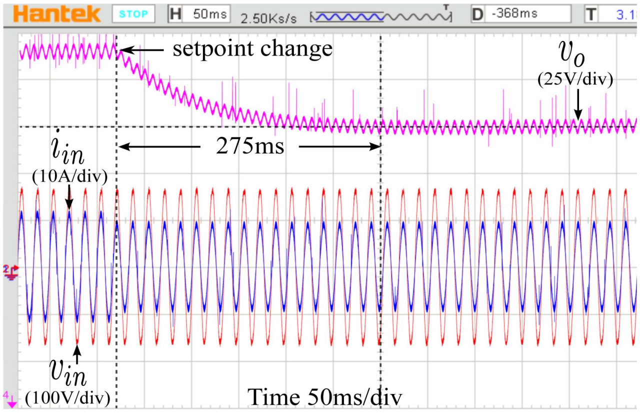


Fig. 9. Experimental results when the set point of the output voltage is reduced from 400 to 375 V.

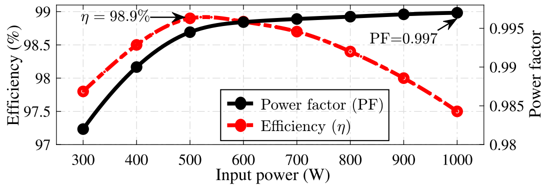


Fig. 10. PF and efficiency on the grid side of the converter with relation to output power levels.

4) PF and Efficiency Profile: Fig. 10 shows the PF and efficiency (η) of the converter at different operating points. The PF is as low as 0.53 when the control system is turned OFF, but this PF reaches values close to 1 when the controller is working. PF rises with increasing operating power because the current amplitude increases, while the maximum ripple amplitude remains constant due to the fixed switching frequency, limiting the harmonic distortion. The use of GaN switches with low turn-ON resistance and short switching time allows the prototype to reach an efficiency of 97.5% over the entire operating range, achieving a maximum efficiency of 98.9% at 500 W.

B. Experimental Comparisons Between the Proposed Approach and the State-of-the-Art Methods

1) Steady-State and Dynamic Performances: For comparison purposes, the steady-state and dynamic performances of the proposed control scheme with respect to several control methods reported in the recent scientific literature are summarized in Table IV. In this comparison, cascade control loops equipped with a linear PI controller or hybrid systems including PI control loops are the most widely used methods, accounting for 66.6% of the converters analyzed [32], [33], [34]. The application of the PI controller in combination with the following control schemes are reported: Harmonic elimination parallel control (HEPC) [35], dead-beat current controller (DBCC) [36], average current control (ACC) [37], and proportional resonant (PR) [38]. When PI controllers are applied, the reported settling time of v_o is from 80 ms up to 1.6 s, voltage overshoot is from 10 V up

TABLE IV
EXPERIMENTAL COMPARATIVE ANALYSIS OF STEADY-STATE AND DYNAMIC PERFORMANCE

Ref.	Controller type	Switching Frequency (kHz)	THD$_i$ (%)	EMI noise	Zero-crossing Deformation	Power (W)	Rise time (ms)	V_o settling time (ms)	Grid cycles to reach SS in i_{in}	overshoot (V)	undershoot (V)	SS error (%)
[33]	PI	20	4.5	Medium	High	300	–	80	3	55	–	–
[34]	DC	300	5	Low	High	1000	–	–	–	–	–	0
[36]	PI & HEPC	39.1-139.7	2.9	Low	High	120	–	–	–	–	–	–
[39]	PI & PR	20	3.7	High	Low	1000	40	180	8	40	50	–
[35]	PI	100	–	Medium	High	200	80	270	12	25	–	3
[40]	MFC	50	2.5	Medium	Medium	1000	–	57	2	12	12	–
[37]	DBCC & PI	50	2.7	Low	Low	500		150	9	10	10	–
[38]	PI & ACC	65	3.2	High	High & phase shift	850	–	1600	25	84	75	–
Proposed work	AHB & SMC & OSM	50	3.2	Low	Very low	1000	275	0	1	0	0	0

The bold entities highlight the column headings and the most significant results.

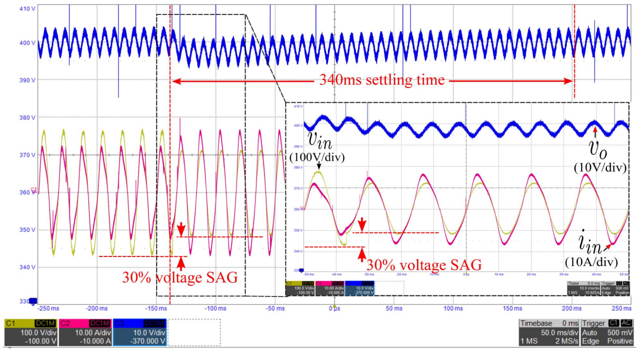


Fig. 11. Experimental results under a 30% of voltage sag when using linear cascade controller and PLL.

to 84 V, and operating powers from 120 W up to 1000 W were used. The application of the droop control strategy reports a high deformation of the input current at the zero crossing and harmonic distortion of 5%, significantly affecting the quality of the power absorbed from the utility grid. Model-free control (MFC) displays undershoots and overshoots of 12 V in v_o and a settling time of 57 ms. In comparison with previous works, the proposed method exhibits low zero-crossing current deformation and a THD_i of 3.2%. In addition, the absence of undershooting or overshooting in v_o allows settling time to be 0 s.

2) Performance Under 30% Sag Failure Conditions: The prototype response to a 30% sag faulty condition is exhibited in Fig. 11. The cascade controller with PI linear loops and the PLL-based synchronization method are used. The PI linear control system is tuned by the pole placement method for its operation around 1 kW and 120 V$_{\text{rms}}$ input voltage. When the fault takes place, the supply input power is reduced creating an unbalance of power between the ac and dc sides, which is exhibited by a decrease in v_o. The external control loop regulates the dc voltage by increasing the input current set point in the internal loop and driving v_o at the desired value, this response enables it to reach the dc voltage reference in 340 ms. Considering the current set point changes, the internal current control loop modifies the PWM modulation index to increase the current amplitude. Under these conditions, an undervoltage of 5 V is present in v_o. The latency caused by the external control loop results in a current distortion at the input until reaching a THD_i of 15.8%. Besides, the current i_{in} exhibits a significant distortion at zero crossing.

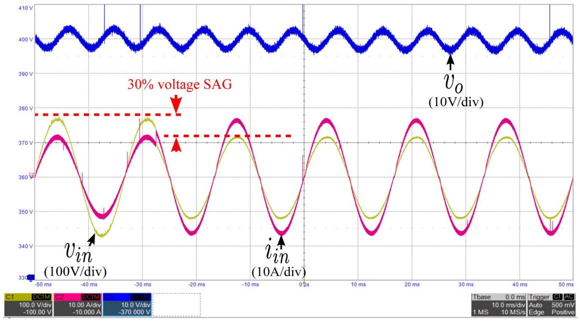


Fig. 12. Experimental results under a 30% of voltage sag when the SMC with the AHB and the O-splines method are implemented.

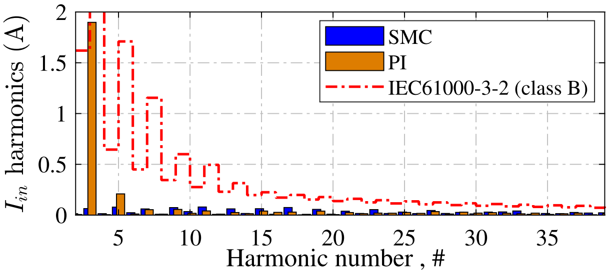


Fig. 13. Current harmonic components compared to IEC-61000-3-2 (class B) limits for the SMC and PI controllers, respectively.

When the sliding mode controller is working and the fault takes place, as shows in Fig. 12, the proposed sliding surface and the AHB drive the input current amplitude to the new reference value in a single switching cycle, maintaining the regulation of v_o without undervoltages. Under these operating conditions, the THD_i is 3.2%.

3) Harmonic Components: A harmonic content comparison of the prototype working at 1 kW with an input voltage of 120 V$_{\text{rms}}$ and controlled by the PI and SMC approaches is illustrated in Fig. 13. Notice that the magnitude of the current harmonic components (i_{in}) with both controllers does not exceed the harmonic current limits according to IEC 61000-3-2 standard [40]. The magnitude of harmonic components is significantly lower when the SMC is employed (blue columns in Fig. 13).

4) Computational Burden Comparison: By executing a Matlab-based real-time profiler of the generated code on a

TABLE V
COMPARISON OF EXECUTION TIME PROFILES FOR PLL AND O-SPLINE ESTIMATORS

	Algorithm	**Execution time (us)**	**Clock cycles**
PI & PLL	PLL	13.6	2719
	PWM	4.43	886
	sinωt	0.855	171
	PI cascade controllers	0.905	181
	Total	**19.785**	**3957**
AHB & SMC & OSM	O-splines	1.65	330
	Sliding surface	1.26	252
	AHB calculations	0.520	104
	I_{peak}	0.460	92
	Total	**3.89**	**778**

The bold entities highlight the column headings and the most significant results.

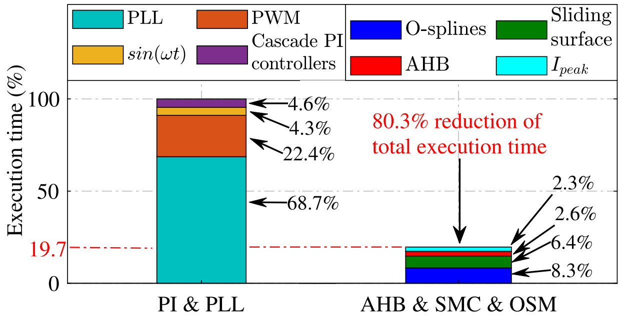


Fig. 14. Execution time comparison between the cascade PI controller with PLL (left bar) and AHB-SM controller with O-splines (right bar).

TABLE VI
POWER FACTOR AND TOTAL HARMONIC DISTORTION (*THD*) COMPARISON FOR UNIVERSAL INPUT RANGE WORKING AT 1 KW

	PI & PLL		**AHB & SMC & OSM**	
v_{in} ($\mathrm{V_{RMS}}$)	PF	THD_i (%)	PF	THD_i (%)
86	0.99	12.4	0.9986	2.65
120	0.982	15.80	0.9987	3.2
160	0.974	20.06	0.9977	4.1
185	0.6	117	0.997	6.7
230	0.56	138	0.9968	7.8
265	0.52	155	0.996	8.2

The bold entities highlight the column headings and the most significant results.

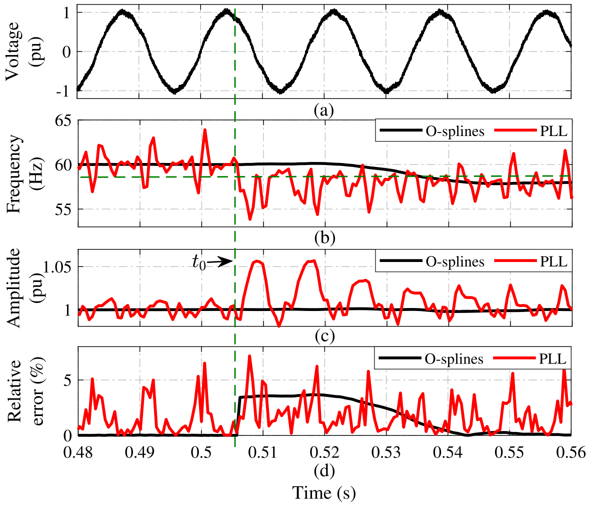


Fig. 15. O-spline and PLL-based responses to a frequency change in presence of harmonic distortion and noise.

TMS320F28379D processor for the linear cascade controller with PLL and the proposed SM controller with O-spline estimator, the attained results exhibit a significant reduction in computation time and clock cycles implied to complete the proposed approach and compared against the traditional linear control structure. Table V and Fig. 14 depict that the SMC with AHB and OSM requires 19.7% of the execution time needed to complete all PI and PLL tasks.

5) Performance Comparison Between at Universal Input Voltage Range: Within the universal input voltage range (85 $\mathrm{V_{RMS}}$–264 $\mathrm{V_{RMS}}$ at 50/60 Hz), the nominal voltage of the prototype is 120 $\mathrm{V_{RMS}}$ 60 Hz complying with the American voltage tolerance standard ANSI C84.1 [41]. According to this norm, the tolerance for range B utilization voltage is +5.8% to –13.3%. Given this voltage tolerance, our prototype was tested over the full universal input voltage range. Table VI depicts the comparison of PF and THD$_i$ at the input of the circuit driven by the AHB & SMC & OSM scheme and the traditional PI with PLL synchronization method in an input voltage range from 86 $\mathrm{V_{RMS}}$ until 265 $\mathrm{V_{RMS}}$. Results show that the proposed controller preserve the PF close to the unity and the harmonic distortion below the limits of the ANSI C84.1 standard, working at rated voltage. THD$_i$ rises to 8.2% when increasing v_{in} due to the higher ripple of i_{in}. When using the PI controller and the PLL, PF decreases and THD$_i$ rises significantly when v_{in} increases under the universal input voltage range.

When the PI controller is operating and v_{in} is increased, the amplitude of i_{in} is reduced to maintain the operating power at 1 kW. When v_{in} experiments large excursions within the universal voltage range, the performance of the PI linear controller is degraded, since it is tuned for single-point operation. Furthermore, under these conditions, the ripple and zero-crossing distortion become significant, increasing the magnitude of the high harmonic components. As a consequence, the THD$_i$ rises and the PF drops. Besides, the integral action increases the response time of the internal PI control loop that tracks i_{in}, since the controller is responding to the accumulated error over time. Hence, this latency in the response of the linear controller magnifies the sinusoidal current deformation at the input, also increasing THD$_i$. Under these circumstances, the PI controller is unable to preserve the sinusoidal waveform for input voltages greater than 160 $\mathrm{V_{RMS}}$, failing to achieve the primary purpose of this circuit, which is the automatic regulation of the PF, as shown in Table VI.

C. Comparison Between O-Spline and PLL-Based Synchronization Methods

1) Test Including Noise, Harmonic Distortion, and Sudden Frequency Change: In this test, the sensed voltage includes the electrical noise coupled to the cables and harmonic distortion with 1%, 2%, 1%, and 2% of amplitude for the 3rd, 5th, 7th, and 9th components, respectively. In addition, a frequency excursion from 60 to 58 Hz is programmed in the ac source to analyze the transient performance of the PLL and O-splines methods. Results are enclosed in Fig. 15(a)–(d). In steady-state, the O-splines algorithm rejects high-frequency noise and provides a stable estimation of the frequency and amplitude of v_{in}, smoothly

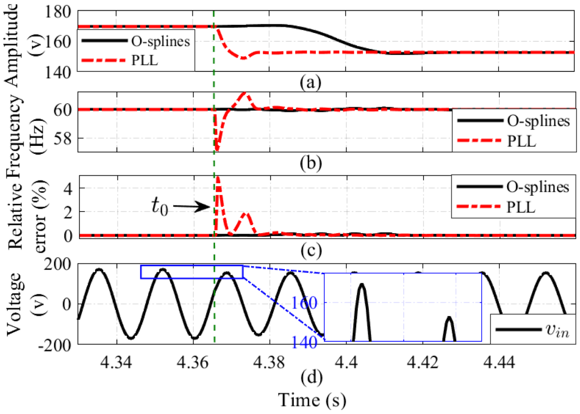


Fig. 16. O-spline and PLL-based responses to a 10% voltage sag.

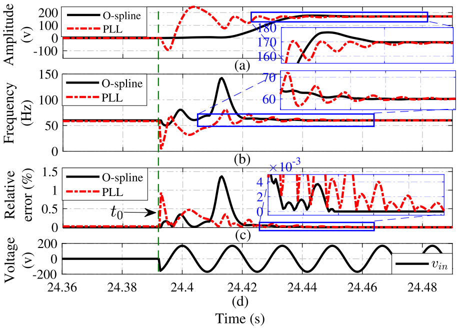


Fig. 17. O-spline and PLL-based responses to a starting condition.

tracking the reference values. In contrast, the PLL algorithm exhibits large deviations from v_{in} frequency between 57 and 63 Hz and excursions in the estimated amplitude between 0.97 and 1.06 p.u., as depicted in Fig. 15(b) and (c). When the step change in frequency takes place at t_0, the O-splines method requires two cycles of the network to estimate the frequency of v_{in}, showing an error in the transient time of less than 5%, without affecting the amplitude estimation, as depicted in Fig. 15(b)–(d). Frequency and amplitude estimations by PLL retain significant deviations from the reference values. It is noteworthy to remark that the O-splines approach outperforms the PLL algorithm thanks to the flat-top at the central frequency and the stop-bands at the harmonics in the frequency response in Fig. 4, likewise the first differentiator is not influenced by harmonics for the frequency estimation.

2) Test Under Voltage Condition: A 10% voltage sag is applied to the input voltage from 169 to 152 V, provoking an amplitude reference change, as depicted in Fig. 16(a). Notice that the PLL-based strategy in Fig. 16(b) experiments large frequency excursions below 58 Hz up to 61 Hz and exhibits fluctuations lasting more than 60 ms that represent estimation errors over 4.9%. In this test, it is noteworthy that the smallest amplitude and error (0.2%) stand for the O splines-based strategy which in turn achieves the steady state in a short time [Fig. 16(c) and (d)].

3) Test to Reference Signal Starting: The test begins with all reference signals OFFfor both estimation strategies, then these signals are switched ON at t_0. This turning-ON sequence indicates a zero voltage condition at the beginning that quickly needs to track the voltage amplitude from 0 V up to 170 V (Fig. 17). As expected, the O-spline produces a smooth estimation of amplitude without oscillations. In contrast, the PLL introduces large oscillations, as is shown in Fig. 17(a). Meanwhile, the O-spline in Fig. 17(b) attains the frequency estimation via its first differentiator in less than two cycles and with fewer oscillations than that the PLL exhibits. Despite the frequency excursion in the O-spline strategy, errors in steady-state still are less than that of the PLL one (Fig. 17).

V. CONCLUSION

This article introduces a novel synchronization method based on the O-splines of the discrete-time Taylor-Fourier transform to effectively estimate the frequency, amplitude, and phase of the input voltage used to generate the grid-side current reference for rectifiers with automatic power factor correction. Experimental tests were conducted on a prototype of a semibridgeless boost rectifier circuit controlled by an integral SMC. This investigation demonstrates the effectiveness of the O-splines for network synchronization purposes thanks to their versatility in smoothly tracking the changes of the input voltage waveforms polluted with harmonic content. The proposed approach also includes an adaptive hysteresis band which enables fixing the switching frequency and significantly reduce the input current distortion at zero crossing, in comparison with the conventional hysteresis modulation-based SMCs. Tests performed on a 1 kW GaN-based prototype illustrate that the proposed control scheme regulates the voltage on the load, and it corrects the power factor at the input side, retaining its efficiency higher than 97% over the full operating range.

The feasibility of our proposal was also verified under static and dynamic conditions, showing that the proposed controller achieves a power factor of 0.997 and an input current with a *THD* of 3.2%. Thus, all performed tests to load changes (variation up to 50%) illustrate that the sliding mode controller has the shortest possible response time, timely updating the input current's amplitude in a single switching cycle. Meanwhile, all tests related to the set point's changes at the output voltage exhibit that the closed-loop system reaches the steady-state condition in 275 ms, without undervoltages. The results unveil the robustness and high dynamic performance achieved with the proposed integral sliding surface to the presence of sudden changes in operating conditions.

Comprehensive comparisons among the real-time execution profiles and the dynamic performance of the proposed control framework with O spline-based estimator and the conventional PI-based controller with PLL were conducted resulting in that the proposed controller and synchronization method reduces the execution time by 80.3%. In addition, all performed tests to the presence of changes in amplitude, frequency deviations and harmonic distortion at the input voltage showed that the O-splines method estimates the signal parameters with smaller oscillations than those presented with the PLL method. This dynamic behavior benefits the stability of the controller to the presence of unexpected changes at the point of coupling with the network.

REFERENCES

[1] P. Lamo, F. López, A. Pigazo, and F. J. Azcondo, "An efficient FPGA implementation of a quadrature signal-generation subsystem in SRF PLLs in single-phase PFCs," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3959–3969, May 2017.

[2] R. Haroun, A. Cid-Pastor, A. E. Aroudi, and L. Martínez-Salamero, "Synthesis of canonical elements for power processing in DC distribution systems using cascaded converters and sliding-mode control," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1366–1381, Mar. 2014.

[3] A. Marcos-Pastor, E. Vidal-Idiarte, A. Cid-Pastor, and L. Martinez-Salamero, "Interleaved digital power factor correction based on the sliding-mode approach," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4641–4653, Jun. 2016.

[4] P. R. Mohanty and A. K. Panda, "Fixed-frequency sliding-mode control scheme based on current control manifold for improved dynamic performance of boost PFC converter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 576–586, Mar. 2017.

[5] M. Alam, W. Eberle, D. S. Gautam, and C. Botting, "A soft-switching bridgeless AC–DC power factor correction converter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7716–7726, Oct. 2017.

[6] *Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*, IEEE Std 519-2014, 2014, pp. 1–29.

[7] *IEEE Recommended Practice-Adoption of IEC 61000-4-15:2010, Electromagnetic Compatibility (EMC)-Testing and Measurement Techniques*, IEEE Std 1453-2011, 2011, pp. 1–58.

[8] Z. Chen, B. Liu, Y. Yang, and H. Wang, "Bridgeless PFC topology simplification and design for performance benchmarking," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5398–5414, May 2021.

[9] X. Ren, Y. Zhou, Z. Guo, Y. Wu, Z. Zhang, and Q. Chen, "Analysis and improvement of capacitance effects in 360–800 Hz variable on-time controlled CRM boost PFC converters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7480–7491, Jul. 2020.

[10] K. Yao, Z. Zhang, J. Yang, J. Liu, J. Li, and F. Shao, "Quasi-fixed switching frequency control of CRM boost PFC converter based on variable inductor in wide input voltage range," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1814–1827, Feb. 2021.

[11] K. K. Siu, Y. He, C. N. M. Ho, H. S. Chung, and R. T. Li, "Advanced digital controller for improving input current quality of integrated active virtual ground-bridgeless PFC," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3921–3936, Apr. 2019.

[12] H. Sira-Ramirez, "Sliding motions in bilinear switched networks," *IEEE Trans. Circuits Syst.*, vol. 34, no. 8, pp. 919–933, Aug. 1987.

[13] V. I. Utkin, "Sliding mode control design principles and applications to electric drives," *IEEE Trans. Ind. Electron.*, vol. 40, no. 1, pp. 23–36, Feb. 1993.

[14] S. Tan, Y. M. Lai, and C. K. Tse, "General design issues of sliding-mode controllers in DC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1160–1174, Mar. 2008.

[15] J. Ye, P. Malysz, and A. Emadi, "A fixed-switching-frequency integral sliding mode current controller for switched reluctance motor drives," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 2, pp. 381–394, Jun. 2015.

[16] V. Repecho, D. Biel, J. M. Olm, and E. F. Colet, "Switching frequency regulation in sliding mode control by a hysteresis band controller," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1557–1569, Feb. 2017.

[17] S. H. Chincholkar and C. Chan, "Design of fixed-frequency pulsewidth-modulation-based sliding-mode controllers for the quadratic boost converter," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 64, no. 1, pp. 51–55, Jan. 2017.

[18] A. Dixit, K. Pande, and S. Gangavarapu, "DCM-based bridgeless PFC converter for EV charging application," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 1, no. 1, pp. 57–66, Jul. 2020.

[19] A. Mallik, J. Lu, and A. Khaligh, "Sliding mode control of single-phase interleaved totem-pole PFC for electric vehicle onboard chargers," *IEEE Trans. Veh. Technol.*, vol. 67, no. 9, pp. 8100–8109, Sep. 2018.

[20] V. Repecho, D. Biel, and P. G. Vega, "Fixed-switching frequency interleaved sliding mode eight-phase synchronous buck converter," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 676–688, Jan. 2018.

[21] V. Repecho, D. Biel, and J. M. Olm, "A simple switching-frequency-regulated sliding-mode controller for a VSI with a full digital implementation," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 569–579, Feb. 2021.

[22] M. Pichan and H. Rastegar, "Sliding-mode control of four-leg inverter with fixed switching frequency for uninterruptible power supply applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6805–6814, Aug. 2017.

[23] P. Lamo, F. López, A. Pigazo, and F. J. Azcondo, "Stability and performance assessment of single-phase t /4 PLLs with secondary control path in current sensorless bridgeless PFCs," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 674–685, Jun. 2018.

[24] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Single-phase PLLs: A review of recent advances," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9013–9030, Dec. 2017.

[25] S. Lu, C. Ding, L. Liu, Y. Mei, K. D. T. Ngo, and G. Q. Lu, "Heteromagnetic swinging inductor and its application for power factor correction converters," *IEEE Trans. Ind. Appl.*, vol. 56, no. 5, pp. 5292–5298, Sep./Oct. 2020.

[26] C. Ku, D. Chen, C. Huang, and C. Liu, "A novel SFVM-M control scheme for interleaved CCM/DCM boundary-mode boost converter in PFC applications," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2295–2303, Aug. 2011.

[27] A. Leon-Masich, H. Valderrama-Blavi, J. M. Bosque-Moncusí, and L. Martínez-Salamero, "A high-voltage sic-based boost PFC for LED applications," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1633–1642, Feb. 2016.

[28] J. R. Ortiz-Castrillón, G. E. Mejía-Ruíz, N. Muñoz-Galeano, J. M. López-Lezama, and S. D. Saldarriaga-Zuluaga, "PFC single-phase ac/dc boost converters: Bridge, semi-bridgeless, and bridgeless topologies," *Appl. Sci.*, vol. 11, no. 16, 2021, Art. no. 7651. [Online]. Available: https://www.mdpi.com/2076-3417/11/16/7651

[29] E. E. Henao-Bravo, C. A. Ramos-Paja, and A. J. Saavedra-Montes, "Adaptive control of photovoltaic systems based on dual active bridge converters," *Computation*, vol. 10, no. 6, pp. 1–24, 2022. [Online]. Available: https://www.mdpi.com/2079-3197/10/6/89

[30] J. A. de la O Serna, "Dynamic harmonic analysis with FIR filters designed with O-splines," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 5092–5100, Dec. 2020.

[31] J. A. de la O Serna, "Dynamic phasor estimates for power system oscillations," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 5, pp. 1648–1657, Oct. 2007.

[32] Y. Cui, H. Han, Y. Liu, G. Xu, M. Su, and S. Xie, "An efficiency-improved single-phase PFC rectifier with active power decoupling," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10784–10796, Sep. 2022.

[33] D. Shahzad, M. Farooq, S. Pervaiz, and K. K. Afridi, "A high-power-density high-efficiency soft-switched single-phase universal input to 28-V isolated AC–DC converter module designed for paralleled operation," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8262–8280, Jul. 2022.

[34] S. K. Rastogi, M. S. Rana, and S. K. Mishra, "A single-input multiple-output unity power factor rectifier," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10127–10141, Sep. 2021.

[35] K. Yao, J. Li, F. Shao, and B. Zhang, "Parallel fixed switching frequency CRM and DCM boost PFC converter with high power factor," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 3247–3258, Mar. 2022.

[36] M. Pourmahdi, H. Heydari-doostabad, R. Ghazi, and T. O'Donnell, "Buck–boost common ground bridgeless PFC (CGBPFC) rectifies with positive/negative output," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1272–1282, Feb. 2022.

[37] Z. Chen, J. Xu, P. Davari, and H. Wang, "A mixed conduction mode-controlled bridgeless boost PFC converter and its mission profile-based reliability analysis," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9674–9686, Aug. 2022.

[38] H. Ma, K. Zheng, H. Jiang, and H. Yin, "A family of dual-boost bridgeless five-level rectifiers with common-core inductors," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12565–12578, Nov. 2021.

[39] H. Zhang, H. Li, J. Mao, C. Pan, and Z. Luan, "Model-free control of single-phase boost AC/DC converters," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 11828–11838, Oct. 2022.

[40] Limits for Harmonics Current Emissions (Equipment Current $\leq$ 16APer Phase), International Standard IEC 61000-3-2, 2018.

[41] American National Standard for Electric Power Systems and Equipment—Voltage Ratings for Electric Power Systems and Equipment, ANSI Standard C84.1-2020, 2020.