Investigation and Comparison of Temperature-Sensitive Electrical Parameters of SiC MOSFET at Extremely High Temperatures

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***Abstract*—Due to the excellent silicon carbide (SiC) material characteristics, SiC MOSFETs can operate at extremely high temperatures and can be used in harsh environment applications. In this case, it is crucial to ensure the reliability of the power electronic systems. The temperature-sensitive electrical parameters (TSEPs) have been used for online junction temperature monitoring to monitor the health condition of the SiC MOSFET at low temperatures (<175 °C). However, the performance of the TSEPs at extremely high temperatures is still unknown, and the influence of temperature on the TSEPs of SiC MOSFETs at extremely high temperatures is unclear. In this article, the theoretical mechanisms of the impact of the extremely high temperature on TSEPs are investigated in detail. In particular, the different effects of high temperature on the turn-ON delay time and turn-OFF delay time are discussed carefully. Based on the proposed high-temperature characteristic test method, the TSEPs of SiC MOSFET (including static and dynamic characteristics) are tested and analyzed comprehensively from room temperature to 375 °C. And the sensitivity and linearity of the TSEPs in different temperature ranges are analyzed and compared. According to the results, threshold voltage and turn-OFF delay time are the two TSEPs with good sensitivity and linearity over a wide temperature range (from room temperature to 375 °C). And the linearity of the turn-OFF delay time is the best among all TSEPs over a wide temperature range.**

***Index Terms*—Extremely high temperatures, linearity, online junction temperature monitoring, sensitivity, SiC MOSFET, temperature-sensitive electrical parameters (TSEPs).**

I. Introduction

SILICON carbide (SiC) power semiconductors can safely operate at extremely high temperatures because the bandgap of the SiC material is three times that of silicon (Si) [1], [2]. Therefore, the SiC MOSFET can be used in harsh environments, such as the down-hole oil and gas industry [3], aerospace electronic systems, and automotive and on-engine electronics [4]. In these applications, the operating temperature of the SiC MOSFET can be well above 175 °C. And the safety requirements of the power electronic systems are more stringent. In this case, ensuring the reliability of the power electronic systems operating in harsh environments is crucial.

It is shown that 31% of power electronic system breakdowns are caused by power semiconductor failures, and nearly 60% of the power semiconductor failures are thermally induced [5]. Overheating and temperature fluctuation are two main failure factors of power semiconductors, leading to transient failures (such as thermal breakdown, bond wire crack, and solder melting) and aging failures (such as bond wire fatigue and solder degradation) [6]. Based on junction temperature, the aging levels of devices can be evaluated, and the life prediction can be carried out. Additionally, the failure rate of the power semiconductor doubles for every 10 °C increase in junction temperature [7]. Therefore, online junction temperature monitoring is essential for lifetime estimation, thermal management, and the reliable operation of power electronic systems at extremely high temperatures.

There are four kinds of junction temperature measurement methods: sensor-based physical contact method, optical method, model-based thermal network method, and temperature-sensitive electrical parameter (TSEP) method [8]. Among these methods, the optical methods have limitations to implement physically in applications, and the physical contacting methods have a slow response in the measurement [9]. The model-based thermal network method is one of the indirect measurement methods to predict junction temperature, whose accuracy mainly depends on the accuracy of the thermal model. However, the more accurate the thermal model is, the more complex it will be, which brings a complicated calculation and solution process and a longer response time [8]. In addition, the thermal model may change as the device ages, and the material medium exhibits cavitation, oxidation, or other damage, leading to a deviation in the junction temperature estimation results. By contrast, the TSEP method has attracted considerable attention because it is easier to integrate, more responsive, and more accurate.

Numerous TSEPs have been used for online junction temperature monitoring of SiC MOSFETs at low temperatures, including on-resistance [10], threshold voltage [9], turn-ON dI_{DS}/dt [11],

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turn-ON delay time [12], and turn-OFF delay time [13]. In [10], the V_{on} is measured at different temperatures and current conditions ranging from 25 °C to 145 °C. And the results show the feasibility of online temperature monitoring. In [9], a measurement circuit for quasi-threshold voltage is proposed. The test results show that the quasi-threshold voltage has a sensitivity of −4.37 mV/°C from 36 °C to 118 °C. In [11], the $d\beta/dT$ is considered to be negligible, so the dI_{DS}/dt increases linearly with temperature ranging from 25 °C to 150 °C due to dV_{th}/dT and can be used for online junction temperature monitoring. In [12], the variation of turn-ON delay time at different temperatures is considered to be caused by the threshold voltage. Therefore, the linearity and sensitivity of the turn-ON delay time with temperatures are good from 25 °C to 150 °C. In [13], it is pointed out that the turn-OFF delay time is temperature dependent because of the miller voltage. And the linearity of the relationship between turn-OFF delay time and temperature is also good from 25 °C to 150 °C. As can be seen, various TSEPs of SiC MOSFET have been studied and proved to have good linearity and sensitivity at low temperatures.

As temperature rises, it is still unknown whether the TSEPs at extremely high temperatures can maintain good linearity and sensitivity at low temperatures and whether the analysis of the TSEPs in previous studies can accurately reflect the performance of the TSEPs at extremely high temperatures. However, since high operating temperature is one of the most significant advantages of the SiC MOSFET, working at extremely high temperatures must be an essential direction for the application of the SiC MOSFET in the future. In this case, online junction temperature monitoring at extremely high temperatures is crucial for overtemperature protection and condition monitoring. Therefore, it is necessary to investigate the performance of TSEPs at extremely high temperatures and analyze it from theoretical perspective.

The rest of this article is organized as follows. The influence of temperature on TSEPs is analyzed in detail in Section II, especially at extremely high temperatures. In Section III, the specific test method used in this article, which can accurately measure the characteristics of the SiC MOSFET at extremely high temperatures, is introduced in detail. Based on the test method presented in Section III, the TSEPs are tested from room temperature to 375 °C, and the results are presented in Section IV. Then, the sensitivity and linearity of the TSEPs in different temperature ranges are analyzed and compared in Section V. Finally, Section VI concludes this article.

II. Influence of Temperature on TSEPs

A. Threshold Voltage

The threshold voltage (V_{th}) of the SiC MOSFET can be expressed as follows [14], [15]:

$$V_{th} = V_{FB} + 2\Psi_B + \frac{1}{C_{OX}}\left(\sqrt{2\varepsilon_S q N_A (2\Psi_B)} + q\int_{E_i}^{E_i+\Psi_B} D_{it}(E)\,dE\right) \quad (1)$$

where ε_S is the dielectric constant of the semiconductor, q is the electronic charge, N_A is the doping concentration of the P-base region, V_{FB} is the flat-band voltage (which includes the effect of the fixed charges), Ψ_B is the bulk potential, and D_{it} is the interface state density. The Ψ_B decreases almost linearly with increasing temperature [16]. If the D_{it} is neglected, the ideal value of V_{th} will decrease with the temperature almost linearly [15], [17]. Due to the negatively charged interface states, there is a positive shift in V_{th}. And the D_{it} is also temperature dependent, which decreases as temperature (T) rises. As a result, the V_{th} decreases with the temperature with a decreasing $|dV_{th}/dT|$ at cryogenic temperatures [18]. But the positive shift caused by D_{it} will no longer be significant at extremely high temperatures. Therefore, the change in $|dV_{th}/dT|$ is small at extremely high temperatures.

B. On-resistance

For medium-voltage MOSFETs, the channel resistance (R_{CH}), junction field effect transistor (JFET) region resistance (R_{JFET}), and drift region resistance (R_D) are the main parts of the on-resistance ($R_{DS(on)}$). The specific on-resistance contributed by the channel can be expressed as follows [19]:

$$R_{CH\_SP} = \frac{L_{CH} W_{Cell}}{2\mu_{ni}(T)\, C_{OX}\,(V_{GS} - V_{th}(T))} \quad (2)$$

where μ_{ni} is the inversion layer mobility, C_{OX} is the specific capacitance of the oxide, L_{CH} is the channel length, W_{Cell} is the cell width, T is the junction temperature, and V_{GS} is the gate–source voltage. In (2), the μ_{ni} and V_{th} are temperature-dependent parameters. When the V_{GS} is 15 V, the μ_{ni} increases from room temperature to 50 °C and decreases slowly with temperatures beyond 50 °C [20]. It can be considered that the change in μ_{ni} is negligible at low temperatures. Therefore, the R_{CH_SP} decreases with temperature due to the decrease in V_{th} at low temperatures. At extremely high temperatures, the decrease in R_{CH_SP} with temperature will be smaller due to the reduction of the μ_{ni}. When T is fixed, the R_{CH_SP} will increase with the decrease in V_{GS}. The specific on-resistance contributed by the JFET region can be expressed as follows [19]:

$$R_{JFET\_SP} = \frac{\rho_{JFET} x_{JP} W_{Cell}}{a} = \frac{x_{JP} W_{Cell}}{q\mu_{nj}(T)\, N_{DJ} a} \quad (3)$$

where ρ_{JFET} is the resistivity of the JFET region, x_{JP} is the P-base junction depth, a is the width of the current flow, μ_{nj} is the bulk mobility of the JFET region, and N_{DJ} is the doping concentration of the JFET region. The R_{JFET_SP} is only related to the ρ_{JFET} and the geometry of the JFET region. The μ_{nj} is the only temperature-dependent parameter in (3). Since the μ_{nj} decreases with the increase in T [14], the R_{JFET_SP} increases with T and is independent of the V_{GS}. The relationship between R_{D_SP} and T is the same as the R_{JFET_SP}. The R_{D_SP} is also related to the ρ_D and geometry of the drift region. Due to the decrease in μ_{nd}, R_{D_SP} also increases as T rises.

As a result, at low temperatures, the R_{CH} dominates the $R_{DS(on)}$ decrease with the temperature. At extremely high temperatures, the R_{CH} and the change in the R_{CH} with temperature are relatively small. Therefore, the R_{JFET}+R_D dominates the

$R_{DS(on)}$ increase with temperature at extremely high temperatures. The variation of $R_{DS(on)}$ with the temperature at low temperatures may be nonmonotonic. In addition to temperature and current mentioned in [10], the $R_{DS(on)}$ is also severely affected by V_{GS} at low temperatures. At extremely high temperatures, because the $R_{JFET}+R_D$ is independent of V_{GS}, the $R_{DS(on)}$ increases monotonically with temperature, and the difference in $R_{DS(on)}$ at different V_{GS} will be slight.

C. V_{GS} at Constant I_{DS_sat}

When the SiC MOSFET works in the saturation region, the drain–source voltage (V_{DS}) will be borne mainly by the channel. If it is assumed that the channel voltage is equal to the V_{DS}, the saturated drain–source current (I_{DS_sat}) per unit area can be written as follows [19]:

$$J_{DS\_sat} = \frac{\mu_{ni}(T) C_{OX}}{W_{Cell} L_{CH}} (V_{GS} - V_{th}(T))^2. \tag{4}$$

The μ_{ni} and V_{th} are temperature-dependent parameters in (4). If the influence of μ_{ni} is not considered, the transfer characteristic curve should conform to the square law. Different from (2), in which the SiC MOSFET works in the ohmic region and the V_{GS} is constant, the SiC MOSFET works in the saturation region, and the V_{GS} is variable in (4). Since the μ_{ni} is related to temperature and V_{GS}, the average channel mobility (μ_{ni_av}) at different V_{GS} is used to analyze the temperature-dependent transfer characteristic for simplicity. Since the μ_{ni_av} first increases and then decreases with the increasing temperature, the change in μ_{ni_av} is relatively small at low temperatures [17]. If it is assumed that V_{th} decreases linearly with temperature, the curve of the transfer characteristic will shift to the left with the same distance at the same temperature step, and the V_{id} (the value of V_{GS} at fixed I_{DS_sat}) will decrease with the temperature almost linearly at low temperatures. At extremely high temperatures, the decrease in μ_{ni_av} will cause the J_{DS_sat} to decrease with T, which means that the curve of the transfer characteristic will shift to the left with decreasing distance at the same temperature step. As a result, the V_{id} decreases with the temperature at a decreasing $|dV_{id}/dT|$ at extremely high temperatures.

D. Turn-ON and Turn-OFF Delay Times

The precise starting points of the V_{GS} and I_{DS} rise are difficult to obtain by testing. Therefore, the turn-ON delay time (t_{d_on}) is defined as the time interval from 10% of V_{GS} to 10% of I_{DS}. The turn-OFF delay time (t_{d_off}) is defined as the time interval from 90% of V_{GS} to 10% of V_{DS}.

During the turn-ON process, the t_{d_on} can be divided into two parts. The first part (t_{d_on1}) is the period during which the V_{GS} increases from 10% of V_{GS} (V_{ton}) to V_{th}. The V_{GS} can be expressed as follows:

$$V_{GS}(t) = V_{cc} - (V_{cc} - V_{ee}) e^{-\frac{t}{R_G(C_{GS}+C_{GD\_HV})}} \tag{5}$$

where V_{cc} is the high level of the V_{GS}, V_{ee} is the low level of the V_{GS}, R_G is the gate resistance, C_{GS} is the gate–source capacitance, and C_{GD_HV} is the gate–drain capacitance at high V_{DS} (which can be approximated as the dc voltage during t_{d_on}).

The t_{d_on1} can be calculated as follows:

$$t_{d\_on1} = R_G (C_{GS} + C_{GD\_HV}) \ln\left(\frac{V_{cc} - V_{ton}}{V_{cc} - V_{th}}\right). \tag{6}$$

At the end of this part, the V_{GS} exceeds V_{th}. Therefore, the SiC MOSFET enters the saturation region, and the I_{DS} starts to rise from 0. The second part (t_{d_on2}) is the period during which the I_{DS} increases from 0 to 10% of the load current. In this period, the SiC MOSFET works in the saturation region. According to (4), the I_{DS} can be expressed as follows:

$$I_{DS} = J_{DS\_sat} S = \frac{\mu_{ni}(T) C_{OX} S}{W_{Cell} L_{CH}} (V_{GS}(t) - V_{th}(T))^2 \tag{7}$$

where S is the area of the die. If it is assumed that V_{id_on} is the value of V_{GS} at 10% of the rising I_{DS}, then t_{d_on2} is also the period during which the V_{GS} increases from V_{th} to V_{id_on}. During the current rise, there will be a voltage drop in V_{DS} caused by the parasitic inductance. But the V_{DS} is still high enough that the voltage drop has little effect on the gate–drain capacitance (C_{GD}). Therefore, (5) still holds, and the t_{d_on2} can also be expressed as follows:

$$t_{d\_on2} = R_G (C_{GS} + C_{GD\_HV}) \ln\left(\frac{V_{cc} - V_{th}}{V_{cc} - V_{id\_on}}\right). \tag{8}$$

Therefore, t_{d_on} can be expressed as follows:

$$t_{d\_on} = t_{d\_on1} + t_{d\_on2} = R_G (C_{GS} + C_{GD\_HV}) \ln\left(\frac{V_{cc} - V_{ton}}{V_{cc} - V_{id\_on}}\right). \tag{9}$$

Different from the analysis presented in [12], it can be found that the t_{d_on} at different temperatures depends mainly on the V_{id_on}, not on the V_{th}.

During the turn-OFF process, the t_{d_off} can also be divided into two parts. The first part (t_{d_off1}) is the period during which the V_{GS} decreases from 90% of the falling V_{GS} (V_{nof}) to the Miller voltage (V_{miller}). The V_{GS} can be expressed as follows:

$$V_{GS}(t) = V_{ee} + (V_{cc} - V_{ee}) e^{-\frac{t}{R_G(C_{GS}+C_{GD\_LV})}} \tag{10}$$

where C_{GD_LV} is the gate–drain capacitance at low V_{DS} (which is close to 0). The t_{d_off1} can be expressed as follows:

$$t_{d\_off1} = R_G (C_{GS} + C_{GD\_LV}) \ln\left(\frac{V_{nof} - V_{ee}}{V_{miller} - V_{ee}}\right). \tag{11}$$

At the end of this part, the V_{DS} reaches $V_{miller}-V_{th}$. The second part (t_{d_off2}) is the period during which the V_{DS} increases from $V_{miller}-V_{th}$ to 10% of the rising V_{DS}. In the ideal case, the I_{DS} remains constant at I_L, and the V_{GS} remains constant at V_{miller}. The slope of the increasing V_{DS} with time (dV_{DS}/dt) can be expressed as follows:

$$\frac{dV_{DS}}{dt} = \frac{dV_{DG}}{dt} = -\frac{I_{miller}}{C_{GD}(V_{DS})} = -\frac{V_{ee} - V_{miller}}{R_G C_{GD}(V_{DS})} \tag{12}$$

where I_{miller} is the gate current in this period. Since the V_{DS} is low, the change in the C_{GD} with V_{DS} is very large. Therefore, dV_{DS}/dt is mainly affected by $C_{GD}(V_{DS})$. As temperature rises, dV_{DS}/dt decreases due to the decreasing V_{miller}. But the change in dV_{DS}/dt with temperature is small. In this case, the t_{d_off2} at different temperatures can be expressed by a constant value of C.

Since the V_{miller} is the value of V_{GS} at the load current ($V_{\text{id\_off}}$), the $t_{\text{d\_off}}$ can be expressed as follows:

$$t_{\text{d\_off}} = t_{\text{d\_off1}} + t_{\text{d\_off2}} = R_{\text{G}}\left(C_{\text{GS}} + C_{\text{GD\_LV}}\right)\ln\left(\frac{V_{\text{nof}} - V_{\text{ee}}}{V_{\text{id\_off}} - V_{\text{ee}}}\right) + C. \tag{13}$$

According to (9), the slope of the $t_{\text{d\_on}}$ changing with temperature can be expressed as follows:

$$\frac{dt_{\text{d\_on}}}{dT} = R_{\text{G}}\left(C_{\text{GS}} + C_{\text{GD\_HV}}\right)\frac{1}{V_{\text{cc}} - V_{\text{id\_on}}}\frac{dV_{\text{id\_on}}}{dT}. \tag{14}$$

Since $V_{\text{id\_on}}$ decreases with temperature, if it is assumed that $dV_{\text{id\_on}}/dT$ is constant, $dt_{\text{d\_on}}/dT < 0$ and $|dt_{\text{d\_on}}/dT|$ decrease with the increasing temperature. Therefore, although the change in $dV_{\text{id\_on}}/dT$ is small at low temperatures, the $t_{\text{d\_on}}$ decreases with the temperature at a decreasing $|dt_{\text{d\_on}}/dT|$ at low temperatures. It is just that the nonlinearity of the relationship between $t_{\text{d\_on}}$ and T is not significant at low temperatures.

According to (13), the slope of the $t_{\text{d\_off}}$ changing with temperature can be expressed as follows:

$$\frac{dt_{\text{d\_off}}}{dT} = -R_{\text{G}}\left(C_{\text{GS}} + C_{\text{GD\_LV}}\right)\frac{1}{V_{\text{id\_off}} - V_{\text{ee}}}\frac{dV_{\text{id\_off}}}{dT}. \tag{15}$$

Since the $V_{\text{id\_off}}$ decreases with temperature, if it is assumed that the $dV_{\text{id\_off}}/dT$ is constant, the $dt_{\text{d\_off}}/dT > 0$ and the $|dt_{\text{d\_off}}/dT|$ increases with the increasing temperature. Similarly, the $t_{\text{d\_off}}$ increases with temperature, with an increasing $|dt_{\text{d\_off}}/dT|$ at low temperatures.

Besides, the $t_{\text{d\_on}}$, $t_{\text{d\_off}}$, $|dt_{\text{d\_on}}/dT|$, and $|dt_{\text{d\_off}}/dT|$ are proportional to $R_{\text{G}}(C_{\text{GS}}+C_{\text{GD}})$. Therefore, the larger R_{G}, the larger $t_{\text{d\_on}}$, $t_{\text{d\_off}}$, $|dt_{\text{d\_on}}/dT|$, and $|dt_{\text{d\_off}}/dT|$. Since the $C_{\text{GD\_LV}}$ is much larger than the $C_{\text{GD\_HV}}$, the $t_{\text{d\_off}}$ is larger than the $t_{\text{d\_on}}$, and the $|dt_{\text{d\_off}}/dT|$ is larger than $|dt_{\text{d\_on}}/dT|$. Comparing (9) and (14), the $t_{\text{d\_on}}$ is related to the V_{ton}, but the $|dt_{\text{d\_on}}/dT|$ is not related to the V_{ton}. Similarly, the $t_{\text{d\_off}}$ is related to the V_{nof}, but the $|dt_{\text{d\_off}}/dT|$ is not related to the V_{nof}. In other words, the starting point of $t_{\text{d\_on}}$ ($t_{\text{d\_off}}$) only affects its value but does not affect its slope with temperature.

For easy comprehension, the curve of $t_{\text{d\_on}}/R_{\text{G}}/(C_{\text{GS}}+C_{\text{GD\_HV}})$ versus $V_{\text{id\_on}}$ and the curve of $(t_{\text{d\_off}}-C)/R_{\text{G}}/(C_{\text{GS}}+C_{\text{GD\_LV}})$ versus $V_{\text{id\_off}}$ are shown in Fig. 1. Since the V_{id} decreases with temperature, the axis of the T is in the opposite direction to the axis of V_{id}. If $dV_{\text{id\_on}}/dT$ ($dV_{\text{id\_off}}/dT$) is constant, the $V_{\text{id\_on}}$ ($V_{\text{id\_off}}$) is proportional to T. The $t_{\text{d\_on}}/R_{\text{G}}/(C_{\text{GS}}+C_{\text{GD\_HV}})$ is proportional to the $t_{\text{d\_on}}$, and $(t_{\text{d\_off}}-C)/R_{\text{G}}/(C_{\text{GS}}+C_{\text{GD\_LV}})$ is proportional to the $t_{\text{d\_off}}$, so the black curves in Fig. 1 can directly demonstrate how the $t_{\text{d\_on}}$ and $t_{\text{d\_off}}$ change with T. As shown by the black curves in Fig. 1, the $t_{\text{d\_on}}$ decreases with T with a decreasing $|dt_{\text{d\_on}}/dT|$, and the $t_{\text{d\_off}}$ increases with T with an increasing $|dt_{\text{d\_off}}/dT|$, consistent with the (14) and (15). However, the V_{id} decreases with T with a decreasing $|dV_{\text{id}}/dT|$ at extremely high temperatures, so the changes in $|dt_{\text{d\_on}}/dT|$ and $|dt_{\text{d\_off}}/dT|$ decrease as T rises. As a result, the nonlinearity of the V_{id} exacerbates the nonlinearity of the $t_{\text{d\_on}}$ but weakens the nonlinearity of the $t_{\text{d\_off}}$, as shown by the red curves in Fig. 1. In other words, the linearity of the $t_{\text{d\_on}}$ at extremely high temperatures is worse than that at low temperatures, but the linearity of the $t_{\text{d\_off}}$ at extremely high temperatures is better than that at low temperatures.

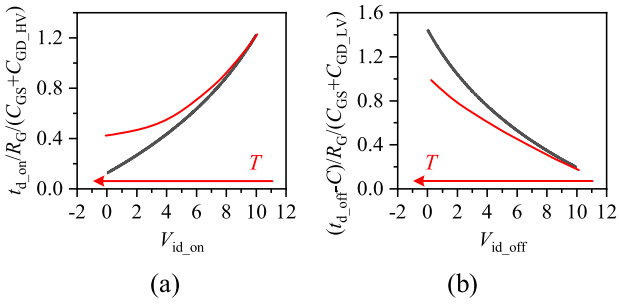

Fig. 1. Effect of the nonlinearity of the V_{id} on the (a) $t_{\text{d\_on}}$ and (b) $t_{\text{d\_off}}$. The black curves are (a) $t_{\text{d\_on}}/R_{\text{G}}/(C_{\text{GS}}+C_{\text{GD\_HV}}) = \ln((V_{\text{cc}}-V_{\text{ton}})/(V_{\text{cc}}-V_{\text{id\_on}}))$ and (b) $(t_{\text{d\_off}}-C)/R_{\text{G}}/(C_{\text{GS}}+C_{\text{GD\_LV}}) = \ln((V_{\text{nof}}-V_{\text{ee}})/(V_{\text{id\_off}}-V_{\text{ee}}))$, respectively ($V_{\text{cc}} = 15$ V, $V_{\text{ee}} = -4$ V, $V_{\text{ton}} = -2$ V, $V_{\text{nof}} = 13$ V). The red curves illustrate the effect of the nonlinearity of the V_{id}.

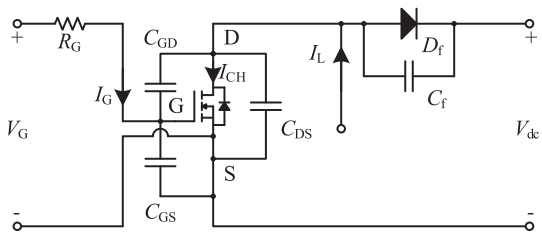

Fig. 2. Operating conditions of the SiC MOSFET. D_{f} is a SiC Schottky barrier diode (SBD), and the C_{f} is the capacitance of D_{f}. I_{L} is the load current of an inductive load.

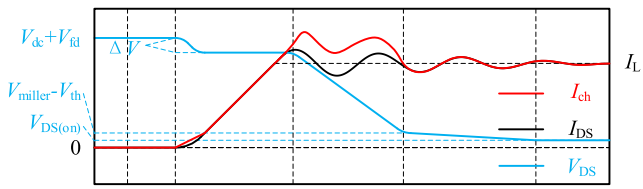

Fig. 3. Turn-ON process of the SiC MOSFET.

E. Turn-ON Switching Rate of Current

The operating conditions of the SiC are shown in Fig. 2. In this case, the I_{DS} can be expressed as follows:

$$I_{\text{DS}} = I_{\text{L}} - C_{\text{f}}\frac{dV_{\text{DS}}}{dt} = I_{\text{CH}} + C_{\text{DS}}\frac{dV_{\text{DS}}}{dt} + C_{\text{DG}}\frac{dV_{\text{DG}}}{dt} \tag{16}$$

where I_{CH} is the channel current.

During the current rise phase of the turn-ON process, it is assumed that the V_{DS} is maintained at a constant value of $V_{\text{dc}}+V_{\text{fd}}-LdI_{\text{DS\_on}}/dt$, as shown in Fig. 3 (the V_{fd} is the forward value of the D_{f}). The slope of the rising current ($dI_{\text{DS\_on}}/dt$) can

be expressed as follows:

$$\frac{dI_{\mathrm{DS\_on}}}{dt}=\frac{2\mu_{\mathrm{ni}}(T)C_{\mathrm{OX}}S}{W_{\mathrm{Cell}}L_{\mathrm{CH}}}\left(V_{\mathrm{GS}}(t)-V_{\mathrm{th}}(T)\right)\frac{dV_{\mathrm{GS}}(t)}{dt}. \tag{17}$$

According to (17), the slope of $dI_{\mathrm{DS\_on}}/dt$ changing with temperature ($d^2I_{\mathrm{DS\_on}}/dtdT$) can be expressed as follows:

$$\frac{d^2I_{\mathrm{DS\_on}}}{dtdT}=\frac{2C_{\mathrm{OX}}S}{W_{\mathrm{Cell}}L_{\mathrm{CH}}}\frac{dV_{\mathrm{GS}}(t)}{dt}\times\left(\frac{d\mu_{\mathrm{ni}}(T)}{dT}\left(V_{\mathrm{GS}}(t)-V_{\mathrm{th}}(T)\right)-\mu_{\mathrm{ni}}(T)\frac{dV_{\mathrm{th}}(T)}{dT}\right) \tag{18}$$

where $d\mu_{\mathrm{ni}}/dT<0$ and $dV_{\mathrm{th}}/dT<0$, so

$$\frac{d^2I_{\mathrm{DS\_on}}}{dtdT}=\frac{2C_{\mathrm{OX}}S}{W_{\mathrm{Cell}}L_{\mathrm{CH}}}\frac{dV_{\mathrm{GS}}(t)}{dt}\times\left(\mu_{\mathrm{ni}}(T)\left|\frac{dV_{\mathrm{th}}(T)}{dT}\right|-\left(V_{\mathrm{GS}}(t)-V_{\mathrm{th}}(T)\right)\left|\frac{d\mu_{\mathrm{ni}}(T)}{dT}\right|\right). \tag{19}$$

According to (19), the relationship between $dI_{\mathrm{DS\_on}}/dt$ and temperature is mainly affected by μ_{ni} and V_{th}. At low temperatures, the $d\mu_{\mathrm{ni}}/dT$ is small, and the $d^2I_{\mathrm{DS\_on}}/dtdT$ is mainly dependent on the $\mu_{\mathrm{ni}}|dV_{\mathrm{th}}/dT|$. Therefore, the dI_{DS}/dt increase with temperature almost linearly at low temperatures. However, at extremely high temperatures, the μ_{ni} decreases with temperature. In this case, the $d^2I_{\mathrm{DS\_on}}/dtdT$ decreases with temperature, which means that the $dI_{\mathrm{DS\_on}}/dt$ increases with temperature at a decreasing slope.

III. Construction of the Accurate Test Platform for Extremely High-Temperature Characteristics

A. Test Method for Extremely High-Temperature Study

There are two problems in the extremely high-temperature studies of the SiC MOSFET. The first problem is the operating temperature (<175 °C) limitation of the conventional package. Even though there are some studies about the high-temperature power module [21], [22], the maximum operating temperature is still lower than 250 °C. The high-temperature probe station [26] is unsuitable for the dynamic characteristic test. And the operating temperature of the conventional plastic package (TO-247) used in [23] is usually lower than 175 °C. The encapsulant can be damaged by high-temperature exposure [24] because of the limitation of the packaging materials [4], [25]. In addition, other equipment in the test platform also cannot withstand high temperatures, such as capacitors and oscilloscope probes.

The second problem is the error caused by the parasitic parameters of the package during the test. As shown in Fig. 4, L_{p} and R_{p} are the parasitic inductance and resistance of the package in the power loop, respectively. In the static characteristic test, the test result of the voltage (V_{t}) can be expressed as follows:

$$V_{\mathrm{t}}=V_{\mathrm{DS}}+I_{\mathrm{t}}R_{\mathrm{p}}=I_{\mathrm{t}}\left(R_{\mathrm{DS(on)}}+R_{\mathrm{p}}\right). \tag{20}$$

Since the $R_{\mathrm{DS(on)}}$ of the latest SiC MOSFET is very low, the errors caused by the R_{p} will become very significant in the static characteristic test. In the dynamic characteristic test, V_{t} can be expressed as follows:

$$V_{\mathrm{t}}=V_{\mathrm{DS}}+I_{\mathrm{t}}R_{\mathrm{p}}+L_{\mathrm{p}}\frac{dI_{\mathrm{t}}}{dt}. \tag{21}$$

Because of the high switching speed of the SiC MOSFET, the parasitic inductance will cause significant errors in V_{t} and dV_{t}/dt.

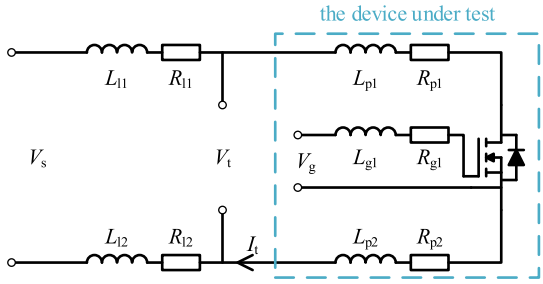

Fig. 4. Equivalent circuit schematic of the test connection.

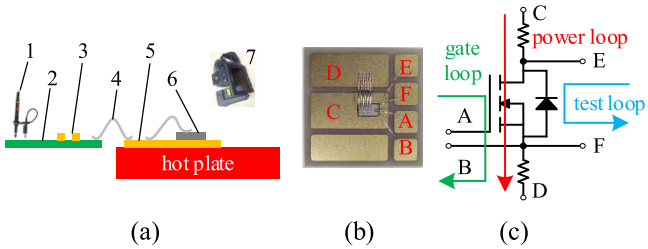

Fig. 5. (a) Schematic diagram of the test platform: 1: probe, 2: PCB, 3: capacitors, 4: bonding wire, 5: DBC, 6: die under test, and 7: infrared camera. (b) Single-chip module. (c) Equivalent circuit schematic of the test lines' connection.

This article proposes a specific test method for extremely high-temperature static and dynamic characterization to solve the problems of high-temperature exposure and test accuracy. The test method is based on the combination of printed circuit board (PCB) and direct bonding copper (DBC), as shown in Fig. 5(a). The die under test is on the DBC, and the other devices and the test equipment are all on the PCB. And the bonding wires are used to connect the DBC and the PCB. A single-chip module is manufactured to ensure that the test can be carried out at extremely high temperatures, as shown in Fig. 5(b). The die is mounted on an AlN DBC by nanosilver sintering to avoid the melting of the solder layer [26]. Since the operating temperature of the Si-gel-based encapsulants is lower than 250 °C [27], [28], [29], a thin layer of polyimide is cured on the top surface of the module for insulation. During the test, the single-chip module is the only part that is heated. In this case, the first problem can be solved.

However, the parasitic parameters in the power loop are larger because the test points are far from the die in this situation. Therefore, the problem of accuracy becomes more serious. To eliminate the influence of parasitic parameters on test results, another two terminals (E and F, directly connected to the drain and source of the die) are designed on the DBC to form the

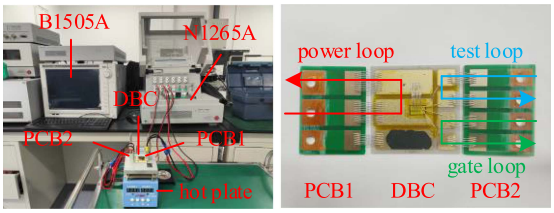

Fig. 6. (a) Test platform for static characterization. (b) Connection of the DBC and PCB.

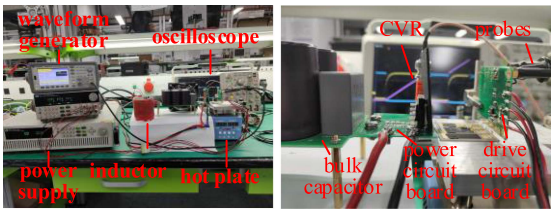

Fig. 7. Double-pulse test platform.

four-terminal Kelvin sensing. Therefore, the test circuit can be directly connected to the die, as shown in Fig. 5(c), avoiding the influence of the parasitic parameters in the power loop on the test result. In this case, V_t is equal to V_{DS}, different from (20) and (21). Thus, the error caused by the parasitic parameters of the package can be eliminated.

B. Test Platform for Static Characterization

Based on the method proposed, a test platform for static characterization is built, as shown in Fig. 6(a). An Agilent B1505A power device analyzer/curve tracer is used to measure the static characteristics of the SiC MOSFET (CPW3-1200-13A, 13 mΩ, 149 A). A hot plate heats the single-chip module during the test. An infrared (IR) camera (FLIR T630SC) is used to monitor the junction temperature of the die. A layer of black coating with an emissivity of 0.94 is applied to the top surface of the module to ensure the accuracy of the IR camera. The connection between the PCB and the DBC is shown in Fig. 6(b). Two PCBs are used to separate the test lines from the DBC to prevent the test lines from being exposed to high temperatures.

C. Double-Pulse Test Platform for Dynamic Characterization

The double-pulse test platform is also based on the combination of DBC and PCB, as shown in Fig. 7. The single-chip module is used directly to ensure that the test can be carried out at extremely high temperatures. The two PCBs in the double-pulse test platform are more complex: the drive circuit board and the power circuit board. The decoupling capacitors, coaxial current shunt, and freewheeling diode are on the power circuit board. The bulk capacitor board and the inductor are also connected to the power circuit board. The drive circuit and the test points of V_{GS} and V_{DS} are on the drive circuit board. During the test, the drive circuit board is suspended vertically above the hot plate, and the probes are placed on the top of the drive circuit board to prevent the PCB and probes from being heated. The two terminals for the V_{DS} test mentioned before (E and F) are connected to the probe across the drive circuit board so that the influence of the parasitic inductors on the test results can be eliminated.

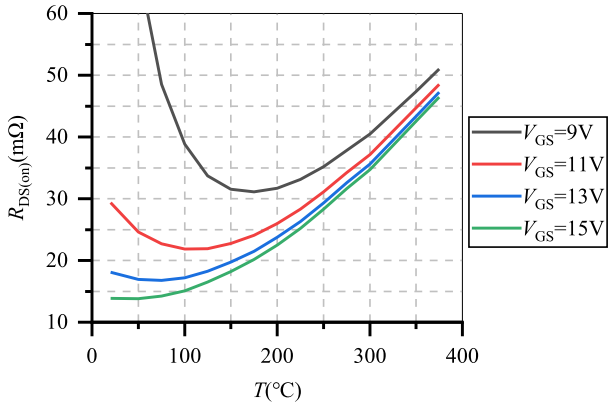

Fig. 8. Temperature-dependent $R_{DS(on)}$ at V_{GS} of 9, 11, 13, and 15 V. Measurement conditions: The I_{DS} is equal to 75 A.

The double-pulse test is carried out at 400 V. A negative turn-OFF gate driver is used ($V_{cc} = 15$ V, $V_{ee} = -4$ V). Both turn-ON and turn-OFF gate resistors are 5 Ω. The first and second pulses are 8 and 2 μs respectively, with a 2-μs interval in the middle. A SiC diode is used as the freewheeling diode, paralleled with a 73-μH single-layer air core inductor. A Tektronix Digital Phosphor Oscilloscope (DPO 4104B, 1 GHz) is used to display the current and voltage waveforms. A Tektronix voltage probe (TPP1000, 1 GHz) is used to obtain the gate–source voltage, and another Tektronix voltage probe (TPP0850, 800 MHz) is used to measure the drain–source voltage during the test. The drain current is measured by a coaxial current shunt (SSDN-414-01). The IR camera (FLIR T630SC) is used to monitor the junction temperature.

IV. TSEPs of SiC MOSFET Over a Wide Temperature Range

A. On-resistance

The $R_{DS(on)}$ and output characteristics at V_{GS} of 9, 11, 13, and 15 V are tested from room temperature to 375 °C. During the test of the output characteristics, the V_{DS} increases from 0 to 10 V, and the I_{DS} increases from 0 to 150 A. The curves of $R_{DS(on)}$ changing with temperature under different V_{GS} are shown in Fig. 8, while the I_{DS} equals 75 A. At low temperatures, the R_{CH} dominates the decrease in the $R_{DS(on)}$ with increasing temperature. At extremely high temperatures, the R_{JFET} and R_D dominate the increase in $R_{DS(on)}$ with increasing temperature. And the temperature at the minimum $R_{DS(on)}$ decreases with increasing V_{GS} due to the decrease in R_{CH}.

At low temperatures, R_{CH} dominates the $R_{DS(on)}$, which is related to the V_{GS}. Therefore, the difference between the $R_{DS(on)}$ at different V_{GS} is huge and the distribution of output characteristic curves at different V_{GS} is scattered, as shown in

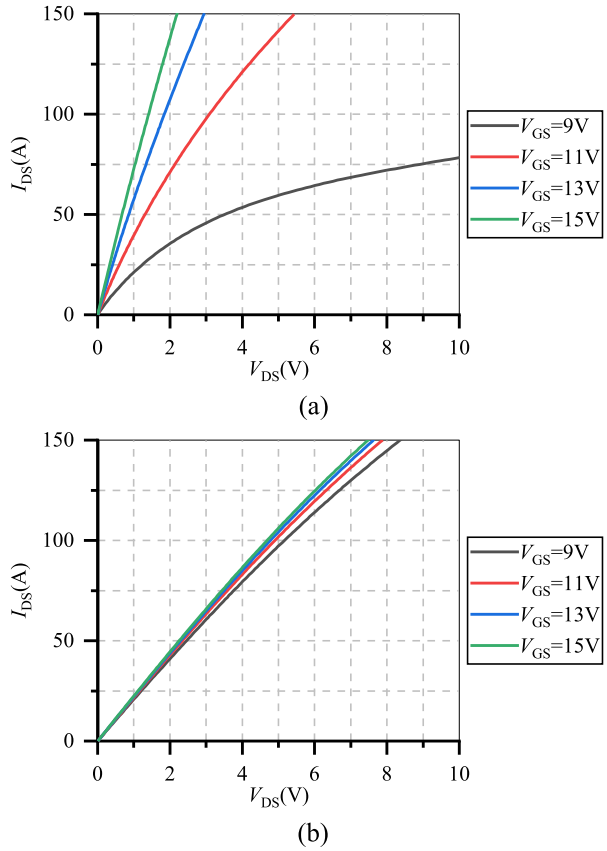

Fig. 9. Output characteristics at different V_{GS}. Measurement conditions: The temperature is (a) 20 °C and (b) 375 °C.

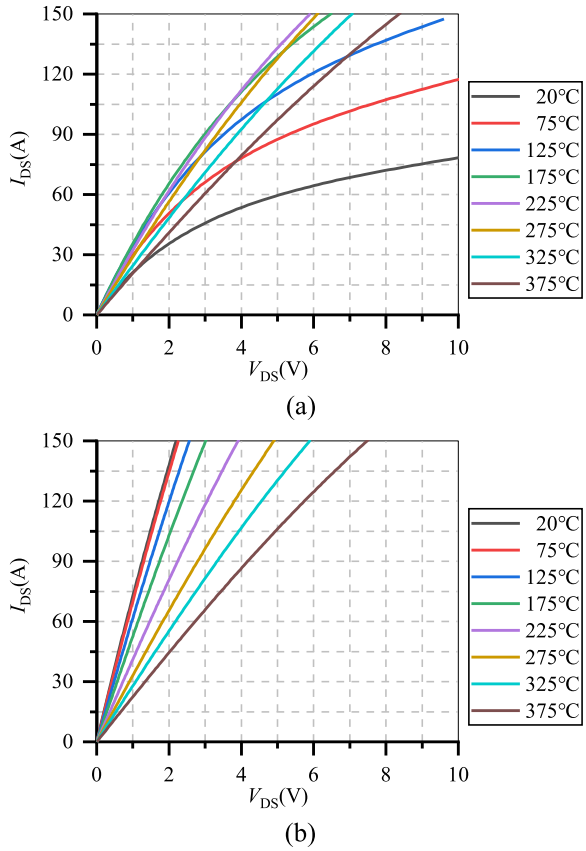

Fig. 10. Output characteristics at different temperatures. Measurement conditions: (a) V_{GS} is equal to 9 V and (b) V_{GS} is equal to 15 V.

Fig. 9(a). At extremely high temperatures, the R_{JFET} and the R_D, which are not affected by the V_{GS}, become the dominant part of the $R_{DS(on)}$. Therefore, the difference of $R_{DS(on)}$ at different V_{GS} is tiny, as shown in Fig. 8, and the distribution of the output characteristic curves at different V_{GS} is very close, as shown in Fig. 9(b).

When V_{GS} is equal to 9 V, the slope of the output characteristic curve first increases and then decreases as the temperature rises, as shown in Fig. 10(a). In addition, the device under test quickly enters the saturation region with increasing I_{DS} at low temperatures. As a result, the output characteristic curves under 9 V V_{GS} at different temperatures cross each other. This is a problem if the V_{on} is used for online junction temperature monitoring because there are two different junction temperatures at the duplicate I_{DS} and V_{DS}. To avoid this problem, the V_{GS} should be high enough. As shown in Fig. 10(b), the slope of the output characteristic curve decreases monotonically with the temperature at V_{GS} of 15 V. And the $R_{DS(on)}$ increases monotonously from 13.8 to 46.5 mΩ (3.34 times 13.8 mΩ) from room temperature to 375 °C, as shown in Fig. 8. However, the change in $dR_{DS(on)}/dT$ at 15 V V_{GS} is significant at low temperatures, due to the decrease in R_{CH}. At extremely high temperatures, the change in $dR_{DS(on)}/dT$ at 15 V V_{GS} is small. But the influence of I_{DS} dependence on the $R_{DS(on)}$ becomes serious. As shown in Fig. 10(b), the decrease in the slope of the output characteristic curve with the increasing I_{DS} is more obvious at high temperatures, which means that the increase in $R_{DS(on)}$ due to the increasing I_{DS} is more significant.

B. Threshold Voltage

In this article, the V_{th} of the SiC MOSFET is measured by testing the I_{DS} and the V_{GS} with a temperature step of 25 °C. During the test, the V_{GS} increases with a step of 0.005 V and the I_{DS} is limited to below 25 mA. The V_{DS} is set to 10 V. The V_{th} is defined as the value of V_{GS} when the I_{DS} equals 10 mA.

The temperature-dependent V_{th} is shown in Fig. 11. The V_{th} decreases from 3.09 to 1.33 V as the temperature increases from 20 °C to 375 °C. The $|dV_{th}/dT|$ below 100 °C is a little bit higher than that at higher temperatures because the influence of the D_{it} on V_{th} is more obvious at cryogenic temperatures. But the difference is negligible. At extremely high temperatures, the change in the $|dV_{th}/dT|$ is small, and the linearity of the V_{th} is better. The V_{th} decreases with T almost linearly, with a slope of 0.50 V/100 °C over the entire temperature range. The V_{th} at 375 °C is 43% of the V_{th} at room temperature.

C. V_{GS} at Constant I_{DS_sat}

The V_{id} is investigated by testing the transfer characteristic from room temperature to 375 °C with a temperature step of 50 °C. During the test, the V_{DS} is set to 10 V, the same as the test

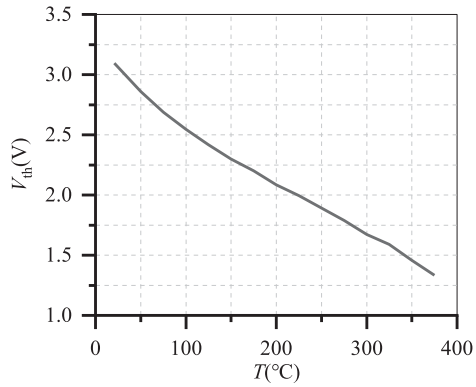

Fig. 11. Temperature-dependent $V_{\rm th}$, which is defined as the value of $V_{\rm GS}$ when the $I_{\rm DS}$ reaches 10 mA.

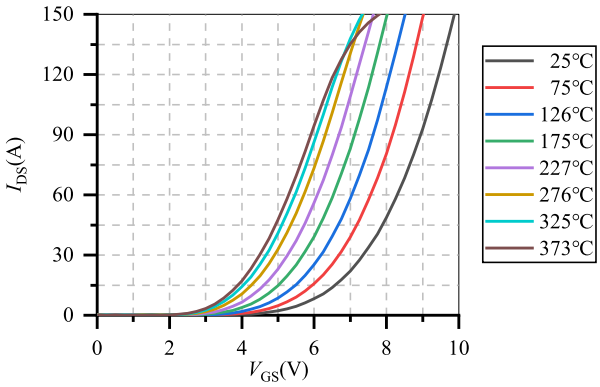

Fig. 12. Transfer characteristics at different temperatures. Measurement conditions: The step of the gate–source voltage is equal to 0.25 V, and the drain–source voltage is set to 10 V.

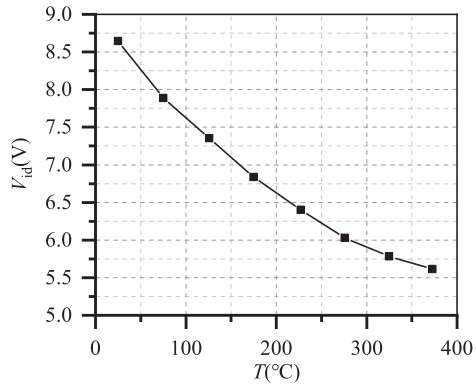

Fig. 13. Temperature-dependent $V_{\rm id}$. Measurement conditions: The $I_{\rm DS}$ is equal to 75 A.

of $V_{\rm th}$. The $V_{\rm GS}$ increases from 0 to 10 V with a step of 0.25 V. The $I_{\rm DS}$ is limited below 150 A since the maximum continuous $I_{\rm DS}$ of the SiC MOSFET die under test is 149 A ($V_{\rm GS}$ = 15 V, $T_{\rm C}$ = 25 °C). The curves of transfer characteristics at different temperatures are shown in Fig. 12.

As shown in Fig. 12, at low temperatures, the change in $\mu_{\rm ni}$ is relatively small, and the $V_{\rm th}$ decreases with the temperature almost linearly. Hence, the curve of the transfer characteristic

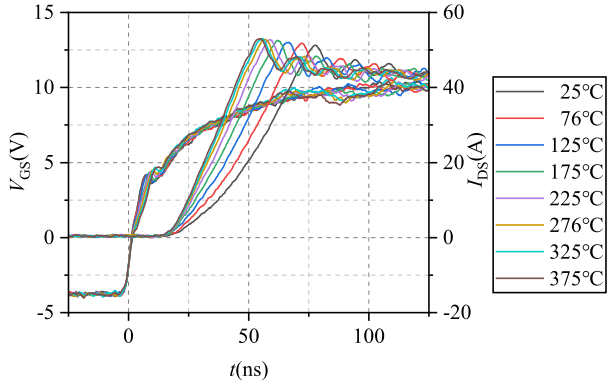

Fig. 14. Turn-ON transient waveforms of $V_{\rm GS}$ and $I_{\rm DS}$ at different temperatures. These waveforms are aligned at the point $V_{\rm GS} = -2$ V. The turn-ON gate resistance is 5 Ω.

shifts to the left with almost the same distance, and the $V_{\rm id}$ also decreases with the temperature almost linearly. At extremely high temperatures, the decreases in the $\mu_{\rm ni}$ cause the $I_{\rm DS}$ to decrease. Therefore, the distance in the x-axis direction between two adjacent curves gradually decreases, as previously analyzed. As a result, the $V_{\rm id}$ decreases at a decreasing $|dV_{\rm id}/dT|$ at extremely high temperatures. Over the entire temperature range, the $V_{\rm id}$ decreases from 8.64 V at 25 °C to 5.61 V at 373 °C.

D. Turn-ON Delay Time

The measured waveforms of $V_{\rm GS}$ and $I_{\rm DS}$ during the turn-ON process at different temperatures are shown in Fig. 14. According to (5), the $V_{\rm GS}$ is temperature independent during the $t_{\rm d\_on}$. Therefore waveforms of $V_{\rm GS}$ at different temperatures overlap during the $t_{\rm d\_on}$, as shown in Fig. 14. It should be noted that the measured $V_{\rm GS}$ in Fig. 14 is not equal to the $V_{\rm GS}$ in Section II due to the partial voltage of the internal gate resistance. In this section, the $t_{\rm d\_on}$ is defined as the time interval from $V_{\rm GS} = -2$ V to $I_{\rm DS} = 4$ A. The starting point should be −1.9 V (10% of $V_{\rm cc}-V_{\rm ee}$). But, as previously analyzed in Section II, only the $t_{\rm d\_on}$ is related to the starting point. The $dt_{\rm d\_on}/dT$ is independent of the starting point, so an approximation is selected as the starting point. The waveform of $I_{\rm DS}$ shifts to the left with the increasing temperature, as shown in Fig. 14, indicating a decreasing $t_{\rm d\_on}$. The temperature-dependent $t_{\rm d\_on}$ is shown in Fig. 15.

As previously analyzed, both $t_{\rm d\_on}$ and $|dt_{\rm d\_on}/dT|$ are small due to the small $C_{\rm GD}$. The maximum value of $t_{\rm d\_on}$ is only 26.4 ns at 25 °C. As temperature rises, the $t_{\rm d\_on}$ decreases to 20.0 ns at 375 °C. The range of the $t_{\rm d\_on}$ variation is only 6.4 ns over 350 °C. In addition, the linearity of the $t_{\rm d\_on}$ is worse at extremely high temperatures. The $|dt_{\rm d\_on}/dT|$ decreases as temperature rises, as previously analyzed. Since the nonlinearity of $V_{\rm id}$ exacerbates the nonlinearity of $t_{\rm d\_on}$, the $|dt_{\rm d\_on}/dT|$ is smaller at extremely high temperatures. The average value of $|dt_{\rm d\_on}/dT|$ from 25 °C to 175 °C is 0.035 ns/°C. However, the average value of $|dt_{\rm d\_on}/dT|$ from 175 °C to 375 °C is only 0.006 ns/°C, which is almost one-sixth of that at low temperatures. As a result, if the $t_{\rm d\_on}$ is used for online junction

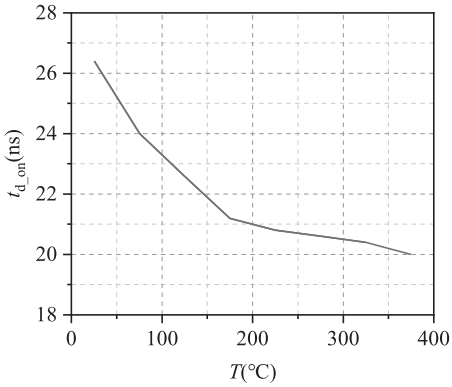

Fig. 15. Curve of t_{d_on} versus temperature.

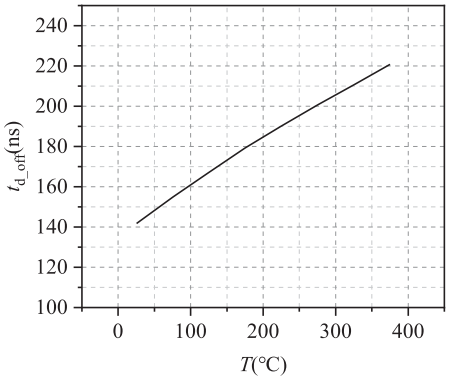

Fig. 17. Curve of t_{d_off} versus temperature.

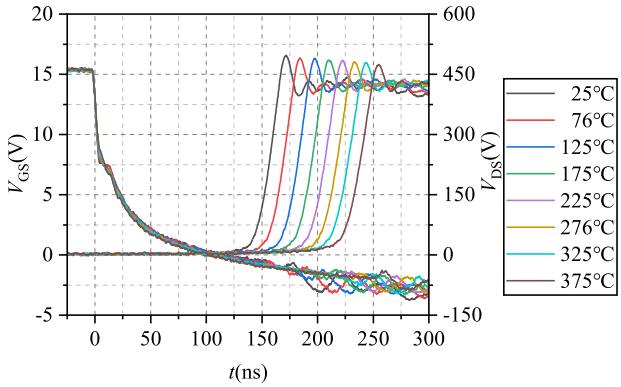

Fig. 16. Turn-OFF transient waveforms of V_{GS} and V_{DS} at different temperatures. These waveforms are aligned at the point $V_{GS} = 13$ V. The turn-OFF gate resistance is 5 Ω.

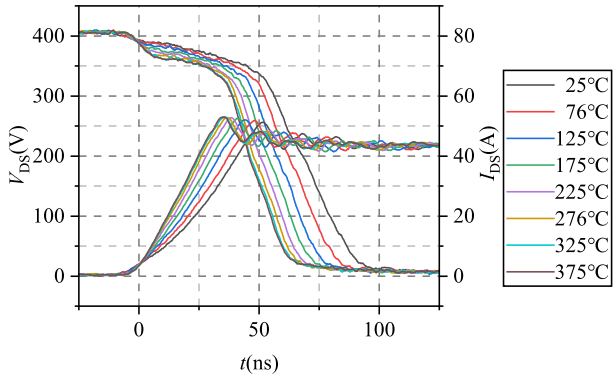

Fig. 18. Turn-ON transient waveforms of V_{DS} and I_{DS} at different temperatures. These waveforms are aligned at the point $I_{DS} = 4$ A. The turn-ON gate resistance is 5 Ω.

temperature monitoring, the requirements for the test equipment are very stringent. The common solution to increase $|dt_{d\_on}/dT|$ is to increase the R_G.

E. Turn-OFF Delay Time

The measured waveforms of V_{GS} and V_{DS} during the turn-OFF process at different temperatures are shown in Fig. 16. These waveforms are aligned at the point $V_{GS} = 13$ V. Similarly, only the t_{d_off} is related to the starting point. The $|dt_{d\_off}/dT|$ is independent of the starting point. Therefore, the t_{d_off} is defined as the time interval from $V_{GS} = 13$ V to $V_{DS} = 40$ V. As shown in Fig. 16, the waveform of V_{DS} shifts to the right with the increasing temperature, indicating an increasing t_{d_off}. The temperature-dependent t_{d_off} is shown in Fig. 17.

As analyzed in Section II, the change in dV_{DS}/dt with temperature is small at low V_{DS}. Therefore, the waveforms of the V_{DS} at different temperatures almost overlap below 40 V, as shown in Fig. 16. According to (13), the t_{d_off} is proportional to the C_{GD}, and the C_{GD} is very large during the t_{d_off} due to the low V_{DS}. Therefore, the t_{d_off} is larger than t_{d_on} (at the same R_G). At 25 °C, the t_{d_off} is 141.8 ns, which is 5.4 times the t_{d_on}. As the temperature rises, the t_{d_off} increases to 220.8 ns at 375 °C, which is 11.0 times the t_{d_on}. Moreover, the nonlinearity of V_{id} weakens the nonlinearity of t_{d_off}, and the linearity of the t_{d_off} is still good at extremely high temperatures. Since the $|dt_{d\_off}/dT|$ is also proportional to the C_{GD}, the $|dt_{d\_off}/dT|$ is also larger than the $|dt_{d\_on}/dT|$. The average value of $|dt_{d\_off}/dT|$ from 25 °C to 375 °C is 0.226 ns/°C, which is 37.7 times the $|dt_{d\_on}/dT|$ from 175 °C to 375 °C. One problem is that the t_{d_off} is related to the V_{miller}, which means the value of t_{d_off} is affected by the load current.

F. Turn-ON Switching Rate of Current

According to (17), the dI_{DS_on}/dt varies with t (or $I_{DS\_on}(t)$). In this article, the dI_{DS_on}/dt at $I_{DS\_on} = 20$ A (almost 50% of the load current) is chosen and calculated. To reduce the error, a linear regression analysis is performed on the curve of I_{DS_on} from $I_{DS\_on} = 15$ A to $I_{DS\_on} = 25$ A, to calculate the dI_{DS_on}/dt. The dI_{DS_on}/dt at different temperatures is shown by the black curve in Fig. 19. The dI_{DS_on}/dt increases from 0.94 A/ns at 25 °C to 1.49 A/ns at 375 °C, which means the speed of the current rise becomes faster as the temperature increases, as shown in Fig. 18.

The linear regressing equation of dI_{DS_on}/dt versus temperature is also calculated and shown by the red curve in Fig. 19, and the slope of this red curve ($d^2I_{DS\_on}/dtdT$) is 0.0016 A/ns/°C. It can be seen that although linear regression is used to calculate the dI_{DS_on}/dt, the residual is still large, as shown in Fig. 19.

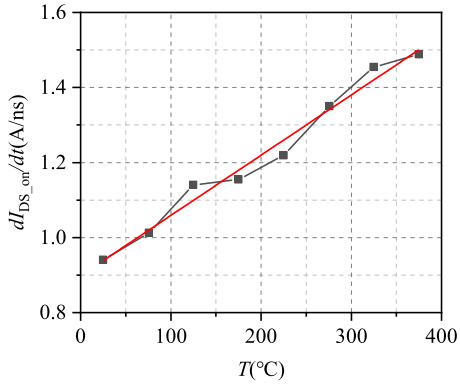

Fig. 19. Black curve is the curve of dI_{DS_on}/dt versus temperature, and the red curve is the curve of the linear regression equation.

This is because the range of the data source is not exactly from 15 to 25 A (such as 15.07–24.80 A at 175 °C and 15.47–24.58 A at 225 °C) and the dI_{DS_on}/dt at different $I_{DS\_on}(t)$ is different. As a result, the decreases in $d^2I_{DS\_on}/dtdT$ with temperature at extremely high temperatures mentioned in the previous analysis are not evident in Fig. 19.

V. Comparison of Different TSEPs of the SiC MOSFET

To explore the influence of high temperature on the TSEPs, the TSEPs at high temperature are compared and analyzed from two aspects: sensitivity and linearity.

A. Sensitivity

The following ratio is used for the comparison of different TSEPs' sensitivity [30]:

$$S = \frac{|s|}{|\mathrm{val}_{\max}|} \tag{22}$$

where s is the slope of the TSEP change with temperature (e.g., $d^2I_{DS\_on}/dtdT$ [A/ns/°C]) and the $\mathrm{val}_{\max}$ is the maximum value of the TSEP in the temperature range (e.g., dI_{DS_on}/dt [A/ns]). In this case, the unit of the S is $°C^{-1}$ and can be used as the comparison criteria for different TSEPs. The s of different TESPs at different temperature ranges are calculated by linear regression, namely from 25 °C to 175 °C (low temperatures), from 225 °C to 375 °C (high temperatures), and from 25 °C to 375 °C (the entire temperature range). Finally, the S values of different TSEPs at different temperature ranges are calculated, as shown in Fig. 20.

There are two situations in which the value of S will decrease. If the $|\mathrm{val}_{\max}|$ is constant, the S will decrease with the decreasing $|s|$. In this case, the range of the TSEP variation with temperature becomes smaller. If the s is constant, the S will decrease with the increasing $|\mathrm{val}_{\max}|$. In this case, although the range of the TSEP variation with temperature remains the same, the ratio of the range of the TSEP variation with temperature to the range from 0 to $|\mathrm{val}_{\max}|$ decreases. Both of these cases are not conducive to the use of TSEPs in online junction temperature monitoring.

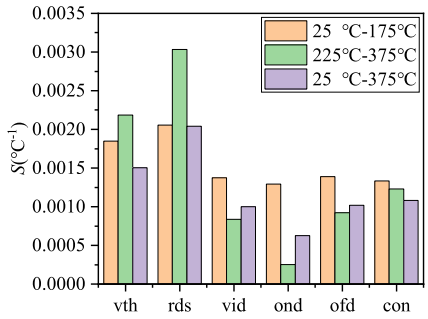

Fig. 20. S of different TSEPs at different temperature ranges, where vth is the threshold voltage, rds is on-resistance, the vid is the V_{GS} at a constant I_{DS_sat}, ond is turn-ON delay time, ofd is turn-OFF delay time, and con is dI_{DS_on}/dt.

The S of the V_{th} at high temperatures is larger than that at low temperatures because the V_{th} decreases with temperature with an almost constant $|s|$. Since the influence of the D_{it} is more obvious at low temperatures, the $|s|$ of the V_{th} at low temperatures is larger than that over the entire temperature range, and the S of the V_{th} at low temperatures is also larger. Similarly, the $|s|$ of t_{d_off} also almost remains constant over the entire temperature range. Since the t_{d_off} increases with temperature, the S of t_{d_off} at high temperature is smaller than that at low temperature and is close to that over the entire temperature range, as shown in Fig. 20.

Different from the V_{th} and t_{d_off}, the $|s|$ of the $R_{DS(on)}$, V_{id}, and t_{d_on} are quite different at low and high temperatures. As a result, the S of the $R_{DS(on)}$ at high temperatures is larger than that at low temperatures, even though the $R_{DS(on)}$ increases with the temperature. This is due to the influence of the channel resistance, the $|s|$ of the $R_{DS(on)}$ at low temperatures is relatively small. In contrast, the S of the V_{id} at high temperatures is smaller than that at low temperatures, even though the V_{id} decreases with the temperature. This is due to the influence of μ_{ni}, the $|s|$ of the V_{id} at high temperatures is relatively small. Similar to the V_{id}, the $|s|$ of the t_{d_on} at high temperatures is much smaller than that at low temperatures. As a result, the S of the t_{d_on} at high temperatures is much smaller than that at low temperatures, although the $|\mathrm{val}_{\max}|$ at high temperatures is smaller. In addition, the difference in $|s|$ at high temperatures and low temperatures introduces big errors in the calculation of $|s|$ over the entire temperature range. Therefore, the S of these three TSEPs can only be used as a reference for qualitative analysis.

During the turn-ON process, the $d^2I_{DS\_on}/dtdT$ decreases with temperature particularly at extremely high temperatures mentioned in the previous analysis. However, the nonlinearity of dI_{DS_on}/dt is not evident due to the residuals. Therefore, the S values of the dI_{DS_on}/dt at high temperatures are smaller than those at low temperatures because the dI_{DS_on}/dt increases with temperature.

B. Linearity

The Pearson correlation coefficient (also known as Pearson's r, denoted as R_p) is used to evaluate the linear correlation between TSEP and temperature. The value of Pearson's r is always between -1 and 1. If Pearson's r is less than 0, the TSEP

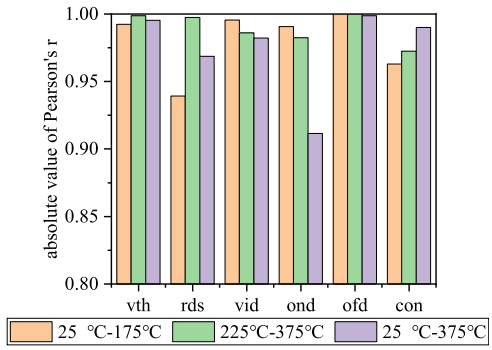

Fig. 21. Absolute value of Pearson's r of different TSEPs at different temperature ranges, where vth is the threshold voltage, rds is on-resistance, the vid is the $V_{\rm GS}$ at a constant $I_{\rm DS\_sat}$, ond is turn-ON delay time, ofd is turn-OFF delay time, and con is $dI_{\rm DS\_on}/dt$.

and temperature are negatively correlated; otherwise, they are positively correlated. The closer Pearson's r is to 1 or -1, the stronger the linear correlation between TSEP and temperature. And the closer the Pearson's r is to 0, the weaker the linear correlation between TSEP and temperature. The Pearson's r values between TSEPs and temperature are calculated at different temperature ranges. And the absolute values of Pearson's r of different TSEPs at different temperature ranges are shown in Fig. 21.

Since the influence of the $D_{\rm it}$ is more obvious at low temperatures and the change in $|dV_{\rm th}/dT|$ is small at extremely high temperatures, the $|R_{\rm p}|$ of $V_{\rm th}$ at high temperatures is larger than that at low temperatures. Also, the $|R_{\rm p}|$ of $V_{\rm th}$ over the entire temperature range is a little smaller than that at high temperatures; it is still larger than that at low temperatures and is close to 1. Therefore, the linearity of $V_{\rm th}$ is good over the entire temperature range, as shown in Fig. 21.

Because the channel resistance decreases but the JFET and drift region resistance increase with temperature, the $|R_{\rm p}|$ of $R_{\rm DS(on)}$ is small at low temperatures. Since the channel resistance and the change in the channel resistance at high temperatures is small, the $|R_{\rm p}|$ of $R_{\rm DS(on)}$ at high temperatures is much larger than that at low temperatures. Because the $|s|$ of the $R_{\rm DS(on)}$ at low temperatures is quite different from that at high temperatures, the $|R_{\rm p}|$ of $R_{\rm DS(on)}$ over the entire temperature range is smaller than that at high temperatures, which means that the linearity of $R_{\rm DS(on)}$ over the entire temperature range is worse than that at high temperatures.

In contrast, the linearity of the $V_{\rm id}$ at low temperatures is better than that at high temperatures because the change in $\mu_{\rm ni}$ at low temperatures is small. Therefore, the $|R_{\rm p}|$ of $V_{\rm id}$ at low temperatures is larger, as shown in Fig. 21. Due to the decrease in $\mu_{\rm ni}$ at high temperatures, the $|dV_{\rm id}/dT|$ decreases with the temperature. As a result, the $|R_{\rm p}|$ of $V_{\rm id}$ at high temperatures is smaller than that at low temperatures. Because of the variation of $|dV_{\rm id}/dT|$, the $|R_{\rm p}|$ of $V_{\rm id}$ over the entire temperature range is even lower than that at high temperatures.

As mentioned earlier, due to the different effects of $V_{\rm id}$ on $t_{\rm d\_on}$ and $t_{\rm d\_off}$, the linearity of $t_{\rm d\_on}$ is worse, but the linearity of $t_{\rm d\_off}$ is better at high temperatures. The $|R_{\rm p}|$ of $t_{\rm d\_on}$ is large at low temperatures, which means that the linearity of $t_{\rm d\_on}$ at low temperatures is good. At high temperatures, the $|R_{\rm p}|$ is smaller due to the variation in $|dt_{\rm d\_on}/dT|$. As a result, the $|R_{\rm p}|$ of $t_{\rm d\_on}$ over the entire temperature range is much smaller, as shown in Fig. 21, which means worse linearity. Unlike the $t_{\rm d\_on}$, the $|dt_{\rm d\_off}/dT|$ remains almost constant over the entire temperature range. Therefore, the $|R_{\rm p}|$ value of $t_{\rm d\_off}$ at low temperatures, high temperatures, or the entire temperature range is very large, almost equal to 1. Therefore, the linearity of $t_{\rm d\_off}$ is excellent at different temperature ranges, as shown in Fig. 21.

There are two reasons for the reduction of the $|R_{\rm p}|$ value: the variation of $|s|$, and the increase in residual. Although the $dI_{\rm DS\_on}/dt$ is calculated by linear regression, the residual is still evident, as shown in Fig. 19. In addition, because the number of data points is small, the $|R_{\rm p}|$ of $dI_{\rm DS\_on}/dt$ at low or high temperatures is small. But the $|R_{\rm p}|$ of $dI_{\rm DS\_on}/dt$ over the entire temperature range is larger.

C. Summary of TSEP Performance

1) The sensitivity and linearity of $V_{\rm th}$ at high temperatures are better than those at low temperatures. Therefore, the $V_{\rm th}$ for online junction temperature monitoring performs slightly better at high temperatures. Although the sensitivity over the entire temperature range is worse than that at low and high temperatures, the $|R_{\rm p}|$ values of $V_{\rm th}$ at different temperature ranges are very close. Therefore, the $V_{\rm th}$ for online junction temperature monitoring performs well at different temperature ranges, especially at high temperatures.
2) The sensitivity and linearity of $R_{\rm DS(on)}$ at high temperatures are much better than those at low temperatures. At high temperatures, the S value of $R_{\rm DS(on)}$ is the largest of all the TSEPs, and the $|R_{\rm p}|$ value of $R_{\rm DS(on)}$ is very close to 1. However, the sensitivity and linearity of $R_{\rm DS(on)}$ over the entire temperature range are bad due to the bad performance at low temperatures. Therefore, the $R_{\rm DS(on)}$ ($V_{\rm on}$) for online junction temperature monitoring performs better at high temperatures. However, it is essential to note that $R_{\rm DS(on)}$ is dependent on $I_{\rm DS}$ and the $V_{\rm GS}$ should be high enough.
3) Since the influence of $\mu_{\rm ni}$ on $V_{\rm id}$ is evident at high temperatures, the sensitivity and linearity of $V_{\rm id}$ at low temperatures are much better than those at high temperatures. Even though the $|R_{\rm p}|$ difference of the $V_{\rm id}$ between the entire temperature range and low temperature is not significant, the linearity of the $V_{\rm id}$ over the entire temperature range worsens as the temperature increases further. Therefore, the $V_{\rm id}$ for online junction temperature monitoring performs better at low temperatures. And the $V_{\rm id}$ is also $I_{\rm DS}$ dependent.
4) At low temperatures, the sensitivity and linearity of $t_{\rm d\_off}$ are slightly better than $t_{\rm d\_on}$, but the difference is negligible. Due to the different effects of $V_{\rm id}$ on $t_{\rm d\_on}$ and $t_{\rm d\_off}$, the $|s|$ of $t_{\rm d\_on}$ decreases with temperature, but the $|s|$ of $t_{\rm d\_off}$ remains almost constant over the entire temperature range. As a result, the sensitivity of $t_{\rm d\_on}$ at high temperatures and the linearity of $t_{\rm d\_on}$ over the entire temperature range are bad. The $t_{\rm d\_on}$ for online junction temperature

monitoring performs better at low temperatures. The linearity of t_{d_off} is the best of all TSEPs, no matter what temperature range. And the S of t_{d_off} is much larger than that of t_{d_on} at high temperatures. Therefore, the t_{d_off} for online junction temperature monitoring performs well at different temperature ranges. But the t_{d_off} is related to the load current. Besides, there is a difficulty in applying t_{d_on} and t_{d_off} for online temperature detection, which is that the t_{d_on} and t_{d_off} are too short. It is difficult to detect them directly.

5) The dI_{DS_on}/dt is difficult to use for online junction temperature monitoring directly because dI_{DS_on}/dt varies with I_{DS}, making the true values of dI_{DS_on}/dt difficult to get. Even though the dI_{DS_on}/dt is calculated by linear regression, the residuals are still obvious. Some studies try to use the maximum value of switching speed for online junction temperature monitoring, such as the dI_{DS_off}/dt_{max}. The dI_{DS_off}/dt_{max} can be simply represented by the peak value of the parasitic inductance (in the power loop) voltage [31]. However, the dI_{DS_off}/dt_{max} depends not only on the load current but also on the dc voltage. Therefore, a complicated look-up table is required if the dI_{DS_off}/dt_{max} is used for online junction temperature monitoring.

VI. Conclusion

To explore the application of online junction temperature monitoring at extremely high temperatures, the influence of high temperatures on the TSEPs of the SiC MOSFET is theoretically analyzed in detail. Based on the test platform built in this article, the TSEPs of SiC MOSFET are characterized up to 375 °C. According to the results, the TSEPs are compared in terms of sensitivity and linearity in different temperature ranges. The t_{d_off} is the best TSEP for linearity in different temperature ranges, no matter what temperature range. But the value of t_{d_off} is small and related to the load current. The sensitivity and linearity of V_{th} are also good at different temperature ranges. Although the linearity of V_{th} is slightly worse than that of t_{d_off}, the V_{th} is more sensitive and easier to measure. The sensitivity and linearity of $R_{DS(on)}$ (or V_{on}) at high temperatures are much better than those at low temperatures. In contrast, V_{id} and t_{d_on} perform better at low temperatures than at high temperatures. But the V_{id} is related to I_{DS}. Since the value of t_{d_on} is much smaller than t_{d_off}, the requirements for the test equipment of t_{d_on} are more stringent. As the dI_{DS_on}/dt varies with I_{DS} and the true values of dI_{DS_on}/dt are difficult to get, the dI_{DS_on}/dt is difficult to use directly for online junction temperature monitoring.

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