# Double-Side Cooled SiC MOSFET Power Modules With Sintered-Silver Interposers for a 100-kW/L Traction Inverter

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***Abstract*—Low-profile double-side cooled power modules are emerging in electric-drive inverters to achieve higher power density and efficiency. However, the rigid interconnection between the devices and two substrates raises the thermomechanical reliability issue of double-side cooled modules. In the prior work, we proposed the use of porous sintered-silver (Ag) interposers in the double-side cooled modules, resulting in reduced thermomechanical stresses, better heat extraction, and lower package parasitic inductance. To further improve the power density and demonstrate the benefits of using the sintered-Ag interposers, we proposed a revised half-bridge module layout that further reduced the power-loop parasitic inductance by 23%, improved the power handling capability by 44%, and retained a similar thermomechanical stress reduction. After carefully selecting high-temperature packaging materials, we fabricated the improved module layout with a reasonably high yield due to the deformable feature of sintered-Ag interposers. The thermal testing showed that the module had excellent power handling capability with a junction-to-fluid thermal resistance of 0.76 °C/W due to the double-sided cooling. The electrical characterization at elevated temperatures up to 250 °C and the switching characterization validated the functionalities of the power modules with SiC devices aimed for high-temperature and fast switching. Six of the double-side cooled power modules with sintered-Ag interposers were assembled into a segmented traction inverter, demonstrating a high power density of over 100 kW/L.**

***Index Terms*—Double-side cooled power module, high-density traction inverter, high temperature, SiC MOSFET, sintered Ag.**

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## I. Introduction

THE demand for electric vehicles (EVs) has been significantly increased over recent years, associated with the desire for better performance, longer range, and lower cost. Power electronics are one of the major components of EVs that need to be improved to satisfy those desires. The United States Department of Energy (DOE) has announced technical targets of the power electronics density to achieve 100 kW/L by 2025, increasing five times from the year 2020 of 18 kW/L [1], [2]. Achieving this target would require replacing the current silicon (Si) power devices with wide bandgap (WBG) devices, e.g., silicon carbide (SiC) [3], [4]. SiC devices can be made into a much smaller footprint than that of Si devices with the same voltage and current ratings, which not only saves the cost but also enables more compact power module designs. However, the higher heat flux density of SiC devices due to the smaller footprint presnets challenges to module packaging. To improve the package's thermal performance, double-side cooled modules have been introduced [5], [6], [7], [8]. The device chips are sandwiched between two electrically and thermally conductive substrates with short metal interposers covering a significant portion of the device area. The resulting package has significantly improved thermal performance due to double-sided cooling, as well as a smaller footprint and lower package parasitic inductances. But there is still concern about their thermomechanical reliability due to the rigid interconnection between the devices and two substrates. Researchers have been exploring various approaches to reducing the thermomechanical stresses by using different interposer materials (e.g., molybdenum instead of copper (Cu) [9], [10], [11]) or varied interposer geometries (e.g., trenched Cu plate [12], X-shaped, octagon shaped [13], and silver (Ag) tubing [14]). But all the above approaches have to pay the price of increased thermal resistance of the power modules. In the prior work [15], we introduced a porous interposer made from sintered Ag. Compared with Cu, the thermomechanical stress at the most vulnerable interfaces of the double-sided module was reduced by over 40% without sacrificing thermal performance. We also demonstrated the use of sintered-Ag interposers for simplifying the fabrication process of double-side cooled power modules since the interposers are deformable under pressure.

Another benefit of SiC devices over Si counterparts is their capability of operating at higher junction temperatures. To support

the operation of SiC devices, the high-temperature capability of the module package needs to be addressed. In [16], [17], [18], [19], and [20], wire-bonded power modules with SiC devices have been fabricated and tested up to 200 °C or 250 °C junction temperatures. In [21], wire bonds were replaced by Cu interposers, and solder joints were replaced by sintered-Ag joints. The power modules were demonstrated to operate reliably at 200 °C junction temperature. With the sintered-Ag interposers, we also achieved sintered-Ag joints for all the critical bonded interfaces, making it possible to work reliably at high junction temperatures. In this work, we proposed a revised half-bridge module layout with less parasitic inductance, reduced thermomechanical stresses, and better thermal performance to further demonstrate the benefits of using sintered-Ag interposers in a double-side cooled module. Afterward, we carefully selected module packaging materials for high temperatures (e.g., >200 °C) and to improve fabrication yield. Twelve double-side cooled power modules of the improved design have been fabricated for characterization and inverter demonstration. Thermal testing was conducted to validate the power handling capability of double-side cooled power modules. Electrical characterizations at elevated temperatures up to 250 °C were conducted to characterize the SiC device's high-temperature performance. The functionality of the power module with low parasitic inductance was verified by the double-pulse test. Finally, six power modules were assembled into a segmented traction inverter to demonstrate a high power density of over 100 kW/L.

## II. Module Design and Simulations

### A. Module Layout

In the prior work [15], we reported one layout design (Layout #1) of a planar SiC MOSFET half-bridge module with double-sided cooling as shown in Fig. 1(a). In this work, we proposed another module layout design (Layout #2) after conducting extensive electrical and thermal simulations of various layouts for improved package parasitic inductances and thermal performances. The SiC MOSFETs (CPM3-1200-0013A) were purchased from CREE with dimensions of 7.26 mm × 4.36 mm × 0.18 mm. Layout #2 and the exploded view are shown in Fig. 1(b) and (c), respectively. The overall dimensions were the same as Layout #1 measuring at 2.4 cm × 1.8 cm × 0.4 cm. The small footprint and low profile allowed us to achieve the target power density demonstrated in Section IV. Layout #1 has two SiC MOSFETs placed on the bottom substrate and six metal posts were used to interconnect the top substrate. The parasitic inductances of power loop and gate loop were 4.4 and 3.0 nH, respectively, as determined by ANSYS Q3D. Instead of placing two chips on the bottom substrate, Layout #2 has two SiC MOSFETs facing up and down, placed on top and bottom substrates, respectively. In this way, the number of metal posts used for interconnection was reduced to four and the power-loop parasitic inductance was reduced to 3.4 nH due to a shorter conduction path in the power-loop. The gate-loop parasitic inductance remains the same. A negative temperature coefficient thermistor (Vishay, NTCC200E4203FT) was also added to Layout #2 to monitor

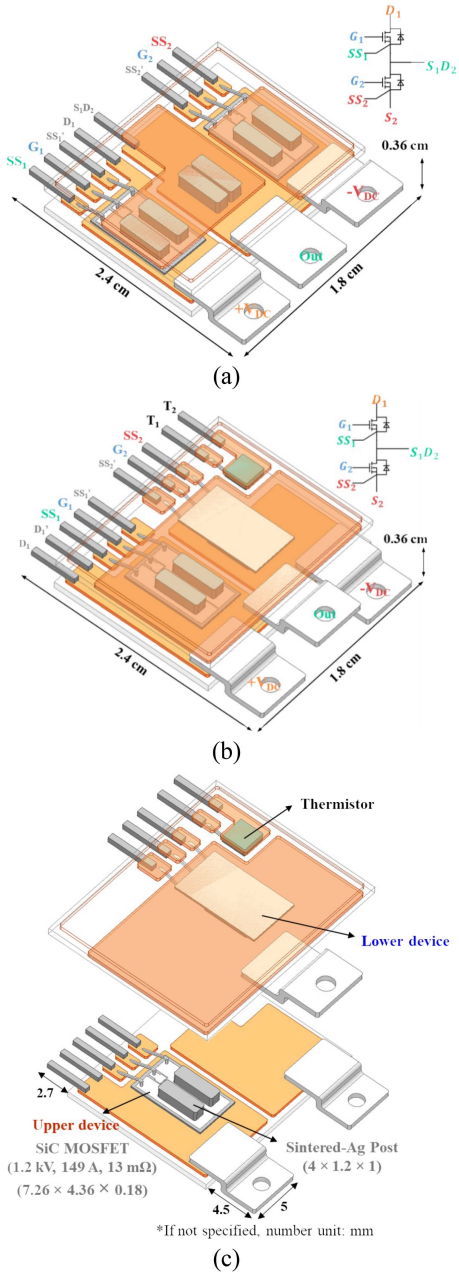



Fig. 1. Layout designs of the SiC MOSFET double-side cooled half-bridge module. (a) Layout #1 having both devices mounted on the bottom substrate [15]. (b) Layout #2 having one MOSFET on the bottom substrate and the other on the top substrate. (c) Exploded view of Layout #2.

the module temperature. All the power terminals were designed on one side, and the connectors for the thermistor, gate drivers, and current sensing were designed on the other side.

### B. Thermal Simulation

The thermal performance of the two layouts was simulated by ANSYS Workbench for comparison. First, the temperature distributions of the two layouts were simulated. The ambient temperature was set at 22 °C, the thermal conductivity of sintered Ag was assigned as 175 W/m·°C, and other material parameters

TABLE I
MAXIMUM VON MISES STRESS IN EACH COMPONENT OF MODULE LAYOUT #1 AND #2

| von Mises stress (MPa) | | Interposer | Chip | Interposer-substrate attach | Interposer-chip attach | Chip attach |
|---|---|---|---|---|---|---|
| Layout #1 | Sintered Ag | 9.2 | 41.0 | 14.9 | 14.1 | 12.9 |
| Layout #2 | Sintered Ag | 23.6 | 166.4 | 10.2 | 14.0 | 13.4 |
| | Cu | 193.2 | 210.8 | 13.1 | 17.3 | 14.1 |
| | Mo | 181.1 | 167.2 | 12.8 | 13.4 | 14.7 |

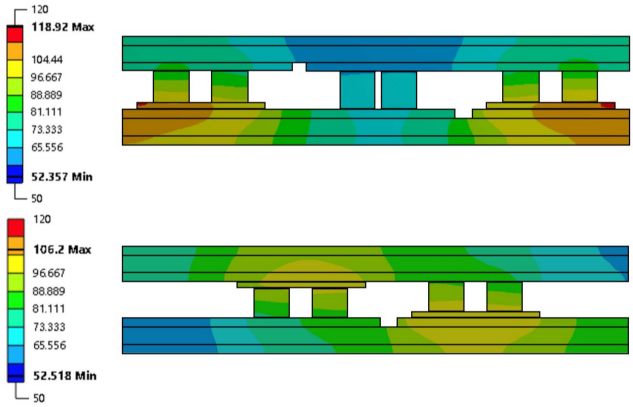



Fig. 2. Simulated steady-state temperature distributions of module Layout #1 and Layout #2.

can be found in [[15], Table I]. A fixed convection coefficient of 8000 W/m$^2$·°C was applied on both sides of the substrates for both layouts. A power dissipation of 100 W was applied on each SiC MOSFET. The simulated temperature distributions of the two layouts are shown in Fig. 2. It can be seen that under the same power loss and cooling conditions, Layout #2 is much cooler than Layout #1. For Layout #1, junction-to-case thermal resistances ($R_{\mathrm{thjc}}$) of the drain side and source side were 0.103 and 0.404 °C/W, respectively, resulting in an equivalent $R_{\mathrm{thjc}}$ per chip of 0.0820 °C/W. The drain side and source side $R_{\mathrm{thjc}}$ of Layout #2 were calculated to be 0.0737 and 0.255 °C/W, respectively. The equivalent $R_{\mathrm{thjc}}$ per chip for Layout #2 is 0.0572 °C/W.

To investigate the power handling capability of the two layouts under different cooling conditions, steady-state thermal simulations were run for plots of the heat flux density per chip versus the heatsink convection coefficient with the maximum allowed junction temperature of 200 °C. A parametric study was conducted in the simulations by varying the convection coefficients ($h_i$) from 0 to 20 000 W/m$^2$·°C. For double-sided cooling configurations of the two layouts, $h_i$ was applied on the exposed side of each substrate. For the single-sided cooling configuration of Layout #1, we assumed a fixed convection coefficient of 20 W/m$^2$·°C at the top substrate and applied $h_i$ to the bottom substrate. From the results shown in Fig. 3, when the convection coefficient is 10000 W/m$^2$·°C as indicated by a gray dashed line, Layout #1 can handle a maximum heat flux density per chip of 468 W/cm$^2$ if cooled from one side and

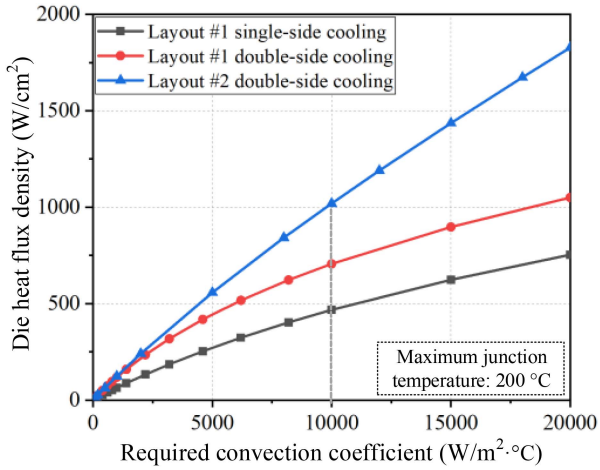



Fig. 3. Steady-state thermal simulation results of the heat flux density per chip versus the required convection coefficient for different layouts with a single-sided cooling or a double-sided cooling at a maximum junction temperature of 200 °C.

706 W/cm$^2$ if cooled from both sides, respectively. By using double-sided cooling, the module is capable of handling 51% more die heat flux. For Layout #2, the maximum heat flux per chip is further increased to 1020 W/cm$^2$, which is 44% more than that of Layout #1 with double-sided cooling. Overall, the maximum allowed heat flux density per chip for Layout #2 is 118% higher than that of Layout #1 with single-side cooling.

### C. Thermomechanical Simulation

Sintered Ag has a much lower elastic modulus, compared to solid Cu or Mo, resulting in a reduction of thermomechanical stresses in double-side cooled power modules. To quantify the stress reduction, we used the ANSYS Workbench to simulate thermomechanical stresses in Layout #2 with sintered Ag, Cu, and Mo interposers, respectively. The Anand viscoelasticity model was used in the simulation to describe the viscoelastic behavior of sintered Ag. The parameters for the Anand model and other material parameters can be found in [22]. The major components are SiC chips, interposers, and three sintered-Ag attachment layers: interposer-to-substrate attach, interposer-to-chip attach, and chip attach. The thermomechanical stresses in each component were simulated. In the simulations, the modules were cooled from the sintering temperature (245°C) down to room temperature, and heated up by a power loss of 100 W (316 W/cm$^2$) per chip to reach the steady state. The stress-free temperature was set at the sintering temperature of 245°C. Table I summarizes the maximum von Mises stresses in each component of Layout #2. The conclusion for Layout #2 is similar to that of Layout #1 as we presented in [15]. The bonded interfaces in a module are usually the first to fail [13], [23]. The stresses at the bonded interfaces with the sintered-Ag interposer are much lower than those with the Cu interposer while they are similar to those with the Mo interposer. For example, if we consider the interposer-chip attach as the most vulnerable interface as it has the highest stress among the three bonded layers, the one with

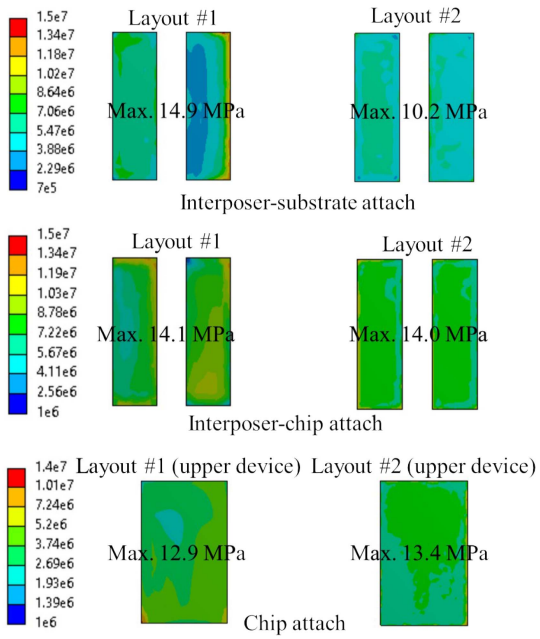



Fig. 4. von Mises stress distributions of three bonded interfaces in module Layout #1 and Layout #2.

sintered Ag has 19% lower stress compared to that with solid Cu interposers.

The stresses in Layout #1 are also listed in Table I for comparison. As the bonded interfaces are the most vulnerable components in power modules, we included the von Mises stress distributions of the interposer-substrate-attach, interposer-chip-attach, and chip-attach layers for the two module layouts, respectively, in Fig. 4. Compared to Layout #1, the maximum stress at the interposer-substrate-attach layer of Layout #2 was reduced by 32%. The stresses at the interposer-chip-attach layers remain similar for both layouts. Additionally, Layout #1 requires six interposers for interconnections, whereas Layout #2 only requires four interposers. The reduction in the number of interposers not only reduces the material cost but also reduces the interposer-substrate-attach interfaces, which are prone to fail during thermomechanical reliability tests. The stress at the chip-attach layer of Layout #2 increased by 4% compared to Layout #1. In Section III on module fabrication, we employed pressure-assisted silver sintering for the chip-attach layers to achieve better bonding strength and thermomechanical reliability.

### D. Module Layouts Comparison

In this section, we summarized the comparison between module Layout #1 and Layout #2 in Table II. The two layouts have the same dimensions. By placing the two devices on two substrates facing up and down, the power-loop parasitic inductance can be reduced by 23%, the junction-to-case thermal resistance can be reduced by 30%, and the thermomechanical stress at the interposer-substrate-attach layer can be reduced by 32%. The number of interposers required for interconnections was also reduced with the improved layout, resulting in a lower cost and easier assembly process. Additionally, the module temperature can be monitored in Layout #2 by the thermistor embedded in the module.

TABLE II
COMPARISON BETWEEN MODULE LAYOUT #1 AND #2

| | Layout #1 | Layout #2 |
|---|---|---|
| Dimensions (cm) | 2.4 × 1.8 × 0.4 | 2.4 × 1.8 × 0.4 |
| Power-loop parasitic inductance (nH) | 4.4 | 3.4 |
| Junction-to-case thermal resistance per MOSFET (°C/W) | 0.0820 | 0.0572 |
| von Mises stress at the interposer-substrate-attach Layer layer (MPa) | 14.9 | 10.2 |
| Number of interposers | 6 | 4 |
| Temperature monitoring by thermistor | No | Yes |

## III. MODULE FABRICATION

To fabricate module Layout #2 with high-temperature capability and a reasonably high yield, we carefully selected other packaging materials and tested the assembly processes. In [15], a silver paste was used for die-attach, but we encountered a yield issue with the device's drain-to-source leakage currents since the wet paste tended to be squeezed out and shorted the device. We replaced the nano-silver paste with a silver preform (nanoTach-Pf from NBE Tech) for die-attach. The silver preform is pre-dried and resolves the squeezing-out issue, thus helping to improve the fabrication yield. Also, the die-attach by silver preform was achieved by pressure-assisted sintering, which reduced thermal and electrical resistances of the module package. The substrate used in the package was a direct bonded copper from Rogers (Curamik AlN, 0.3 mm Cu/0.63 mm AlN/0.3 mm Cu). As for encapsulation materials, we selected silicone rubber (Nusil-r2188) to cover the device area to make the module workable at higher junction temperatures. In [24] and [25], Nusil-r2188 was thermally aged at 250 °C and no cracks were generated until 28 days, while the dielectric strength dropped to 12 kV/mm, it is still deemed to be enough to encapsulate the 1.2-kV device used in this work. The remaining module area was filled with an epoxy resin (ME-531 from LORD) to provide mechanical support.

Fig. 5 shows in detail the fabrication processes. Layout #2 has one SiC MOSFET placed on the bottom substrate and the other placed on the top substrate. So, the top and bottom pieces were processed separately as shown in Fig. 5(a)–(f). Having one chip on each substrate for Layout #2 also improved the fabrication yield compared to Layout #1 with two chips on the bottom substrate. The die-attach was achieved by pressure-assisted silver-sintering with a silver preform. The preform was transferred to the chip backside at 130 °C and under a mechanical force equivalent to 2 MPa pressure. Then, the device with preform was attached to direct bond copper (DBC) substrate by sintering at 250 °C for 30 min and under 3 MPa as shown in Fig. 5 (b). After the die-attach, a silver paste was stencil-printed on the source pad of the device with a stainless stencil, and then two

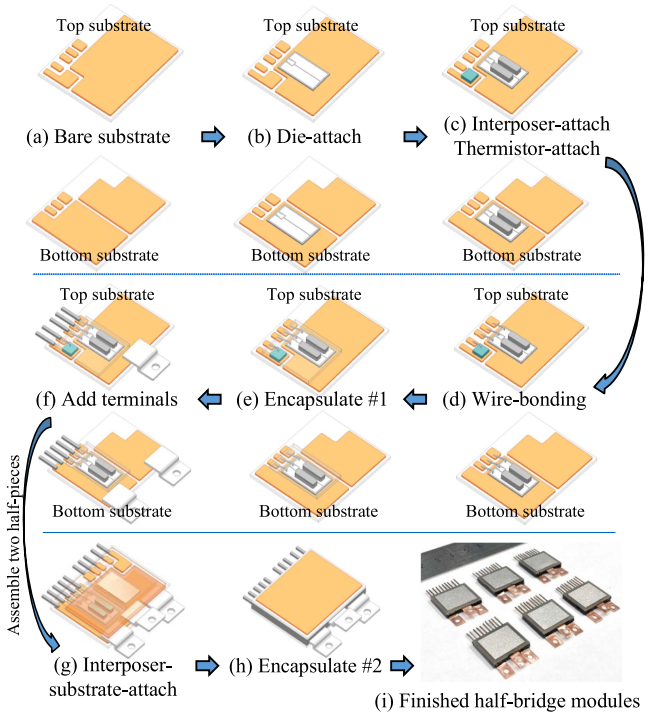



Fig. 5. Fabrication steps of the double-side cooled half-bridge modules in Layout #2.

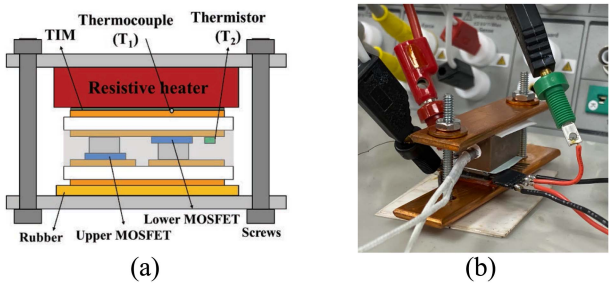



Fig. 6. (a) Schematic and (b) experimental test setup for the electrical measurements at elevated temperatures.

sintered-Ag posts were placed on the device for interconnection. To ensure the alignment and bonding strength, a mechanical force equivalent to 2 MPa pressure was applied to the posts and sintered at 245 °C for 15 min. The thermistor was soldered on the substrate at the step shown in Fig. 5(c). After the wire bonding with a 10-mil aluminum wire for the gate and Kelvin source, the selected silicone rubber was used to encapsulate the device area to protect the device for subsequent fabrication steps. In Fig. 5(f), the copper terminals and pins for the gate and Kelvin source connection were soldered on the DBC substrates. Then, the two half-pieces were tested with a curve tracer (Agilent B1505A) on forward conduction and blocking to ensure the fabrication process did not deteriorate the device's characteristics. The testing at this step ensures that the half-pieces were workable before assembling the whole half-bridge module. The two half-pieces were attached by silver-sintering at 245 °C for 15 min under 2 MPa. Finally, the spacing between the two DBC substrates was filled by the epoxy resin. Fig. 5(i) shows six fabricated phase-leg modules measured at 2.4 cm × 1.8 cm × 0.4 cm.

## IV. Module Characterization

### A. Electrical Characteristics at Elevated Temperatures

One benefit of SiC devices over Si devices is their ability to operate at high temperatures, which also presents challenges for module packaging. With sintered-Ag joints at all the critical interfaces and silicone rubber to encapsulate the device area, the fabricated module has the potential to support the SiC MOSFET working at high junction temperatures. To investigate the device's performance at high junction temperatures, we conducted the electrical characterizations of the fabricated module at elevated temperatures up to 250 °C. Fig. 6 shows the schematic and the experimental setup for measurements. The electrical characteristics of the module were tested on the curve tracer. A resistive heater was added to the top side of the module to heat up the lower MOSFET. The resistance of the thermistor was monitored to indicate the device temperature. A thermocouple lead was also attached to the surface of the top substrate to ensure valid and consistent temperature readings. The tests were all conducted on the lower MOSFET since the heater and the thermistor were close to it. A thermal interface material (TIM) was added between the heater and the top side of the module and a clamping plate was used to ensure good thermal contacts. A rubber layer was added between the bottom side of the module and the clamping plate to uniform clamping pressure and reduce the cooling from the bottom side. The electrical characteristics of the module were tested at around 25 °C, 50 °C, 100 °C, 150 °C, 200 °C, and 250 °C, respectively.

Fig. 7(a) shows drain–source leakage currents ($I_D$) measured at drain–source voltages ($V_{\rm DS}$) of 800 V and 1200 V, respectively. 800 V was selected according to the dc bus voltage of the traction inverter and 1200 V is the rating of the MOSFET. At 25 °C, $I_D$ of the bare die is 1 $\mu$A specified in the device datasheet (CPM3-1200-0013A, CREE). $I_D$ of the packaged die is 0.29 $\mu$A at 1200 V, proving that our packaging process did not alter the device's blocking capability. At $V_{\rm DS}$ of 800 V, $I_D$ increases with the temperature and there is a significant increase after 200 °C. A similar trend can be also observed at $V_{\rm DS}$ of 1200 V. Overall, the leakage currents of the SiC MOSFET are less than 20 $\mu$A, which indicates a low off-state loss over a wide temperature range up to 250 °C.

Fig. 7(b) shows the threshold voltage ($V_{\rm th}$) at elevated temperatures extracted by the extrapolation in the linear region (ELR) method. $V_{\rm th}$ decreases gradually with the increase in temperature and drops to only 2.4 V at 250 °C. A negative turn-OFF bias voltage is usually desired to avoid false triggering during operation.

The *I–V* output characteristics at elevated temperatures are shown in Fig. 7(c) with a gate-source voltage ($V_{GS}$) of 7 V and 15 V to partially and fully turn on the device, respectively. The warmer the line color indicates the higher temperature. At $V_{GS}$ of 7 V, the slopes of the *I–V* curves increase with the temperature

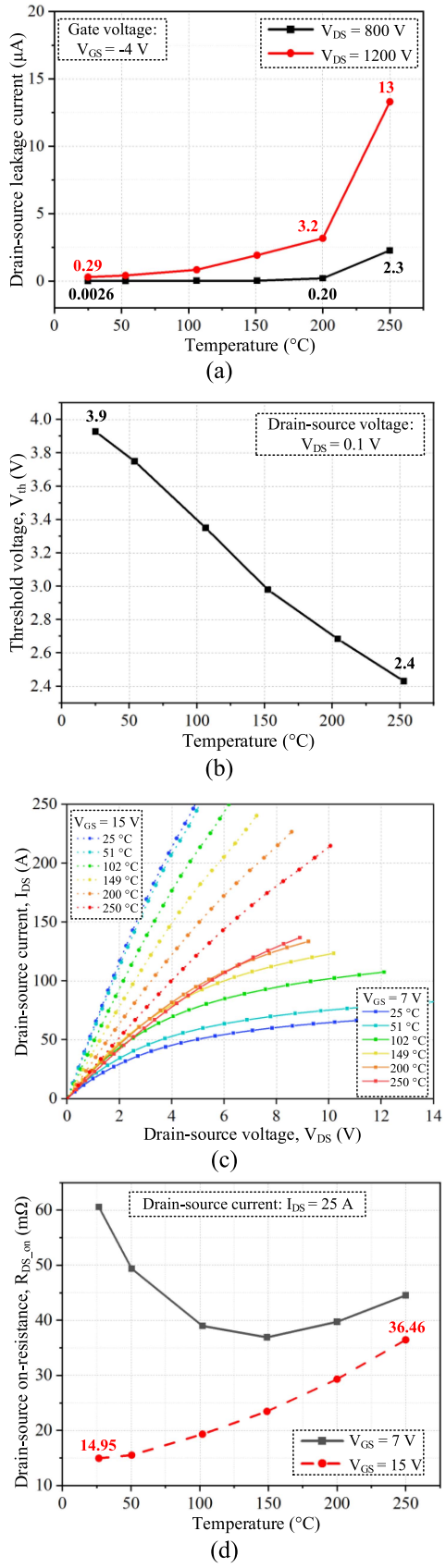



Fig. 7. Electrical measurements of the fabricated phase-leg module at elevated temperatures. (a) Drain–source leakage current. (b) Threshold voltage. (c) Output characteristics at $V_{GS} = 7$ V and $V_{GS} = 15$ V. (d) Drain–source ON-state resistance at $V_{GS} = 7$ V and $V_{GS} = 15$ V.

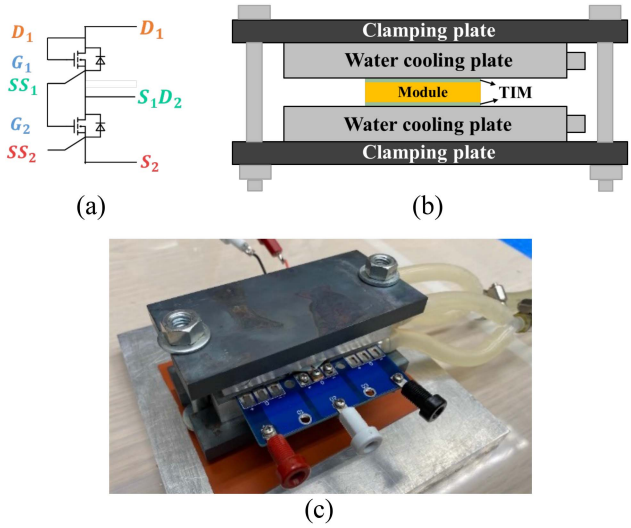



Fig. 8. (a) Schematic of connections for the thermal testing, (b) schematic of the setup, and (c) experimental test setup.

and then decrease, which means the drain–source ON-resistance ($R_{DS\_ON}$) decreases with the increasing temperature first and then increases. At the recommended operational value (e.g., $V_{GS} = 15$ V), the slopes of *I–V* curves decrease with the temperature, showing a monotonically increasing $R_{DS\_ON}$. The different trends of $R_{DS\_ON}$ versus temperature at different $V_{GS}$ can be attributed to the competing temperature dependence of the SiC MOSFET's channel resistance ($R_{CH}$) and bulk resistance ($R_{Bulk}$) [26], [27]. The device channel mobility increases as the temperature increases, causing a constantly reducing $R_{CH}$. On the contrary, the electron mobility at the drift region decreases with increasing temperature, causing an increase in $R_{Bulk}$. The temperature dependence of $R_{DS\_ON}$ is determined by the sum of $R_{CH}$ and $R_{Bulk}$. $R_{DS\_ON}$ versus temperature at two different $V_{GS}$ and at $I_{DS}$ of around 25 A were plotted in Fig. 7(d). At $V_{GS}$ of 7 V, the decreasing effect of $R_{CH}$ dominates until around 150 °C, beyond which the increasing of $R_{Bulk}$ dominates and causes the $R_{DS\_ON}$ to increase gradually. At $V_{GS}$ of 15 V, the device is fully turned on and $R_{Bulk}$ dominates and the $R_{DS\_ON}$ increases monotonically in the testing temperature range. It should be noted that the valley point at that of $V_{GS} = 7$ V still exists, but it is not within 25–250 °C [19]. At 25 °C, $R_{DS\_ON}$ of the packaged device is only around 15 mΩ, which means that our packaging interconnections including power terminals, bonded interfaces, and the interposers only added about 2 mΩ ON-resistance to the bare chip.

### B. Thermal Testing

To experimentally study the power handling capability of module Layout #2, we conducted thermal testing on the fabricated module. Fig. 8(a) and (b) show the schematic of connections, the schematic of the setup, and the experimental setup for thermal testing, respectively. The drain and gate of the device were shorted and a voltage source was applied to partially turn on the device and heat up the module. The voltage and current

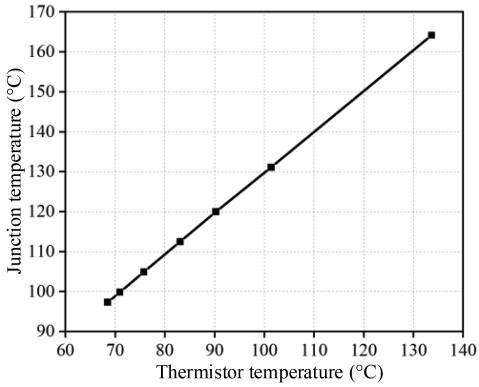



Fig. 9. Thermal simulation results on the junction temperature versus thermistor temperature.

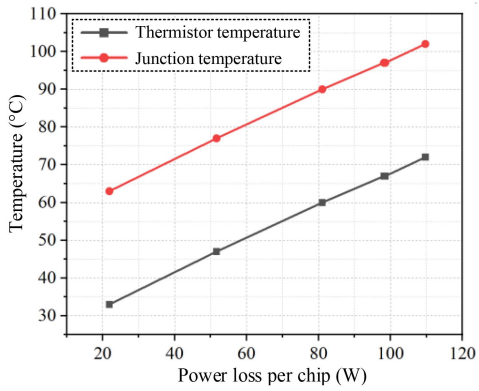


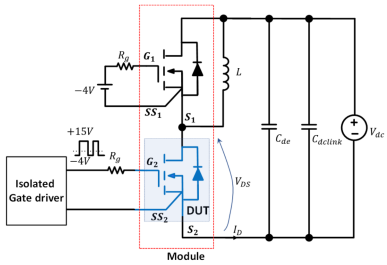

Fig. 10. Thermal testing results of the device junction temperature versus power loss per chip.

between each device were measured to calculate the power consumption of each chip. The phase-leg module was sandwiched between two aluminum water cooling plates (M-type channel, 40 mm × 80 mm × 12 mm from Alexnld). Two stainless steel clamping plates and TIMs inserted between the module and cooling plates were used to ensure good thermal contact. The TIMs (Gap Pad 5000S35) were purchased from Henkel with a thermal conductivity of 5 W/m·K and a thickness of 0.5 mm. The water coolant temperature was 22 °C and the flow rate was set at 1.4 L/min. The device junction temperature was monitored by the thermistor embedded in the phase-leg module. There is a temperature difference between the thermistor and the junction when the module is heated by the device itself as the power source. To determine the temperature difference, we conducted a thermal simulation by sweeping the device's power loss and plotted the junction temperature versus thermistor temperature. As shown in Fig. 9, the temperature difference between the junction and the thermistor was consistent at about 30 °C during the temperature range of interest. During the test, we measured the thermistor temperature after the module reached a thermally steady state (less than 0.1 °C temperature change within one minute), and added 30 °C to the thermistor temperature to indicate the junction temperature.

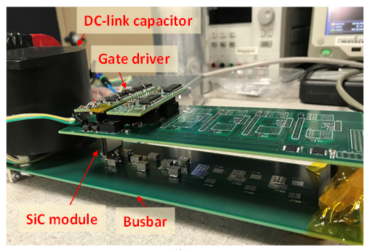
The thermal testing results on the junction temperature versus power loss per chip are shown in Fig. 10, indicating that the module has excellent power handling capability. For example, the junction temperature is 98 °C with a 100 W power loss per chip, indicating a junction-to-fluid thermal resistance per chip of only 0.76 °C/W.

### C. Switching Characteristics

Dynamic characteristics of the fabricated half-bridge module are obtained from the double-pulse test (DPT). The configuration and test setup are shown in Fig. 11(a) and (b), respectively. The bottom device was selected as the device under test (DUT). The gate voltage to the top device was set as -4 V so that the MOSFET was always OFF, and the freewheeling current flowed through its body diode during the OFF time of the bottom device. A double pulse was generated to the bottom device via the isolated gate




(a)




(b)

Fig. 11. (a) Configuration and (b) setup of the double-pulse test.

driver. The components used in the DPT are listed in Table III. The experiment was conducted at the ambient temperature, a dc-link voltage of 800 V, and a load current of 120 A. The switching voltage $V_{DS}$ across the bottom device was measured by a 200 MHz 1.5 kV differential probe (Tektronix, THDP0200), and its current $I_D$ was measured by a 30 MHz 120 A Rogowski coil probe (Powertek, CWTUM/06/B). The Rogowski coil enables a maximum *di/dt* measurement rate of 70 kA/$\mu$s. All the measured signals were recorded by an oscilloscope (Tektronix, MSO5204) with a bandwidth of 2 GHz.

The switching waveforms of the bottom device are presented in Fig. 12(a). Fig. 12(b) and (c) present the magnified areas of the turn-ON and turn-OFF transients during the second pulse in Fig. 12(a). It is observed that the switching voltage $V_{DS}$ has a small overshoot, which is below 11% of the dc-link voltage. For the switching current, the measured *di/dt* during the turn-ON and turn-OFF transients are around 2 kA/$\mu$s and 6.5 kA/$\mu$s, respectively. The switching loss was derived from the measured

TABLE III
COMPONENTS USED IN THE DOUBLE-PULSE TEST

| Component | Value | Descriptions |
|---|---|---|
| DC-link capacitor | 100 µF, 1.2 kV | Film capacitor from Kyocera AVX |
| Decoupling capacitor | 0.75 µF, 900 V | Ceramic capacitor from TDK |
| DPT inductor | 60 µH | U-shape ferrite core from Hitachi |
| Turn-on gate resistor | 10 Ω, 1 W | SMD resistor from Vishay/Dale |
| Turn-off gate resistor | 5 Ω, 1 W | SMD resistor from Vishay/Dale |
| Gate driver | 5 A | STGAP1S from STMicroelectronics |

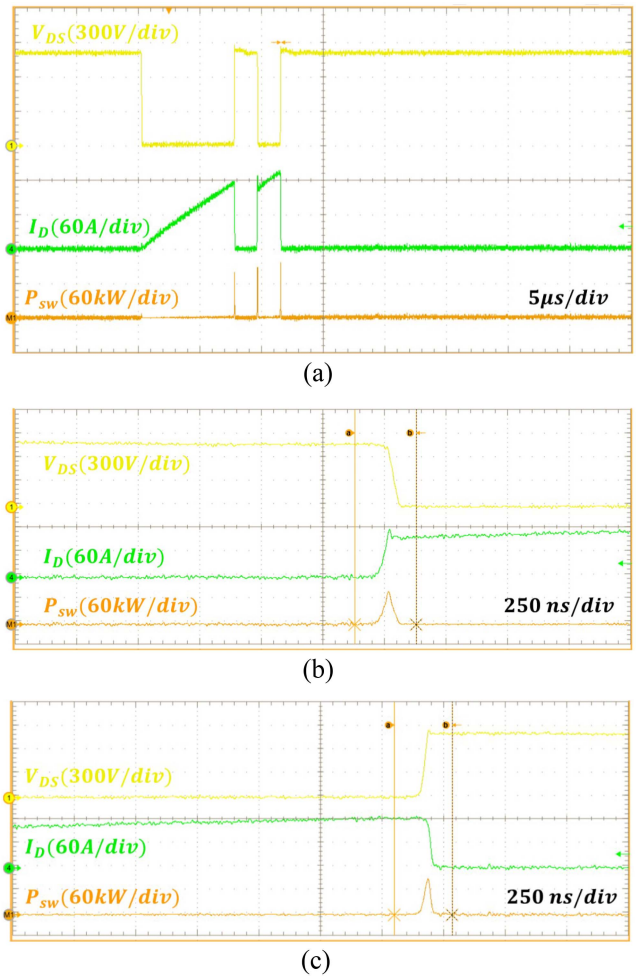



Fig. 12. (a) Waveforms of the voltage $V_{DS}$, the current $I_D$, and the switching loss of the bottom device, (b) magnified view of the turn-ON process of the second pulse, and (c) magnified view of the turn-OFF process of the second pulse.

waveforms of $V_{\mathrm{DS}}$ and $I_D$ by applying the math function in the oscilloscope. The turn-ON and turn-OFF losses calculated by the average function in the oscilloscope are about 3.82 mJ and 3.07 mJ, respectively. The tests were also conducted on five different power modules and the results are shown in Table IV.

TABLE IV
TURN-ON AND TURN-OFF SWITCHING LOSSES OF DIFFERENT FABRICATED POWER MODULES

| Module Sample # | Turn-on loss (mJ) | Turn-off loss (mJ) |
|---|---|---|
| 1 | 3.82 | 3.07 |
| 2 | 4.02 | 3.16 |
| 3 | 4.09 | 3.17 |
| 4 | 3.94 | 3.20 |
| 5 | 4.18 | 3.05 |

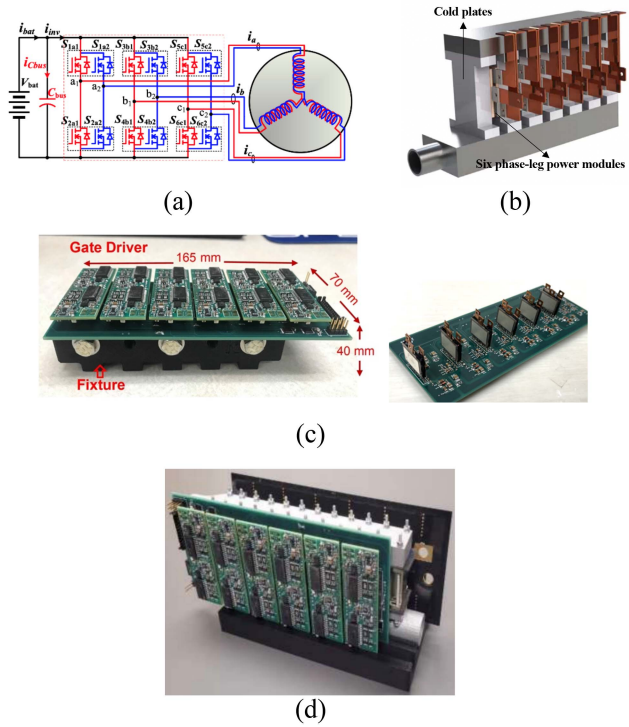



Fig. 13. (a) Schematic of a segmented three-phase inverter, (b) 3-D rendering of six phase-leg power modules sandwiched by cold plates, (c) subassembly with six phase-leg modules mounted on a gate-driver board, and (d) inverter prototype with a power density of 100 kW/L by ORNL [29].

The results were consistent among different DUTs, indicating a consistent device performance and fabrication process of the power modules with sintered-Ag interposers. The fast-switching speed and low switching losses demonstrate the superior performance of SiC devices and the corresponding package structures with low parasitic inductance to support the fast switching of WBG devices.

## IV. SYSTEM INTEGRATION AND POWER DENSITY

To demonstrate the high power density of the traction inverter with the double-side cooled power modules developed in this work, we collaborated with Oak Ridge National Laboratory (ORNL) to fabricate a traction inverter targeting a power density of 100 kW/L as specified by the DOE 2025 [1], [2]. A schematic of the segmented three-phase inverter [28] is shown in Fig. 13(a).

Six of the phase-leg modules were clamped by cold plates as illustrated in Fig. 13(b). The gate driving and current sensing circuit were connected on one side and the dc bus was on the other side. Fig. 13(c) shows a subassembly with six phase-leg modules mounted on a gate-driver board measured at 165 mm $\times$ 70 mm $\times$ 40 mm (0.46 L). The completed demonstration of the traction inverter is shown in Fig. 13(d) with power modules, gate drivers, current sensors, cooling systems, dc bus, capacitors, etc. [29]. The 100-kW segmented inverter was measured at 0.98 L, indicating a high power density of over 100 kW/L. More information on this inverter and other subassemblies will be presented by ORNL.

## V. Conclusion

In prior work, we demonstrated using sintered-Ag interposers instead of solid Cu in a double-side cooled power module to reduce thermomechanical stresses. To further increase the power density and explore the benefits of using the sintered-Ag interposers, we proposed an improved half-bridge module layout with two devices on two substrates facing up and down. Compared to the previous design with two devices on the same substrate, the power-loop parasitic inductance was reduced by 23%, the power handling capability was improved by 44%, and the thermomechanical stress reduction remained similar. The electrical characterization at elevated temperatures and the switching testing validated the functionalities of the power modules and the superior performance of SiC devices aiming for high-temperature and fast switching. The steady-state thermal characterization demonstrated the module has excellent power handling capability with a junction-to-fluid thermal resistance of 0.76 °C/W. Six of the double-side cooled power modules with sintered-Ag interposers were assembled into a traction inverter in collaboration with ORNL, featuring a high power density of over 100 kW/L.

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## References

[1] U.S. Drive, "Electrical and electronics technical team roadmap," Partnership Plan, Roadmaps, Other Documents, Dept. Energy, Washington, DC, USA, 2013.

[2] M. Liu, A. Coppola, M. Alvi, and M. Anwar, "Comprehensive review and state of development of double-sided cooled package technology for automotive power modules," *IEEE Open J. Power Electron.*, vol. 3, pp. 271–289, 2022.

[3] H. Lee, V. Smet, and R. Tummala, "A review of SiC power module packaging technologies: Challenges, advances, and emerging issues," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 239–255, Mar. 2020.

[4] Y. Yang, L. Dorn-Gomba, R. Rodriguez, C. Mak, and A. Emadi, "Automotive power module packaging: Current status and future trends," *IEEE Access*, vol. 8, pp. 160126–160144, 2020.

[5] S. Haque et al., "An innovative technique for packaging power electronic building blocks using metal posts interconnected parallel plate structures," *IEEE Trans. Adv. Packag.*, vol. 22, no. 2, pp. 136–144, May 1999.

[6] L. Ménager, M. Soueidan, B. Allard, V. Bley, and B. Schlegel, "A lab-scale alternative interconnection solution of semiconductor dice compatible with power modules 3-D integration," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1667–1670, Jul. 2010.

[7] R. A. Beaupre, A. V. Gowda, L. D. J. Stevanovic, and S. A. Solovitz, "Double side cooled power module with power overlay," U.S. Patent 8,358,000, Jan. 22, 2013.

[8] E. Vagnon, P.-O. Jeannin, J.-C. Crebier, and Y. Avenas, "A bus-bar-like power module based on three-dimensional power-chip-on-chip hybrid integration," *IEEE Trans. Ind. Appl.*, vol. 46, no. 5, pp. 2046–2055, Sep./Oct. 2010.

[9] C. DiMarino et al., "Design and experimental validation of a wire-bondless 10-kV SiC MOSFET power module," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 381–394, Mar. 2020.

[10] M. Wang et al., "Reliability improvement of a double-sided IGBT module by lowering stress gradient using molybdenum buffers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1637–1648, Sep. 2019.

[11] J. Li, A. Castellazzi, T. Dai, M. Corfield, A. K. Solomon, and C. M. Johnson, "Built-in reliability design of highly integrated solid-state power switches with metal bump interconnects," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2587–2600, May 2015.

[12] X. Cao, G.-Q. Lu, and K. D. T. Ngo, "Planar power module with low thermal impedance and low thermomechanical stress," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 2, no. 8, pp. 1247–1259, Aug. 2012.

[13] J. Jeon, J. Seong, J. Lim, M. K. Kim, T. Kim, and S. W. Yoon, "Finite element and experimental analysis of spacer designs for reducing thermomechanical stress in double-sided cooling power modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 3883–3891, Aug. 2021.

[14] G.-Q. Lu, D. Berry, and Y. Mei, "Methods and apparatus for connecting planar power electronics devices," U.S. Patent 13/889,017, Nov. 7, 2013.

[15] C. Ding, H. Liu, K. D. T. Ngo, R. Burgos, and G.-Q. Lu, "A double-side cooled SiC MOSFET power module with sintered-silver interposers: I-design, simulation, fabrication, and performance characterization," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11672–11680, Oct. 2021.

[16] P. Ning et al., "SiC wirebond multi-chip phase-leg module packaging design and testing for harsh environment," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 16–23, Jan. 2010.

[17] P. Ning, T. G. Lei, F. Wang, G.-Q. Lu, K. D. T. Ngo, and K. Rajashekara, "A novel high-temperature planar package for SiC multichip phase-leg power module," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2059–2067, Aug. 2010.

[18] Z. Chen et al., "Development of a 1200 V, 120 A SiC MOSFET module for high-temperature and high-frequency applications," in *Proc. 1st IEEE Workshop Wide Bandgap Power Devices Appl.*, 2013, pp. 52–59.

[19] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, May 2014.

[20] R. Wang, Z. Chen, D. Boroyevich, L. Jiang, Y. Yao, and K. Rajashekara, "A novel hybrid packaging structure for high-temperature SiC power modules," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1609–1618, Jul./Aug. 2013.

[21] M. Horio, Y. Iizuka, Y. Ikeda, E. Mochizuki, and Y. Takahashi, "Ultra compact and high reliable SiC MOSFET power module with 200 °C operating capability," in *Proc. 24th Int. Symp. Power Semicond. Devices ICs*, 2012, pp. 81–84.

[22] D.-J. Yu, X. Chen, G. Chen, G.-Q. Lu, and Z.-Q. Wang, "Applying Anand model to low-temperature sintered nanoscale silver paste chip attachment," *Mater. Des.*, vol. 30, no. 10, pp. 4574–4579, 2009.

[23] X. Cao, T. Wang, K. D. T. Ngo, and G.-Q. Lu, "Parametric study of joint height for a medium-voltage planar package," *IEEE Trans. Compon. Packag. Technol.*, vol. 33, no. 3, pp. 553–562, Sep. 2010.

[24] Y. Yao, Z. Chen, G.-Q. Lu, D. Boroyevich, and K. D. T. Ngo, "Characterization of encapsulants for high-voltage high-temperature power electronic packaging," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 2, no. 4, pp. 539–547, Apr. 2012.

[25] Y. Yao, G.-Q. Lu, D. Boroyevich, and K. D. T. Ngo, "Survey of high-temperature polymeric encapsulants for power electronics packaging," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 5, no. 2, pp. 168–181, Feb. 2015.

[26] S. L. Rumyantsev et al., "Channel mobility and on-resistance of vertical double implanted 4H-SiC MOSFETs at elevated temperatures," *Semicond. Sci. Technol.*, vol. 24, no. 7, 2009, Art. no. 075011.

[27] L. Cheng, A. K. Agarwal, S. Dhar, S.-H. Ryu, and J. W. Palmour, "Static performance of 20 A, 1200 V 4H-SiC power MOSFETs at temperatures of −187 °C to 300 °C," *J. Electron. Mater.*, vol. 41, no. 5, pp. 910–914, 2012.

[28] I. Husain et al., "Electric drive technology trends, challenges, and opportunities for future electric vehicles," *Proc. Inst. Electr. Electron. Eng.*, vol. 109, no. 6, pp. 1039–1059, Jun. 2021.

[29] G.-J. Su, "High-voltage, high-power density traction drive inverter," 2022 U.S DOE Veh. Technol. Office Annu. Merit Rev., Oak Ridge Nat. Lab., Jun. 21, 2022.