Avalanche Dynamics Model of SiC MOSFET Considering Thermal Runaway Phenomenon

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***Abstract*—A compact SPICE model is proposed in this article, which predicts the avalanche dynamics of the planar SiC MOSFET in high accuracy. Different to the existing models, the proposed model takes the dynamic avalanche resistance into consideration, so the avalanche trajectory in safety state can be accurately simulated. In novelty, the proposed model describes the thermal runaway phenomenon inside the SiC MOSFET, so the avalanche trajectory in failure state can also be correctly simulated. The proposed model is verified in the unclamped inductive switching test, the double pulse test, and the power factor correction converter respectively. The simulation results agree well with the experiment, and good convergence is verified in different SPICE softwares. The proposed model is totally based on the measurements, and no physical information is required. Therefore, the proposed SiC MOSFET model would be favorable for the application engineers to observe the single-pulse avalanche dynamic out of the safe-operating-area.**

***Index Terms*—Avalanche behavior, device model, dynamic characteristic, SiC MOSFET.**

I. Introduction

WITH the rapid development of the power electronics technology, the third-generation SiC MOSFETs have been widely commercialized. The state-of-art SiC MOSFET have lower on-state resistance and faster switching speed than before, which helps the power converters achieve the high efficiency and high power density [1].

Comparing to the manufacturing technology, the modeling technology of the SiC MOSFET is still under developing. For the application engineers, the actual behavior of the devices in the converter is more important than the physical structure of the devices, and an accurate device model is necessary for the simulation and design of the converters [2]. However, the existing models are insufficient in predicting the dynamic behavior of the SiC MOSFETs. On the one hand, the accuracy of the model needs to be improved, and more microeffects should be included in the model [3]. On the other hand, the application scope of the model needs to be enlarged, and the model should be accurate in a wide operating range [4]. Due to the fast switching speed, the SiC MOSFET easily works out of the safe-operating-area (SOA), and the over-voltage or over-current conditions are the main reasons for the device failure [5]. Nevertheless, few existing SiC MOSFET model has the ability to describe the dynamic behavior out of the SOA, then the failure could never be observed during the simulation [6]. Therefore, an improved SiC MOSFET model should be developed to describe the device robustness.

The avalanche dynamic is one of the robustness issues for the SiC MOSFET, where the SiC MOSFET undergoes the over-voltage condition. Once the drain-source voltage exceeds the breakdown value which may reach thousand volts, the avalanche breakdown is occurred in the SiC MOSFET [7]. Such over-voltage induced avalanche dynamic is easily generated due to the parasitic inductance, and the high current slew rate of the SiC MOSFET will worsen the case [8]. The avalanche dynamic could also be caused by the open-circuit failure of the freewheeling diode in the converters. In this case, the energy blocked in the load inductance is forced to release on the device [9]. Moreover, the external surge voltage is another possible cause of the avalanche dynamic of the SiC MOSFET [10]. During the avalanche dynamics, the SiC MOSFET suffers from the high voltage and high current at the same time. An enormous amount of heat is generated inside the device, and an irreversible failure might be occurred [11].

There are already some existing researches, including the avalanche capacity limit of the device [12], [13], the avalanche failure mechanism of the device [14], [15], [16], [17], [18], [19], and the possible methods to improve the avalanche capacity limit of the device [20], [21]. There are different explanations on the avalanche failure mechanism of the planar SiC MOSFET, such as the melting of the metallization on the die surface in [11] and [16], the latch-up of the parasitic bipolar junction transistor (BJT) in [12] and [23]. Although there are some ambiguities in the avalanche failure mechanism, the over-temperature condition is commonly agreed to be the leading cause of the avalanche failure for the planar SiC MOSFET [24], [25], [26]. Besides, the width of the junction field effect transistor region is found to have the significant impact on the avalanche capacity limit of the SiC MOSFET. In [21], the thermal management is proven to be important in avoiding the avalanche failure. However, even if some qualitative analyses are available, no accurate and compact avalanche model that could be employed in the SPICE software has been reported yet.

In this article, a compact SPICE model is developed to predict the single-pulse avalanche dynamics of the planar SiC MOSFET in high accuracy. The model includes five sub-models, namely

Manuscript received 28 December 2022; revised 21 March 2023; accepted 3 May 2023. Date of publication 9 May 2023; date of current version 21 June 2023. This work was supported in part by the National Key R&D Program under Grant 2021YFB2500704 and in part by the Major Project of National Natural Science Foundation of China under Grant 51991384. Recommended for publication by Associate Editor H. Krishnamoorthy. *(Corresponding author: Jianzhong Zhang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3274520.

Digital Object Identifier 10.1109/TPEL.2023.3274520

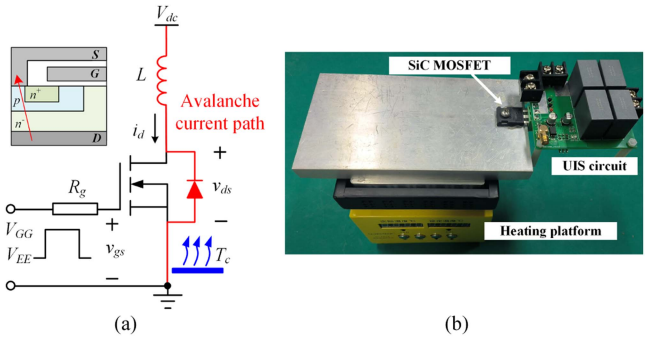


Fig. 1. UIS test setup. (a) Schematic. (b) Prototype.

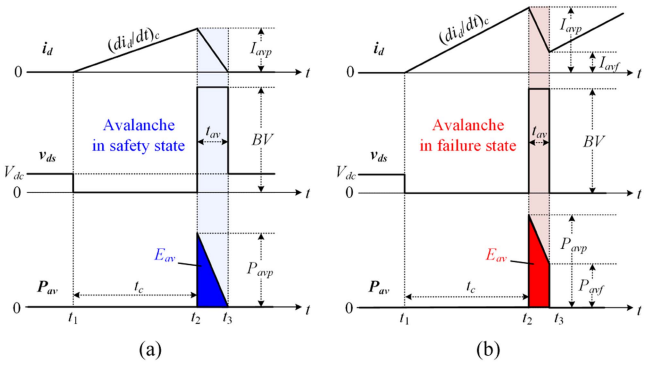


Fig. 2. Simplified avalanche trajectory in (a) safety state; and (b) failure state. Avalanche energy E_{av} is integration of P_{av} from t_2 to t_3.

the breakdown voltage model, the thermal network model, the over-temperature threshold model, the failure delay time model, and the internal resistance model. The innovations of this article include the following.

1) The comprehensive investigation about the avalanche behavior is carried out, and the avalanche capacity limit is analyzed under various slew rate of current, case temperature and negative driving voltage.
2) The detailed model considering the avalanche dynamics is discussed in depth, and all the model parameters are based on the measurements rather than the physical information.
3) The practical implement method of the proposed model in the SPICE software is shown in detail, and the compact sub-circuit structure ensure the good convergence.
4) The relatively complete validations of the proposed model are fulfilled in the unclamped inductive switching (UIS) test, the double pulse test (DPT), and the power factor correction (PFC) converter, respectively.

The rest of this article is organized as follows. In Section II, the avalanche behaviors of the SiC MOSFET are discussed. In Section III, the proposed model considering the avalanche dynamics is shown in detail. In Section IV, the simulation and experiment validations are carried out. Finally, Section V concludes this article.

II. Avalanche Behaviors

The UIS test is generally adopted to test the avalanche behaviors of the SiC MOSFET, as shown in Fig. 1.

In Fig. 1(a), $V_{\rm dc}$ is the bus voltage, L is the load inductance, R_g is the gate driving resistance, V_{GG} is the positive driving voltage, V_{EE} is the negative driving voltage, i_d is the drain current of the SiC MOSFET, v_{gs} and v_{ds} are the gate-source and drain-source voltage of the SiC MOSFET, respectively. The SiC MOSFET C3M0120065D (CREE, 650 V/120 mΩ, planar-gate) [22] is selected in this article. $V_{\rm dc}$ is 100 V, R_g is 10 Ω, V_{GG} is 20 V and other parameters are adjustable. The case temperature T_c of the SiC MOSFET is controlled by the heating platform.

The avalanche trajectory could be used to describe the avalanche behaviors of the SiC MOSFET. Fig. 2(a) shows the simplified avalanche trajectory in safety state. In the duration (t_1, t_2), the SiC MOSFET is turned on, and the i_d rises up with a certain slew rate $(di_d/dt)_c$. The charging time of L is defined as t_c. At the moment t_2, the SiC MOSFET is turned off, and the SiC MOSFET enters the avalanche dynamic (t_2, t_3). In this duration, the voltage across L is reversed, and a large number of electron-hole pairs are generated by the high impact-ionization inside the SiC MOSFET. So v_{ds} of the SiC MOSFET rises up to the breakdown voltage BV, and the body diode of the SiC MOSFET conducts the avalanche current from the drain to source. The avalanche current at the moment t_2 is defined as I_{avp}, and the avalanche time is defined as t_{av}. At the moment t_3, the energy blocked in L is totally released, so the avalanche dynamic is over and v_{ds} rises back to V_{dc}. The avalanche power P_{av} shows a triangular shape with the peak value P_{avp}. The avalanche energy of the SiC MOSFET during the avalanche dynamic is defined as E_{av}, and it has

$$E_{av} = \int_{t_2}^{t_3} v_{ds} i_d dt \tag{1}$$

where the avalanche energy E_{av} equals the integration of the avalanche power P_{av} in the duration (t_2, t_3).

By extending the charging time t_c, the thermal runaway phenomena will be occurred in the SiC MOSFET if I_{avp} is high enough. Fig. 2(b) shows the simplified avalanche trajectory of the SiC MOSFET in failure state. At the moment t_3, the SiC MOSFET cannot survive the serious shock induced by the avalanche energy. So the thermal runaway phenomenon is observed in the SiC MOSFET, and the device is short-circuited which leads to the drain current i_d rising up again at the time t_3. The drain current i_d and the avalanche power P_{av} at t_3 are defined as I_{avf} and P_{avf}, respectively. Different to the avalanche in safety state, the power P_{av} in failure state shows a trapezoidal shape.

Fig. 3 shows the tested avalanche trajectories of the SiC MOSFET, where the BV has the obvious fluctuations instead of constant value shown in Fig. 2. This phenomenon is related to the junction temperature and the avalanche resistance. Moreover, after the moment t_3, the voltage v_{ds} cannot directly go back to $V_{\rm dc}$. A negative bias and oscillation could be found in v_{ds}. This is because the output capacitance C_{oss} of the SiC MOSFET will discharge when v_{ds} decreases from BV, and the discharging current through L cannot disappear abruptly. So, v_{ds} will be clamped at a negative bias by the body diode for a while, then an oscillation induced by L and C_{oss} is observed.

The relationship between the avalanche trajectory and the SOA is shown in Fig. 4(a), where the SOA is given by the datasheet of the CREE device C3M0120065D. It is obvious

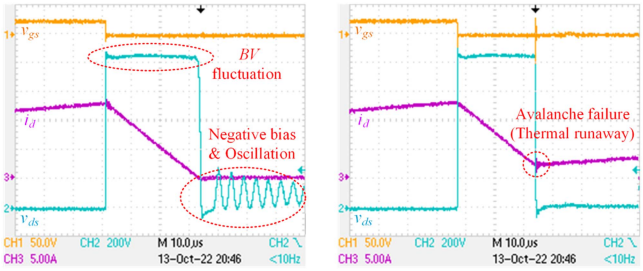


Fig. 3. Tested avalanche trajectory in (a) safety state; and (b) failure state ($T_c = 25$ °C, $L = 2$ mH, $V_{EE} = -4$ V).

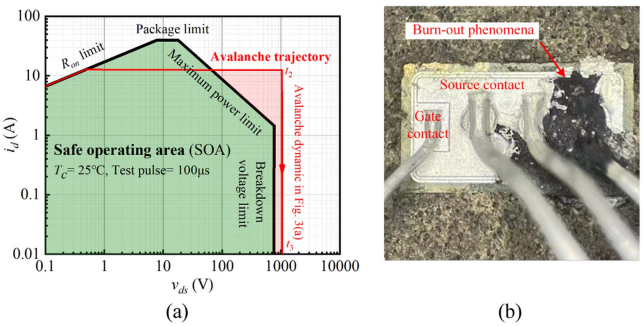


Fig. 4. Avalanche behaviors of SiC MOSFET. (a) Avalanche trajectory and SOA. (b) Decapsulated device.

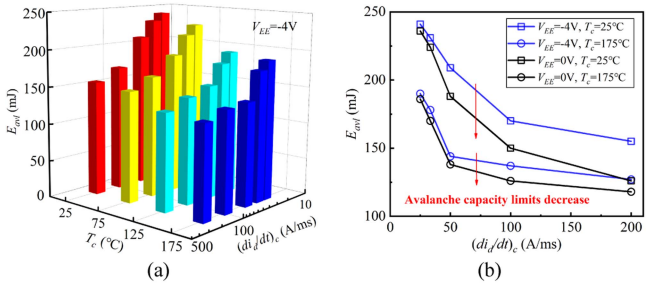


Fig. 5. Avalanche capacity limit with various (a) $(di_d/dt)_c$ and T_c. (b) V_{EE}.

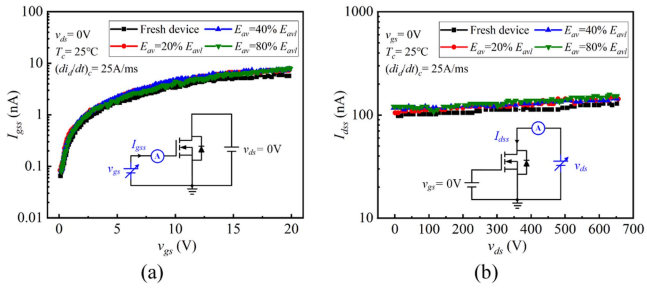


Fig. 6. Leakage current after avalanche in safety state. (a) I_{gss}. (b) I_{dss}.

that the avalanche trajectory is out of the SOA. On the one hand, the avalanche trajectory breaks the breakdown voltage limit, which means the over-voltage condition. On the other hand, the avalanche trajectory breaks the maximum power limit, which means the over-temperature condition. Once the junction temperature T_j of the SiC MOSFET exceeds the limit, the thermal runaway phenomenon would be occurred. Fig. 4(b) shows the decapsulated device, whose avalanche trajectory in failure state is tested shown as Fig. 3(b). The obvious burn-out phenomenon can be seen on the source contact, while the gate contact remains intact.

It is valuable to find the avalanche capacity limit, which describes the ultimate ability of the SiC MOSFET to withstand the avalanche shock. As shown in Fig. 2(a), almost all the energy blocked in L is dissipated by the SiC MOSFET in safety state. In the duration (t_1, t_2), the slew rate of i_d and the value of I_{avp} can be expressed as

$$\left(\frac{di_d}{dt}\right)_c = \frac{V_{\rm dc}}{L} \tag{2}$$

$$I_{avp} = \left(\frac{di_d}{dt}\right)_c t_c. \tag{3}$$

So, the energy blocked in the L at t_2 can be calculated as

$$E_L = \frac{1}{2}LI_{avp}^2 = \frac{1}{2}V_{\rm dc}\left(\frac{di_d}{dt}\right)_c t_c^2. \tag{4}$$

Fig. 2(b) shows the energy E_L is related to the avalanche failure of the SiC MOSFET and the avalanche capacity limit is associated with the energy E_L leading to the avalanche failure. In this article, the avalanche capacity limit E_{avl} is defined as the avalanche energy in the last UIS test before the avalanche failure. It should be noted that the case temperature T_c, the current slew rate $(di_d/dt)_c$ and the driving voltage V_{EE} have the significant impacts on E_{avl}, as shown in Fig. 5. Fig. 5 shows the tested E_{avl} on the SiC MOSFET samples, where the charging time t_c increases in the step of 1 μs until the avalanche failure is occurred. The adjustment of $(di_d/dt)_c$ is fulfilled by changing the inductance L according to (2). At the condition of the dc-bus voltage $V_{\rm dc} =$ 100 V, the load inductance L is selected as 4, 3, 2, 1, 0.5 mH, respectively, which is correspond to the $(di_d/dt)_c$ at the value 25, 33.3, 50, 100, 200 A/ms, respectively.

Fig. 5(a) shows that the avalanche capacity limit E_{avl} decreases as $(di_d/dt)_c$ increases. This is due to the large $(di_d/dt)_c$ causing enlarged E_L which accelerates the avalanche failure according to (4). Meanwhile, E_{avl} decreases with T_c increases. It is understandable that higher case temperature will increase the junction temperature of the SiC MOSFET. Moreover, E_{avl} is slightly decreased when the negative driving voltage is replaced by the zero driving voltage, as shown in Fig. 5(b). Therefore, when the limit E_{avl} is adopted to describe the ability of the SiC MOSFET to withstand the avalanche shock, the variables $(di_d/dt)_c$, T_c and V_{EE} must be specified. Obviously, an accurate model considering the avalanche dynamics is of vital for the industrial applications of the SiC MOSFET.

Fig. 6 shows the gate-source leakage current I_{gss} and the drain-source leakage current I_{dss} of the planar device C3M0120065D after the single-pulse avalanche dynamic in safety state ($T_c =$ 25 °C, $(di_d/dt)_c = 25$ A/ms, $V_{EE} = -4$ V), where the avalanche energy E_{av} varies from 20% to 80% of the avalanche capacity limit E_{avl}. In order to reduce the accumulation effects, each

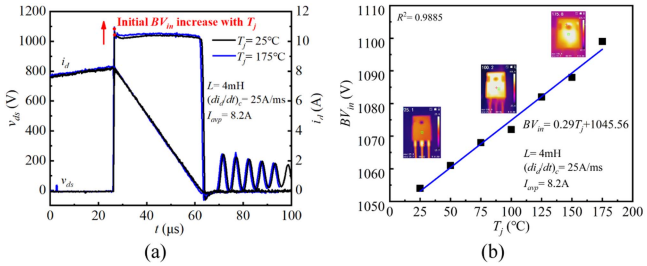


Fig. 7. Junction temperature impact on BV. (a) Avalanche trajectory with different T_j. (b) Fitting result of relation between BV_{in} and T_j.

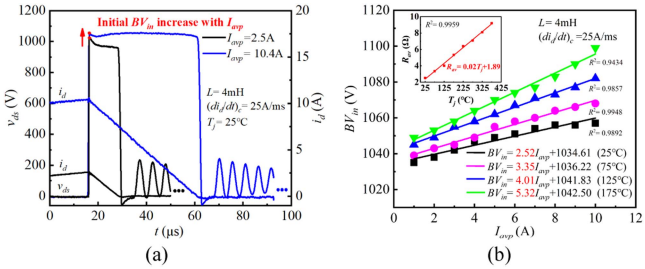


Fig. 8. BV characteristics. (a) Avalanche trajectory with different I_{avp}. (b) Fitting result of $BV_{\rm in}$ with different I_{avp} and T_j.

avalanche test is started from a fresh device. Fig. 6(a) shows that I_{gss} keeps stable below 10 nA and a good insulation between the gate and source is existed after the avalanche dynamic. This is because that the gate oxide of the planar device is well protected by the p-well. It is shown in Fig. 6(b) that I_{dss} remains around 100 nA with the increasing of E_{av}. The good insulation between the drain and source is due to the good robustness of the body diode during the avalanche dynamic, where the mature technology in material epitaxy growth reduces the device defects greatly.

III. Proposed Model

It is mentioned in Section I that five submodels, the breakdown voltage model, the thermal network model, the over-temperature threshold model, the failure delay time model and the internal resistance model are included in the developed compact SPICE model considering avalanche dynamics. In the following sub-sections, the SiC MOSFET C3M0120065D (CREE, 650 V/120 mΩ) is studied and all the model parameters are based on the UIS test. It should be noted that the datasheet recommended $V_{EE} = -4$ V is chosen in the following tests. The proposed model for other planar SiC MOSFETs is available as long as the test device is replaced.

A. Breakdown Voltage

It is widely known that the breakdown voltage BV is positively sensitive to the temperature [7]. Defining the initial breakdown voltage at the moment t_2 as $BV_{\rm in}$, it can be seen from Fig. 7(a) that $BV_{\rm in}$ increases with the increasing T_j under constant $(di_d/dt)_c$ and I_{avp}. In the existing models of the breakdown voltage BV, $BV(T_j)$ is considered as the unary function of T_j. Fig. 7(b) shows the curve fitting result of $BV(T_j)$ based on the measurement, where the function has only single variable. Actually, the drain current in avalanche dynamics also has the significant impacts on BV. Fig. 8(a) shows the test results on the UIS test, where $BV_{\rm in}$ goes higher as I_{avp} increases from 2.5 A to 10.4 A. This is due to the effect of the avalanche resistance R_{av} which has voltage drop and enhances the value of BV. Fig. 8(b) gives the relation between $BV_{\rm in}$ and I_{avp}, where R_{av} of the SiC MOSFET is about 2.52 Ω at the junction temperature $T_j = 25$ °C. It is much larger than the on-state resistance ($R_{on} = 120$ mΩ), and R_{av} obviously increases as T_j increasing. R_{av} at $T_j = 175$ °C is 5.32 Ω, which is more than twice of that at $T_j = 25$ °C. Fig. 8(b) shows the positive temperature sensitivity of R_{av}.

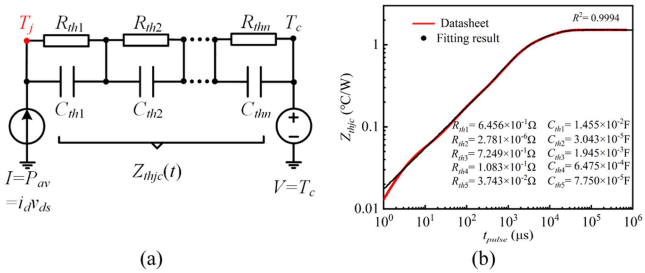


Fig. 9. Foster thermal network. (a) Thermal network structure. (b) Fitting result of transient thermal impedance curve in datasheet.

During the avalanche dynamics, the drain current i_d of the SiC MOSFET varies continuously. Considering the breakdown voltage BV is simultaneously influenced by T_j and i_d during the avalanche dynamic, the breakdown voltage could be established as

$$BV(i_d, T_j) = \underbrace{(aT_j + b)}_{R_{av}(T_j)} i_d + cT_j + d \tag{5}$$

where a, b, c, and d are the undermined coefficients. In (5), the coefficients can be determined based on the data in Fig. 8, where the avalanche current I_{avp} and $BV_{\rm in}$ at moment t_2 are used to describe the BV characteristics. In this article, a is 0.02, b is 1.89, c is 0.126, d is 1012.

B. Thermal Network

The thermal network model plays an important role in the estimation of T_j. In this article, the Forster thermal network model is chosen to obtain T_j, as shown in Fig. 9. The junction temperature T_j can be calculated as

$$T_j = T_c + Z_{thjc}(t) P_{av} \tag{6}$$

where $Z_{thjc}(t)$ is the transient thermal impedance, and it has

$$Z_{thjc}(t) = \sum_{i=0}^{n} R_{thi} \left(1 - e^{-\frac{t}{R_{thi} C_{thi}}}\right) \tag{7}$$

where R_{thi} and C_{thi} ($i = 0, 1, \ldots, n$) are distributed resistance and capacitance of the network, respectively. Fig. 9(b) shows the transient thermal impedance of the device C3M0120065D provided in the datasheet and the fitting results of the transient

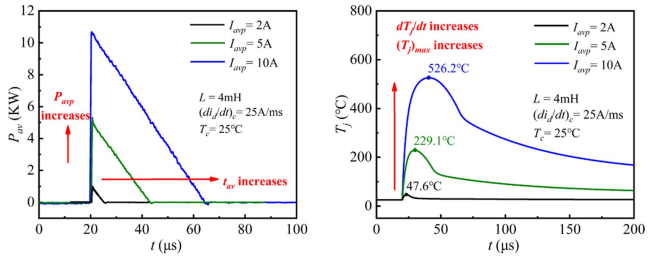


Fig. 10. Impact of avalanche current peak I_{avp} on (a) P_{av} trajectory and (b) T_j trajectory.

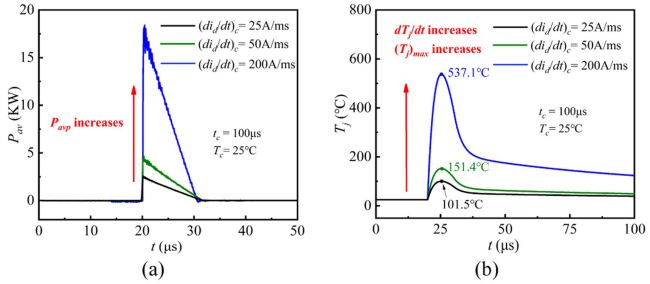


Fig. 11. Impact of charging current slew rate $(di_d/dt)_c$ on (a) P_{av} trajectory and (b) T_j trajectory.

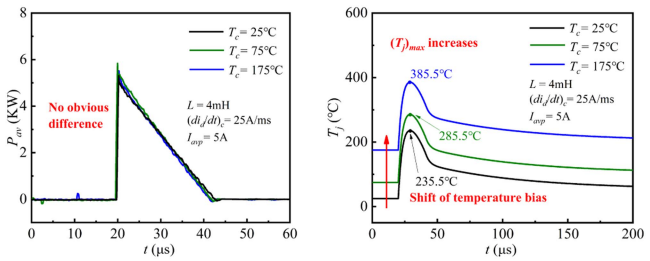


Fig. 12. Impact of case temperature T_c on (a) P_{av} trajectory and (b) T_j trajectory.

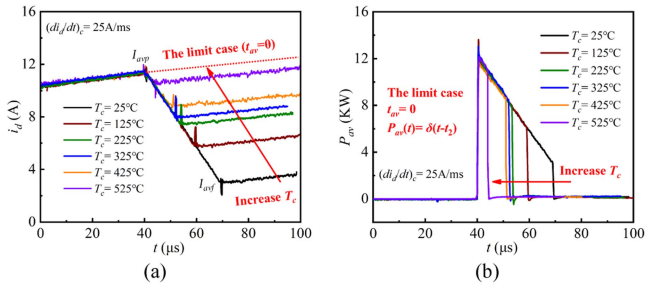


Fig. 13. Impact of T_c on (a) i_d trajectory and (b) P_{av} trajectory (failure state).

thermal impedance. It can be seen from Fig. 9(b) that the fifth-order thermal network model is accurate enough.

Based on the thermal network, the dynamic T_j can be observed in real-time. Fig. 10 shows the observed junction temperature of the SiC MOSFET C3M0120065D under various I_{avp}. In Fig. 10(a), the peak value of P_{av} goes higher as I_{avp} increases, which means that the SiC MOSFET should tolerate more serious avalanche shock. Fig. 10(b) shows both the slew rate and the peak value of T_j obviously increasing as enlarged I_{avp}. Once T_j exceeds the limit of the device, the thermal runaway phenomena would be occurred.

Fig. 11 shows the junction temperature of the SiC MOSFET under various $(di_d/dt)_c$. It can be seen in Fig. 11(a) that P_{avp} is significantly enlarged as $(di_d/dt)_c$ increases. The temperature differential dT_j/dt and temperature peak $(T_j)_{\max}$ become higher with the large $(di_d/dt)_c$, as shown in Fig. 11(b). It explains that the avalanche capacity limit E_{avl} decreases with larger $(di_d/dt)_c$, as shown in Fig. 5(a). This is due to the obvious rising of the junction temperature with higher $(di_d/dt)_c$.

The impacts of T_c on the SiC MOSFET are shown in Fig. 12, where the shape of P_{av} is almost unchanged with various T_c. In Fig. 12(b), it is shown that the curve of T_j shifts up in parallel as T_c increasing. So the limit E_{avl} decreases according to the increase of T_c shown as Fig. 5(a), which is due to the higher T_j at large T_c. Therefore, the heat dissipation is essential to improve the avalanche capacity limit of the SiC MOSFET.

C. Over-Temperature Threshold

It is commonly agreed that the avalanche failure is caused by the over-temperature inside the SiC MOSFET during the avalanche dynamics. Then it is important to estimate the over-temperature threshold T_{jl} of the SiC MOSFET. In the traditional model, T_{jl} equals the melting point of the aluminum (660 °C), which deviates from the actual situation. In modern manufacturing art, the alloy is widely applied in the surface contact of the SiC MOSFET, and the melting point of the alloy would be below 660 °C. Furthermore, the parasitic BJT might be activated at T_j below 660 °C, and the avalanche failure might not strictly synchronize with the melting of the surface contact. In order to obtain T_{jl} of the SiC MOSFET, the extrapolation method is applied to the over-temperature threshold model. The detailed process is described as follows.

First step, the SiC MOSFET is externally heated by the heating platform for several minutes, and this sufficient heating time ensures the junction temperature T_j equals to the case temperature T_c. Second step, the SiC MOSFET is switched OFF when the peak avalanche current I_{avp} is large enough for entering failure state. And the avalanche time t_{av} is recorded. Third step, increasing the case temperature T_c, the first and second steps are repeated and finished until t_{av} is close to zero.

According to (6), the junction temperature during the avalanche dynamics is related to P_{av} and t_{av}. If t_{av} is short enough, the increase of T_j during the avalanche dynamics will be trivial. Therefore, T_c at the third step with t_{av} close to zero could be taken as T_{jl}. In the other words, P_{av} with t_{av} close to zero makes limited contribution to T_j, and T_c directly leads to the thermal runaway phenomenon of the SiC MOSFET.

Fig. 13(a) shows i_d trajectory of failure state under various T_c. The avalanche time t_{av} decreases as T_c increases, and I_{avf} gets closer to I_{avp}. At the case with t_{av} close to zero, the points of I_{avf} and I_{avp} are overlapped, and it has $T_{jl} = T_c$. Fig. 13(b) shows P_{av} trajectory of failure state, where the amplitude of the P_{av} trapezoid decreases if T_c increases. At the case with $t_{av} =$

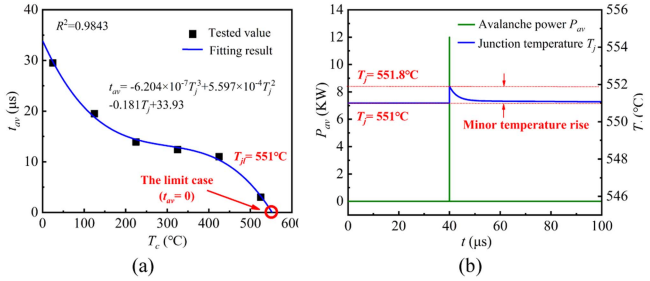


Fig. 14. Over-temperature threshold. (a) Fitting result of relation between t_{av} and T_c. (b) Simulation result when t_{av} is close to zero.

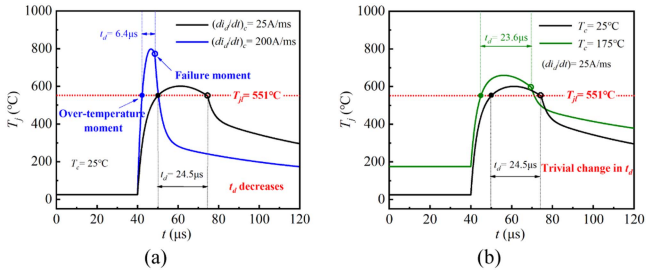


Fig. 15. T_j trajectory of failure state with different (a) $(di_d/dt)_c$ and (b) T_c.

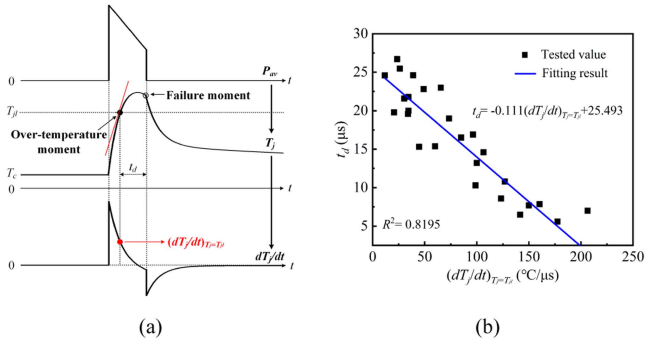


Fig. 16. Failure delay time. (a) Definition of T_j differential. (b) Fitting result of relation between t_d and $(di_d/dt)_c$.

0, P_{av} could be considered as an impulse function, which has an extremely short operating time and a great intensity.

Fig. 14(a) shows the tested data reflecting the relation between t_{av} and T_c. It could be fitting by the unary cubic function as

$$t_{av}(T_c) = eT_c^3 + fT_c^2 + gT_c + h \tag{8}$$

where e, f, g, h are the coefficients of the fitting function. In Fig. 14(a), the coefficients e, f, g, h of the tested MOSFET are $-6.2 \times 10^{-7}, 5.6 \times 10^{-4}, -0.18, 33.93$, respectively. Supposing t_{av} is zero, T_{jl} could be approximately estimated as 551 °C by (8).

Fig. 14(b) shows the simulation results of the over-temperature threshold by using the thermal network model shown in Fig. 9, where an isosceles triangle current source (12 000 A, 100 ns) is adopted to emulate the impulse function of P_{av}. Only minor temperature rising within 1 °C is observed when P_{av} is close to the impulse function. So the extrapolated T_{jl} is reasonable, because the temperature rising caused by P_{av} has been effectively excluded. It should be noted that T_{jl} is the lowest limit value of the avalanche failure. The SiC MOSFET is heated externally with the stable temperature in the modeling process, but in the industrial applications, the SiC MOSFET is self-heated internally for quite short time during the avalanche dynamics. Therefore, both the over-temperature conditions with (T_j>T_{jl}) and sufficient time should be guaranteed when modeling the avalanche failure of the SiC MOSFET.

D. Failure Delay Time

The avalanche failure of the SiC MOSFET is not abruptly occurred when T_j exceeds T_{jl}, since it takes time for the heat diffusion in the device cells or the burn-out of the surface metallization requires certain time. Defining the duration from the over-temperature moment ($T_j = T_{jl}$) to the failure moment as the failure delay time t_d, the modeling of t_d is as follows.

Fig. 15(a) shows T_j trajectory of failure state with various $(di_d/dt)_c$ where T_c is fixed at 25 °C. Obviously, the avalanche failure is not immediately occurred at the moment of over-temperature. It takes a certain time t_d from the over-temperature moment to the failure moment. As $(di_d/dt)_c$ increases from 25 to 200 A/ms, t_d decreases from 24.5 to 6.4 μs. The high $(di_d/dt)_c$ leads to the high dT_j/dt, then the higher dT_j/dt leads to the shorter t_d. So the faster avalanche failure is observed. Fig. 15(b) shows T_j trajectory of failure state with various T_c as $(di_d/dt)_c$ is fixed at 25 A/ms. It is shown that the increase of T_c only slightly contributes to the decrease of t_d. So the bias of T_j has limited influence on t_d. Based on the above analysis, dT_j/dt at the over-temperature moment is a good independent variable to describe the variable t_d.

Fig. 16(a) shows the independent variable $(dT_j/dt)_{Tj} = {}_{Tjl}$, namely the slew rate of T_j at the over-temperature moment. In this article, T_j trajectory is obtained meantime when evaluating the avalanche capacity limit of the SiC MOSFET shown in Fig. 5(a). And the relation between $(dT_j/dt)_{Tj} = {}_{Tjl}$ and t_d is shown in Fig. 16(b). It is obvious that the higher $(dT_j/dt)_{Tj} = {}_{Tjl}$ would lead to the lower t_d, and the relation could be fitting by

$$t_d(x) = mx + n \quad x = (dT_j/dt)_{T_j=T_{jl}} \tag{9}$$

where m and n is the undetermined slope and the intercept of the fitting function. In this article, m is -0.111 and n is 25.493. The local disorder of the data is due to the manufacturing differences between the samples.

E. Internal Resistance

The avalanche failure will result to short-circuit between the terminals of the SiC MOSFET, and then the device is uncontrollable and has a resistance feature. Certain resistance between terminals is called internal resistance and it is important to evaluate its real value after the happening of the avalanche failure. The internal resistance could be modeled by the measured resistance between the terminals, where R_{gs1}, R_{gd1}, and R_{ds1} are the measured resistance between gate and source, gate and drain,

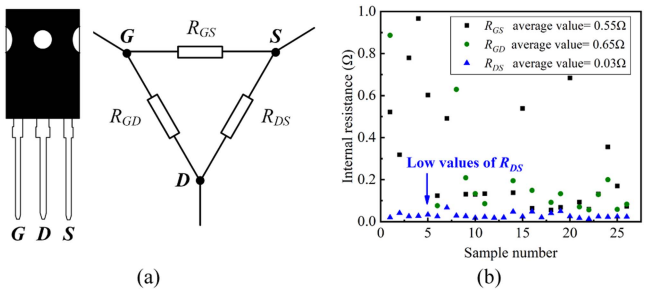


Fig. 17. Internal resistance. (a) Connection form. (b) Measured values of internal resistance for failure samples.

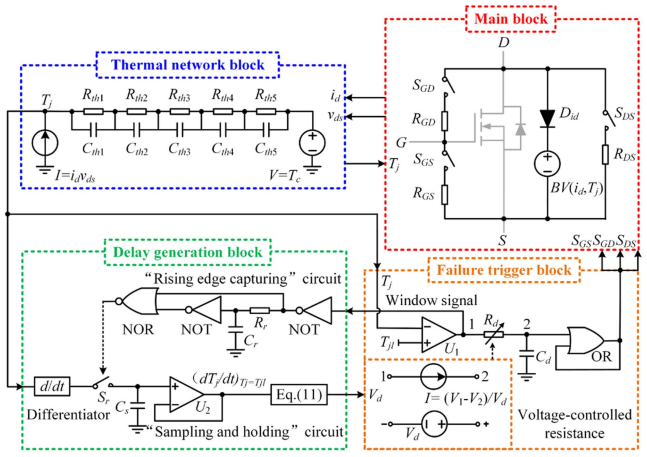


Fig. 18. Structure of general SPICE model.

drain and source with the third terminal floating, respectively. Since the internal resistances R_{GS}, R_{GD}, and R_{DS} are connected in a triangle shape inside the SiC MOSFET, as shown in Fig. 17(a), the internal resistances should be transformed from the measured resistances as

$$\begin{cases} R_{GS} = \frac{(R_{gs1}+R_{ds1}-R_{gd1})(R_{gs1}+R_{gd1}-R_{ds1})}{2(R_{gd1}+R_{ds1}-R_{gs1})} + R_{gs1} \\ R_{GD} = \frac{(R_{gd1}+R_{ds1}-R_{gs1})(R_{gs1}+R_{gd1}-R_{ds1})}{2(R_{gs1}+R_{ds1}-R_{gd1})} + R_{gd1}. \\ R_{DS} = \frac{(R_{gd1}+R_{ds1}-R_{gs1})(R_{gs1}+R_{ds1}-R_{gd1})}{2(R_{gs1}+R_{gd1}-R_{ds1})} + R_{ds1} \end{cases} \quad (10)$$

Fig. 17(b) shows the internal resistances based on the failure samples. Obviously R_{GS}, R_{GD} and R_{DS} of all the samples are very low, which means the short-circuit is happened inside the SiC MOSFET. Moreover, R_{DS} is lowest one among the three internal resistances, because the avalanche shock is mainly exerted on the *PN* junction between the drain and source. In this article, the average value of each internal resistance is selected for the model, and $R_{GS} = 0.55\ \Omega$, $R_{GD} = 0.65\ \Omega$,and $R_{DS} = 0.03\ \Omega$ are selected for the test MOSFET.

F. Implementation of Proposed Model

The SPICE softwares are widely used for the simulation of power electronic converters, such as Pspice and Simetrix. In this article, five sub-models are effectively embedded into four blocks for all SPICE models. The detailed structure of the general SPICE model is shown in Fig. 18, where the avalanche dynamic model is implemented around the basic model of the manufacturer. The relation between the five sub-models and the four blocks of the general SPICE model is shown in the Table I.

TABLE I
RELATION BETWEEN MODELS AND BLOCKS

Block	Sub-model	Equation
Main block	Breakdown voltage model	(5)
	Internal resistance model	(10)
Thermal network block	Thermal network model	(6), (7)
Failure trigger block	Over-temperature threshold model	(8)
Delay generation block	Failure delay time model	(9), (11)

The main block of the general SPICE model could perform the variations of *BV* and the short-circuit phenomenon after the avalanche failure. The signals S_{GS}, S_{GD}, S_{DS} of the voltage-controlled switches output from the failure trigger block and T_j output from the thermal network block are the inputs of the main block. The outputs of the main block are i_d and v_{ds}. The actual *BV* is decided by the ideal diode D_{id} and the voltage source $BV(i_d, T_j)$. The diode D_{id} ensures v_{ds} equals to $BV(i_d, T_j)$ during the avalanche dynamics. When the avalanche failure is occurred, three internal resistances R_{GS}, R_{GD}, and R_{DS} will be enabled by triggering three switches S_{GS}, S_{GD} and S_{DS}. Then, the SiC MOSFET will be in short-circuited state.

The thermal network block of the general SPICE model could generate T_j, which is required in other three blocks. The inputs of the thermal block are i_d and v_{ds} which come from the main block. The failure trigger block of the general SPICE model could make the SiC MOSFET operate in failure state by triggering the switches S_{GS}, S_{GD}, S_{DS}. The inputs of this block are T_j from the thermal network block and V_d from the delay generation block. The outputs are the voltage-controlled switch signals S_{GS}, S_{GD}, S_{DS}, and the window signal to reflect T_j exceeding T_{jl}. The window signal generated by the comparator U_1 reflects that the over-temperature condition is occurred inside the SiC MOSFET. R_d and C_d form a delay network, and the delay time equals to the failure delay time t_d. The voltage-controlled resistance R_d is determined by V_d from the delay generation block. The OR gate with the feedback function could lock the rising edge of the delayed window signal (point 2). Therefore, once T_j exceeds T_{jl}, S_{GS}, S_{GD} and S_{DS} will be triggered after a certain delay time t_d.

The delay generation block generates the control signal for the voltage-controlled resistance R_d to determine the failure delay time t_d. The inputs of this block include the window signal from the failure trigger block and T_j from the thermal network block. The output of this block is V_d to control R_d of the failure trigger block. Two NOT gates, one NOR gate, R_r and C_r form a "rising edge capturing" circuit. The voltage-controlled switch S_r, the sampling capacitance C_s and the follower U_2 form the "sampling and holding" circuit. When T_j exceeds T_{jl}, the failure trigger block outputs the window signal to the delay generation block. The "rising edge capturing" circuit generates a short pulse synchronizing with the rising edge of the window signal, and this short pulse can trigger S_r. At the same time, a differentiator is applied to calculate the slew rate of T_j. So the "sampling and holding" circuit can record $(dT_j/dt)_{Tj} = {}_{Tjl}$. The delay t_d

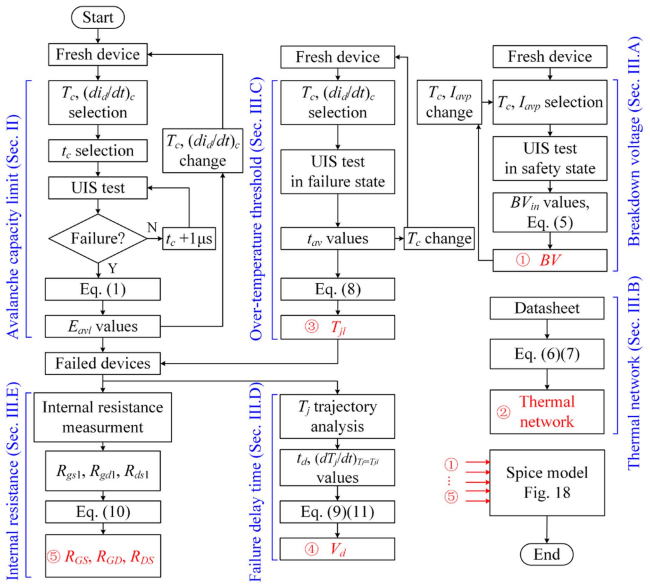


Fig. 19. Flowchart for avalanche dynamic model of SiC MOSFET.

is negatively related to $(dT_j/dt)_{Tj} = {}_{Tjl}$ according to (9). And the voltage-controlled resistance R_d numerically equals to V_d. Therefore, V_d that decides t_d can be determined by

$$V_d = \frac{m\left(\frac{dT_j}{dt}\right)_{T_j=T_{jl}} + n}{0.69C_d} \tag{11}$$

It is obvious that only basic components are adopted in the proposed model shown in Fig. 18. Then good convergence and generality is ensured in the compact SPICE model.

The proposed model requires six tests. The tests in Section III-A and Section III-B are non-destructive. The tests in Section II and Section III-C are destructive, and they provide the failure samples for the tests in Section III-D and Section III-E. In this article, 20 samples are used in Section II, and 6 samples are used in Section III-C. Only one sample is required in Section III-A. Therefore, at least 27 samples are required to setup the proposed model without considering of the screening and misoperation factors. Fig. 19 shows the flowchart for the avalanche dynamic model of the SiC MOSFET.

IV. Validations

In this article, the SPICE model is applied in Pspice16.6, and the computer configuration with Intel Core i5-4.5 GHz, 16 G is adopted. The accuracy and the convergence of the proposed SiC MOSFET model considering the avalanche dynamic is verified in the UIS test, the DPT, and the PFC converter respectively.

A. UIS Test

The traditional model provided by the CREE does not consider the dynamics of the BV and is incapable of describing the thermal runaway phenomena. Fig. 20(a) shows the avalanche trajectory in safety state simulated with the CREE model. The

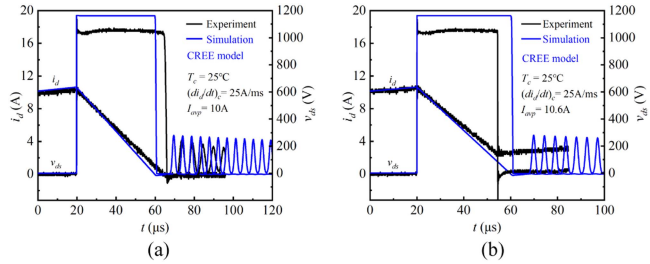


Fig. 20. Avalanche trajectory with CREE model. (a) Avalanche in safety state. (b) Avalanche in failure state.

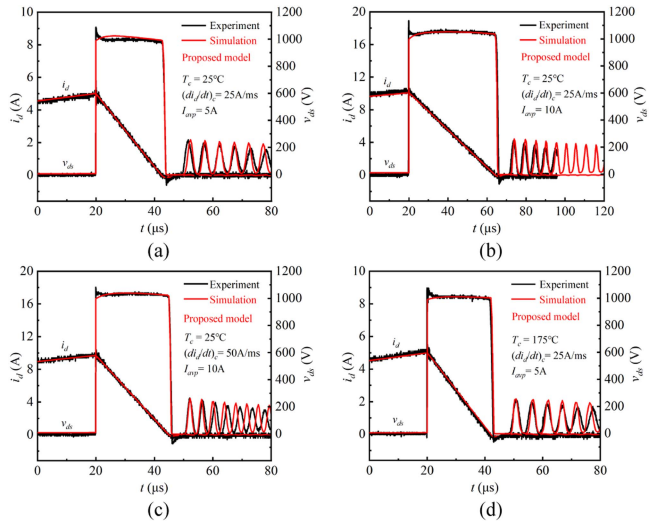


Fig. 21. Avalanche trajectory in safety state with proposed model. (a) T_c = 25 °C, $(di_d/dt)_c$ = 25 A/ms, I_{avp} = 5 A. (b) T_c = 25 °C, $(di_d/dt)_c$ = 25 A/ms, I_{avp} = 10 A. (c) T_c = 25 °C, $(di_d/dt)_c$ = 50 A/ms, I_{avp} = 10 A. (d) T_c = 175 °C, $(di_d/dt)_c$ = 25 A/ms, I_{avp} = 5 A.

obvious errors of the i_d and v_{ds} can be seen between the experiment and the simulation. v_{ds} during the avalanche dynamic is clamped at a fixed value, so t_{av} and E_{av} are not correct in simulation results. Fig. 20(b) shows the avalanche trajectory in failure state simulated by the CREE model. Even if the avalanche failure has been occurred in the experiment of the SiC MOSFET, the CREE model still outputs the avalanche trajectory in safety state. This is unacceptable when evaluating the robustness of the SiC MOSFET.

The proposed model could accurately predict the behaviors of the SiC MOSFET during the avalanche dynamics. Fig. 21 shows the experimental and simulation results of the proposed model when evaluating the avalanche trajectory in safety state. It is obvious that the simulation results agree well with the experiment in different I_{avp}, $(di_d/dt)_c$ and T_c. The BV fluctuation could be clearly observed in the proposed model, which is important for evaluating t_{av} and E_{av}.

Fig. 22 shows the experimental and simulation results of the proposed model under various switching speed, where the gate resistance R_g varies from 1 to 60 Ω. Obviously, the proposed model keeps accurate in a wide switching speed range of the SiC MOSFET.

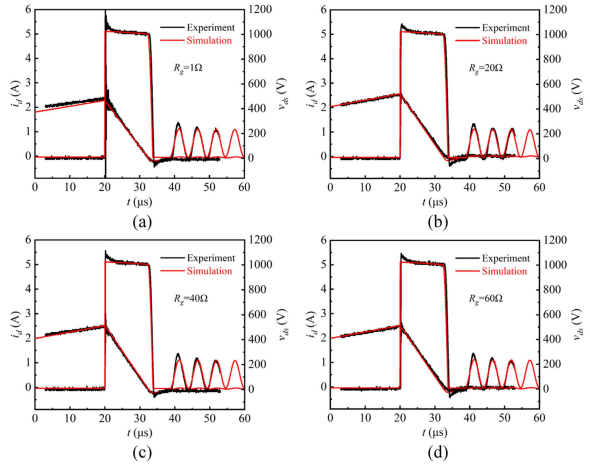


Fig. 22. Avalanche trajectory in safety state with proposed model. $T_c = 25$ °C, $I_{avp} = 2.5$ A, $(di_d/dt)_c = 25$ A/ms. (a) $R_g = 1$ Ω. (b) $R_g = 20$ Ω. (c) $R_g = 40$ Ω. (d) $R_g = 60$ Ω.

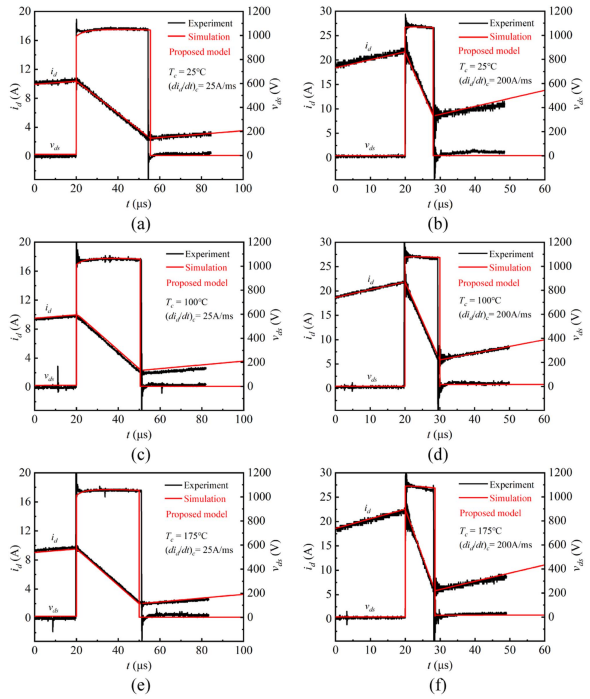


Fig. 23. Avalanche trajectory in failure state with proposed model. (a) $T_c = 25$ °C, $(di_d/dt)_c = 25$ A/ms. (b) $T_c = 25$ °C, $(di_d/dt)_c = 200$ A/ms. (c) $T_c = 100$ °C, $(di_d/dt)_c = 25$ A/ms. (d) $T_c = 100$ °C, $(di_d/dt)_c = 200$ A/ms. (e) $T_c = 175$ °C, $(di_d/dt)_c = 25$ A/ms. $T_c = 175$ °C, $(di_d/dt)_c = 200$ A/ms.

The proposed model is also capable of describing the avalanche failure of the SiC MOSFET. Fig. 23 shows the experimental and simulation results of the proposed model when evaluating the avalanche trajectory in failure state. Obviously, the thermal runaway phenomena after the avalanche failure could be accurately simulated with the proposed model. The error of t_{av} could keep in a low value with different I_{avp}, $(di_d/dt)_c$ and T_c.

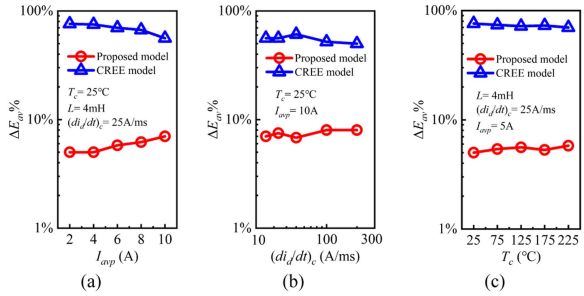


Fig. 24. Comparisons of accuracy with various (a) I_{avp}. (b) $(di_d/dt)_c$. (c) T_c.

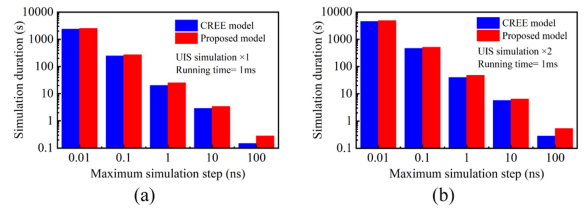


Fig. 25. Convergence validation. (a) One UIS. (b) Two UIS.

Fig. 24 shows the relative errors of the avalanche energy between the simulation and the experiment with different I_{avp}, $(di_d/dt)_c$ and T_c. The relative error of the avalanche energy ΔE_{av}% is expressed as

$$\Delta E_{\text{av}}\% = \left| \frac{E_{\text{av\_exp}} - E_{\text{av\_sim}}}{E_{\text{av\_exp}}} \right| \times 100\% \tag{12}$$

where $E_{\text{av\_exp}}$ and $E_{\text{av\_sim}}$ is the avalanche energy obtained from the experiment and simulation, respectively. It is obvious that the proposed model has higher accuracy than the CREE model in the wide operating range of the SiC MOSFET. Fig. 24(c) shows the proposed model is valid when T_c varies from 25 °C to 175 °C, which is adequate for the common industrial applications.

Fig. 25 shows the simulation durations of the UIS test with the CREE model and the proposed model. Only minor increase in the simulation duration can be seen, when the proposed model replaces the CREE model. So a relatively high simulation speed of the proposed model is validated. Furthermore, even if the maximum simulation step is as short as 0.01 ns, no divergence problem is occurred in the proposed model. Therefore, a good convergence is verified in the proposed model.

B. DPT

The over-voltage condition caused by the parasitic inductance during the switching transient easily makes the SiC MOSFET operate in the avalanche dynamics. In this case, the DPT could be used to test the switching transient of the SiC MOSFET. In this article, the DPT platform is conveniently reformed from the UIS test platform shown in Fig. 1. A SiC Schottky diode C4D40120D (CREE, 1200 V/54 A) is connected in parallel with the load inductance L, so a reverse freewheeling loop is established. The decoupling capacitors on the bus are removed, so the high parasitic inductance is obtained. V_{dc} is selected as 400 V, L is 1 mH, $I_L = 40$ A.

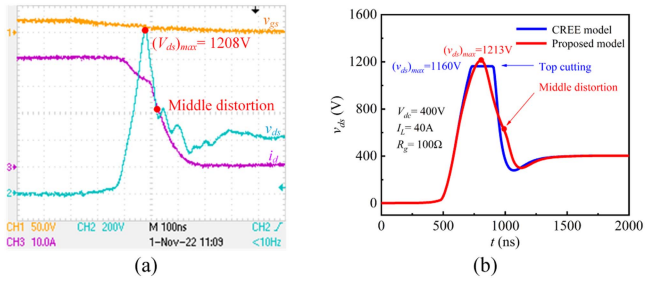


Fig. 26. Turn-OFF transients of DPT. (a) Experiment. (b) Simulation.

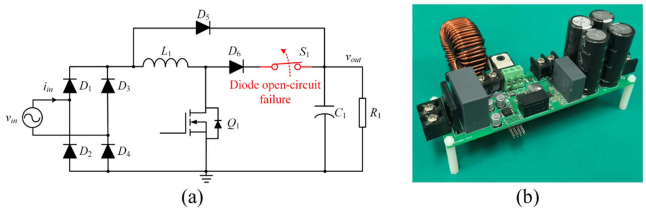


Fig. 27. Single-phase PFC converter. (a) Schematic. (b) Prototype.

Fig. 26 shows the turn-OFF transient of the SiC MOSFET in the experiment. Obviously, a significant voltage-overshoot can be seen, when the load current and the parasitic inductance is high. The maximum value of v_{ds} reaches 1208 V, which is close to the twice of the rated value. It should be noted that a significant distortion is observed around the middle of v_{ds} waveform. This phenomenon shows that the SiC MOSFET operates in the avalanche dynamics. Fig. 26(b) shows the simulation results of v_{ds} waveform with the CREE model and the proposed model. It is obvious that an abnormal top cutting is shown in v_{ds} waveform simulated with the CREE model. This is because of BV seen as a constant in the CREE model. In contrast, the proposed model could well present the shape of v_{ds} waveform. The simulated maximum value of v_{ds} is 1213 V, which is close to the experimental result. Moreover, the middle distortion can also be seen in v_{ds} waveform simulated by the proposed model. This is because the dynamic BV is considered in the proposed model.

C. PFC Converter

In order to verify the performance of the proposed model in an industrial converter, a single-phase PFC converter is fulfilled. The schematic and the prototype of the PFC converter are shown in Fig. 27. In the PFC converter, the surge current may age the wiring bond of the boost diode. Once the wiring bond of the boost diode lifts off from the die, the SiC MOSFET would quickly operate in the avalanche dynamics due to the loss of the freewheeling loop. In order to reproduce this extreme condition, an additional switch S_1 is connected between the boost diode D_6 and the output capacitor C_1 to create the diode open-circuit failure. Thus, the performance of the PFC converter can be investigated in the normal operation or in the avalanche dynamics. The detailed information about the prototype is shown in the Table II.

TABLE II
PARAMETERS OF PFC CONVERTER PROTOTYPE

Name	Denotation	Parameters
Rectifier bridge	D_1~D_4	GBJ2006
Pre-charge diode	D_5	1N5406
Boost diode	D_6	CI15S120M3
SiC MOSFET	Q_1	C3M0120065D
Electric relay	S_1	HF115F/012-2ZS4
Boost inductor	L_1	1 mH
Output capacitor	C_1	400 μF
Load resistor	R_1	530 Ω
Controller	-	UCC28019
Switching frequency	f_{sw}	65 KHz
Input voltage	V_{in}	220 V/50 Hz
Output voltage	V_{out}	400 V

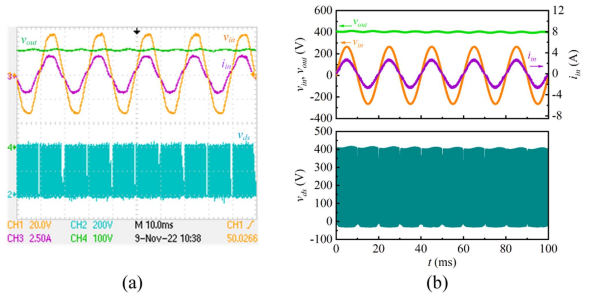


Fig. 28. Steady state of PFC converter. (a) Experiment. (b) Simulation.

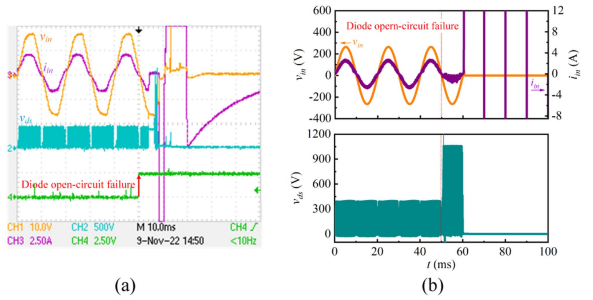
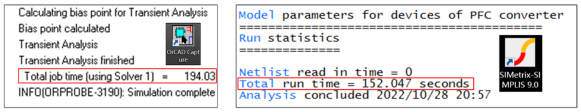


Fig. 29. Transient state of PFC converter. (a) Experiment. (b) Simulation.

Fig. 28 shows the steady sate of the PFC converter in the experiment and the simulation. The converter normally operates in the continuous current conduction mode, and the input current shows a sinusoidal waveform synchronizing with the input voltage. Therefore, a high power factor is obtained. It is obvious that the proposed model works well in the simulation, and the voltage and current waveforms effectively agree with the experiment.

Fig. 29 shows the transient sate of the PFC converter in the experiment and the simulation, where the diode open-circuit failure happens. Obviously, the serious over-voltage is occurred in the SiC MOSFET. The avalanche failure of the SiC MOSFET directly leads to the failure of the PFC converter. As shown in Fig. 29(b), the proposed model could well reflect the extreme operating condition of the converter. Some critical details do correspond to the experiment, such as the divergence of the input current i_{in}, the pulling down of the input voltage $v_{\rm in}$ and the

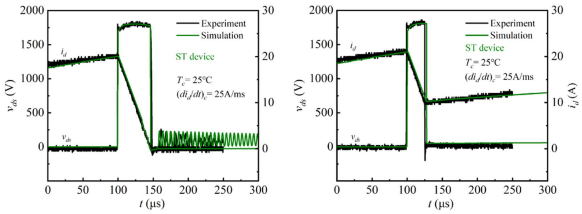


(a) (b)

Fig. 30. Simulation report (running time 2s). (a) Pspice16.6. (b) Simetrix9.0.

TABLE III
MODEL PARAMETERS OF ST DEVICE

Sub-models	Parameters
Breakdown voltage	$a = 0.01$, $b = 1.04$, $c = 0.09$, $d = 1707$
Thermal network	$R_1 = 0.00581\ \Omega$, $C_1 = 0.00963$ F $R_2 = 0.01179\ \Omega$, $C_2 = 0.00102$ F $R_3 = 0.03940\ \Omega$, $C_3 = 0.00379$ F $R_4 = 0.27645\ \Omega$, $C_4 = 0.00786$ F $R_5 = 0.30082\ \Omega$, $C_5 = 0.18369$ F
Over-temperature threshold	$T_{jl} = 582$ °C
Failure delay time	$m = -0.122$, $n = 29.65$
Internal resistance	$R_{GS} = 0.78\ \Omega$, $R_{GD} = 0.92\ \Omega$, $R_{DS} = 0.05\ \Omega$



(a) (b)

Fig. 31. Avalanche trajectory of ST device with proposed model. (a) In safety state. (b) In failure state ($T_c = 25$ °C, $(di_d/dt)_c = 25$ A/ms, $V_{EE} = -8$ V).

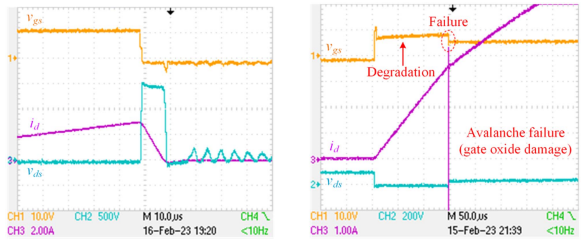
over-voltage of v_{ds}. Therefore, the proposed model is potential to evaluate the robustness of the converter during the avalanche dynamics.

It is important to verify the generality of the proposed model in different SPICE softwares. The simulation of the PFC converter shown in Fig. 29(b) is carried out in the Simetrix9.0 additionally, where the computer configuration and the running time for the simulation are the same in different SPICE softwares. Fig. 30 shows the simulation reports of different SPICE softwares. It is obvious that the proposed model convergences well both in the Pspice16.6 and the Simetrix9.0. And the higher simulation speed is seen in the Simetrix9.0, which adopts a more advanced solver. Therefore, the good generality of the proposed model has been verified in different commercial SPICE softwares.

D. Different Device Type

In order to verify the proposed model for the devices produced by different manufacturers, another device SCT30N120 (ST, 1200 V/90m Ω, planar-gate) is modeled [28]. This device has different test profile with CREE device C3M0120065D, where the negative driving voltage V_{EE} equals −8 V for the validation of the accuracy of the proposed model for different devices and test profiles. The detailed model parameters of the new device are given in Table III.

Fig. 31 shows the experimental and simulation results of the proposed model for the ST device, where the modeling processes



(a) (b)

Fig. 32. Avalanche trajectory of double-trench device. (a) In safety state. (b) In failure state with gate oxide damage ($T_c = 25$ °C, $(di_d/dt)_c = 25$ A/ms, $V_{EE} = -4$ V).

shown in Fig. 19 are repeated for the ST device under $V_{EE} = -8$ V. Obviously, the ST device has the similar trajectories with the CREE device, which means they have the consistent avalanche mechanism. Fig. 31 shows the proposed model has high accuracy in predicting the avalanche dynamics of the ST device. Therefore, the generality of the proposed model in the planar devices from different manufacturers has been verified.

It should be noted that the trench SiC MOSFET has the totally different avalanche failure mechanism compared to the planar SiC MOSFET. Fig. 32 shows the tested avalanche trajectory of the device SCT3120AL (ROHM, 650 V/120 mΩ, double-trench gate) in safety state and in failure state [29]. Compared with Fig. 3, it shows that the avalanche trajectories in safety state are similar between the planar device and trench device. However, two types of devices have different avalanche trajectories in failure state. As shown in Fig. 32(b), the significant drops can be seen in v_{gs} of the trench device, while v_{gs} of the planar device keeps stable during the avalanche test shown in Fig. 3(b). This is due to the difference of the avalanche failure mechanisms between the trench device and the planar device, where the degradation and failure of the gate oxide is the main cause for the double-trench SiC MOSFET, while the thermal runaway is the main cause for the planar device [18], [19]. Therefore, it should be cautious by applying the proposed model to the SiC MOSFET to avoid misuse of the trench device.

V. CONCLUSION

A compact SPICE model is proposed in this article, which accurately predicts the single-pulse avalanche dynamics of the planar SiC MOSFET. The proposed model includes five submodels, namely the breakdown voltage model, the thermal network model, the over-temperature threshold model, the failure delay time model, and the internal resistance model. On the one hand, the proposed model could effectively perform the avalanche trajectory in safety state, because the effect of the avalanche resistance is taken into consideration. On the other hand, the proposed model could also perform the avalanche trajectory in failure state, because the thermal runaway phenomena inside the SiC MOSFET is correctly described. Furthermore, the general SPICE model is discussed in detail, which is compact and efficient. The proposed model is validated in the UIS test, DPT and PFC converter, respectively. The high accuracy is verified, and good convergence is confirmed in different SPICE softwares.

Therefore, the proposed model has the potential in observing the single-pulse avalanche dynamics of the SiC MOSFET for the application engineers.

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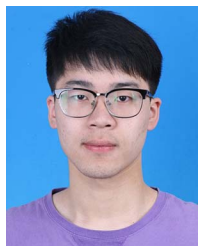

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