Analysis and Design of a Duty-Cycle-Controlled Amplitude Shift Keying Class-E Power Amplifier

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***Abstract*—This article presents a method for implementing amplitude modulation in class-E power amplifiers (PAs). The output voltage amplitude of a class-E PA is proportional to the input signal duty cycle. The proposed method exploits this feature in order to implement amplitude shift keying modulation in the standard class-E PA. The conditions for the optimum operation of a class-E PA while using two different input duty cycles are analyzed. The desired conditions are derived at the same time to reduce differences between optimum circuit elements while using different input duty cycles. The resulting class-E PA satisfies both zero voltage switching and zero derivatives of voltage at switching conditions by changing only one capacitor. This method neither degrades the efficiency nor needs many changes in circuit components. A step-by-step design procedure based on the proposed method is introduced. The simulations and measurement results verify the accuracy of the proposed method. The fabricated PA is designed to operate at 1-MHz frequency with $V_{DD} = 2$ V and 50-Ω load. The input duty cycle is changed from 25% to 49%, resulting in output amplitudes of 1.2 and 3.68 Vpp, and efficiencies of 88% and 94%, respectively.**

***Index Terms*—Amplitude shift keying (ASK), class-E power amplifier (PA), high efficiency, minimal circuit change, zero derivatives of voltage at switching (ZDVS) conditions, zero voltage switching (ZVS).**

I. Introduction

ENERGY-EFFICIENT transmission of data is one of the most important aspects of biomedical implant design, such as cardiac pacemakers, cochlear implants, retinal prostheses, and neuromuscular stimulators. Considering the battery's large size, most implants are batteryless and must be powered from an external source [1], [2]. Furthermore, in biomedical implants powered directly from the batteries for a fixed lifetime, due to the problems associated with surgical intervention for replacing them, power delivery is still considered for recharging these batteries [3], [4]. In addition, data transmission must be implemented for controlling these devices from outside. The use of transdermal or percutaneous wires has a risk of infections or skin damage. Therefore, a wired connection between the external controller and the device inside the body is avoided [3], [5].

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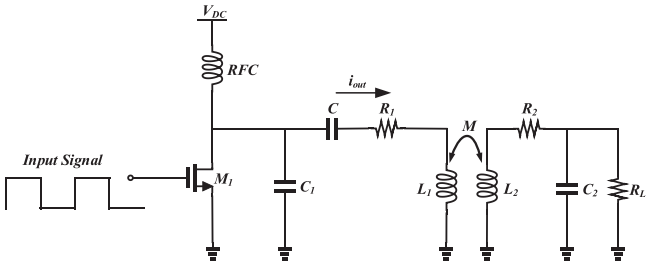

Fig. 1. Inductive link driven by a class-E PA.

There are several methods to transmit power and data wirelessly, such as near-field inductive coupling, near-field capacitive coupling, ultrasonic, and mid-field and far-field electromagnetic (EM) coupling [3]. Inductive coupling is the most popular and effective way to realize a link for transmitting power, data, or both to biomedical implants [6]. Data and power transmission via inductive coupling are also applicable in radio-frequency identification, smartcards, and wireless microelectronic mechanical systems [7]. Because of the low coupling link between the transmitter and the receiver coils, an implanted system needs high-efficiency power amplifiers (PAs) to drive the transmitter coil. Usually, a Class-E PA is used because of its simplicity and high operating efficiency (>90%) [8], [9]. Fig. 1 shows an inductive link driven by a Class-E PA.

Among different modulation strategies, frequency shift keying (FSK) and phase-shift keying (PSK) schemes can provide a constant-envelope carrier signal and then a constant power flow to the implant [1], [10]. However, due to the high bandwidth needed for transmitting different frequencies of the FSK scheme, the power dissipation of the power link increases [5]. Moreover, the demodulator circuits for FSK and PSK are power-hungry, offsetting their advantages [1]. On the other hand, the amplitude shift keying (ASK) scheme has simple and low power demodulation circuitry without needing clock and carrier synchronization [1], [5].

Different methods have been proposed for performing ASK modulation. For amplitude modulation, the amplitude of output current must be considered since induced electromotive force in the receiving coil on the implant side is a function of the time-varying current of the transmitter coil [2], [3]. For this purpose, the simplest method is shown in Fig. 2(a) [11], [12], [13]. The MOS transistor M_1 is driven by a signal that results from AND-ing the input voltage signal and the data stream. When the data are zero, the transistor M_1 will be OFF; hence, the

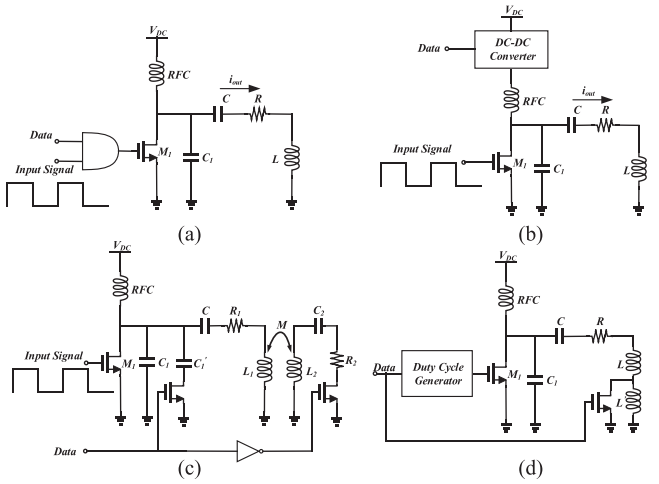

Fig. 2. Modulating output current amplitude by (a) OOK scheme, (b) changing DC level of supply voltage, (c) changing load resistor, and (d) changing input signal duty cycle.

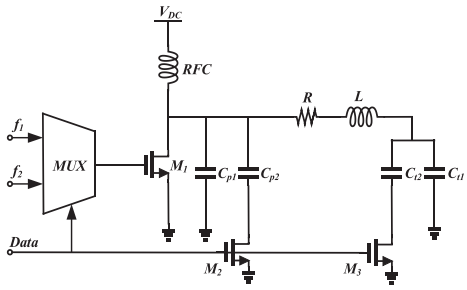

Fig. 3. Proposed circuit of Ahmadi and Ghandi [22] to implement FSK in class-E PA.

current amplitude will be zero. When the data are one, M_1 will be switched by an input voltage signal, and the output current amplitude rises. This form of ASK modulation is called ON–OFF keying (OOK) modulation having a modulation index (MI) of 100%. The key drawback of this method is the nonuniform power flow through the inductive link [1], [2]. As derived in the following sections, the output current amplitude for a high Q Class-E PA in nominally tuned operating point, which means it satisfies zero-voltage switching (ZVS) and zero-voltage-derivative switching conditions [14], is a function of the dc level of supply voltage, load resistor, and input signal duty cycle. In [8], [15], [16], [17], [18], and [19], output current amplitude is modulated by changing the dc level of the supply voltage. Changing the dc supply voltage does not affect the frequency response of the Class-E PA and, hence, the power efficiency [5], [15]. Therefore, this method requires just a dc–dc converter between the power source and V_{DC} [see Fig. 2(b)]. However, the power dissipation of the dc–dc converter reduces the power efficiency of the system. Navaii et al. [2] proposed an ASK modulation technique to surmount this problem by changing the load resistor using EM coupling [see Fig. 2(c)]. Although the class-E PA sticks to its optimum operating point in this technique, the reflected load dissipates some power in one data level. Alternatively, amplitude modulation can be performed by changing the duty cycle of the input signal. Most of the prior investigations have focused on changing the supply voltage and few of them noticed data modulation using duty cycle of the input signal. However, this technique can achieve higher power efficiency and a data rate to carrier frequency ratio of 100% [20]. Mirbozorgi et al. [20] proposed a method for modulation by changing input signal duty cycle. In this study, since the quality factor (Q) of the circuit at the output of the class-E PA is low, harmonics are less attenuated. Then, the duty cycle variations of the input signal are visible on the output voltage signal. However, in this work, the class-E PA operation does not satisfy the ZVS condition, which leads to power efficiency reduction. For the second data level, efficiency reduces since the output frequency response of the class-E PA is changed by variation of input signal duty cycle. Moreover, power transmission efficiency reduces due to the low quality factor of the LC tank in the transmitter circuit.

On the other hand, Chiu et al. [21] proposed a high Q class-E PA for generating two high-efficiency sine-wave voltages for electrical stimulation to the nerve in the implant side using the duty cycle of the input signal [see Fig. 2(d)]. This article extends the concept of duty-cycle-controlled ASK modulation for class-E PAs with any Q at the output LC network. In [22], FSK modulation is implemented in class-E PA, as shown in Fig. 3. However, the proposed method requires two component changes to maintain the Class-E operation at two different frequencies. Sections II and III present the proposed method using approximate and exact equations, respectively. The measurement results are brought in Section IV. Finally, Section V concludes this article.

II. ASK Modulation in Class-E PA With Approximate Equations

A. Basic Idea

In Section I, different methods for implementing ASK modulation in class-E PAs have been explained; however, they have some drawbacks, such as needing more circuit components, EM coupling, and more importantly, power efficiency reduction. Since power efficiency is one of the most significant features of a class-E PA, we have tried to find a method for implementing ASK in class-E PAs without reducing efficiency. In the proposed method, neither the efficiency is reduced, nor higher extra components used. In addition, it does not need EM coupling.

In [23], it has been mentioned that the output voltage amplitude of a class-E PA is proportional to its input voltage duty cycle (D). It can be inferred that by changing the input duty cycle, the output voltage amplitude will be changed, which is needed for ASK. The basic idea in this work is to use this property, which is shown graphically in Fig. 4. In this figure, a schematic of a class-E PA is depicted in which M is the core transistor of the class-E PA, RFC is the RF choke, C_1 is the shunt capacitor, L and C constitute series resonance circuit, and R is the load, which the power is delivered to. A capacitor in parallel with C (C') will be activated in one of the duty cycles to change the effective capacitance. The reason for using this extra

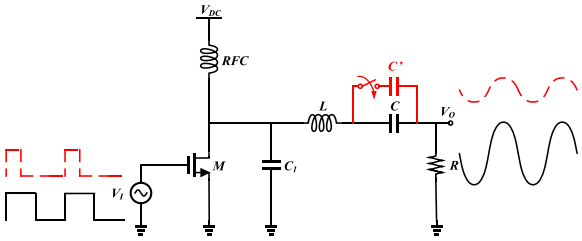

Fig. 4. Signals with different duty cycles in class-E PA.

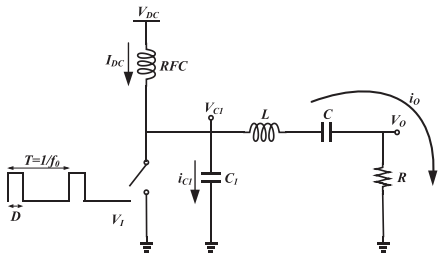

Fig. 5. Input signal and equivalent circuit of class-E PA when the transistor is OFF.

capacitor will be explained in next sections. V_{DC}, V_i, and V_o denote supply voltage, input, and output voltages, respectively. Changing the input duty cycle in conjunction with changing the series capacitor will result in output voltage amplitude change.

The optimum conditions in which ASK can be implemented are calculated in the following sections using the equations governing the class-E PA. Derivations are performed in two sections. This section uses approximate equations to give a quick understanding of the circuit behavior with acceptable accuracy, and the next section uses exact equations, which are more complicated.

B. Approximate Equations

The basic idea was explained in previous section. In this section, equations governing class-E PA assuming high Q have been considered to derive circuit elements for having optimum operation. Some approximations are used to clarify the idea and ease the calculations. In Fig. 5, the input signal applied to the amplifier is shown, where f_0 and D denote the frequency and duty cycle of the input signal, respectively.

The goal is to find the equations governing the amplifier operation. At the first step, the drain voltage of the transistor is calculated. When the input signal is high, the transistor is ON, and consequently, the drain voltage will be zero. When the transistor is OFF, it acts as an open circuit, and the equivalent circuit is illustrated in Fig. 5. In this figure, I_{DC}, i_{C1}, and i_{O} are dc current, C_1 current, and the output current, respectively. The RFC used for biasing the circuit has a high inductance; therefore, I_{DC} can be assumed constant. However, this is an assumption and for the RFC to act as a constant current source, the RFC value should be infinity. The current of the RFC can be calculated by integrating the voltage across the RFC divided by the RFC value. The variations of this current should be much lower than I_{DC} and by setting a specified amount of acceptable error, the minimum value of RFC can be calculated, which depends on supply voltage, I_{DC}, duty cycle, and frequency.

The series tank circuit's quality factor is also assumed to be high ($Q>>1$). By using this assumption, higher harmonics of the output current can be ignored. As a result, the output current can be considered as

$$i_O = I_0 \cos(\omega t + \theta_0) \tag{1}$$

where I_0 and θ_0 are the amplitude and phase of the output current, respectively. If RFC is high enough to keep dc current (I_{DC}) constant, i_{c1} will be

$$i_{C1} = I_{\mathrm{DC}} - I_0 \cos(\omega t + \theta_0). \tag{2}$$

The drain voltage is equal to C_1 voltage and can be obtained using i_{c1} as follows:

$$V_{C1} = \frac{1}{C_1}\int i_{C1}dt = \frac{I_{DC}}{C_1}t - \frac{I_0}{\omega C_1}\sin(\omega t + \theta_0) + k \tag{3}$$

where k is the constant of integration. By applying both ZVS and zero derivatives of voltage at switching (ZDVS) conditions and energy conversion law to the aforementioned equation, unknown parameters are obtained as

$$\theta_0 = \tan^{-1}\left(\frac{\pi(1-D)}{\sin^2(\pi D)} + \cot(\pi D)\right) \tag{4}$$

$$I_0 = \frac{2V_{\mathrm{DC}}}{R}\frac{1}{\sqrt{1+\tan^2(\theta_0)}} \tag{5}$$

$$I_{\mathrm{DC}} = \frac{2V_{\mathrm{DC}}}{R}\frac{1}{1+\tan^2(\theta_0)} \tag{6}$$

$$k = \frac{I_{\mathrm{DC}}}{C_1\omega}(\tan(\theta_0) - 2\pi). \tag{7}$$

By writing a KVL in the circuit of Fig. 5, we have

$$V_{C1} = RI_0\cos(\omega t + \theta_0) + XI_0\sin(\omega t + \theta_0) \tag{8}$$

where X is equal to

$$X = \frac{1}{C\omega} - L\omega. \tag{9}$$

It is assumed that the output current contains only one harmonic. V_{C1} derived in (3) contains all of the harmonics. Consequently, for comparing (3) with (8), the Fourier series of (3) is calculated, and its first harmonic coefficient is compared with (8), so we have

$$C_1 = \frac{A_1 - B_1\tan(\theta_0)}{R\omega(1+\tan^2(\theta_0))} \tag{10}$$

$$X = \frac{RB_1(1+\tan^2(\theta_0))}{A_1 - B_1\tan(\theta_0)} + R\tan(\theta_0) \tag{11}$$

where A_1 and B_1 are

$$A_1 = \frac{2}{T}\int_D^T \left(\omega t - \frac{\sin(\omega t+\theta_0)}{\cos(\theta_0)} + \tan(\theta_0) - 2\pi\right)\cos(\omega t)\,dt \tag{12}$$

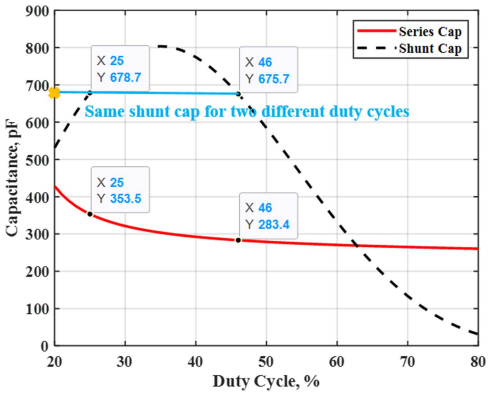

Fig. 6. Optimum capacitance values of the class-E PA for different input duty cycles using approximate equations.

$$B_1 = \frac{2}{T}\int_D^T \left(\omega t - \frac{\sin(\omega t+\theta_0)}{\cos(\theta_0)} + \tan(\theta_0) - 2\pi\right)\sin(\omega t)\,dt. \tag{13}$$

Now, the optimum values of the circuit elements can be found. C_1 and X are calculated in (10) and (11). X contains both L and C. By considering one of them known, the other one's value can be obtained. Until here, optimum circuit elements and the drain voltage of the transistor are obtained; thus, V_o can be expressed as

$$V_O = i_O \times R = I_0 R\cos(\omega t + \theta_0)\,. \tag{14}$$

Observing (14), it can be figured out that V_O amplitude is related to the D (θ_0 and consequently, I_0 are proportional to D). It can be seen that by changing the input voltage duty cycle, output voltage amplitude will be shifted.

According to (10) and (11), optimum values of the circuit elements for satisfying ZVS and ZDVS conditions are proportional to D. Thus, when D is changed, the circuit element values ought to be changed for optimum operation. It is not desired to change all of the circuit elements; therefore, a circuit with minimal changes while using different duty cycles is sought. R is the load and cannot be changed. In addition, it is assumed that the inductor value is constant. If ZVS and ZDVS conditions for different duty cycles are satisfied by changing only one capacitor, the circuit has minimal changes. To understand whether this concept is possible or not, R and L values are kept constant, and capacitor values are calculated based on different duty cycles. In this scenario, V_{DC}, f, and R are assumed to be 2 V, 1 MHz, and 50 Ω, respectively. L is assumed to be 100 μH, which is a typical inductor value. Considering this value for the inductor, the series tank's quality factor equals 12.56, which passes the $Q>>1$ condition. Fig. 6 illustrates calculated capacitive values based on different duty cycles.

It can be seen from Fig. 6 that two duty cycles can be found at which needed C_1 values are the same. Only by changing the series capacitor, ZVS and ZDVS conditions are satisfied for two different duty cycles. For better comprehending this concept, the equations obtained for class-E PA of Fig. 4 are drawn in Fig. 7(a) and (b) using V_{DC}, f, R, L, and C_1 with respective values of 2 V, 1 MHz, 50 Ω, 100 μH, and 678 pF. The input signal frequency is considered to be constant, but the duty cycles are 25% and 46%. It should be noted that these two duty cycles are chosen arbitrarily and any two other duty cycles, which have same shunt capacitance, can be chosen. Many horizontal lines similar to the one shown in Fig. 6 can be drawn to determine two duty cycles, which yield same shunt capacitance. Based on design and system requirements, the duty cycles should be selected. The value of duty cycle can affect output power, MI, etc. According to Fig. 6, the optimum series capacitance values for these duty cycles are 353 and 283 pF. Fig. 7(a) and (b) depicts the transistor's drain voltage and the output voltage of the PA for the aforementioned duty cycles. As it is evident from Fig. 7(a) and (b), the ZVS and ZDVS conditions are met. The amplitudes of the output voltages shown in Fig. 7 are different, validating the proposed ASK concept in the class-E PAs. In these simulations, only series capacitance is changed and the rest of the circuit is kept constant. To evaluate the accuracy of the equations, the circuit is simulated using mentioned element values. In this simulation, the transistor is a switch having switching voltage, ON-resistance, and OFF-resistance of $V_{DC}/2$, 1 Ω, and 1 MΩ, respectively. The simulated drain voltage of the transistor and the output voltage of the class-E PA are shown in Fig. 7(a) and (b). By comparing equations and simulations, it can be figured out that the simulations verify the equations and there is good conformity between them.

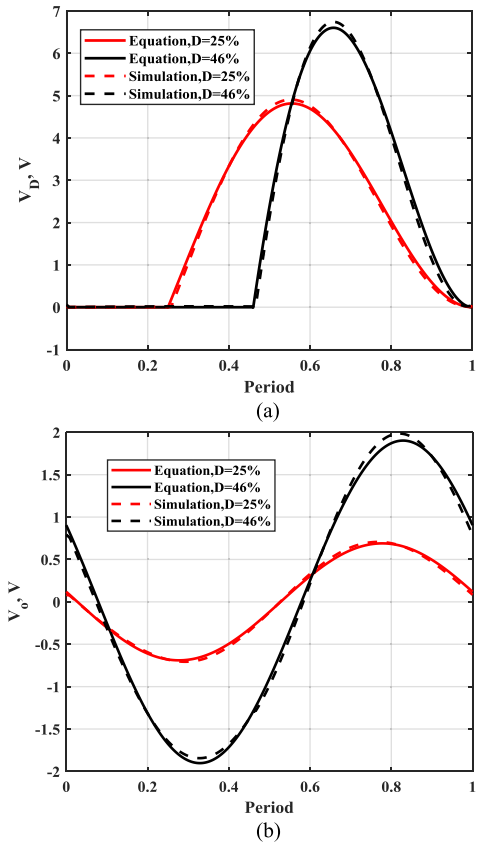

Fig. 7. (a) Drain voltage and (b) the output voltage of the class-E PA for different input duty cycles using equations and simulation.

III. ASK Modulation in Class-E PA With Exact Equations

Although the equations derived in Section II provide an excellent inspection of the circuit behavior and validate the proposed idea, they have some major limitations. The high quality factor assumption ($Q>>1$) may not be valid in some designs and it is required to have equations that can be applied in all of the conditions. In [23], the equations defining the class-E PA's operation for any Q have been derived. The equations have been divided into two categories: $Q \leq 0.5$ and $Q > 0.5$. In practical circuits, Q is usually higher than 0.5; therefore, this category of equations has been used. It can be noted that the same procedure can be used for $Q \leq 0.5$ using relative equations. In these equations, some parameters are defined, determining the differences between resonance frequencies of the circuit when the transistor is ON or OFF. When the transistor is ON, the resonance circuit contains L, C, and R. Thus, the resonance frequency ($W_{o1} = 2\pi f_{o1}$) and loaded quality factor (Q_1) are [23]

$$\omega_{O1} = \frac{1}{\sqrt{LC}} \tag{15}$$

$$Q_1 = \frac{\omega_{O1} L}{R}. \tag{16}$$

When the transistor is OFF, the resonance circuit contains L, C, C_1, and R. Therefore, the resonance frequency ($W_{o2} = 2\pi f_{o2}$) and loaded quality factor (Q_2) are [23]

$$\omega_{O2} = \frac{1}{\sqrt{\frac{LCC_1}{C+C_1}}} \tag{17}$$

$$Q_2 = \frac{\omega_{O2} L}{R}. \tag{18}$$

Since these frequencies (f_{o1} and f_{o2}) are different from the operating frequency of the circuit (f), the following ratio of the frequencies can be defined [23]:

$$A_1 = \frac{f_{O1}}{f} \tag{19}$$

$$A_2 = \frac{f_{O2}}{f}. \tag{20}$$

Also, the loaded quality factor at the operating frequency is defined by [23]

$$Q_L = \frac{\omega L}{R} = \frac{Q_1}{A_1} = \frac{Q_2}{A_2}. \tag{21}$$

The goal is to find a method for applying ASK in the class-E PAs without reducing efficiency and having minimal changes in the circuit. Using the equations brought in [23], the circuit elements for having the class-E PA's optimum operation with arbitrary duty cycles can be found and if two different duty cycles are selected for having ASK, the respective circuit elements can be calculated. Although the calculated circuit elements result in optimum efficiency, the minimal circuit change criterion is not met as circuit elements are found independently. The obtained circuit elements for different duty cycles have different values and there is no common value between them. It is intended to find and apply conditions to the equations of Kazimierczuk and Puczko [23], which help obtain some common circuit elements for different duty cycles. First, it is considered to find a condition in which L, C_1, and R are kept constant (common for different duty cycles) and only C is variable to satisfy ZVS and ZDVS conditions. Operating frequency is assumed to be constant, and only the duty cycle is changed, so we have

$$f = \frac{f_{O1}}{A_1} = \frac{1}{2\pi A_1 \sqrt{LC}} = cte \Rightarrow A_1\sqrt{LC} = cte. \tag{22}$$

By dividing frequency ratios of A_2 and A_1, it can be obtained that

$$\frac{A_2}{A_1} = \frac{f_{O2}}{f_{O1}} = \frac{\sqrt{LC}}{\sqrt{\frac{LCC_1}{C+C_1}}} = \sqrt{\frac{C+C_1}{C_1}} \tag{23}$$

$$\Rightarrow C = C_1\left(\left(\frac{A_2}{A_1}\right)^2 - 1\right). \tag{24}$$

Substituting (24) in (22) results in

$$\Rightarrow A_1\sqrt{LC_1\left(\left(\frac{A_2}{A_1}\right)^2 - 1\right)} = cte \tag{25}$$

$$\Rightarrow A_2^2 - A_1^2 = cte. \tag{26}$$

R is also assumed to be constant. Accordingly, the following relations can be found

$$Q_1 = \frac{\omega_{O1} L}{R} \Rightarrow R = \frac{1}{Q_1}\sqrt{\frac{L}{C}} = cte \tag{27}$$

$$\Rightarrow CQ_1^2 = cte \Rightarrow Q_1^2\left(\left(\frac{A_2}{A_1}\right)^2 - 1\right) = cte \tag{28}$$

Equations (29)–(30) shown at the bottom of the next page.

According to the aforementioned equations, both $A_2^2 - A_1^2$ and $Q_1^2((\frac{A_2}{A_1})^2 - 1)$ need to be constant if only C is considered to be variable. A_1 and A_2 are among the initial values in this procedure. They could be found by numerically solving [23, eqs. (31) and (32)]. For faster and easier calculations, approximate equations for A_1 and A_2 have been calculated using the curve fitting approach on data obtained from solving [23, eqs. (31) and (32)] and interpolated points between them. These approximate equations shown in (29) and (30) have more than 98% accuracy for Q_1s higher than three and make calculations easier.

Using obtained parameters (A_1 and A_2), situations in which $A_2^2 - A_1^2$ and $Q_1^2((\frac{A_2}{A_1})^2 - 1)$ are constant across different duty cycles can be found. In Section II, the optimum values of the circuit elements for satisfying ZVS and ZDVS conditions while having 25% and 46% duty cycles were calculated. It should be noted that those derivations were approximate; however, in this section, the exact equations without approximation are used. Assuming one of the duty cycles to be 25% and sweeping the other duty cycle to find the ones in which $A_2^2 - A_1^2$ and $Q_1^2((\frac{A_2}{A_1})^2 - 1)$ are kept constant, we arrive at 48% to 54% (1% steps). However, it should be noted that any of these duty cycles (48%–54%) have intersection points with 25% duty cycle in their respective Q_1. If the second duty cycle is considered to be 49%,

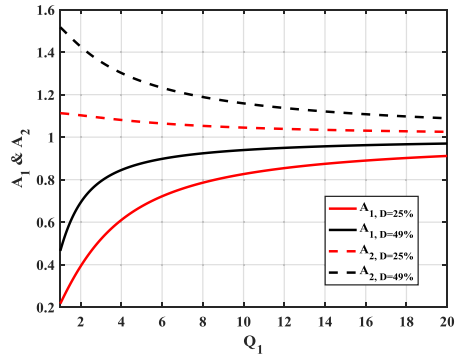

Fig. 8. A_1 and A_2 based on Q_1 for $D = 25\%$ and $D = 49\%$.

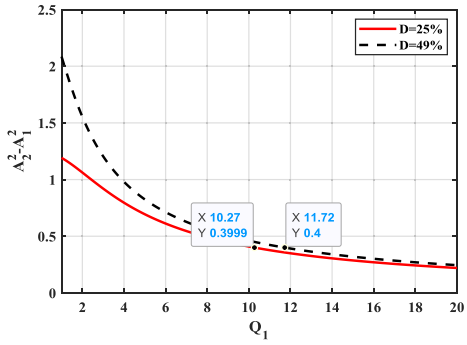

Fig. 9. $\boldsymbol{A_2^2 - A_1^2}$ based on Q_1 for $D = 25\%$ and $D = 49\%$ and obtaining Q_1 when $\boldsymbol{A_2^2 - A_1^2}$= 0.4.

the resulting Q_L is 12.367, which is closest to the quality factor of the circuit of Section II. The reason for obtaining different second duty cycles in Sections II and III originates from the fact that exact equations are used in Section III, and intersection points are considered a single point. Section II's results can be repeated if answers for satisfying the condition of constant $A_2^2 - A_1^2$ and $Q_1^2((\frac{A_2}{A_1})^2 - 1)$ are admitted with an acceptable error range. To better understand what happens, relative figures for finding the intersection point of 25% and 49% have been drawn. For finding intersection points with other duty cycles, the same procedure can be repeated. Fig. 8 shows A_1 and A_2 for $D = 25\%$ and $D = 49\%$ based on Q_1. Then, $A_2^2 - A_1^2$ for $D = 25\%$ and $D = 49\%$ versus Q_1 are illustrated in Fig. 9. The goal is to find Q_1s that result in constant $A_2^2 - A_1^2$ and $Q_1^2((\frac{A_2}{A_1})^2 - 1)$ for the different duty cycles. To find these quality factors, $Q_1^2((\frac{A_2}{A_1})^2 - 1)$ is drawn based on $A_2^2 - A_1^2$ for each D

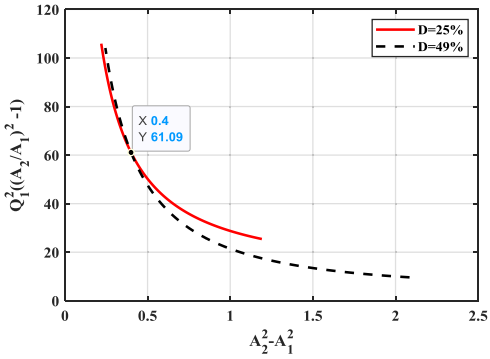

Fig. 10. $\boldsymbol{Q_1^2((\frac{A_2}{A_1})^2 - 1)}$ based on $\boldsymbol{A_2^2 - A_1^2}$ for $D = 25\%$ and $D = 49\%$.

and depicted in Fig. 10. The intersection point of the curves can be used to find Q_1s. In this example, the intersection happens where $A_2^2 - A_1^2$ is equal to 0.4. Using Fig. 9, relative Q_1 for each duty cycle can be obtained.

Since it was intended to compare this section's results with the results of Section II, f and R are assumed to be 1 MHz and 50 Ω. The other parameters are obtained using Q_1, A_1, and A_2 and summarized in Table I.

It should be noted that the intersection point cannot be always found. It means that the minimal circuit change criterion is not satisfied for any two arbitrary duty cycles. The procedure must be carried out to know if the intersection point exists or not. Fig. 11 illustrates D1 and D2 pairs, which have intersection with each other. The figure is generated by following the proposed procedure for different D1/D2 in the range of 20% to 80% and Q_1 in the range of 1 to 20. Summary of the procedure is delineated in Fig. 12. For duty cycles in the range of 58% to 80%, there were no cross points with other duty cycles.

For any D1 in the range of 20% to 58%, there is a range of D2s in which minimum circuit change criteria can be satisfied. As illustrated in Fig. 13, different D2s lead to different Q_Ls, which will translate to different circuit parameters and output voltage properties (amplitude and waveform). Fig. 11 can be used as a reference for choosing the initial D1 and D2 pair.

Till this section, optimum circuit elements for the desired duty cycles have been calculated. To evaluate this procedure's correctness, the circuit of Fig. 4 is simulated using element values of Table I. The transistor's drain voltage and the output voltage of the class-E PA are shown in Fig. 14. As it can be seen, ZVS and ZDVS conditions are satisfied.

$$A_1 = -0.8437 + 5.289D + 0.282Q_1 - 6.884D^2 - 0.4151DQ_1 - 0.02815Q_1^2 + 3.711D^3 + 0.3314D^2Q_1 + 0.01936DQ_1^2 + 0.001723Q_1^3 - 0.2011D^3Q_1 - 0.001486D^2Q_1^2 - 0.0006773DQ_1^3 - 5.615e-5Q_1^4 + 0.003606D^3Q_1^2 - 0.0001624D^2Q_1^3 + 1.302e-5DQ_1^4 + 7.306e-7Q_1^5 \quad (29)$$

$$A_2 = -0.1922 + 16.05D + 0.01874Q_1 - 81.49D^2 - 0.05848DQ_1 - 0.002185Q_1^2 + 212.9D^3 - 0.5256D^2Q_1 + 0.01374DQ_1^2 + 4.61e-5Q_1^3 - 268.3D^4 + 1.056D^3Q_1 - 0.007961D^2Q_1^2 - 0.0002619DQ_1^3 + 135.5D^5 - 0.912D^4Q_1 + 0.009453D^3Q_1^2 + 1.406e-5D^2Q_1^3. \quad (30)$$

TABLE I
CALCULATED CIRCUIT ELEMENTS FOR $D = 25\%$ AND 49% USING Q_1, A_1, AND A_2

D	Q_1	A_1	A_2	Q_2	Q_L	R	L	C	C_1
25 %	10.2733	0.8307	1.0440	12.9112	12.367	50 Ω	98.415 µH	373 pF	643 pF
49 %	11.729	0.9484	1.1399	14.0973	12.367	50 Ω	98.415 µH	286 pF	643 pF

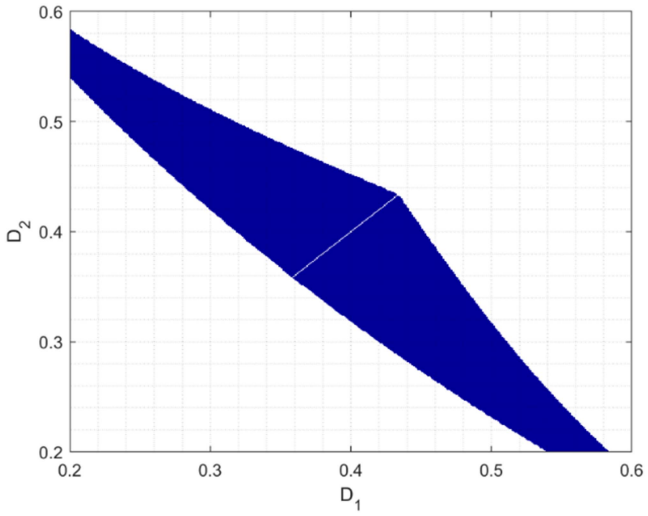

Fig. 11. Range of D1/D2 pairs in which intersection point can be found.

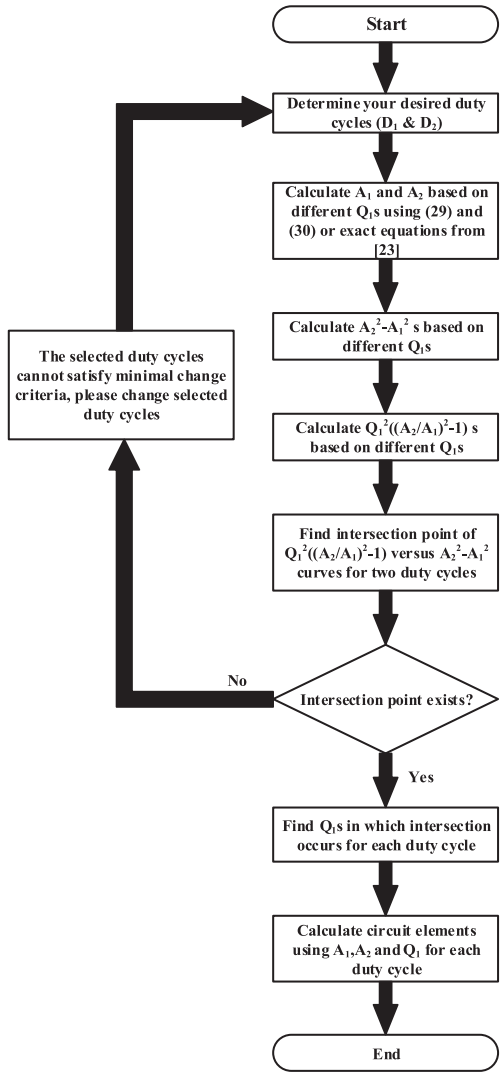

Fig. 12. Flowchart showing procedures for calculating circuit elements of proposed method using exact equations.

In this procedure, it was assumed that C_1 is constant and C is variable. The same procedure can be carried out by assuming C to be constant and C_1 to be variable. In this way, no intersection points will be found. Therefore, it is not explained here.

There are articles discussing the effect of circuit variations on the performance of a standard Class-E PA. Raab's work [24] is the most cited work on this subject. In general, increasing the quality factor of the *LC* circuit increases the sensitivity of the Class-E circuit, in terms of waveform optimal shape and dc-to-load efficiency. This is expected because an *LC* circuit with a high Q factor has a narrow-band nature, and is more sensitive to any variation in the circuit element values or input frequency/duty cycle. The aforementioned work discusses various types of circuit element changes and their effect on the PA performance. The adopted quality factor in our design is about 12. To examine the effect of variations, we changed each circuit element by $\pm 5\%$, and observed the drain waveform and total efficiency. These changes in the inductor, shunt capacitor, and load resistor have almost similar effects on the drain waveform and efficiency. According to various simulations, the series capacitor has the maximum sensitivity and can be changed only by $\pm 2\%$; in order not to cause a significant reduction in efficiency and optimal waveform.

IV. MEASUREMENT RESULTS

To demonstrate the validity of the proposed circuit, derived equations, and design procedure, a test board has been manufactured using discrete components. The goal is to deliver about 20-mW power to a 50-Ω load from a 2-V supply.

As derived in Section III, the circuit elements are as follows: $L = 98.415\ \mu$H, $C_1 = 643$ pF, and C is switched between 373 and 286 pF for duty cycles of 25% and 49%, respectively. A 1-mH ferrite drum core inductor is used as RF choke in the supply path of the amplifier (RFC in Fig. 4). In addition to multiple through-hole and surface mount ceramic multilayer capacitors for series and shunt capacitors (C and C_1), variable capacitors (Trimmer) are used in order to tune the circuit for the best response and compensating parasitic capacitors of the inductor, transistor, and the printed circuit board itself. A small size SOT-23 package MOSFET from ON-Semiconductors is used as the main switch of the amplifier.

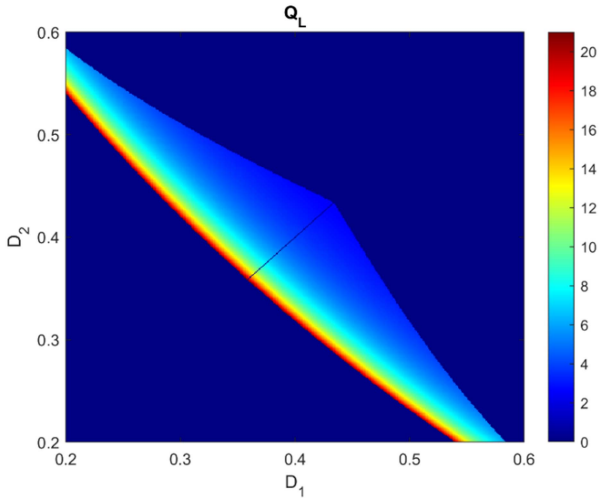

Fig. 13. Q_L of intersection points.

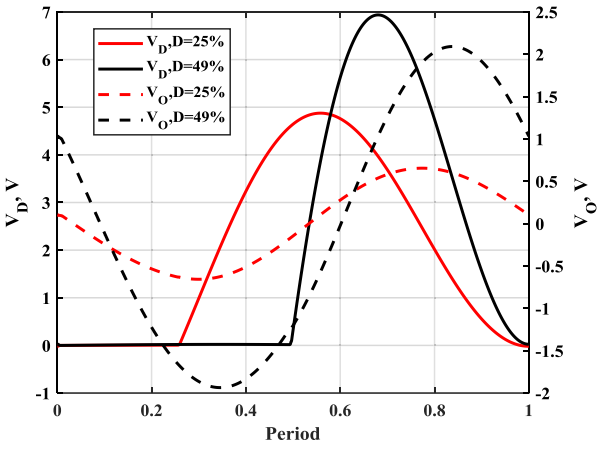

Fig. 14. Drain voltage and output voltage of the class-E PA using elements of Table I.

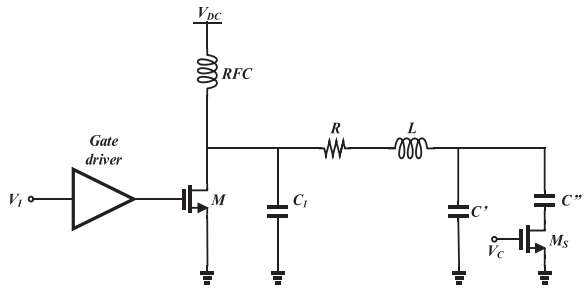

Fig. 15. Schematic of the fabricated test board.

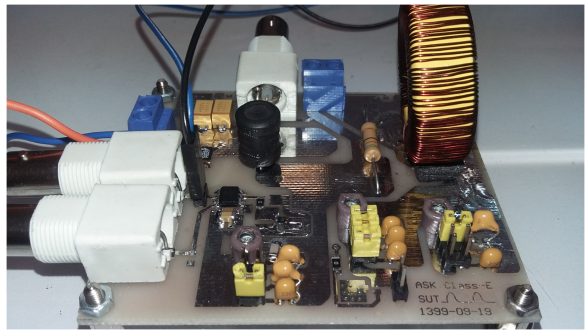

Fig. 16. Fabricated test board.

The very low parasitic capacitances of the MMBF170 along with its relatively high pulsed voltage and current capability make it ideal for this application. The gate-source capacitance of the FET increases the ON/OFF time. It is up to the gate drive circuitry to charge and discharge this capacitance in a short time. We used a general-purpose high-speed gate driver UCC27524 from Texas Instruments. It has a maximum sink and source current of 5 A, which results in rise and fall times lower than 10 ns for 1.8-nF capacitive load. The gate-source capacitance of the FET is about 24 pF, so the gate is charged and discharged in a very short time compared to the period of the 1-MHz input signal. The drain-source capacitance of the FET is 17 pF and will be absorbed in the shunt capacitance of the resonant circuit (C_1). The parasitic inductances of the FET have a significant effect on the waveform, especially in the switching instants. Only a 10-nH series inductance in the drain or source terminals results in a significant ringing in the drain voltage waveform when the transistor is switched ON or OFF. This parameter is usually neither included in the device datasheet nor in the spice model. We examined several FETs, including FDC3512, MMBF170, FDN335, and FDN305 from ON-Semiconductors, IRF7807 from International Rectifier, and only MMBF170 had an acceptable response in terms of ringing at the switching times. Another bottleneck in the implementation of the circuit was the inductor in the output resonant circuit. The inductor should have a value of about 100 μH, which is not a strict criterion. Besides, it should have a low ESR ($\sim$1 Ω) compared to the 50-Ω load resistor. Factors that determine the ESR are the copper resistance considering the skin effect at 1 MHz, and the core loss. Moreover, the inductor should have a high self-resonant frequency (SRF) compared to the operating frequency of 1 MHz. We tested several ready-from-market inductors, including a power SMD inductor, toroidal inductor, and radial inductor. All of them failed to achieve the aforementioned conditions together. So, we designed and winded an inductor with a well-characterized core from MICROMETALS. We used the T130-6 iron powder core and 25 AWG wire to wind 105 turns of wire around the toroidal core. According to measurement results with an *RLC* meter, the resulting inductor has about 97.5-μH inductance, 3.5-Ω series resistance at 1 MHz, and SRF of about 10 MHz.

The test board schematic and the fabricated prototype are shown in Figs. 15 and 16, respectively. The circuit is almost the same with the original class-E circuit, except an auxiliary MOSFET used to switch the series capacitor, i.e., change the effective value of *C*. Table II summarizes the circuit elements used in the test board. As stated before, the inductor has a measured ESR of 3.5 Ω. So, we used a 46-Ω load resistor, in order to have a net load resistor of 49.5 Ω, for which the circuit elements are designed.

After adjusting the trimmers, the optimal waveforms have been obtained. To change the output amplitude and consequently

TABLE II
CIRCUIT ELEMENTS USED IN THE TEST BOARD

Element	Descriptions	
M1	MMBF170	
Gate Driver	UCC27524	
L	Toroidal Core T130-6 105 turns AWG 25 97.5 µH, 3.5 Ω ESR@1 MHz	
C_1	550 pF fixed + 120 pF Trimmer	
C	Constant	242 pF fixed + 120 pF Trimmer
	Switched	100 pF fixed + 120 pF Trimmer
R	46 Ω, wirewound resistor	
L_D	1-mH drum core inductor	

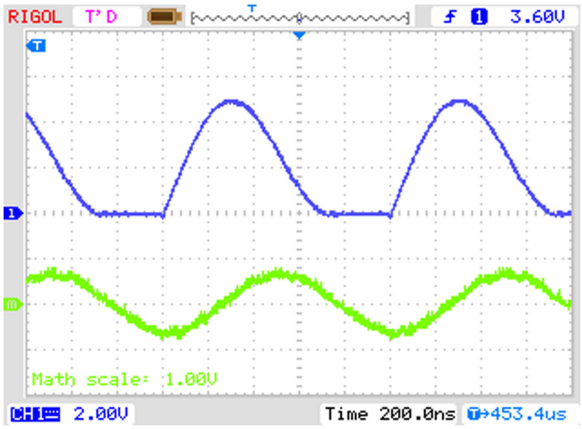

Fig. 17. Drain voltage (upper) and the load resistor voltage (lower) waveforms for 25% input signal duty cycle.

the output power, two changes are required. First, the duty cycle should be changed as it is the basic idea of the circuit. Second, in order to adjust the series capacitor (C), the MOSFET M_S is turned ON, to change the value of C. In this way, the PA's output amplitude is changed only by changing the input signal duty cycle and changing the series capacitor using a MOSFET while maintaining the class-E operation of the circuit, i.e., the ZVS/ZDVS conditions on the drain voltage waveform. The drain voltage waveform and the load resistor voltage waveform for two duty cycles of 25% and 49% are shown in Figs. 17 and 18, respectively. The measured efficiencies are 88% and 94%, and output voltage amplitudes are 1.2 and 3.68 Vpp for input duty cycles of 25% and 49%, respectively.

When the duty cycle changes, the time during which the ON-resistance of the FET and inductor loss contribute to power dissipation also change. This is why the total efficiencies are different for the two input duty cycles of 25% and 49%.

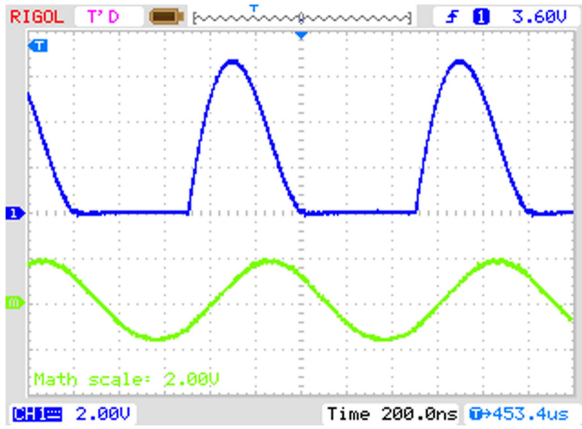

Fig. 18. Drain voltage (upper) and the load resistor voltage (lower) waveforms for 49% input signal duty cycle.

V. CONCLUSION

This article has presented a method for implementing ASK modulation in class-E PAs. A change in the input signal's duty cycle in class-E PAs alters output voltage amplitude, making ASK feasible. Considering this phenomenon, the basic idea for ASK in class-E PAs using two different input duty cycles has been explained. Then, approximate and exact equations are driven to find the circuit elements in which ZVS and ZDVS conditions are preserved for both duty cycles. It has been shown that the optimum operation conditions are met only by changing the series capacitor, which gives us the minimal circuit change criterion. Simulation and experimental measurements verify the accuracy of the method.

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