Analysis and Design of *LCCL* Resonant Converter Based on Time-Domain Model for Bidirectional Onboard Charger Applications

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***Abstract*—A novel bidirectional *LCCL* resonant dc–dc converter is proposed in this article. By substituting the magnetizing inductance of *CLLC* with a parallel resonant capacitor, the *LCCL* resonant converter obtains enhanced voltage gain regulation capability compared to *CLLC* while maintaining zero-voltage switching (ZVS) for the inverting side and zero-current switching for the rectifier side during bidirectional power flow. The state of the isolated bidirectional dc–dc converters is thoroughly reviewed in this article. The operating principle and gain characteristic of *LCCL* under bidirectional power flow are explored in detail adopting time-domain model, which effectively overcomes the drawback of the lower accuracy of the first harmonic approximation in wide voltage range applications and guarantees the achievement of ZVS in time-domain accuracy. A parameters optimization method of *LCCL* is provided to address the wide voltage range of battery applications, which is capable of achieving the required bidirectional voltage gain and ZVS operation over the designed frequency range under the desired load conditions while minimizing reactive power. Finally, a laboratory prototype rated at 1 kW is developed to convert between 400 and 250–450 V bidirectional. The experimental results confirm the feasibility of the proposed *LCCL* topology and the validity of the corresponding parameters optimization method.**

***Index Terms*—Bidirectional resonant dc–dc converter, *LCCL*, time-domain model (TDM), wide voltage conversion, zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

THE intermittent nature of renewable energy sources makes their grid integration and reliability enhancement challenging, leading to potentially severe dynamic mismatches between energy supply and demand. Nonetheless, it has been suggested that the mismatches could be addressed by integrating the batteries of electric vehicles (EVs) into the national grid, which would provide a way of dynamic grid stability, but would require a bidirectional power interface between the grid and EVs for vehicle-to-grid (V2G) energy transfer [1], [2], [3], [4].

Typically, V2G energy transfer is realized with the involvement of a bidirectional onboard charger (OBC), which typically incorporates bidirectional dc–dc converters (BDCs) with a wide voltage range and high efficiency. BDCs can be categorized as nonisolated and isolated. As galvanic isolation is typically recommended for safety standards in battery applications, only the isolated BDCs are discussed in this article [5], [6].

Nowadays, various soft-switching converters focus on minimizing switching loss, eliminating electromagnetic interference and obtaining an attainable high frequency [7], [8], [9]. Among all the soft-switching isolated BDCs topologies, the dual-active-bridge (DAB) converter [10] and bidirectional resonant converter (BRC) are the two most prevalent topologies. DAB harvests bidirectional power flow and zero-voltage switching (ZVS) exclusively via phase-shift (PS) control. In addition, DAB is appropriate for high-power applications due to its simple structure [5], [6], [10], [11], [12]. However, excessive circulating energy and large turn-OFF losses severely limit DAB converter to maintain high efficiency over a wide gain range [13], [14], [15]. In particular, ZVS will be lost under light load, resulting in a further deterioration in efficiency. Therefore, various techniques have been proposed to extend the related soft-switching range and lower the circulating energy. In [16], a higher voltage bridge with PS control was developed to extend ZVS range and reactive current was reduced to enhance corresponding light-load efficiency of DAB. An auxiliary series injection transformer is introduced for DAB to extend the ZVS range and limit reactive power in [17]. Similarly, a modified DAB structure is provided by adding a switch-controlled inductor resonant tank and the peak efficiency reaches 94.6% with an extended ZVS range [15]. However, its efficiency is severely diminished when the voltage gain deviates from unity, leading to a narrow output voltage range. Many advanced multi-PS control methods including extended-PS, dual-PS, and triple-PS modulation have been developed to manipulate the power conversion of DAB [18], [19], [20], [21], [22], [23], [24], which are dedicated to achieving different specific objectives, such as extending ZVS range, reducing reactive current, and minimizing switch loss.

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Besides, switching frequency modulation is also combined with multi-PS control to improve the performance of DAB [25], [26], [27], [28].

As the control dimension increases, the capability and flexibility to achieve optimal operation are unquestionably strengthened. However, the tradeoff is more complex implementation and higher hardware cost. Furthermore, the corresponding efficiency performance of DAB is still inferior to that of its bidirectional resonant counterpart [29], [30].

For bidirectional OBC applications, the battery voltage varies considerably throughout the charging and discharging process. Consequently, the corresponding isolated BDCs should exhibit a significantly wide output voltage range. However, the performance of BRCs is typically not comprehensively optimized for OBC applications. In order to meet the wide voltage range requirements of batteries and further reduce turn-OFF loss, various BRCs topologies have been investigated recently. Unlike DAB with PS control schemes, BRCs usually adopt pulse frequency modulation (PFM), which possesses exclusive advantage of zero-current switching (ZCS).

Bidirectional series resonant converter (SRC) is the simplest resonant converter in structure, with only one additional series resonant capacitor in comparison to DAB. A new control scheme is introduced in a bidirectional SRC operating in discontinuous conduction mode [31]. With the energy accumulated in the resonant tank, SRC has the potential to achieve a voltage gain greater than unity. However, the peak efficiency is only 91% under rated load and the control strategy is complicated. A step-up bidirectional SRC operating in continuous conduction mode was presented in [32], which harvests higher efficiency than the traditional PS DAB over a broad power range. However, PFM causes the current waveform to have a substantial resonant component, resulting in a greater core loss. The bidirectional *LLC* resonant converter can achieve ZVS and ZCS over nearly all load ranges, making it a feasible choice. Nevertheless, *LLC* remains a conventional SRC with voltage gain less than unity during reverse operation [33]. In order to extend the voltage gain range, Zhang et al. [34] introduced an improved *LLC* structure that doubles the voltage gain by switching between half bridge and full bridge. However, the associated resonance parameter's design becomes a new challenge in addressing the wide voltage range of battery applications. A bidirectional *LLC* with automatic transition between forward and backward mode is presented [35]. An auxiliary inductor is inserted to symmetrize the resonant tank and improve voltage regulation during reverse operation. Besides, a modified *LLC* is proposed to maximize the light-load efficiency in [36]. However, its control strategy is complicated and its reverse voltage gain fails to satisfy the requirements of wide range.

Recently, a novel *CLLC* resonant tank derived from *LLC* with a symmetrical structure has been proposed [8], [30], [37], which exhibits similar voltage gain characteristics (e.g., both step-up and step-down) during forward and reverse operation [30]. However, as the OBC power grade increases, the resonant inductance of *CLLC* becomes too small to be realized accurately [33]. Afterward, some topologies have been evolved to achieve bidirectional high-voltage gain. *SLLC* with auxiliary resonant components harvests higher voltage gain while resulting in more power loss [38]. A bidirectional *LCLL* is presented to raise the voltage gain for reverse operation by adding an auxiliary inductor [39]. Additional core loss and conduction loss will come from the current of the auxiliary inductor. In [33], the *CLTC* harvests decent gain characteristics and high efficiency over all load ranges. However, the introduction of auxiliary transformer leads to more core loss and more complex design considerations.

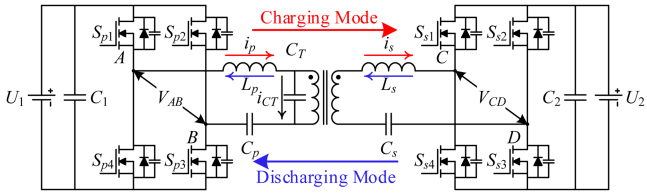

Fig. 1. Topology of the proposed bidirectional *LCCL* resonant converter.

Further article is required to address the wide voltage range requirements of bidirectional OBC applications. Therefore, a novel bidirectional *LCCL* resonant converter is proposed in this article, as shown in Fig. 1. Compared to *CLLC*, *LCCL* harvests similar soft switching characteristics and stronger gain regulation capability. The rest of this article is organized as follows. The topology derivation and operation principles of *LCCL* resonant tank are described in Section II. In Section III, time-domain model (TDM) is adopted to analyze the characteristics of *LCCL* converter in charging and discharging modes for typical OBC applications. Furthermore, a novel design methodology that is capable of achieving the required bidirectional voltage gain and ZVS operation over the designed frequency range under the desired load conditions is developed in Section IV. Experimental results from a 1-kW laboratory prototype are provided in Section V to verify the feasibility of the proposed *LCCL* converter and the validity of the corresponding parameters optimization method. Finally, Section VI concludes this article.

II. Topology Derivation and Operation Principles

A. Topology Derivation

The proposed *LCCL* resonant tank is shown in Fig. 1. Compared with *CLLC*, the magnetizing inductor in parallel with the transformer is replaced by a resonant capacitor C_T. *LCCL* resonant converter gathers the advantages of *LLC*, *CLLC*, and *LCC*. The parallel resonant capacitor C_T can bring stronger voltage gain regulation capability to *LCCL*.

Since *LCCL* resonant tank may have arbitrary parameters, *LCCL* can be classified as D-type *LCCL* ($L_pC_{ap} \neq L_sC_{as}$) with unequal resonant frequency of primary and secondary sides and S-type *LCCL* ($L_pC_p = L_sC_s$) with equal resonant frequency of primary and secondary sides, as illustrated in Fig. 2.

Different from S-type *LCCL*, the unequal resonant frequency of primary and secondary of D-type *LCCL* significantly inconveniences its calculation and analysis. Actually, the genuine resonance frequency of D-type *LCCL* is neither the primary nor the secondary resonance frequency. By equating D-type *LCCL*

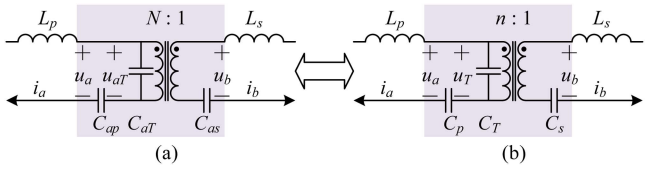

Fig. 2. D-type *LCCL* (a) and S-type *LCCL* (b).

with unequal resonant frequency of primary and secondary to S-type *LCCL* with equal resonant frequency of primary and secondary, the analysis of D-type *LCCL* can be converted to the analysis of its equivalent S-type *LCCL*.

Assuming that the resonant inductors (both L_p and L_s) are the same for D-type *LCCL* and the equivalent S-type *LCCL*. Therefore, only the part containing the resonant capacitors and the ideal transformer (i.e., the highlighted region of Fig. 2) needs to be equated. Equation (1) shows the port voltage (i.e., u_a and u_b) in term of the loop currents (i.e., i_a and i_b) for the capacitors and transformer part of D-type *LCCL* shown in Fig. 2(a). Similarly, the port voltage in term of the loop currents for the capacitors and transformer part of the equivalent S-type *LCCL* shown in Fig. 2(b) is obtained in (2). To ensure that the equivalent S-type *LCCL* and the given D-type *LCCL* possess exactly the same external characteristics (e.g., port voltages and loop currents), (2) should be precisely equal to (1). Due to the reciprocity of passive networks, the equivalence of (2) and (1) corresponds to only three equations. Therefore, an additional constraint is necessary to determine the four unknowns (C_p, C_s, C_T, n) of the equivalent S-type *LCCL*. Fortunately, S-type *LCCL* implies the inherent constraint $L_pC_p = L_sC_s$, which is utilized as $C_p/C_s = L_s/L_p = H_l$ in (3), where H_l represents the resonant inductor ratio between secondary and primary sides for the equivalent S-type *LCCL* and D-type *LCCL*

$$\begin{cases} i_a = C_{ap}\frac{d(u_a-u_{aT})}{dt} \\ i_b = C_{as}\frac{d\left(u_b-\frac{u_{aT}}{N}\right)}{dt} \\ i_a+\frac{i_b}{N} = C_{aT}\frac{du_{aT}}{dt} \end{cases} \Rightarrow \begin{cases} \frac{du_a}{dt} = \left(\frac{1}{C_{ap}}+\frac{1}{C_{aT}}\right)i_a + \frac{1}{NC_{aT}}i_b \\ \frac{du_b}{dt} = \frac{1}{NC_{aT}}i_a + \left(\frac{1}{C_{as}}+\frac{1}{N^2C_{aT}}\right)i_b \end{cases}$$
$$\Rightarrow \begin{bmatrix} \frac{du_a}{dt} \\ \frac{du_b}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{C_{ap}}+\frac{1}{C_{aT}} & \frac{1}{NC_{aT}} \\ \frac{1}{NC_{aT}} & \frac{1}{C_{as}}+\frac{1}{N^2C_{aT}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} \frac{du_a}{dt} \\ \frac{du_b}{dt} \end{bmatrix} = \begin{bmatrix} \frac{1}{C_p}+\frac{1}{C_T} & \frac{1}{nC_T} \\ \frac{1}{nC_T} & \frac{1}{C_s}+\frac{1}{n^2C_T} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix} \tag{2}$$

$$\begin{cases} \begin{bmatrix} \frac{1}{C_p}+\frac{1}{C_T} & \frac{1}{nC_T} \\ \frac{1}{nC_T} & \frac{1}{C_s}+\frac{1}{n^2C_T} \end{bmatrix} = \begin{bmatrix} \frac{1}{C_{ap}}+\frac{1}{C_{aT}} & \frac{1}{NC_{aT}} \\ \frac{1}{NC_{aT}} & \frac{1}{C_{as}}+\frac{1}{N^2C_{aT}} \end{bmatrix}. \\ C_p/C_s = L_s/L_p = H_l \end{cases} \tag{3}$$

To facilitate the subsequent derivation, the normalized parameters associated with D-type *LCCL* are presented as follows, where H_c represents the resonant capacitor ratio between primary and secondary sides and K_a denotes the capacitor ratio between parallel resonant capacitor and primary resonant capacitor:

$$\begin{cases} H_c = C_{ap}/C_{as} \\ K_a = C_{aT}/C_{ap}. \end{cases} \tag{4}$$

By solving (3), corresponding parameters of the equivalent S-type *LCCL* are determined as

$$\begin{cases} C_p = C_{ap}\frac{\left(1+N^2(K_a(H_c+H_l)+H_l)+\xi_0\right)}{2N^2(K_a+1)H_c+2} \\ C_s = C_{ap}\frac{\left(1+N^2(K_a(H_c+H_l)+H_l)+\xi_0\right)}{H_l(2N^2(K_a+1)H_c+2)} \\ C_T = \frac{1}{2}C_{ap}K_a\left(1-N^2\left(K_a\left(H_l-H_c\right)+H_l\right)+\xi_0\right) \\ n = \frac{2N}{1-N^2(K_a(H_l-H_c)+H_l)+\xi_0} \end{cases} \tag{5}$$

where

$$\xi_0 = \sqrt{\left(N^2K_aH_c - N^2\left(K_a+1\right)H_l+1\right)^2+4N^2H_l}. \tag{6}$$

B. Operation Principles

In *topology derivation* part, the equivalence from D-type *LCCL* to S-type *LCCL* has been provided. Therefore, all analyses of D-type *LCCL* can be transformed to the analyses of their equivalent S-type *LCCL*. The following analysis of this article focuses on S-type *LCCL*.

For the S-type *LCCL* shown in Fig. 2(b), we have the following definitions:

$$\begin{cases} k = C_T/C_p \\ h = n^2C_p/C_s = n^2L_s/L_p \end{cases} \tag{7}$$

where k represents the capacitor ratio between parallel resonant capacitor and primary resonant capacitor, and h denotes the symmetry coefficient of S-type *LCCL*.

Both directions of power flow (e.g., charging and discharging) of S-type *LCCL* are regulated with PFM around resonance-like frequency f_{r_l}, as defined in (8). In charging mode, the inverting switches S_{p1} & S_{p3} and S_{p2} & S_{p4} operate with 50% duty cycle, while the rectifier switches S_{s1} & S_{s3} and S_{s2} & S_{s4} are driven by synchronous rectification (SR) signals. In discharging mode, the inverting switches S_{s1} & S_{s3} and S_{s2} & S_{s4} operate with 50% duty cycle, while the rectifier switches S_{p1} & S_{p3} and S_{p2} & S_{p4} are driven by SR signals

$$f_{r\_l} = \sqrt{\frac{hk+h+1}{hk}}\frac{1}{2\pi\sqrt{L_pC_p}} = \sqrt{\frac{hk+h+1}{hk}}\frac{1}{2\pi\sqrt{L_sC_s}}. \tag{8}$$

Fig. 3(a) and (b) illustrates the typical waveforms when *LCCL* operates below resonance-like frequency and above resonance-like frequency, respectively. Furthermore, Fig. 3(c) depicts the typical waveform when *LCCL* operates exactly at resonance-like frequency. Where $V_{GSp1}(V_{GSp3})$ is the drive signal of $S_{p1}(S_{p3})$, $V_{GSp4}(V_{GSp2})$ is the drive signal of $S_{p4}(S_{p2})$, V_{AB} denotes the inverting voltage of the primary resonant tank, i_p and i_s represent the resonant current of primary side and secondary side, respectively, i_{CT} indicates the resonant current of C_T, u_{Cp}, u_{Cs}, and u_{CT} represent capacitor voltage of C_p, C_s, and C_T, respectively, and T_s indicates one switching cycle.

Since several stages of Fig. 3(a)–(c) are similar, only Fig. 3(a) is investigated in detail to explain the operation principles of

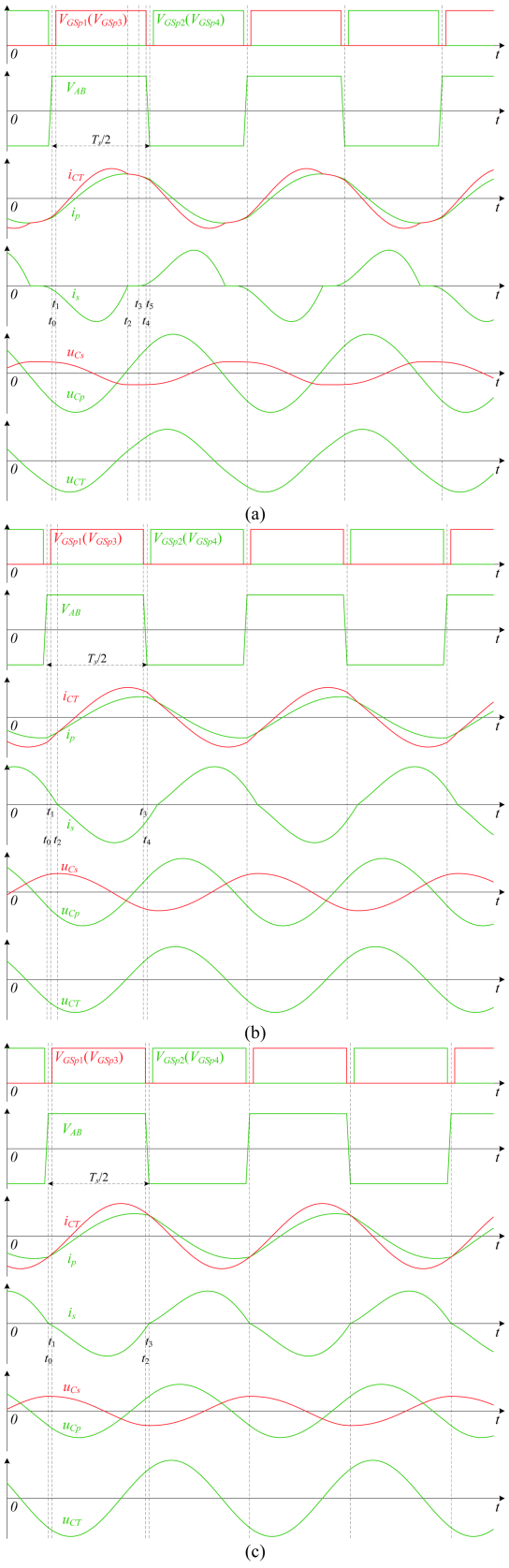

Fig. 3. Typical waveforms of *LCCL*. (a) Below resonance-like frequency. (b) Above resonance-like frequency. (c) Resonance-like frequency.

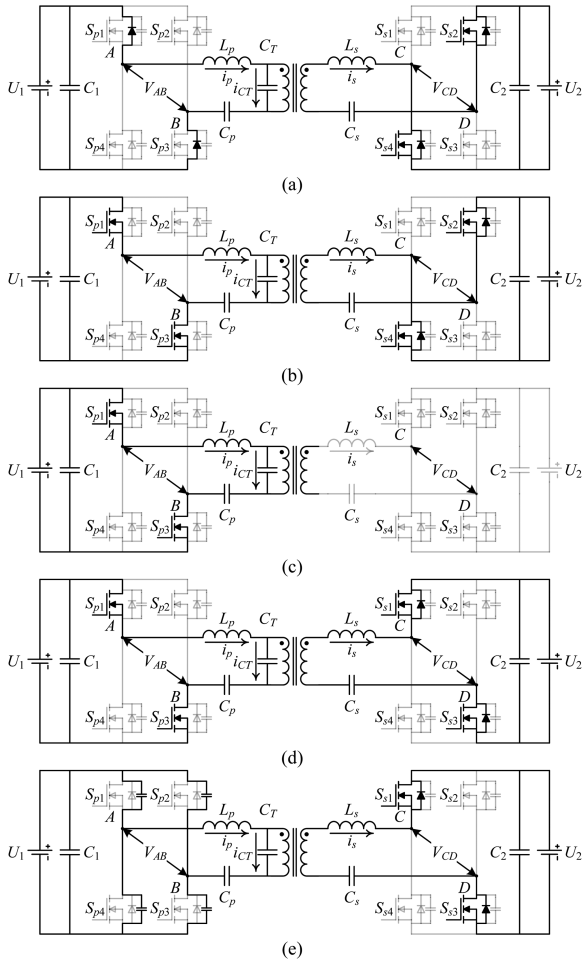

Fig. 4. Equivalent circuits for each stage of *LCCL* operates below resonance-like frequency. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5.

LCCL. Accordingly, the equivalent circuit for each stage of Fig. 3(a) is depicted in Fig. 4.

Stage 1 [t_0, t_1): After the parasitic capacitance of inverting switches has been sufficiently discharged or charged during the dead time, the resonant current i_p begins to flow through the body diodes of S_{p1} & S_{p3} at time t_0.

Stage 2 [t_1, t_2): At time t_1, S_{p1} & S_{p3} turn ON under ZVS conditions and energy is transmitted to the rectifier side through transformer. On the rectifier side, resonant current i_s in proportion to the difference between resonant current i_p and i_{CT} flows through S_{s2} & S_{s4}.

Stage 3 [t_2, t_3): When i_{CT} resonates over its peak, it begins to decrease until it is equal to the increasing resonant current i_p at time t_2. The resonant current i_s on the rectifier side decreases to 0 and S_{s2} & S_{s4} turn OFF under ZCS conditions at time t_2. The voltage u_{Cs} also resonates to its peak. The separation of L_s and C_s from the inverting side causes the free resonance between L_p, C_p, and C_T on the inverting side.

Stage 4 [t_3, t_4): At time t_3, the voltage of C_T resonates to reach the voltage of $n(U_2+u_{Cs})$, S_{s1} & S_{s3} begin conducting, and the resonant component of rectifier side once again participates in the resonance with the inverting side again.

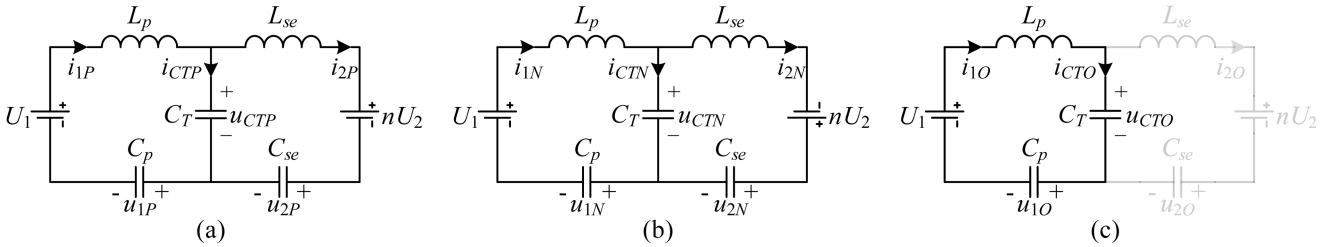

Fig. 5. Equivalent circuit of the *LCCL* in (a) P stage, (b) N stage, and (c) O stage.

Stage 5 [t_4, t_5): At time t_4, S_{p1} & S_{p3} turn OFF. i_p begins to charge the parasitic capacitance of S_{p1} & S_{p3} and discharge that of S_{p2} & S_{p4} simultaneously. This stage ends up with the drain-source voltage of S_{p1} & S_{p3} reaching voltage U_1 and that of S_{p2} & S_{p4} dropping to zero. At time t_5, the inverting voltage V_{AB} has flipped its polarity from U_1 to $-U_1$, the positive half cycle ends, and the converter initiates the subsequent negative half cycle.

In addition, the typical waveforms of *LCCL* resonant converter are quite similar to those of *LLC* or *CLLC*, and *LCCL* that operates at resonance-like frequency can likewise obtain a constant voltage gain (h as discussed later). Therefore, the *LCCL* converter inherits the soft switching features of *LLC* and *CLLC* (e.g., ZVS for inverting side and ZCS for rectifier side).

III. Characteristics of *LCCL* Converter

For typical OBC applications, the input voltage of *LCCL* converter is designed to be a constant value, whereas the battery voltage of output varies significantly during the charging and discharging processes. Therefore, this article concentrates on exploring the characteristics of S-type *LCCL* with wide-range voltage output.

A. Forward Mode

1) Time-Domain Model: Considering that *LCCL* adopts PFM to regulate the output voltage and that the duty cycle remains constant at 50%, the steady states of the resonant tank should be symmetrical in both half cycles. The following analysis focuses on the positive half cycle when V_{AB} is positive. Several assumptions are established to simplify the analysis of TDM: the dead time of drive signals is neglected for the convenience of calculation and the parasitic capacitance of switches is ignored (i.e., inverter voltage V_{AB} can reverse polarity instantaneously).

Due to the presence of switching actions on both the inverting and rectifier sides, *LCCL* behaves as a nonlinear time-varying system, which leads the analysis of its operating principle more complicated. Depending on the difference of switching frequency, parameters specifications, and load conditions, *LCCL* may go through multiple resonant stages in sequence during the positive half cycle. According to the conduction states of rectifier side body diodes, the different resonant stages can be categorized as P stage (the body diodes of S_{s1} & S_{s3} turn ON), N stage (the body diodes of S_{s2} & S_{s4} turn ON), and O stage (no body diodes turn ON). Fig. 5 depicts the equivalent circuits for several resonant stages, where $C_{se} = C_s/n^2$ and $L_{se} = n^2 L_s$.

TABLE I
Abbreviations and Normalizations

Circuit Variable	Symbol	Normalized Variable
Resonant frequency	$\omega_r=2\pi f_r$	-
Characteristic impedance	$Z_r=(L_p/C_p)^{1/2}$	-
Capacitance ratio	$k=C_T/C_p$	-
Symmetry coefficient	$h=n^2L_s/L_p=n^2C_p/C_s$	-
Voltage gain	$M=nU_2/U_1$	-
Time	t	$\theta=\omega_r t$
Second resonant frequency	$\omega_2=(L_pC_pC_T/(C_p+C_T))^{-1/2}$	$\omega_2=((1+k)/k)^{1/2}\omega_r$
Switching frequency	$f_s=1/T_s$	$f_n=f_s/f_r$
Half-cycle	$1/(2f_s)$	$\gamma=\pi/f_n$
Primary resonant capacitor voltage	$u_1(t)$	$m_1(\theta)=u_1(t)/U_1$
Secondary resonant capacitor voltage	$u_2(t)$	$m_2(\theta)=u_2(t)/U_1$
Primary resonant current	$i_1(t)$	$j_1(\theta)=Z_ri_1(t)/U_1$
Secondary resonant current	$i_2(t)$	$j_2(\theta)=Z_ri_2(t)/U_1$
Parallel capacitor voltage	$u_{CT}(t)$	$m_{CT}(\theta)=u_{CT}(t)/U_1$
Parallel capacitor current	$i_{CT}(t)$	$j_{CT}(\theta)=Z_ri_{CT}(t)/U_1$
Reflected output voltage	nU_2	M

For the P stage shown in Fig. 5(a), V_{CD} of the resonant tank is clamped to U_2, and the equivalent circuit can be described as a system of four-order differential equations in (9).

The corresponding normalizations are presented in Table I to facilitate the relevant derivation. In particular, there are four dominant normalization bases in (10).

$$\begin{cases} L_p\frac{di_{1P}}{dt} + u_{CTP} + u_{1P} = U_1 \\ u_{CTP} = L_{se}\frac{di_{2P}}{dt} + nU_2 + u_{2P} \\ i_{1P} = C_p\frac{du_{1P}}{dt}, i_{2P} = C_{se}\frac{du_{2P}}{dt} \\ i_{1P} = C_T\frac{du_{CTP}}{dt} + i_{2P} \end{cases} \tag{9}$$

$$Z_{\text{base}} = Z_r = \sqrt{L_p/C_p}, U_{\text{base}} = U_1,$$
$$I_{\text{base}} = U_{\text{base}}/Z_{\text{base}}, \omega_{\text{base}} = \omega_r = (L_pC_p)^{-1/2} = (L_sC_s)^{-1/2}. \tag{10}$$

The normalized special solution of P stage is derived in (11) shown at the bottom of the next page, where $k_1 = ((hk+h+1)/(hk))^{1/2} = f_{r\_l}/f_r$ is the normalized resonance-like frequency. $M_{1P}(\theta)$, $j_{1P}(\theta)$, $m_{2P}(\theta)$, and $j_{2P}(\theta)$ are the normalized values of u_{1P}, i_{1P}, u_{2P}, and i_{2P} during P stage, respectively. m_{1P0}, j_{1P0}, m_{2P0}, and j_{2P0} represent the initial values of $m_{1P}(\theta)$, $j_{1P}(\theta)$, $m_{2P}(\theta)$, and $j_{2P}(\theta)$, respectively.

Similar to P stage, the normalized special solution of N stage is obtained in (12), shown at the bottom of this page. Accordingly, $m_{1N}(\theta)$, $j_{1N}(\theta)$, $m_{2N}(\theta)$, and $j_{2N}(\theta)$ are the normalized values of u_{1N}, i_{1N}, u_{2N}, and i_{2N} during N stage, respectively. m_{1N0}, j_{1N0}, m_{2N0}, and j_{2N0} represent the initial values of $m_{1N}(\theta)$, $j_{1N}(\theta)$, $m_{2N}(\theta)$, and $j_{2N}(\theta)$, respectively.

As shown in Fig. 5(c), the equivalent circuit of O stage degenerates into a standard *LC* series network. The normalized special solution of O stage is derived in (13)

$$\begin{cases} m_{1O}(\theta) = \frac{1-m_{1O0}-m_{CTO0}}{k_2^2} + \frac{-1+m_{1O0}+m_{CTO0}}{k_2^2}\cos(k_2\theta) \\ \qquad + \frac{j_{1O0}}{k_2}\sin(k_2\theta) + m_{1O0} \\ j_{1O}(\theta) = j_{1O0}\cos(k_2\theta) - \frac{-1+m_{1O0}+m_{CTO0}}{k_2}\sin(k_2\theta) \\ m_{CTO}(\theta) = \frac{1-m_{1O0}-m_{CTO0}}{1+k} + \frac{-1+m_{1O0}+m_{CTO0}}{1+k}\cos(k_2\theta) \\ \qquad + \frac{j_{1O0}k_2}{1+k}\sin(k_2\theta) + m_{CTO0} \\ m_{2O}(\theta) = m_{2O0} \\ j_{2O}(\theta) = 0 \end{cases} \tag{13}$$

where $k_2 = ((k+1)/k)^{1/2}$, $m_{1O}(\theta)$, $m_{CTO}(\theta)$, $m_{2O}(\theta)$, $j_{1O}(\theta)$, and $j_{2O}(\theta)$ represent the normalized values of u_{1O}, u_{CTO}, u_{2O}, i_{1O}, and i_{2O} during O stage, respectively. m_{1O0}, m_{CTO0}, m_{2O0}, and j_{1O0} are the initial values of $m_{1O}(\theta)$, $m_{CTO}(\theta)$, $m_{2O}(\theta)$, and $j_{1O}(\theta)$, respectively.

It should be noted that k_2 is the normalized series resonant frequency of C_p, C_T, and L_p. In practice, the operation region of *LCCL* is usually designed in the ZVS region, and its switching frequency is always greater than k_2.

2) Analysis of Operation Modes: Depending on the sequences of the three resonant stages (P stage, N stage, and O stage) during the positive half cycle, *LCCL* resonant converter has nine possible operation modes: NO, NOP, NP, PN, PON, ON, ONO, N, and O. For the convenience of subsequent analysis, the switching frequency range is divided into three distinct areas: below resonance-like region ($k_2<f_n<k_1$) (BRLR), above resonance-like region ($f_n>k_1$) (ARLR), and resonance-like frequency ($f_n = k_1$). The characteristics associated with each mode are summarized in Table II.

Each operation mode is subject to several constraints. First, the current through inductor and voltage across capacitor should be continuous at the stage boundaries. Second, according to symmetry, the final values of the capacitor voltage and inductor current throughout a half cycle of steady-state operation should be opposite to their initial values. Third, the resonant current of rectifier side equals 0 at the joints of each two adjacent stages. In addition, since the inverting side and rectifier side are separated during O stage, energy is transferred to load only in P and N stages. Consequently, the normalized output current $I_{\text{out\_}n}$ is derived as follows, where θ_{P0} and θ_P represent the beginning and ending of P stage, respectively, and θ_{N0} and θ_N represent the beginning and ending of N stage, respectively:

$$\begin{aligned} I_{out\_n} &= f_n \int_0^{\pi/f_n} |j_2(\theta)| d\theta/\pi \\ &= f_n \left(\int_{\theta_{P0}}^{\theta_P} j_{2P}(\theta) d\theta - \int_{\theta_{N0}}^{\theta_N} j_{2N}(\theta) d\theta \right)/\pi \\ &= f_n (m_{2P}(\theta_P) - m_{2P}(\theta_{P0}) + m_{2N}(\theta_{N0}) \\ &\quad - m_{2N}(\theta_N))/(\pi h). \end{aligned} \tag{14}$$

Furthermore, the normalized output power $P_{\text{out\_}n}$ is obtained in (15). Besides, there is a unique constraint that applies to NO, NOP, ON, PON, and ONO. That is, the resonant current of

$$\begin{cases} m_{1P}(\theta) = \frac{1+hk-M}{1+h+hk} + \frac{-1+M+m_{1P0}+m_{2P0}}{1+h}\cos(\theta) + \frac{j_{1P0}+hj_{2P0}}{1+h}\sin(\theta) - \frac{(h+M)+k_1^2(m_{2P0}-hm_{1P0})}{(1+h)k_1^2}\cos(k_1\theta) \\ \qquad + \frac{h(j_{1P0}-j_{2P0})}{(1+h)k_1}\sin(k_1\theta) \\ j_{1P}(\theta) = \frac{j_{1P0}+hj_{2P0}}{1+h}\cos(\theta) - \frac{-1+M+m_{1P0}+m_{2P0}}{1+h}\sin(\theta) + \frac{h(j_{1P0}-j_{2P0})}{1+h}\cos(k_1\theta) + \frac{(h+M)+k_1^2(m_{2P0}-hm_{1P0})}{(1+h)k_1}\sin(k_1\theta) \\ m_{2P}(\theta) = -\frac{h(-1+M+kM)}{1+h+hk} + \frac{h(j_{1P0}+hj_{2P0})}{1+h}\sin(\theta) + \frac{h(j_{2P0}-j_{1P0})}{(1+h)k_1}\sin(k_1\theta) + \frac{h(-1+M+m_{1P0}+m_{2P0})}{1+h}\cos(\theta) \\ \qquad + \frac{(h+M)+k_1^2(m_{2P0}-hm_{1P0})}{(1+h)k_1^2}\cos(k_1\theta) \\ j_{2P}(\theta) = \frac{j_{1P0}+hj_{2P0}}{1+h}\cos(\theta) + \frac{j_{2P0}-j_{1P0}}{1+h}\cos(k_1\theta) - \frac{-1+M+m_{1P0}+m_{2P0}}{1+h}\sin(\theta) - \frac{(h+M)+k_1^2(m_{2P0}-hm_{1P0})}{h(1+h)k_1}\sin(k_1\theta) \end{cases} \tag{11}$$

$$\begin{cases} m_{1N}(\theta) = \frac{1+hk+M}{1+h+hk} + \frac{-1-M+m_{1N0}+m_{2N0}}{1+h}\cos(\theta) + \frac{j_{1N0}+hj_{2N0}}{1+h}\sin(\theta) - \frac{(h-M)+k_1^2(m_{2N0}-hm_{1N0})}{(1+h)k_1^2}\cos(k_1\theta) \\ \qquad + \frac{h(j_{1N0}-j_{2N0})}{(1+h)k_1}\sin(k_1\theta) \\ j_{1N}(\theta) = \frac{j_{1N0}+hj_{2N0}}{1+h}\cos(\theta) - \frac{-1-M+m_{1N0}+m_{2N0}}{1+h}\sin(\theta) + \frac{h(j_{1N0}-j_{2N0})}{1+h}\cos(k_1\theta) \\ \qquad + \frac{(h-M)+k_1^2(m_{2N0}-hm_{1N0})}{(1+h)k_1}\sin(k_1\theta) \\ m_{2N}(\theta) = -\frac{h(-1-M-kM)}{1+h+hk} + \frac{h(j_{1N0}+hj_{2N0})}{1+h}\sin(\theta) + \frac{h(j_{2N0}-j_{1N0})}{(1+h)k_1}\sin(k_1\theta) + \frac{h(-1-M+m_{1N0}+m_{2N0})}{1+h}\cos(\theta) \\ \qquad + \frac{(h-M)+k_1^2(m_{2N0}-hm_{1N0})}{(1+h)k_1^2}\cos(k_1\theta) \\ j_{2N}(\theta) = \frac{j_{1N0}+hj_{2N0}}{1+h}\cos(\theta) + \frac{j_{2N0}-j_{1N0}}{1+h}\cos(k_1\theta) - \frac{-1-M+m_{1N0}+m_{2N0}}{1+h}\sin(\theta) - \frac{(h-M)+k_1^2(m_{2N0}-hm_{1N0})}{h(1+h)k_1}\sin(k_1\theta) \end{cases} \tag{12}$$

TABLE II
OPERATION CHARACTERISTICS OF *LCCL* RESONANT CONVERTER

	$k_2<f_n<k_1$					$f_n=k_1$			$f_n>k_1$				
Mode	NP	NOP	NO	ONO	O	N	ONO	O	PN	PON	ON	ONO	O
Inverting switches	ZVS/ ZCS	ZVS/ ZCS	ZVS/ ZCS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS
Rectifier switches	Hard switching	ZCS	ZCS	ZCS	OFF	ZCS	ZCS	OFF	Hard switching	ZCS	ZCS	ZCS	OFF
Voltage gain	Indefinite		$M>h$			$M=h$	$M>h$			$M<h$		Indefinite	
Output current	Large→small					Large→small			Large→small				

Zero-voltage switching (ZVS), zero-current switching (ZCS).

rectifier side is continuous and differentiable when the resonant tank is switching from O stage to P or N stage (i.e., the absolute value of V_{CD} reaches U_2 exactly when the circuit is commuting from O stage to P or N stage). NP is selected as an example to demonstrate the aforementioned constraints in (16)

$$\begin{aligned} P_{out\_n} &= MI_{\text{out\_}n} \\ &= Mf_n\left(m_{2P}\left(\theta_P\right)-m_{2P}\left(\theta_{P0}\right)\right. \\ &\quad \left.+m_{2N}\left(\theta_{N0}\right)-m_{2N}\left(\theta_N\right)\right)/(\pi h) \end{aligned} \tag{15}$$

$$\begin{cases} j_{1N}\left(\theta_N\right)=j_{1P}\left(\theta_{P0}\right), j_{2N}\left(\theta_N\right)=0 \\ m_{1N}\left(\theta_N\right)=m_{1P}\left(\theta_{P0}\right), m_{2N}\left(\theta_N\right)=m_{2P}\left(\theta_{P0}\right) \\ j_{1N}\left(\theta_{N0}\right)+j_{1P}\left(\theta_P\right)=0, j_{2N}\left(\theta_{N0}\right)+j_{2P}\left(\theta_P\right)=0 \\ m_{1N}\left(\theta_{N0}\right)+m_{1P}\left(\theta_P\right)=0, m_{2N}\left(\theta_{N0}\right)+m_{2P}\left(\theta_P\right)=0 \\ \theta_{N0}=0, \theta_{P0}=\theta_N, \theta_P=\pi/f_n \\ \int_{\theta_{N0}}^{\theta_P}\left|j_2\left(\theta\right)\right|d\theta=-\int_{\theta_{N0}}^{\theta_N} j_{2N}\left(\theta\right)d\theta+\int_{\theta_{P0}}^{\theta_P} j_{2P}\left(\theta\right)d\theta \\ =\left(m_{2N}\left(\theta_{N0}\right)-m_{2N}\left(\theta_N\right)+m_{2P}\left(\theta_P\right)-m_{2P}\left(\theta_{P0}\right)\right)/h \\ =-2m_{2N}\left(\theta_N\right)/h=\pi I_{\text{out\_}n}/f_n \end{cases} \tag{16}$$

where θ_{N0} represents the beginning of NP mode as 0, θ_P denotes the ending of NP mode as π/f_n, and θ_N or θ_{P0} indicates the moment when the resonant tank is commuting from N stage to P stage. Similarly, nonlinear transcendental equations, such as (16) can be derived for other modes. However, the analytical solutions can only be found for N mode. For other modes, only numerical solutions can be obtained with computer assistance. In conclusion, the numerical solutions of time-domain response of *LCCL* resonant tank for each mode can be accurately obtained. As a demonstration, the precise waveform of NP mode obtained through TDM is shown in Fig. 6.

The analytical solution of N mode is derived in (17) and (18). Actually, $j_{2N}(\theta)$ of N mode should be nonpositive during the positive half cycle. Therefore, the load condition (e.g., the normalized output current $I_{\text{out\_}n}$) of N mode should be no less than a critical value. Otherwise, the resonant tank will operate in ONO mode. The critical load condition of $I_{\text{out\_}n}$ is introduced as I_{b_n}, which is derived in (19)

$$\begin{cases} m_{1N0}=-\pi h I_{\text{out\_}n}/(2k_1) \\ j_{1N0}=-\left(h+1\right)\tan\left(\pi/(2k_1)\right) \\ m_{2N0}=\pi h I_{\text{out\_}n}/(2k_1) \\ j_{2N0}=0 \\ M=h \end{cases} \tag{17}$$

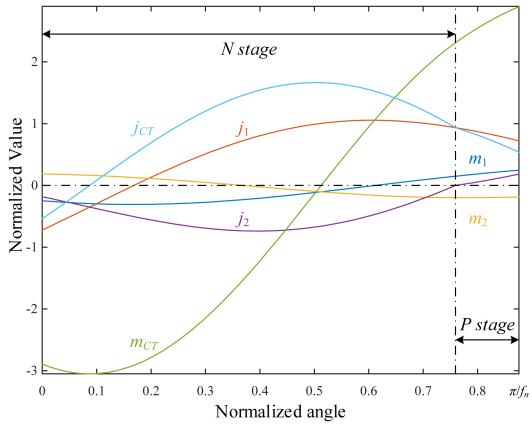

Fig. 6. Typical operation waveform of NP mode.

$$\begin{cases} m_{1N}\left(\theta\right)=1-\cos\left(\theta\right)-\tan\left(\pi/(2k_1)\right)\sin\left(\theta\right) \\ \qquad -\pi h I_{\text{out\_}n}\cos\left(k_1\theta\right)/(2k_1) \\ \qquad -h\tan\left(\pi/(2k_1)\right)\sin\left(k_1\theta\right)/k_1 \\ j_{1N}\left(\theta\right)=\sin\left(\theta\right)-\tan\left(\pi/(2k_1)\right)\cos\left(\theta\right) \\ \qquad +\pi h I_{\text{out\_}n}\sin\left(k_1\theta\right)/2 \\ \qquad -h\tan\left(\pi/(2k_1)\right)\cos\left(k_1\theta\right) \\ m_{2N}\left(\theta\right)=h-h\cos\left(\theta\right)-h\tan\left(\pi/(2k_1)\right)\sin\left(\theta\right) \\ \qquad +\pi h I_{\text{out\_}n}\cos\left(k_1\theta\right)/(2k_1) \\ \qquad +h\tan\left(\pi/(2k_1)\right)\sin\left(k_1\theta\right)/k_1 \\ j_{2N}\left(\theta\right)=\sin\left(\theta\right)-\tan\left(\pi/(2k_1)\right)\cos\left(\theta\right) \\ \qquad -\pi I_{\text{out\_}n}\sin\left(k_1\theta\right)/2 \\ \qquad +\tan\left(\pi/(2k_1)\right)\cos\left(k_1\theta\right) \end{cases} \tag{18}$$

$$I_{b\_n}=\frac{2}{\pi k_1}. \tag{19}$$

3) Mode Boundaries and Distribution: To circumvent the complexity of solving all the voltage gain curves, the boundaries between various modes can be derived first to provide more essential perceptions of *LCCL*. The mode boundary can be considered as a critical case of operation modes or a particular boundary mode, e.g., the mode boundary between NOP and NP is that V_{CD} of a critical NP mode reaches U_2 exactly at the ending of N stage. Consequently, this boundary can be obtained by solving NP mode equations attached with the extra constraint of the previously specified critical NP mode. In addition, the mode boundaries are exclusively associated with the parameters of the resonant tank, and the load condition is no longer required

TABLE III
BOUNDARY CONSTRAINTS OF OPERATION MODES

Mode boundaries	Solving mode	Constraint
ONO/NOP	NO	$m_{CTN}(\theta_{N0})$-$m_{2N}(\theta_{N0})$=-M or $m_{CTO}(\pi/f_n)$-$m_{2O}(\pi/f_n)$=M
NOP/NP	NP	$m_{CTN}(\theta_{P0})$-$m_{2N}(\theta_{P0})$=M
ONO/PON	ON	$m_{CTO}(\theta_{N0})$-$m_{2O}(\theta_{N0})$=-M
PON/PN	PN	$m_{CTP}(\theta_{N0})$-$m_{2P}(\theta_{N0})$=-M

for their derivation. In addition to the regular mode boundary, three boundary modes exist: NO mode at the boundary between ONO and NOP modes, ON mode at the boundary between ONO and PON modes, and O mode under zero-load conditions. All the boundary conditions are provided in Table III, where $m_{CTP}(\theta)$ and $m_{CTN}(\theta)$ are the normalized values of u_{CTP} during P stage and u_{CTN} during N stage, respectively.

For O mode with zero-load condition, no power is delivered to the rectifier side and all energy is circulated in the inverting side resonant tank. The analytical solution of O mode under zero-load is derived as follows:

$$\begin{cases} m_{1O0} = 0 \\ j_{1O0} = -\tan\left(k_2\pi/(2f_n)\right)/k_2 \\ m_{CTO0} = 0 \end{cases} \tag{20}$$

$$\begin{cases} m_{1O}(\theta) = \frac{k}{k+1}\left(1-\tan\left(\frac{k_2\pi}{2f_n}\right)\sin\left(k_2\theta\right)-\cos\left(k_2\theta\right)\right) \\ j_{1O}(\theta) = \frac{1}{k_2}\left(\sin\left(k_2\theta\right)-\tan\left(\frac{k_2\pi}{2f_n}\right)\cos\left(k_2\theta\right)\right) \\ m_{CTO}(\theta) = \frac{1}{k+1}\left(1-\tan\left(\frac{k_2\pi}{2f_n}\right)\sin\left(k_2\theta\right)-\cos\left(k_2\theta\right)\right). \end{cases} \tag{21}$$

Since the output capacitor is separated from the resonant tank during the entire switching cycle of O mode, the absolute value of voltage across parallel capacitor C_T should not exceed the voltage gain M. M_O denotes the gain curve of the critical O mode with zero-load as follows:

$$\begin{aligned} M \geq \left|m_{CTO}\left(\theta\right)\right|_{\max} &= \left|m_{CTO}\left(\frac{\pi}{2f_n}\right)\right| \\ &= \frac{\sec\left(k_2\pi/(2f_n)\right)-1}{k+1} = M_O. \end{aligned} \tag{22}$$

Fig. 7 depicts the typical mode boundaries and distribution of *LCCL* on f_n–M plane, which only depends on parameters k and h.

4) Comparison of Gain Characteristics With Other Bidirectional Resonant Topologies: Considering that the gain curve M_O of the critical O mode can be expressed analytically, the gain characteristics of the critical O mode were adopted as a criterion to evaluate the gain capability of different bidirectional resonant topologies (e.g., *CLLC* [30] and *LCLL* [39]). Referring to the resonance parameter equivalence principle of [30] and [40], the gain characteristics of *LCLL* during bidirectional operations can always be equated to corresponding *LLC*. Furthermore, according to the conclusion of [30], *LLC* is merely an extreme special case of S-type *CLLC*. Therefore, the critical O mode gain curve of *LLC* is the same as *CLLC*. As a result, it is only necessary to compare the gain characteristics of the critical O mode for *LCCL* and *CLLC*. The gain characteristics

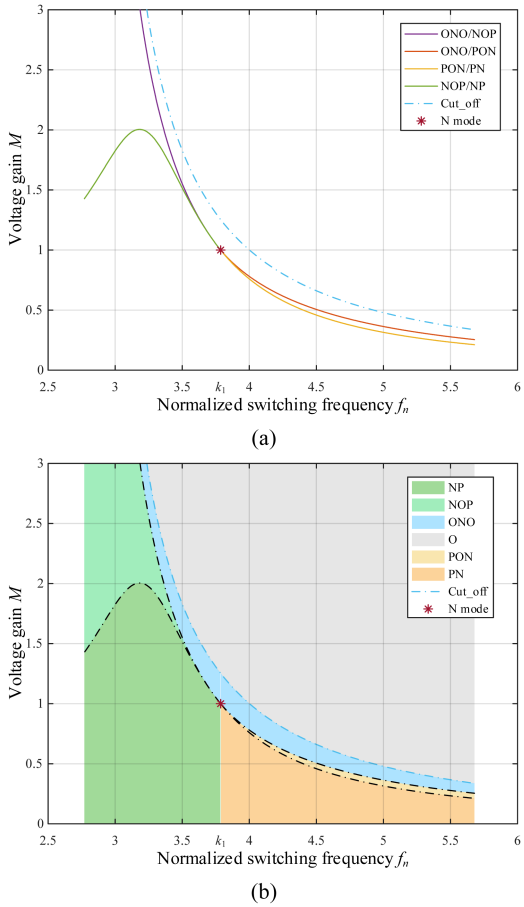

Fig. 7. Typical mode boundaries and distribution of *LCCL* on f_n–M plane. (a) Mode boundaries. (b) Mode distribution.

of the critical O mode for *CLLC* is provided in [30], as follows, where k_L indicates the ratio of the resonant inductance to the magnetizing inductance of *CLLC* inverting side:

$$M_{O\_CLLC} = \frac{1}{k_L+1}\sec\left(\sqrt{\frac{k_L}{k_L+1}}\pi \Big/ (2f_n)\right). \tag{23}$$

To comprehensively compare M_O and $M_{O\cdot CLLC}$, both of them are normalized again according to their constant voltage gain (e.g., $f_n = k_1$, $M = h$ for *LCCL* and $f_n = 1$, and $M = 1$ for *CLLC*), respectively. Therefore, both M_O^* and $M_{O\_CLLC}^*$ are introduced as follows as the normalized M_O and $M_{O\cdot CLLC}$, where f_n^* denotes the relative magnitude of f_n with respect to the respective constant voltage gain frequency (e.g., $f_n = k_1$ for *LCCL* and $f_n = 1$ for *CLLC*):

$$\begin{cases} M_O^* = \frac{M_O}{h} \\ f_n^* = \frac{f_n}{k_1} \end{cases} \Rightarrow M_O^* = \frac{1}{h\left(k+1\right)}\left(\sec\left(\frac{k_2\pi}{2f_n^* k_1}\right)-1\right) \tag{24}$$

$$\begin{cases} M_{O\_CLLC}^* = \frac{M_{O\_CLLC}}{1} \\ f_n^* = \frac{f_n}{1} \end{cases}$$

$$\Rightarrow M_{O\_CLLC}^* = \frac{1}{k_L+1}\sec\left(\sqrt{\frac{k_L}{k_L+1}}\pi \Big/ (2f_n^*)\right). \tag{25}$$

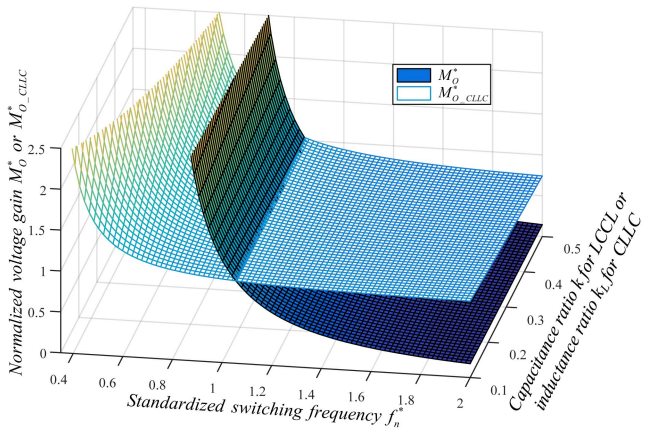

Fig. 8. Variations of normalized voltage gain M_O^* and $M_{O\_CLLC}^*$ with respect to standardized switching frequency f_n^* and (k or k_L).

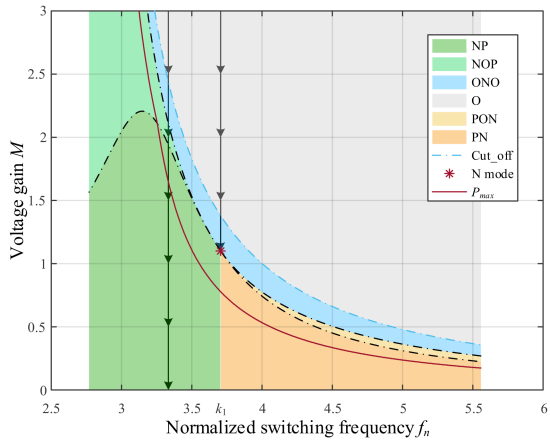

Fig. 9. Modes distribution and $P_{\max}$ at certain frequency of *LCCL* in f_n–M plane.

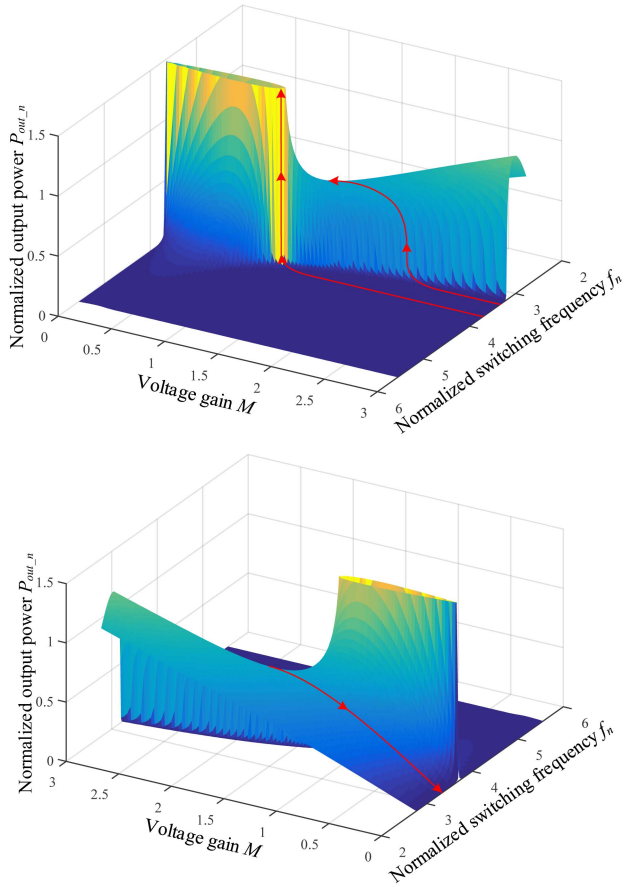

Fig. 10. Variation of $P_{\text{out\_}n}$ versus f_n and M from different perspectives.

The variations of M_O^* and $M_{O\_CLLC}^*$ versus f_n^* and (k or k_L) are illustrated in Fig. 8, in which $k \equiv k_L$, $h = 1$ holds. Obviously, for $f_n^* < 1$, *LCCL* has stronger capability to raise voltage than *CLLC*; for $f_n^* > 1$, *LCCL* possesses superior characteristic to lower voltage compared to *CLLC*. Therefore, at the cost of replacing magnetizing inductance with a parallel resonant capacitor C_T, *LCCL* obtains enhanced voltage gain characteristics compared to *CLLC* and *LCLL*.

5) Output Characteristics Analysis: To analyze the output characteristics of *LCCL* elaborately, all operating points of the entire f_n–M plane are mapped into f_n–M–$P_{\text{out\_}n}$ space through time-domain calculation, as illustrated in Figs. 9 and 10. For an *LCCL* operating at a specific frequency (i.e., the arrow line) depicted in Figs. 9 and 10, as the voltage gain M decreases from a larger value to 0 gradually, the operating mode of resonant tank passes through multiple modes in sequence, beginning with O mode and finally behaving as output short-circuited state with $M = 0$. During the reduction of M, $P_{\text{out\_}n}$ is zero both in O mode and output short-circuited state, indicating that $P_{\text{out\_}n}$ begins by increasing from 0 to some peak value $P_{\max}$ and subsequently reduces to 0. However, for an *LCCL* operating at resonant-like frequency $f_n = k_1$, as the voltage gain M decreases from a larger value to h, the operating mode of *LCCL* sequentially goes through O mode, ONO mode, and finally behaves as N mode at $M = h$. As previously discussed N mode in (19), *LCCL* operating at $f_n = k_1$ will remain N mode as long as $I_{\text{out\_}n} \geqq I_{b\_n}$. Consider the corresponding $P_{\text{out\_}n}$ for N mode is $P_{\text{out\_}n} = MI_{\text{out\_}n} \geqq hI_{b\_n}$, i.e., *LCCL* operating in N mode can provide an infinite amount of power. As M continues to decrease from h, the response of resonant tank will oscillate and diverge, which in practice should be avoided.

Aiming to analyze the output characteristics of *LCCL* more intuitively, both Fig. 10 and corresponding $P_{\max}$ at certain frequency of *LCCL* are projected to f_n–$P_{\text{out\_}n}$ plane, as shown in Fig. 11. Clearly, for an *LCCL* operating at a specific frequency (i.e., the arrow line) depicted in Fig. 10, the variation of $P_{\text{out\_}n}$ is nonmonotonic as M decreases, which means that the relevant projection of Fig. 10 will cover the f_n–$P_{\text{out\_}n}$ plane twice. Therefore, Fig. 11 is further split into two subplots in Fig. 12(a) and (b) illustrated the region where $P_{\text{out\_}n}$ increases or decreases monotonically with M decreases at certain frequency, respectively.

It is not difficult to observe that the mode boundaries ONO/NOP, NOP/NP, ONO/PON, and PON/PN depicted in Fig. 9 intersect at the point (k_1, h) on f_n–M plane. Similarly, those boundaries shown in Fig. 11 also intersect at a certain point

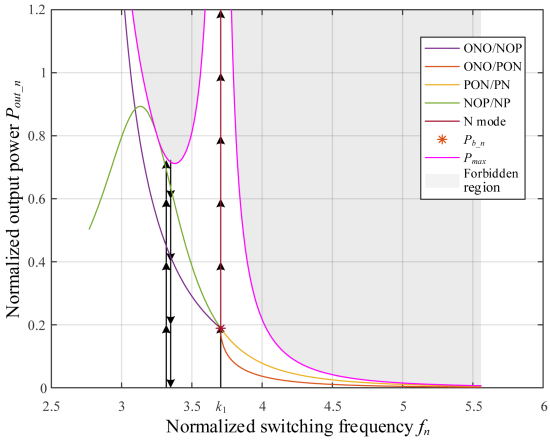

Fig. 11. Modes distribution and $P_{\max}$ at certain frequency of *LCCL* in f_n–$P_{\text{out\_}n}$ plane.

TABLE IV
CONSTRAINTS FOR BOUNDARIES INTERSECTIONS

Intersection	Solving mode	Constraint
ONO/NOP, ONO/PON, PON/PN, NOP/NP	N	$m_{CTN}(\theta_{N0})$-$m_{2N}(\theta_{N0})$=-M=-h or $m_{CTN}(\theta_{P0})$-$m_{2N}(\theta_{P0})$=M=h

P_{b_n} on f_n–$P_{\text{out\_}n}$ plane, indicating that the relevant intersection of those boundaries is a special N mode. Consequently, this particular N mode can be obtained by attaching corresponding mode boundary constraints to N mode. The mode boundary constraints for the intersection are provided in Table IV.

The output current $I_{\text{out\_}n}$ and output power P_{b_n} of the intersection are derived as follows, which is exactly the load condition of the critical N mode in (19):

$$\begin{cases} I_{\text{out\_}n} = \dfrac{2}{\pi k_1} = I_{b\_n} \\ P_{b\_n} = hI_{b\_n} = \dfrac{2h}{\pi k_1}. \end{cases} \tag{26}$$

Finally, the constant $P_{\text{out\_}n}$ projection of Fig. 10 on f_n–M plane is depicted in Fig. 13. By analyzing Figs. 9–13, it is concluded that for an *LCCL* operating in constant $P_{\text{out\_}n}$ mode, the gain curves become nonmonotonic if $P_{\text{out\_}n}$ exceeds the minimum value of $P_{\max}$ in BRLR. Therefore, to obtain monotonic gain curves both in BRLR and ARLR, the maximum value of $P_{\text{out\_}n}$ should be no greater than the minimum value of $P_{\max}$ in BRLR.

The requirement of inverting side of *LCCL* to achieve ZVS during forward operation is described as

$$\begin{aligned} |j_{10}|\, I_{\text{base}} t_{\text{dead}} &\geq 2C_{\text{oss}} U_1 \\ |j_{10}|\, t_{\text{dead}} &\geq 2C_{\text{oss}} Z_r \end{aligned} \tag{27}$$

where j_{10} represents the normalized i_1 at the beginning of the positive half cycle, t_{dead} denotes the dead time, and C_{oss} is the output capacitor of corresponding switches.

The gain curves and corresponding ZVS current j_{10} of *LCCL* under different $P_{\text{out\_}n}$ conditions are precisely obtained through numerical calculation, as shown in Fig. 14.

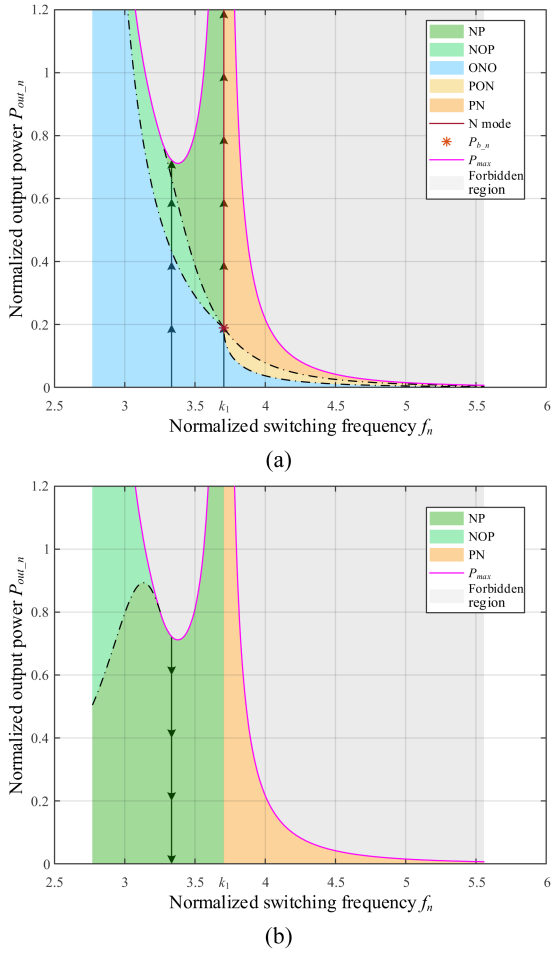

Fig. 12. Variation of $P_{\text{out\_}n}$ as M decreases at certain frequency, (a) where $P_{\text{out\_}n}$ increases monotonically as M decreases and (b) where $P_{\text{out\_}n}$ decreases monotonically as M decreases.

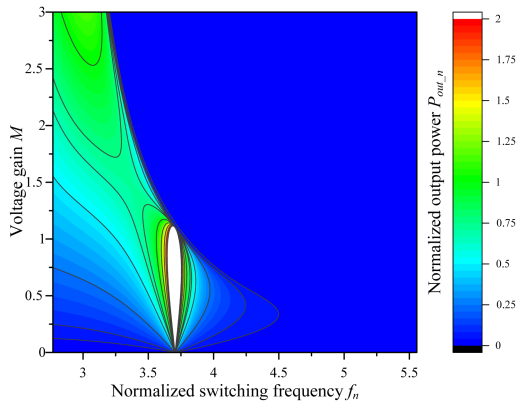

Fig. 13. Projection of constant $P_{\text{out\_}n}$ gain curves on f_n–M plane.

B. Reverse Mode

For the reverse operation of *LCCL* shown in Fig. 15, the following definitions are introduced, where subscript R denotes the corresponding normalization bases adopted for reverse

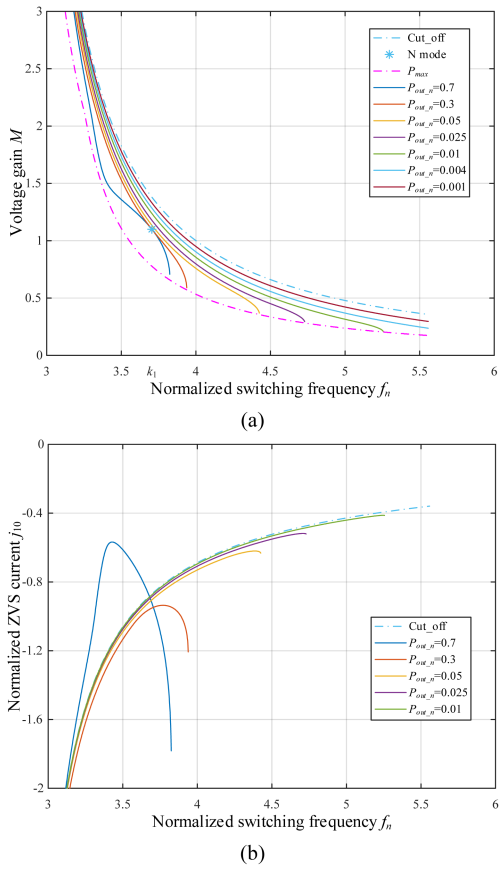

Fig. 14. Gain curves under different $P_{\text{out\_}n}$ (a) and corresponding ZVS current j_{10} (b).

operation:

$$\begin{cases} k' = C_T/C_{se} = hk \\ h' = L_p/L_{se} = 1/h \end{cases} \tag{28}$$

$$Z_{\text{base\_}R} = Z_{r\_R} = \sqrt{L_{se}/C_{se}} = hZ_r, U_{\text{base\_}R} = nU_2,$$
$$I_{\text{base\_}R} = U_{\text{base\_}R}/Z_{\text{base\_}R}, \omega_{\text{base\_}R}$$
$$= \omega_r = (L_{se}C_{se})^{-1/2} = (L_pC_p)^{-1/2}. \tag{29}$$

Clearly, only individual parameters (e.g., k' and h') differ between the reverse and forward modes of *LCCL*. Therefore, the corresponding modes analysis and output characteristics of the reverse mode are similar to those of the forward mode, which will not be further repeated here.

The constraint of inverting side of *LCCL* to achieve ZVS during reverse operation is specified as follows, where j_{20_R} represents the normalized i_{2_R} at the beginning of the positive half cycle:

$$\begin{aligned} n\,|j_{20\_R}|\,I_{\text{base\_}R}t_{\text{dead}} &\geq 2C_{\text{oss}}U_2 \\ n\,|j_{20\_R}|\,\frac{nU_2}{Z_{r\_R}}t_{\text{dead}} &\geq 2C_{\text{oss}}U_2 \\ |j_{20\_R}|\,n^2t_{\text{dead}} &\geq 2C_{\text{oss}}Z_{r\_R}. \end{aligned} \tag{30}$$

TABLE V
DESIGN SPECIFICATIONS FOR *LCCL* RESONANT CONVERTER

Parameter	Symbol	Value
Input voltage	U_1	400V
Battery voltage range	$U_{2m} \sim U_{2M}$	250V~450V
Rated power	P_{rated}	1kW
Resonant-like frequency	f_{r_l}	100kHz
Operating frequency range	$f_{s,min} \sim f_{s,max}$	75kHz~150kHz

IV. DESIGN METHODOLOGY

According to Section III, only five parameters (L_p, C_p, k, h, n) are required to describe *LCCL* fully. The wide range of battery voltage poses significant challenges to the design of bidirectional *LCCL* converter. However, the optimal S-type *LCCL* that addresses the wide voltage range of battery applications can be developed through rational tradeoff of (L_p, C_p, k, h, n). This section will explain the design methodology in detail.

A bidirectional *LCCL* converter rated at 1 kW is adopted as an example to demonstrate the proposed design method. Tabulated in Table V are the corresponding design specifications.

Considering voltage and current levels for bidirectional operations, the SCT3080AL MOSFET is selected for both inverting and rectifier sides. By analyzing its datasheet, it is easy to discern that SCT3080AL's C_{oss} decreases monotonically as the drain-source voltage increases. Since the V_{ds} on the primary side is kept at 400 V, its corresponding C_{oss} is estimated to be 119.3437 pF by data interpolation. Similarly, as the V_{ds} of the secondary side vary within 250–450 V, its corresponding maximum C_{oss} is estimated to be 147.1616 pF by data-interpolation when V_{ds} is 250 V. Considering parasitic parameters and other nonideal factors, a reasonable margin is reserved for the following analysis. The output capacitor of primary switches and secondary switches are set to 125 and 150 pF, respectively. In addition, the dead time is determined to be 100 ns considering the switching frequency and device characteristics, specified as follows:

$$\begin{cases} C_{\text{oss1}} = 125\,\text{pF} \\ C_{\text{oss2}} = 150\,\text{pF} \\ t_{\text{dead}} = 100\,\text{ns}. \end{cases} \tag{31}$$

Initially, the minimum switching $f_{s,\,\text{min}}$ for bidirectional operations should be located in BRLR ($k_2 < f_n < k_1$), as shown in (32). Besides, the capacitor ratio for bidirectional operations should be appropriate. *LCCL* with too small capacitor ratio k or k' degenerates into an SRC, hence weakening its voltage regulation capability. Excessive capacitor ratio k or k' results in large circulating reactive power, which reduces the operating efficiency of *LCCL* converter. Therefore, the capacitor ratio of *LCCL* for bidirectional operations is limited to 0.1 – 0.3 in this article, as shown in (34)

$$\begin{cases} k > 0\ \&\ h > 0\ \&\ \frac{f_{s,\text{min}}}{f_r} > k_2 \\ k' > 0\ \&\ h' > 0\ \&\ \frac{f_{s,\text{min}}}{f_r} > k_2' \\ f_{r\_l} = \sqrt{\frac{hk+h+1}{hk}}f_r = 100\,\text{kHz} \end{cases}$$

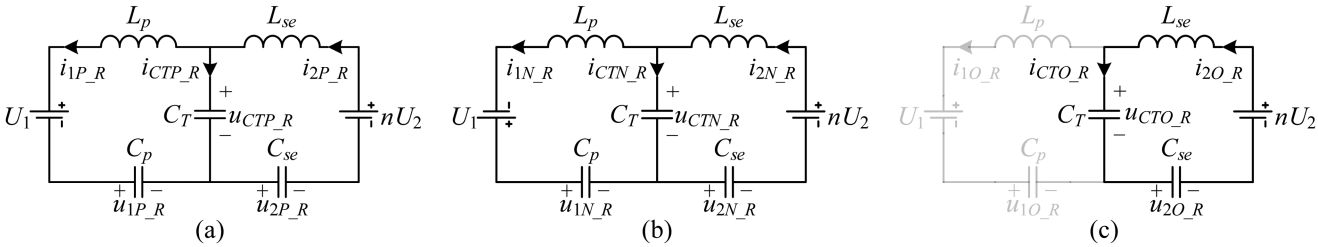

Fig. 15. Equivalent circuit of the *LCCL* in (a) P stage, (b) N stage, and (c) O stage for reverse operation.

$$\Rightarrow \begin{cases} k>0 \;\&\; h>0 \;\&\; \frac{3}{4}\sqrt{\frac{hk+h+1}{hk}} > \sqrt{\frac{k+1}{k}} \\ k>0 \;\&\; h>0 \;\&\; \frac{3}{4}\sqrt{\frac{hk+h+1}{hk}} > \sqrt{\frac{hk+1}{hk}} \end{cases}$$

$$\Rightarrow \begin{cases} k>0 \;\&\; h>0 \;\&\; 7h\,(k+1) \le 9 \\ k>0 \;\&\; h>0 \;\&\; 7k<9 \;\&\; 7hk+7 \le 9h \end{cases} \tag{32}$$

where k'_2 is the normalized series resonant frequency of C_{se}, C_T, and L_{se} during reverse operation, as follows:

$$k'_2 = \sqrt{(k'+1)/k'} = \sqrt{(hk+1)/(hk)} \tag{33}$$

$$\begin{cases} 0.1 \le k \le 0.3 \\ 0.1 \le k' \le 0.3 \end{cases} \Rightarrow \begin{cases} 0.1 \le k \le 0.3 \\ 0.1 \le kh \le 0.3. \end{cases} \tag{34}$$

Furthermore, the influence of n on the bidirectional voltage gain of *LCCL* is characterized in (35). Assuming that *LCCL* will experience N mode at $f_s = f_{r\_l}$ with the rated load during bidirectional operations, the relationship between h and n can be determined as

$$\begin{cases} M_m = \frac{nU_{2m}}{U_1} \le h \le M_M = \frac{nU_{2M}}{U_1} \\ M_{Rm} = \frac{1}{M_M} \le h' = \frac{1}{h} \le M_{RM} = \frac{1}{M_m} \end{cases}$$

$$\Rightarrow \frac{nU_{2m}}{U_1} \le h \le \frac{nU_{2M}}{U_1} \tag{35}$$

where M_m–M_M represents the voltage gain range of forward operation, M_{Rm}–M_{RM} denotes the voltage gain of reverse operation.

In addition, Fig. 16 presented the typical gain curves of *LCCL* under different load conditions of forward operation, where M_{rated} denotes the gain curve for rated power, M_O depicts the gain curve for O mode under zero-load condition, and f_{nM} and f_{nm} are the normalized maximum and minimum frequencies according to Table V, as derived in (36). According to Section III, within the desired operating frequency range, it is more challenging to raise voltage for heavier loads in BRLR and difficult to lower voltage for lighter loads in ARLR. To put it in another way, *LCCL* can achieve the designed maximum voltage gain M_M and M_{RM} under any load condition provided that it is capable of realizing the designed maximum voltage gain M_M and M_{RM} within the designed frequency range in BRLR under rated load conditions. Similarly, the designed minimum voltage gain M_m and M_{Rm} can be attained under any load condition as long as *LCCL* is capable of achieving them within the designed

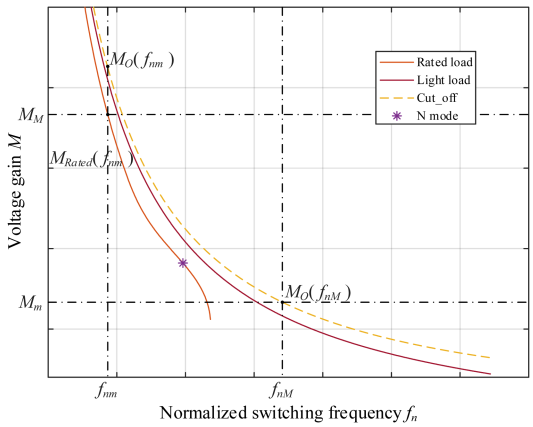

Fig. 16. Typical gain curve of *LCCL* under different load conditions.

frequency range in ARLR under the lightest load condition

$$\begin{cases} f_{nM} = \frac{f_{s,\max}}{f_r} = \frac{f_{s,\max}}{f_{r\_l}/k_1} = \frac{3}{2}\sqrt{\frac{hk+h+1}{hk}} \\ f_{nm} = \frac{f_{s,\min}}{f_r} = \frac{f_{s,\min}}{f_{r\_l}/k_1} = \frac{3}{4}\sqrt{\frac{hk+h+1}{hk}}. \end{cases} \tag{36}$$

The most extreme light-load condition of *LCCL* is zero-load conditions, also known as O mode, which has the strongest capability to raise voltage and the weakest capability to lower voltage. The gain characteristic M_O of the critical O mode is provided in (37). Consequently, it is simple to establish the following constraints for *LCCL* whose characteristics satisfy the forward design voltage gain:

$$M_O = \frac{\sec\left(k_2\pi/(2f_n)\right) - 1}{k+1} \tag{37}$$

$$M_{\text{Rated}}\left(f_{nm}\right) \ge M_M \tag{38}$$

$$M_O\left(f_{nM}\right) \le M_m. \tag{39}$$

Unfortunately, the gain curve of rated power or M_{rated} can only be obtained through numerical calculation, which cannot be utilized for further analytical derivation. Considering that the gain curve M_O for zero-load O mode is described analytically and *LCCL* has the strongest capability to raise voltage at this time, (38) is compromised and deduced into (40) for further derivation. Note that the following equation is a necessary but

insufficient constraint:

$$M_O\left(f_{nm}\right) \geq M_{\text{Rated}}\left(f_{nm}\right) \geq M_M \Rightarrow M_O\left(f_{nm}\right) \geq M_M. \tag{40}$$

So far, the gain constraints for forward operation have been derived, as described in (39) and (40), which are further simplified in (41) and (42), respectively. Here, (41) is a necessary and sufficient condition, while (42) is a necessary but insufficient condition

$$\frac{\sec\left(k_2\pi/(2f_{nM})\right)-1}{k+1} \leq M_m \tag{41}$$

$$\frac{\sec\left(k_2\pi/(2f_{nm})\right)-1}{k+1} \geq M_M. \tag{42}$$

Correspondingly, there are constraints similar to (41) and (42) in (43) and (44) for reverse operation of *LCCL*

$$\frac{\sec\left(k_2'\pi/(2f_{nM})\right)-1}{k'+1} \leq M_{Rm} \tag{43}$$

$$\frac{\sec\left(k_2'\pi/(2f_{nm})\right)-1}{k'+1} \geq M_{RM}. \tag{44}$$

Equations (41), (42), (43), and (44) are further deduced into (45), (46), (47), and (48), respectively, where D_p denotes the potential solution domain of (k, h) associated with (32) and (34).

By combining (45)–(48), shown at the bottom of the next page. it is not difficult to determine the possible value of transformer ratio n as (49). So far, all the design constraints imposed by the design specifications are summarized in (32)–(35) and (41)–(44). Accordingly, for a specific n, the potential design parameters (k, h) that satisfy the specifications can be obtained by combining (32)–(35) and (41)–(44). Fig. 17 depicts the permissible regions for parameters (k, h) when n takes several possible values

$$0.49337 \leq n \leq 2.88267. \tag{49}$$

The possible design parameters (n, k, h) are now derived. However, the specific design parameters remain unknown (e.g., Z_r, L_p, C_p). The iterative process of specific design parameters associated with certain (n, k, h) are interpreted in detail below. Considering the manufacturability of transformer, the transformer ratio n is iterated in steps of 0.1.

Step 1: Given n and the associated permissible region of (k, h) according to (32)–(35) and (41)–(44).

Step 2: By iteratively choosing (k, h) with given n, the associated voltage gain ranges M_m–M_M and M_{Rm}–M_{RM} are determined. TDM is utilized to iteratively solve the maximum normalized power P_{nMt} that achieves the maximum voltage gain M_M in forward mode and the maximum normalized power P_{nRMt} that is capable of realizing the maximum voltage gain M_{RM} during reverse operation within the designed frequency range. The normalized rated power P_n is specified as the lesser of P_{nMt} and P_{nRMt} in (50)

$$P_n = \min\left(P_{nMt}, P_{nRMt}\right). \tag{50}$$

Step 3: The characteristic impedance Z_r is determined according to nominal power P_{rated} and normalized rated power

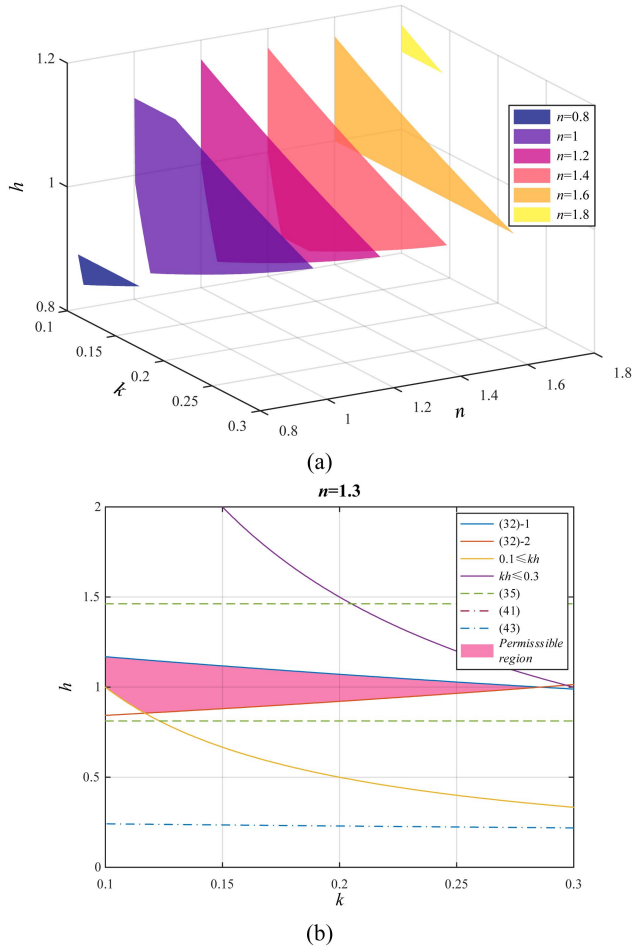

Fig. 17. Permissible regions for parameters (k, h) when n takes several possible values (a) and related constraints when $n = 1.3$ (b).

P_n. The weakest normalized ZVS current $|j_{10}|_{\min}$ and $|j_{20\_R}|_{\min}$ generated by TDM and characteristic impedance Z_r are adopted to verify whether or not the full range of ZVS is achieved in both directions. The related constraints are listed as

$$\begin{cases} Z_r = P_n U_1^2 / P_{\text{rated}} \\ |j_{10}|_{\min} t_{\text{dead}} \geq 2C_{\text{oss1}} Z_r \\ |j_{20\_R}|_{\min} n^2 t_{\text{dead}} \geq 2C_{\text{oss2}} h Z_r \end{cases}$$

$$\Rightarrow \begin{cases} \frac{|j_{10}|_{\min}}{P_n} \geq \frac{2C_{\text{oss1}}}{t_{\text{dead}}} \frac{U_1^2}{P_{\text{rated}}} \\ \frac{|j_{20\_R}|_{\min}}{P_n} \geq \frac{2C_{\text{oss2}} h}{n^2 t_{\text{dead}}} \frac{U_1^2}{P_{\text{rated}}} \end{cases} \tag{51}$$

where $|j_{10}|_{\min}$ and $|j_{20\_R}|_{\min}$ represent the weakest ZVS current during forward and reverse operations, respectively. If the verification validates that full range of ZVS has been accomplished, then the current iteration finishes and Step 4 begins. Otherwise, decrease the value of P_n to obtain stronger ZVS capability (i.e., lesser characteristic impedance Z_r) and go back to Step 3.

Step 4: Check if all (k, h) associated with the given n have been traversed completely. If so, move on to Step 5. Otherwise, go back to Step 2 and initiate another round of iterations for (k, h) associated with the given n.

Step 5: Check if all permissible values of n have been traversed completely. If so, the iteration is finished. Otherwise, go back to Step 1 and start another round of iterations for permissible n.

The complete iterative procedure is demonstrated in Fig. 18. After finishing the iterative process, the corresponding P_n and Z_r are obtained for each set of (n, k, h). In addition, the specific design parameters associated with each certain (n, k, h) can be derived as

$$\begin{cases} \omega_{r\_l} = \sqrt{\frac{hk+h+1}{hk}}\frac{1}{\sqrt{L_pC_p}} \\ Z_r = \sqrt{\frac{L_p}{C_p}} \end{cases}$$

$$\Rightarrow \begin{cases} L_p = \frac{Z_r}{\omega_{r\_l}}\sqrt{\frac{hk+h+1}{hk}} \\ C_p = \sqrt{\frac{hk+h+1}{hk}}\Big/(Z_r\omega_{r\_l}) \\ C_T = kC_p = \frac{k}{Z_r\omega_{r\_l}}\sqrt{\frac{hk+h+1}{hk}} \\ L_s = \frac{hL_p}{n^2} = \frac{hZ_r}{n^2\omega_{r\_l}}\sqrt{\frac{hk+h+1}{hk}} \\ C_s = \frac{n^2C_p}{h} = \frac{n^2}{hZ_r\omega_{r\_l}}\sqrt{\frac{hk+h+1}{hk}}. \end{cases} \tag{52}$$

For various combinations of (n, k, h), the iteration result with the minimum parallel capacitor is chosen as the optimal design, because the circulating reactive power is minimized with the minimum parallel capacitor. However, the equivalent parallel capacitor from inverting side in forward operation is C_t, while the equivalent parallel capacitor from inverting side in reverse operation is n^2C_t. Therefore, C_t+n^2C_t is defined as the generalized equivalent parallel capacitor in this article, which is adopted to evaluate the optimal design parameters. The iteration results with the minimum generalized equivalent parallel capacitor of each permissible n are listed in Table VI.

TABLE VI
ITERATION RESULTS

Permissible n	(k, h)	P_n	Z_r	C_t	C_t+n^2C_t
0.5	-	-	-	-	-
…	-	-	-	-	-
0.7	-	-	-	-	-
0.8	(0.12, 0.86)	0.20	32	26.031nF	42.691nF
0.9	(0.14, 0.88)	0.25	40	22.462nF	40.656nF
1	(0.12, 0.86)	0.28	44.8	18.594nF	37.187nF
1.1	(0.12, 0.86)	0.34	54.4	15.312nF	33.841nF
1.2	(0.12, 0.86)	0.45	72	11.569nF	28.229nF
1.3	**(0.11, 0.91)**	**0.48**	**76.8**	**10.215nF**	**27.479nF**
1.4	(0.25, 0.97)	0.79	126.4	9.508nF	28.144nF
1.5	(0.1, 1)	0.51	81.6	8.938nF	29.048nF
1.6	(0.11, 1)	0.54	86.4	8.875nF	31.593nF
1.7	(0.12, 1.07)	0.61	97.6	8.097nF	31.497nF
1.8	(0.13, 1.13)	0.68	108.8	7.487nF	31.744nF
1.9	-	-	-	-	-
…	-	-	-	-	-
2.8	-	-	-	-	-

The bold entities are the iterative optimal design parameters.

According to Table VI, the associated permission region (k, h) for $n = 0.5$–0.7 and 1.9–2.8 is an empty set. By traversing the iterative results of $n = 0.8$–1.8, the optimal design parameters are obtained in (53). The gain curves of the optimal S-type *LCCL* operating in both forward and reverse modes under constant power conditions (e.g., $P_{\text{out\_}n}$ and $P_{\text{out\_}n\_R}$) are precisely obtained through time-domain calculations. As illustrated in

$$\exists (k,h) \in D_p, \frac{\sec\left(k_2\pi/(2f_{nM})\right)-1}{k+1} \le M_m \Rightarrow \frac{nU_{2m}}{U_1} \ge \min_{(k,h)\in D_p}\left(\frac{\sec\left(k_2\pi/(2f_{nM})\right)-1}{k+1}\right)$$

$$\Rightarrow \frac{nU_{2m}}{U_1} \ge \left.\frac{\sec\left(k_2\pi/(2f_{nM})\right)-1}{k+1}\right|_{\substack{k=0.11688\\h=0.85555}}$$

$$\Rightarrow n \ge \frac{U_1}{U_{2m}}\left.\frac{\sec\left(k_2\pi/(2f_{nM})\right)-1}{k+1}\right|_{\substack{k=0.11688\\h=0.85555}}$$

$$\Rightarrow n \ge 0.49337 \tag{45}$$

$$\exists (k,h) \in D_p, \frac{\sec\left(k_2\pi/(2f_{nm})\right)-1}{k+1} \ge M_M \Rightarrow \frac{nU_{2M}}{U_1} \le \max_{(k,h)\in D_p}\left(\frac{\sec\left(k_2\pi/(2f_{nm})\right)-1}{k+1}\right) \Rightarrow n > 0 \tag{46}$$

$$\exists (k,h) \in D_p, \frac{\sec\left(k_2'\pi/(2f_{nM})\right)-1}{k'+1} \le M_{Rm} \Rightarrow 1\Big/\frac{nU_{2M}}{U_1} \ge \min_{(k,h)\in D_p}\left(\frac{\sec\left(k_2'\pi/(2f_{nM})\right)-1}{k'+1}\right)$$

$$\Rightarrow \frac{U_1}{nU_{2M}} \ge \left.\frac{\sec\left(k_2'\pi/(2f_{nM})\right)-1}{k'+1}\right|_{\substack{k=0.1\\h=1.16883}}$$

$$\Rightarrow n \le \frac{U_1}{U_{2M}}\Big/\left.\frac{\sec\left(k_2'\pi/(2f_{nM})\right)-1}{k'+1}\right|_{\substack{k=0.1\\h=1.16883}} \Rightarrow n \le 2.88267 \tag{47}$$

$$\exists (k,h) \in D_p, \frac{\sec\left(k_2'\pi/(2f_{nm})\right)-1}{k'+1} \ge M_{RM} \Rightarrow 1\Big/\frac{nU_{2m}}{U_1} \le \max_{(k,h)\in D_p}\left(\frac{\sec\left(k_2'\pi/(2f_{nm})\right)-1}{k'+1}\right) \Rightarrow n > 0 \tag{48}$$

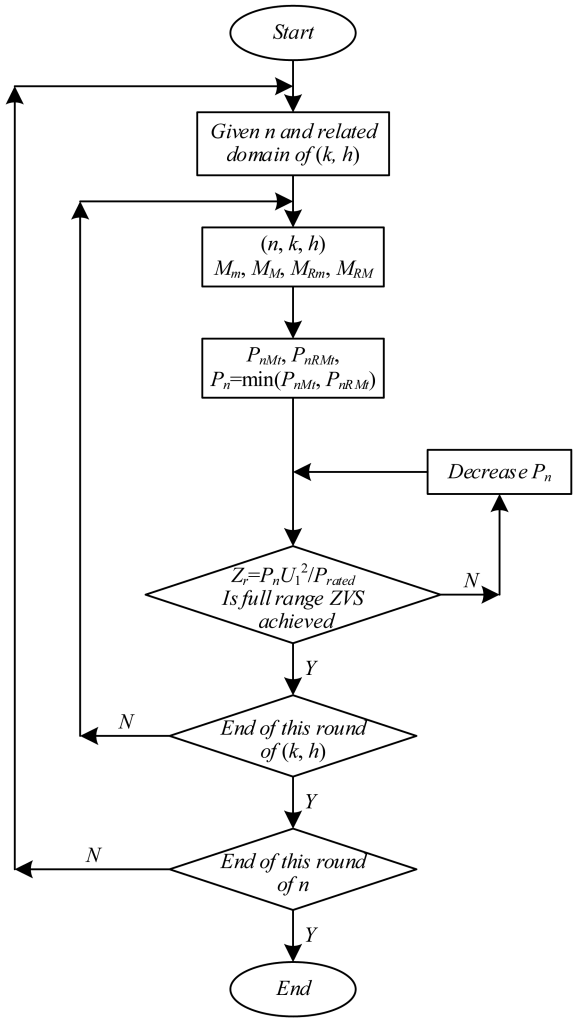

Fig. 18. Flowchart of the proposed design methodology.

Fig. 19, where $P_{\text{out\_}n\_R}$ is the noamlized output power of reverse operation

$$\begin{cases} n = 1.3 \\ k = 0.11 \\ h = 0.91 \\ Z_r = 76.8\,\Omega \\ f_{r\_l} = 100\,\text{kHz} \end{cases} \Rightarrow \begin{cases} L_p = 547.738\,u\text{H} \\ C_p = 92.8647\,\text{nF} \\ C_T = 10.215\,\text{nF} \\ L_s = 294.936\,u\text{H} \\ C_s = 172.463\,\text{nF}. \end{cases} \tag{53}$$

V. Experimental Results and Performance Comparisons

To verify the proposed *LCCL* topology and corresponding theoretical analysis, an S-type *LCCL* with parameters in (53) was constructed to satisfy the specifications of Table V. The key circuit component values are summarized in Table VII. The experimental setup is presented in Fig. 20.

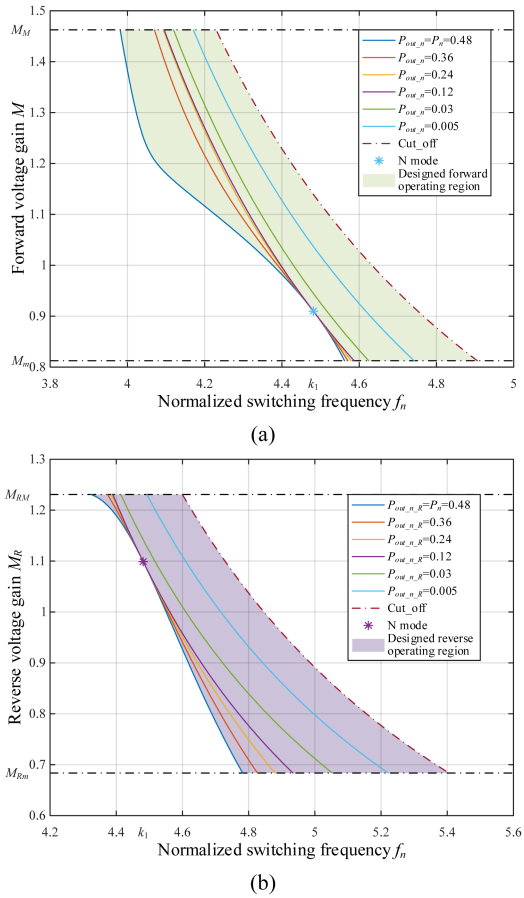

Fig. 19. Gain curves of the optimal *LCCL* for bidirectional operation. (a) Charging mode. (b) Discharging mode.

TABLE VII
Key Design Parameters of the *LCCL* Prototype

Components	Parameter/Part#
Primary voltage U_1	400V
Secondary voltage U_2	250V~450V
Primary resonant inductance L_p	547.738μH
Secondary resonant inductance L_s	294.936μH
Parallel resonant capacitance C_T	10.215nF
Primary resonant capacitance C_p	92.8647nF
Secondary resonant capacitance C_s	172.463nF
Turns ratio n	1.3
Resonant-like frequency f_{r_l}	100kHz
Switching frequency f_s	75kHz~150kHz
Rated power	1kW
MOSFETs	ROHM SCT3080AL

Fig. 20. Experimental setup. (a) *LCCL* prototype. (b) Experimental test platform.

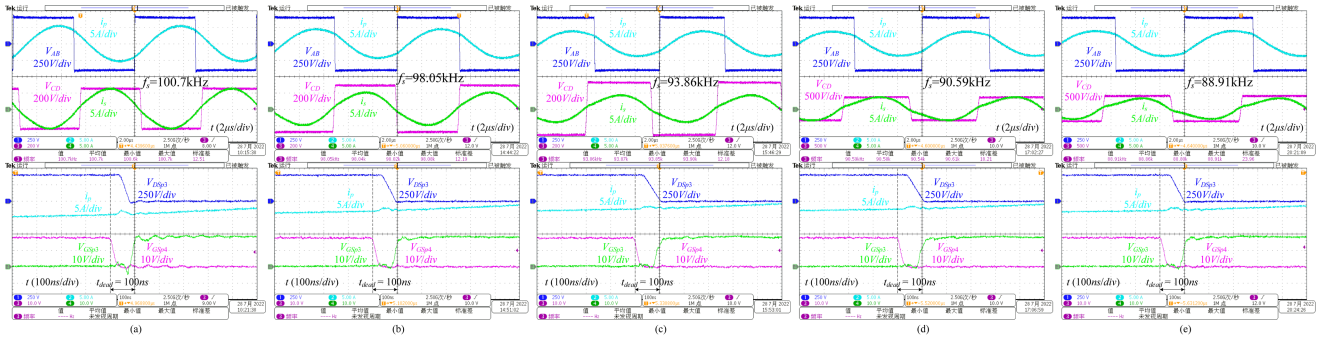

Fig. 21. Experimental waveforms of the prototype operating in forward mode with 1-kW load condition. (a) $U_1 = 400$ V and $U_2 = 250$ V. (b) $U_1 = 400$ V and $U_2 = 298.1$ V. (c) $U_1 = 400$ V and $U_2 = 348.7$ V. (d) $U_1 = 400$ V and $U_2 = 399.4$ V. (e) $U_1 = 400$ V and $U_2 = 450$ V.

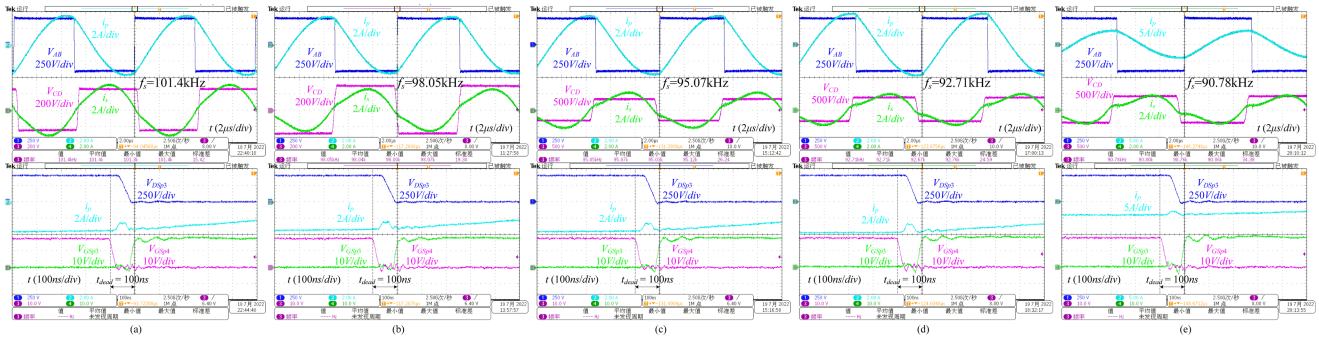

Fig. 22. Experimental waveforms of the prototype operating in forward mode with 500 W load condition. (a) $U_1 = 400$ V and $U_2 = 250$ V. (b) $U_1 = 400$ V and $U_2 = 298.1$ V. (c) $U_1 = 400$ V and $U_2 = 348.7$ V. (d) $U_1 = 400$ V and $U_2 = 399.4$ V. (e) $U_1 = 400$ V and $U_2 = 450$ V.

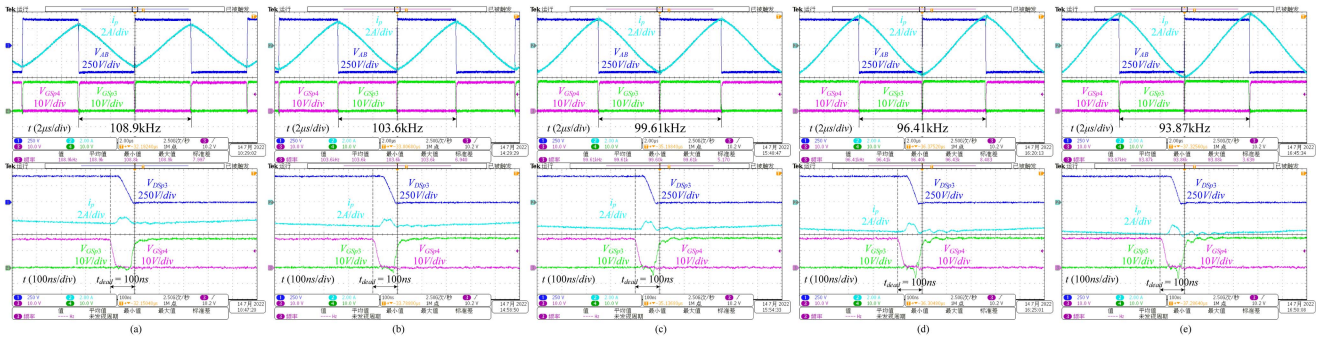

Fig. 23. Experimental waveforms of the prototype operating in forward O mode. (a) $U_1 = 400$ V and $U_2 = 250$ V. (b) $U_1 = 400$ V and $U_2 = 298.1$ V. (c) $U_1 = 400$ V and $U_2 = 348.7$ V. (d) $U_1 = 400$ V and $U_2 = 399.4$ V. (e) $U_1 = 400$ V and $U_2 = 450$ V.

A. Forward Mode

During forward charging operation, the dc power supply wired to U_1 is set at 400 V, and the electronic load wired to U_2 is configured to vary from 250 to 450 V under various load conditions.

Fig. 21 provides the experimental waveforms of the designed prototype operating in charging mode at several typical voltage gains and 1-kW load condition. Clearly, each drain-source voltage V_{DSp3} of inverting side in Fig. 21 can always drop to zero before V_{GSp3} rises to a high level. Therefore, ZVS for the inverting side switches is achieved. Similar waveforms are also presented in Fig. 22 when the load condition is 500 W. As for zero-load O mode of charging operation, corresponding experimental waveforms are shown in Fig. 23. Obviously, ZVS for the inverting side switches is also achieved under this condition. Consequently, the optimized S-type *LCCL* prototype is undoubtedly capable of achieving the designed voltage gain and ZVS during forward operation over the predefined frequency range and under desired load conditions.

B. Reverse Mode

During reverse discharging operation, the dc power supply wired to U_2 is configured to vary from 450 to 250 V, and the electronic load wired to U_1 is set at 400 V under various load conditions.

Fig. 24 shows the experimental waveforms of the designed prototype operating in discharging mode at several typical

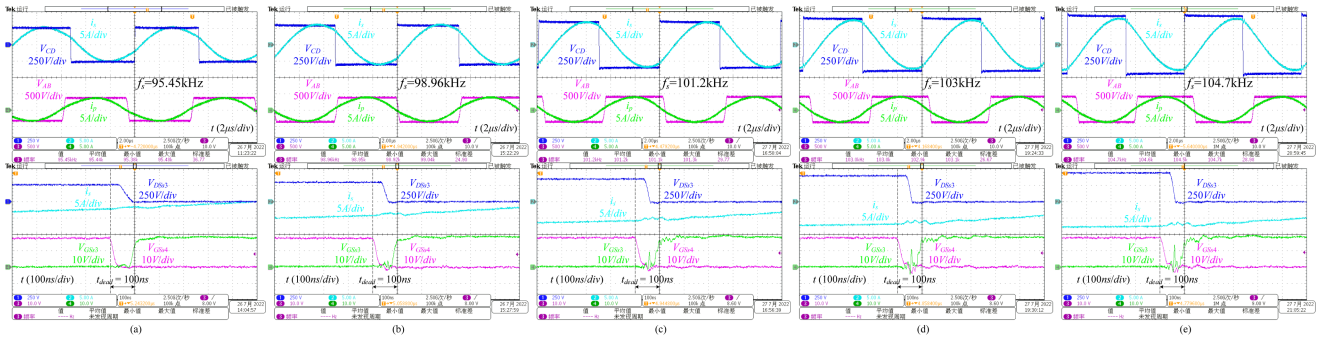

Fig. 24. Experimental waveforms of the prototype operating in reverse mode with 1-kW load condition. (a) $U_2 = 250$ V and $U_1 = 400$ V. (b) $U_2 = 298.1$ V and $U_1 = 400$ V. (c) $U_2 = 348.7$ V and $U_1 = 400$ V. (d) $U_2 = 399.4$ V and $U_1 = 400$ V. (e) $U_2 = 450$ V and $U_1 = 400$ V.

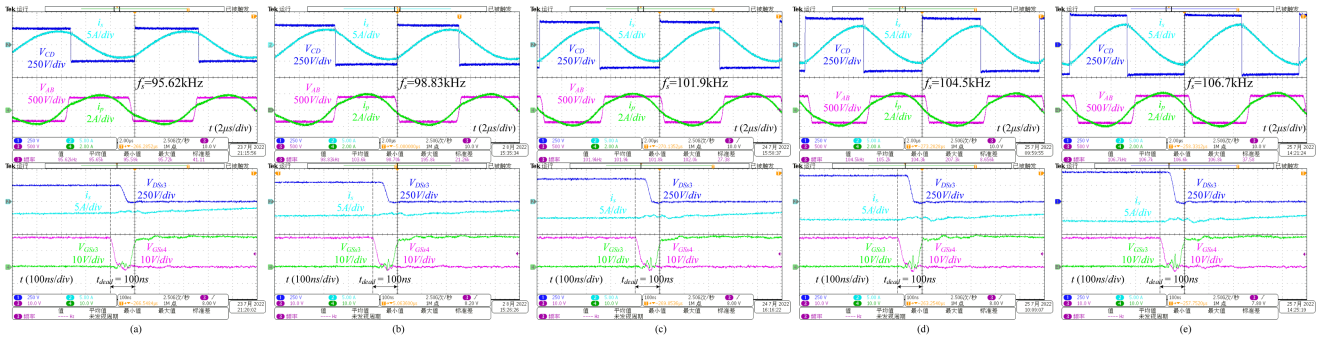

Fig. 25. Experimental waveforms of the prototype operating in reverse mode with 500 W load condition. (a) $U_2 = 250$ V and $U_1 = 400$ V. (b) $U_2 = 298.1$ V and $U_1 = 400$ V. (c) $U_2 = 348.7$ V and $U_1 = 400$ V. (d) $U_2 = 399.4$ V and $U_1 = 400$ V. (e) $U_2 = 450$ V and $U_1 = 400$ V.

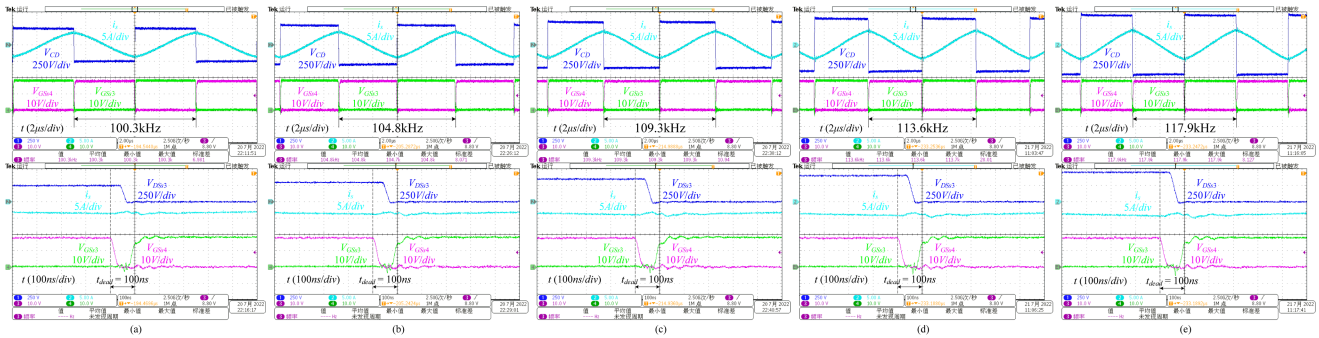

Fig. 26. Experimental waveforms of the prototype operating in reverse O mode. (a) $U_2 = 250$ V and $U_1 = 400$ V. (b) $U_2 = 298.1$ V and $U_1 = 400$ V. (c) $U_2 = 348.7$ V and $U_1 = 400$ V. (d) $U_2 = 399.4$ V and $U_1 = 400$ V. (e) $U_2 = 450$ V and $U_1 = 400$ V.

voltage gains and 1-kW load condition. Apparently, ZVS for the inverting side switches is achieved. Similar waveforms are also displayed in Fig. 25 when the load condition is 500 W. For zero-load O mode of discharging operation, corresponding experimental waveforms are shown in Fig. 26. Clearly, ZVS for the inverting side switches is also achieved under O mode. Therefore, the optimized S-type *LCCL* prototype is certainly capable of achieving the designed voltage gain and ZVS during reverse operation within the predetermined frequency range and under required load conditions.

C. Efficiency Test

Figs. 27 and 28 illustrate the efficiency curves of the optimized S-type *LCCL* prototype operating in forward and reverse mode at several typical voltage gains under different load conditions, respectively. The highest efficiency of the prototype is 97.357% when $U_1 = 400$ V and $U_2 = 424.7$ V with 1-kW output power in charging mode and 96.5% when $U_2 = 250$ V and $U_1 = 400$ V with 750 W output power in discharging mode. Due to the implementation of the full load range ZVS, the efficiency still exceeds 91% even with the minimum load of 250 W.

D. Performance Comparisons

In order to thoroughly demonstrate the performance of the proposed *LCCL*, a detailed comparison of the existing topologies for bidirectional wide-range battery applications and this article is summarized in Table VIII. Compared to *CLLC* [30], *CLTC* [33], *CDT-LC* [41], and *LCLL* [39], which only adopt PFM to obtain the bidirectional wide-range voltage gain, the proposed *LCCL* can achieve the required bidirectional voltage

TABLE VIII
PERFORMANCE COMPARISONS WITH OTHER PUBLISHED TOPOLOGIES

References	Topology	Modulation Strategy	Switching Frequency	Rated Power	Power Range*	Gain Range	Peak Efficiency	Efficiency at Full Load
[30]	CLLC	PFM	50k~200kHz	1kW	50%~100%	1.8X	98.91%	97%~98.4%
[33]	CLTC	PFM	45kHz~160kHz	5kW	0~100%	1.38X	97.1%	93.7%~95.9%
[41]	CDT-LC	PFM	65kHz~135kHz	2.5kW	0~100%	1.58X	97%	93.2%~96.1%
[39]	LCLL	PFM	65kHz~120kHz	1kW	Only 100%	1.5X	95.94%	90.4%~95.94%
[42]	LLC	PWM and Phase-Shift	100kHz	1kW	0~100%	2X	96.5%	93.5%~96%
[32]	SRC	PFM and PWM	40kHz~80kHz	6kW	0~100%	2X	93%	85%~90%
[43]	DAB	PWM and Phase-Shift	500kHz	3.3kW	Only 100%	1.5X	98%	90.5%~98%
This work	**LCCL**	**PFM**	**88kHz~120kHz**	**1kW**	**0~100%**	**1.8X**	**97.357%**	**93.25%~97.35%**

*The corresponding topology guarantees that the designed voltage gain and ZVS can be achieved within the specified output power range.

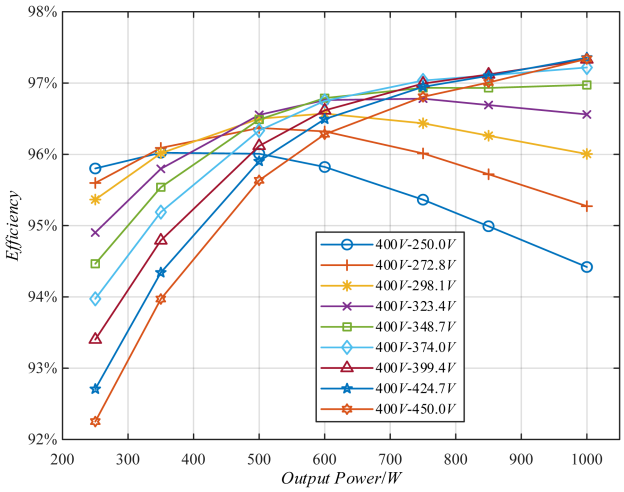

Fig. 27. Efficiency curves of forward operation.

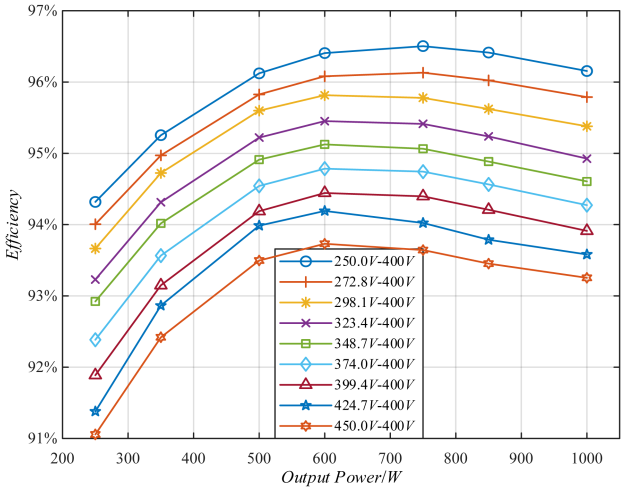

Fig. 28. Efficiency curves of reverse operation.

gain within the narrowest frequency range. This is also consistent with the conclusion of Section III that *LCCL* obtains enhanced voltage gain characteristics at the cost of replacing magnetizing inductance with a parallel resonant capacitor C_T. Admittedly, the overall efficiency of *LCCL* is slightly lower than that of *CLLC* [30], which is caused by the fact that *CLLC* only achieves a power range of 50%–100% and the *LCCL* sacrifices accordingly to achieve a power range of 0%–100%. Generally, both *LLC* and SRC utilizing only PFM cannot achieve bidirectional wide-range output (e.g., both step-up and step-down). Therefore, both *LLC* [42] and *SRC* [32] adopt extra modulation strategies (e.g., PWM and PS) to address the wide voltage range of battery applications, which evidently increases the complexity of control. Even combing with various complex modulation strategies (e.g., extended-PS, dual-PS, and triple-PS), it is still difficult for DAB to guarantee the achievement of ZVS over the full power range (0%–100%). Besides, the efficiency of DAB [43] is still inferior to that of this article. In comparison, the proposed *LCCL* provides a better balance between modulation strategy, power range, and efficiency.

VI. CONCLUSION

This article proposed a bidirectional *LCCL* resonant converter with enhanced voltage gain regulation capability, which possesses soft-switching features as ZVS for the inverting side and ZCS for the rectifier side. Based on the port characteristics of *LCCL* resonant tank, the topology derivation between D-type *LCCL* and S-type *LCCL* was presented. The operation principles of the proposed converter have been analyzed and illustrated. Then, TDM is adopted to characterize S-type *LCCL* in charging and discharging operations for typical OBC applications. Combining the TDM analysis's conclusions, the corresponding design parameter optimization method is proposed, which is capable of achieving the demanded bidirectional voltage gain and ZVS operation over the specified frequency range under desired load conditions while minimizing the reactive power. Finally, an S-type *LCCL* prototype rated at 1 kW with the optimized design parameters was established to convert between 400 and 250–450 V bidirectional. The experimental results verified the feasibility of the proposed *LCCL* topology and the validity of the corresponding parameters optimization method. The excellent features of *LCCL* topology were thoroughly demonstrated over the entire power range (0%–100%) by experiments. Specifically, the prototype achieves the designed voltage gain range of 1.8 times within the switching frequency from 88 to 120 kHz and the measured peak efficiency reaches 97.357%. Therefore, the proposed *LCCL* converter provides an alternative choice for wide output range and high-efficiency bidirectional dc converter in OBC applications. Future article will be conducted to establish the small-signal model of *LCCL* topology to better guide the design of the corresponding closed-loop controller.

REFERENCES

[1] U. K. Madawala and D. J. Thrimawithana, "A bidirectional inductive power interface for electric vehicles in V2G systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4789–4796, Oct. 2011.

[2] D. Wu, F. Tang, T. Dragicevic, J. C. Vasquez, and J. M. Guerrero, "A control architecture to coordinate renewable energy sources and energy storage systems in islanded microgrids," *IEEE Trans. Smart Grid*, vol. 6, no. 3, pp. 1156–1166, May 2015.

[3] Y.-F. Wang, L.-K. Xue, C.-S. Wang, P. Wang, and W. Li, "Interleaved high-conversion-ratio bidirectional DC–DC converter for distributed energy-storage systems—Circuit generation, analysis, and design," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5547–5561, Aug. 2016.

[4] W. Jing, C. Hung Lai, S. H. W. Wong, and M. L. D. Wong, "Battery-supercapacitor hybrid energy storage system in standalone DC microgrids: A review," *IET Renewable Power Gener.*, vol. 11, no. 4, pp. 461–469, 2017.

[5] S. Inoue and H. Akagi, "A bidirectional DC–DC converter for an energy storage system with galvanic isolation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2299–2306, Nov. 2007.

[6] N. M. L. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated DC–DC converter for a battery energy storage system," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1237–1248, Mar. 2012.

[7] D. Aggeler, J. Biela, and J. W. Kolar, "A compact, high voltage 25 kW, 50 kHz DC-DC converter based on SiC JFETs," in *Proc. IEEE 23rd Annu. Appl. Power Electron. Conf. Expo.*, 2008, pp. 801–807.

[8] W. Chen, P. Rong, and Z. Lu, "Snubberless bidirectional DC–DC converter with new CLLC resonant tank featuring minimized switching loss," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3075–3086, Sep. 2010.

[9] Y. Guan, Z. Shi, C. Liu, Y. Wang, and D. Xu, "A 10 MHz DC/DC converter with zero-phase difference synchronous driving signal," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13878–13888, Dec. 2021.

[10] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[11] K. Wu, C. W. de Silva, and W. G. Dunford, "Stability analysis of isolated bidirectional dual active full-bridge DC–DC converter with triple phase-shift control," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2007–2017, Apr. 2012.

[12] F. Krismer and J. W. Kolar, "Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 881–891, Mar. 2010.

[13] G. Oggier, G. O. García, and A. R. Oliva, "Modulation strategy to operate the dual active bridge DC-DC converter under soft switching in the whole operating range," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1228–1236, Apr. 2011.

[14] H. Wen, W. Xiao, and B. Su, "Nonactive power loss minimization in a bidirectional isolated DC–DC converter for distributed power systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6822–6831, Dec. 2014.

[15] M. Yaqoob, K. H. Loo, and Y. M. Lai, "Extension of soft-switching region of dual-active-bridge converter by a tunable resonant tank," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9093–9104, Dec. 2017.

[16] G. G. Oggier, R. Leidhold, G. O. Garcia, A. R. Oliva, J. C. Balda, and F. Barlow, "Extending the ZVS operating range of dual active bridge high-power DC-DC converters," in *Proc. IEEE 37th Power Electron. Specialists Conf.*, 2006, pp. 1–7.

[17] Y. Cho, W. Cha, J. Kwon, and B. Kwon, "High-efficiency bidirectional DAB inverter using a novel hybrid modulation for stand-alone power generating system with low input voltage," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4138–4147, Jun. 2016.

[18] H. Bai and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge DC–DC converters using novel dual-phase-shift control," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2905–2914, Nov. 2008.

[19] A. K. Jain and R. Ayyanar, "PWM control of dual active bridge: Comprehensive analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1215–1227, Apr. 2011.

[20] F. Krismer and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2745–2760, Jul. 2012.

[21] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012.

[22] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional DC–DC converter based on dual-phase-shift control for DC distribution application," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1711–1727, Apr. 2013.

[23] B. Zhao, Q. Song, W. Liu, G. Liu, and Y. Zhao, "Universal high-frequency-link characterization and practical fundamental-optimal strategy for dual-active-bridge DC-DC converter under PWM plus phase-shift control," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6488–6494, Dec. 2015.

[24] H. Shi, H. Wen, J. Chen, Y. Hu, L. Jiang, and G. Chen, "Minimum-reactive-power scheme of dual-active-bridge DC–DC converter with three-level modulated phase-shift control," *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5573–5586, Nov./Dec. 2017.

[25] J. Hiltunen, V. Väisänen, R. Juntunen, and P. Silventoinen, "Variable-frequency phase shift modulation of a dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7138–7148, Dec. 2015.

[26] X. He, Z. Zhang, Y. Cai, and Y. Liu, "A variable switching frequency hybrid control for ZVS dual active bridge converters to achieve high efficiency in wide load range," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 1095–1099.

[27] Z. U. Zahid, Z. M. Dalala, R. Chen, B. Chen, and J. -S. Lai, "Design of bidirectional DC–DC resonant converter for vehicle-to-grid (V2G) applications," *IEEE Trans. Transp. Electrific.*, vol. 1, no. 3, pp. 232–244, Oct. 2015.

[28] M. Yaqoob, K. H. Loo, and Y. M. Lai, "A four-degrees-of-freedom modulation strategy for dual-active-bridge series-resonant converter designed for total loss minimization," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1065–1081, Feb. 2019.

[29] Q. Huang, K. Shi, X. Jia, C. Hu, and D. Xu, "A bi-directional resonant DC/DC converter with frequency tracking control," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 4748–4754.

[30] L. Zhao, Y. Pei, L. Wang, L. Pei, W. Cao, and Y. Gan, "Design methodology of bidirectional resonant CLLC charger for wide voltage range based on parameter equivalent and time domain model," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12041–12064, Oct. 2022.

[31] F. Ibanez, J. M. Echeverria, and L. Fontan, "Novel technique for bidirectional series-resonant DC/DC converter in discontinuous mode," *IET Power Electron.*, vol. 6, no. 5, pp. 1019–1028, May 2013.

[32] F. M. Ibanez, J. M. Echeverria, J. Vadillo, and L. Fontan, "A Step-up bidirectional series resonant DC/DC converter using a continuous current mode," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1393–1402, Mar. 2015.

[33] C.-S. Wang, S.-h. Zhang, Y.-f. Wang, B. Chen, and J.-H. Liu, "A 5-kW isolated high voltage conversion ratio bidirectional CLTC resonant DC–DC converter with wide gain range and high efficiency," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 340–355, Jan. 2019.

[34] S. H. Zhang, F. Z. Luo, and Y. F.Wang, "Control method based on demand response needs of isolated bus regulation with series-resonant converters for residential photovoltaic systems," *Energies*, vol. 10, no. 6, Mar. 2017, Art. no. 752.

[35] T. Jiang, J. Zhang, X. Wu, K. Sheng, and Y. Wang, "A bidirectional LLC resonant converter with automatic forward and backward mode transition," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 757–770, Feb. 2015.

[36] Z. Liang, R. Guo, J. Li, and A. Q. Huang, "A high-efficiency PV module-integrated DC/DC converter for PV energy harvest in FREEDM systems," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 897–909, Mar. 2011.

[37] J. Jung, H. Kim, M. Ryu, and J. Baek, "Design methodology of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1741–1755, Apr. 2013.

[38] E.-S. Kim, J.-H. Park, J.-S. Joo, S.-M. Lee, K. Kim, and Y.-S. Kong, "Bidirectional DC-DC converter using secondary LLC resonant tank," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 2104–2108.

[39] Y. Zhang, D. Zhang, J. Li, and H. Zhu, "Bidirectional LCLL resonant converter with wide output voltage range," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11813–11826, Nov. 2020.

[40] Y. Liu, H. Wu, Y. Tai, J. Zou, and Y. Jia, "Optimal design of GaN and PCB-winding based transformer-inductor-integrated magnetics for CLL resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 5430–5435.

[41] B. Chen, P. Wang, Y.-F. Wang, S.-H. Zhang, L. Yang, and R.-L. Ji, "A bidirectional CDT-LC resonant DC–DC converter with a wide voltage range," *IEEE Trans. Ind. Electron.*, vol. 67, no. 3, pp. 2009–2020, Mar. 2020.

[42] T. Jiang, J. Zhang, X. Wu, K. Sheng, and Y. Wang, "A bidirectional three-level LLC resonant converter with PWAM control," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2213–2225, Mar. 2016.
[43] Y. Park, S. Chakraborty, and A. Khaligh, "DAB converter for EV onboard chargers using bare-die SiC MOSFETs and leakage-integrated planar transformer," *IEEE Trans. Transp. Electrific.*, vol. 8, no. 1, pp. 209–224, Mar. 2022.

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