An Extendable Bidirectional High-Gain DC–DC Converter for Electric Vehicle Applications Equipped With IOFL Controller

Tina Sojoudi, Mitra Sarhangzadeh, Javad Olamaei, *Senior Member, IEEE*, and Jaber Fallah Ardashir

***Abstract*—High-gain bidirectional dc–dc converters are so popular in many applications, such as drives, photovoltaic systems, electric vehicles (EVs), etc. This article proposes an extendable bidirectional common-ground dc–dc converter suitable for high-gain applications, such as EVs. The proposed converter uses fewer number of switches to provide high step-up and high step-down voltage converting capabilities in both power flow directions. Since the input and output of this converter share the same ground, the electromagnetic interface is alleviated. In order to assess the versatility of the proposed dc–dc converter and to achieve a fast response, by equipping this converter with an input–output feedback linearization (IOFL) controller, its performance is analyzed in EV applications. To this end, the steady-state calculations are worked out for both charge and discharge directions, then dynamic analysis and control design are presented based on nonlinear controller by IOFL. Simulation and experimental results are provided to prove the feasibility of the proposed converter.**

***Index Terms*—Electric vehicle (EV), extendable converter, high-gain bidirectional dc–dc converter, input–output feedback linearization (IOFL), small-signal analysis, steady-state analysis.**

Nomenclature

V_{in}, V_o	Input and output voltages.
i_{in}, i_o	Input and output currents.
P_{in}, P_o	Input and output powers.
d_1, d_3	Switching duty cycles.
L_1, L_2	Inductors.
C_1, C_2	Capacitors.
R	Resistance.
E	Motor EMF.
$S_{1–4}$	Switches.
$D_{1–2}$	Diodes.
i_{L2}	Currents of L_2.
V_{C1}	Voltages of C_1.
A, B	State and input matrices.
k_1, k_2, k	Constant coefficients.
e_1, e_2, e	Errors.
f, g	Nonlinear equation matrices.

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Tina Sojoudi is with the Department of Electrical Engineering, Kish International Branch, Islamic Azad University, Kish Island, Iran (e-mail: t.sojoudi@iaukishint.ac.ir).

Mitra Sarhangzadeh and Jaber Fallah Ardashir are with the Department of Electrical Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran (e-mail: mitsarhang@iaut.ac.ir; j.fallah@iaut.ac.ir).

Javad Olamaei is with the Department of Electrical Engineering, South Tehran Branch, Islamic Azad University, Tehran, Iran (e-mail: j_olamaei@azad.ac.ir).

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I. Introduction

FOR decades, due to high reliability, internal combustion engines (ICEs) were employed in most of the transportation systems. Nowadays, however, because of ever-rising diesel and gasoline prices, environmental pollution, and limitation in fossil fuel, large automotive industries attempt to find a better alternative fuels, which meet required quality and reliability. Transportation industries are the main pollution source of the global greenhouse gas emissions. According to the U.S. Concerned Scientists, 30% of greenhouse gas emissions are resulted from vehicles traffic [1], [2], [3].

In hybrid electric vehicles (HEVs), the traction is supplied directly through an electric motor, and the ICE is used both to charge the batteries and supply electric motor by virtue of converter as shown in Fig. 1 [4], [5], [6]. In HEVs, the power electronic devices include a rectifier that converts the ac voltage of generator to dc voltage, a dc–dc converter which is used to discharge/charge the batteries, and an inverter is used to convert dc voltage to ac voltage, making it suitable for the electric motor [7]. These kinds of HEVs are durable and require less repairing service [2].

Batteries are one of the main parts of electric vehicles (EVs), which have dc voltage in output with a low-voltage (LV) level of 12, 24, or 48 V [8], [9], [10], [11], [12], [13]. Therefore, a dc–dc converter is needed to convert its LV to high-voltage (HV) level to make it suitable for electric motor and conversely [14].

Voltage gain, efficiency, electromagnetic interference (EMI), power density, and bidirectional power flow capability are the most regarded factors in dc–dc converters in EVs. HV ratio can be achieved by converters including coupling inductors and/or transformers. However, these types of converters can be bulky, inefficient, and suffer from leakage inductance and complexity [15]. So it is preferred to avoid using transformers in the mentioned converters. The EMI problem can be alleviated by using common-ground converters [16]. In addition, the ability of dc–dc converter to transfer power from the battery to the electric

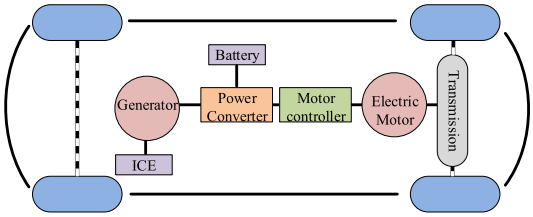


Fig. 1. Schematic of electromotive force of an HEV.

motor and vice versa, is important. Therefore, the unidirectional power supply characteristic of converters limits their application in EVs. Hence, a bidirectional dc–dc converter with HV gain can meet the requirements of EVs [8], [9], [10], [11], [12], [13], [15].

In light of above, in this article, a bidirectional nonisolated common-ground high-gain dc–dc converter for EV applications is proposed. In this converter, the LV side is connected to EV battery and the HV side supplies the EV motor. In the discharging mode, the motor draws power from the battery, so the current flows from LV side to HV side. This process is reversed in the charging mode to charge the LV battery through the HV side [17].

The proposed converter consists of a high-gain quadratic boost converter [18] and two cascaded buck converters [19], in which some elements such as inductors, capacitors, switches, and diodes of mentioned converters are shared with each other to develop bidirectional converter. Therefore, the proposed converter can be extended to achieve a very HV gain in both charging and discharging modes.

The proposed converter is modeled and based on the obtained model, a nonlinear controller is designed to regulate voltage/currents of charging and discharging modes. The designed nonlinear controller, which is based on input–output feedback linearization (IOFL), is a precise and features fast response for any dynamic change [20].

The contents of this article are presented as follows: in Section II, the configuration of the proposed converter along with modeling process is explained. The voltage stress of the utilized semiconductors in the proposed converter in charge and discharge modes are calculated in Section III. In Section IV, the value of passive components is obtained. In Section V, the designed IOFL controller for the proposed converter is explained. The proposed converter is compared with the prior-art bidirectional dc–dc converters in Section VI. The simulation and experimental results are provided in Section VII to investigate the performance of the proposed converter and designed IOFL controller under different operation modes. Finally, the overall article is concluded in Section VIII.

II. Modeling and Analysis of Proposed Converter

The proposed extendable high-gain bidirectional dc–dc converter is based on quadratic boost in [18] and quadratic buck dc–dc converters. The employed quadratic buck converter is composed of two cascaded conventional buck converter [19]. In Fig. 2(a) and (b), the employed quadratic boost and buck dc–dc converters are shown, respectively. The proposed dc–dc converter which is combined of quadratic boost and buck converters is illustrated in Fig. 2(c). The proposed converter has a common ground between input and output terminals and is a nonisolated converter. Thus, the problems of isolated converters such as leakage inductance and HV stress across semiconductors are alleviated in this converter. By extending the proposed converter with n-cell as shown in Fig. 2(d), an HV gain can be achieved. Therefore, with an extended converter, at the same time, it is possible to achieve the HV gain of isolated converters and tackle the problems of isolated converters.

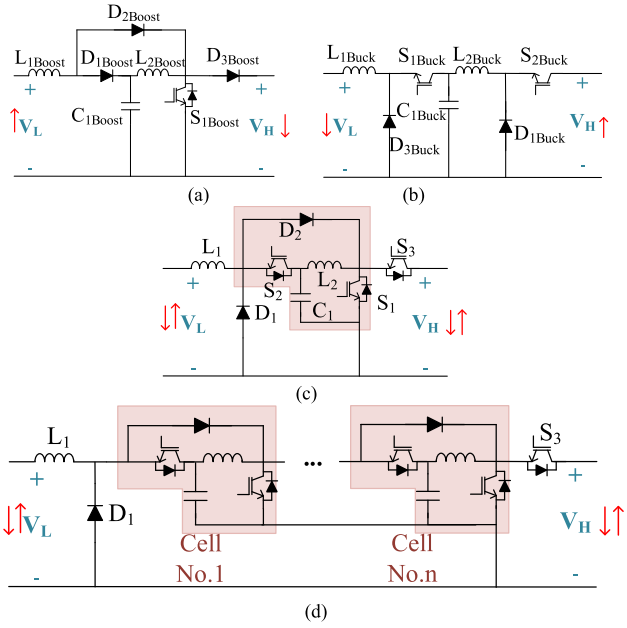


Fig. 2. Configuration of the proposed converter and its contents. (a) Fundamental quadratic boost converter [18]. (b) Cascaded buck converter [19]. (c) Proposed quadratic bidirectional DC–DC converter. (d) Extended configuration of the proposed converter.

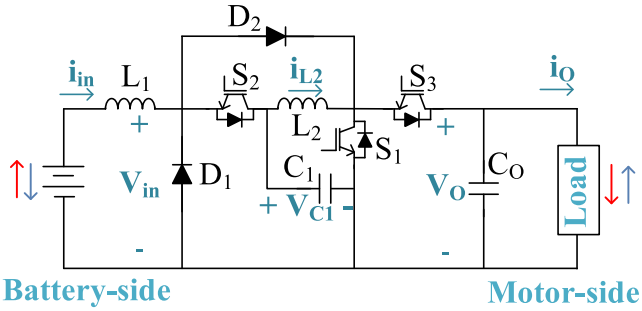


Fig. 3. Basic configuration of proposed converter.

Fig. 3 illustrates the proposed bidirectional dc–dc converter with one cell, which is composed of three switches, two diodes, two inductors, and two capacitors. This converter operates at charging and discharging modes. These modes and related modeling analysis are illustrated in following subsections.

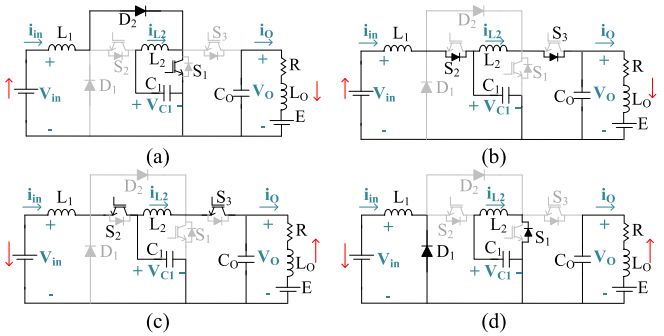


Fig. 4. Operating states of (a) discharge mode (state I), (b) discharge mode (state II), (c) charge mode (state I), and (d) charge mode (state II).

TABLE I
SWITCHING STATES OF DISCHARGE MODE

States	Duration time	Switch/Diodes state				
		S_1	S_2	S_3	D_1	D_2
1	d_1T	on	off	off	off	on
2	$(1-d_1)T$	off	on	on	off	off

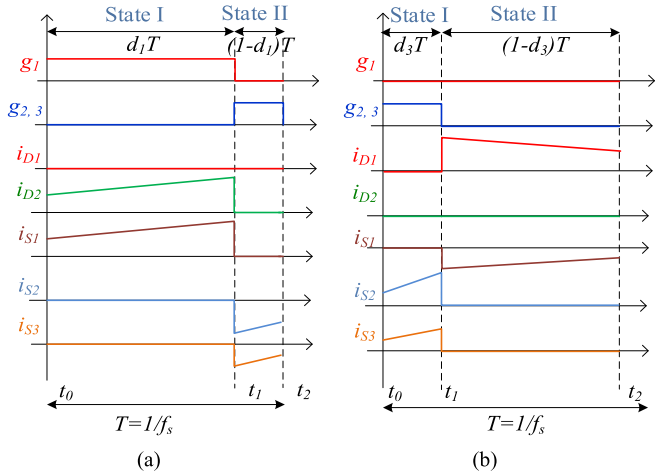


Fig. 5. Waveforms and switching states in (a) discharge mode and (b) charge mode.

A. Discharge Mode

The possible states in the discharging (boost) mode are depicted in Fig. 4(a) and (b). As shown in this figure, there are two states in discharging mode and the switching status of the switches/diodes are listed in Table I.

The voltages and currents of switches and diodes under different operation states are exhibited in Fig. 5(a). As shown in this figure, the switching period is $T = 1/fs$ (from t_0 to t_2), and the duty cycle of S_1 is indicated by d_1. In this figure, g_1, g_2 and g_3 are switching gate signals of S_1, S_2, and S_3 and i_{S1}, i_{S2}, i_{S3}, i_{D1}, and i_{D2} are switches and diodes currents.

The energy exchange of the circuit elements in discharge mode can be overall described as follows:

1) *First state (from t_0 to t_1):* As shown in Figs. 4(a) and 5(a), L_1 is charged through V_{in}, L_2 is charged through C_1, and the output load is supplied through C_o.

2) *Second state (from t_1 to t_2):* As shown in Figs. 4(b) and 5(a), C_1 is charged through L_1, and L_2 both charges C_o and provides the output current.

The state-space of the proposed converter is stated in (1). This equation is obtained by considering the averaging of two operation states

$$x' = Ax + Bu \tag{1}$$

Where the state-space variables (x) and the input vector (u) are defined as

$$x = \begin{bmatrix} i_{\text{in}} \\ i_{L2} \\ V_{C1} \\ V_O \\ i_O \end{bmatrix}, \quad u = \begin{bmatrix} V_{\text{in}} \\ E \end{bmatrix}. \tag{2}$$

The state matric A and the input matric B in (1) are as follows:

$$A = \begin{bmatrix} -\frac{d_1 r_d + r_s + r_{L1}}{L_1} & -\frac{d_1 r_s}{L_1} & \frac{-1+d_1}{L_1} & 0 & 0 \\ -\frac{r_s d_1}{L_2} & -\frac{r_{L2}+r_s}{L_2} & \frac{1}{L_2} & \frac{-1+d_1}{L_2} & 0 \\ \frac{1-d_1}{C_1} & \frac{-1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1-d_1}{C_O} & 0 & 0 & \frac{-1}{C_O} \\ 0 & 0 & 0 & \frac{1}{L_O} & \frac{-R}{L_O} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{-1}{L_O} \end{bmatrix} \tag{3}$$

Where r_s and r_d are switch and diode ON-state resistances, respectively, and r_{L1} and r_{L2} are equivalent series resistance (ESR) of L_1 and L_2, respectively. Using $X_{\text{dc}} = -A^{-1}Bu$ and neglecting ON-state resistances of the switches and diodes ($r_d = r_s = 0$), the dc answer of (1) is given as follows, where the forth row shows relationship between input and output voltages, and the voltage gain of discharge (boost) mode is obtained as $M_{\text{boost}} = \frac{V_O}{V_{\text{in}}}$ [21]

$$X_{\text{dc}} = \begin{bmatrix} i_{\text{in}} \\ i_{L2} \\ V_{C1} \\ V_O \\ i_O \end{bmatrix} = \begin{bmatrix} \frac{V_{\text{in}} - E(1-d_1)^2}{r_{L1}+r_{L2}(d_1(d_1-2)+1)+R(1-d_1)^4} \\ \frac{V_{\text{in}}(1-d_1)+E(d_1-1)^2}{r_{L1}+r_{L2}(d_1(d_1-2)+1)+R(1-d_1)^4} \\ \frac{V_{\text{in}}\left(-(d_1-1)^3 R+(1-d_1)r_{L2}\right)+E r_{L1}(1-d_1)}{r_{L1}+r_{L2}(d_1(d_1-2)+1)+R(1-d_1)^4} \\ \frac{E(r_{L1}+r_{L2}(d_1(d_1-2)+1))+V_{\text{in}}R(1-d_1)^2}{r_{L1}+r_{L2}(d_1(d_1-2)+1)+R(1-d_1)^4} \\ \frac{-E(1-d_1)^4+V_{\text{in}}(1-d_1)^2}{r_{L1}+r_{L2}(d_1(d_1-2)+1)+R(1-d_1)^4} \end{bmatrix}. \tag{4}$$

Neglecting ESR of inductors ($r_{L1} = r_{L2} = 0$), (4) is simplified as

$$X_{\text{dc}} = \begin{bmatrix} i_{\text{in}} \\ i_{L2} \\ V_{C1} \\ V_O \\ i_O \end{bmatrix} = \begin{bmatrix} \frac{V_{\text{in}}}{R(1-d_1)^4} - \frac{E}{R(1-d_1)^2} \\ \frac{V_{\text{in}}}{R(1-d_1)^3} - \frac{E}{R(1-d_1)} \\ \frac{V_{\text{in}}}{1-d_1} \\ \frac{V_{\text{in}}}{(1-d_1)^2} \\ \frac{V_{\text{in}}}{R(1-d_1)^2} - \frac{E}{R} \end{bmatrix}. \tag{5}$$

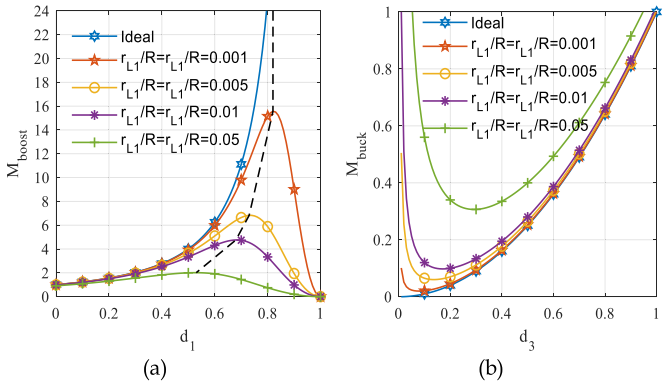


Fig. 6. Static voltage gain ratio as a function of duty cycle considering losses in (a) discharge (boost) and (b) charge (buck) modes.

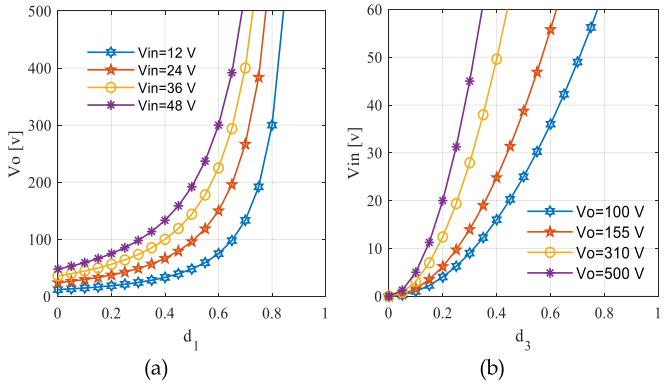


Fig. 7. Relationship between voltage and duty cycles with n cells: (a) V_o and d_1 in discharge (boost) mode for different V_{in} and (b) V_{in} and d_3 in charge (buck) mode for different V_O.

Fig. 6(a) shows static voltage gain with respect to d_1 considering different values of r_{L1} and r_{L2} and using forth row of (4) and (5). It is obvious that taking the losses into account (practical condition) brings limitation in voltage gain.

Fig. 7(a) shows V_O with respect to d_1, neglecting losses (ideal condition) and considering different battery-side voltage values. In the extended converter with n cells, the relation between V_{in} and V_O is as follows:

$$M_{\text{boost}} = \frac{V_O}{V_{\text{in}}} = \frac{1}{(1-d_1)^{n+1}} \tag{6}$$

Where M_{boost} is the voltage gain in boost (discharging) mode.

The variations of M_{boost} with respect to d_1 is shown in Fig. 8(a). It is obvious that, given a certain d_1, the voltage gain raises in line with increasing the number of cells (n).

B. Charge Mode

The charging (buck) mode is depicted in Fig. 4(c) and (d). As shown in this figure, there are two states in charging mode and the switching status of the switches/diodes are listed in Table II. The voltages and currents of switches and diodes under different operation states are exhibited in Fig. 5(b).

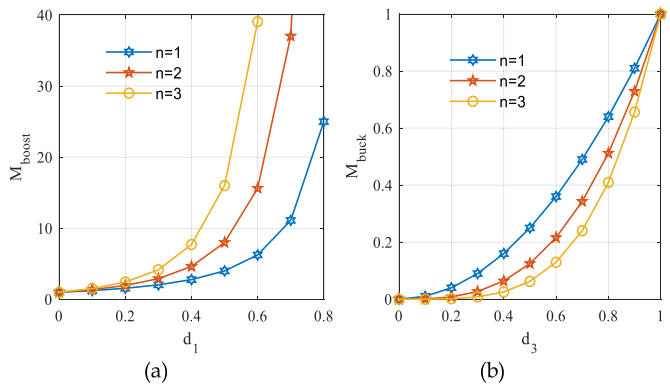


Fig. 8. Relationship between voltage gain and duty cycles with n cells: (a) M_{boost} and d_1 and (b) M_{buck} and d_3.

TABLE II
SWITCHING STATES OF CHARGE MODE

State	Duration time	Switch/Diodes state				
		S_1	S_2	S_3	D_1	D_2
1	d_3T	off	on	on	off	off
2	$(1\text{-}d_3)T$	on	off	off	on	off

As shown in this figure, the switching period is $T = 1/fs$ (from t_0 to t_2), and the duty cycle of S_3 and S_4 is indicated by d_3. In this figure, g_1 and g_2, g_3 are switching gate signals of S_1, S_2, and S_3 and i_{S1}, i_{S2}, i_{S3}, i_{D1}, and i_{D2} are switches and diodes currents.

The energy exchange of the circuit elements in charge mode can be overall described as follows:

1) *First state (from t_0 to t_1):* As shown in Figs. 4(c) and 5(b), C_1 is charged through L_2 and C_o, L_1 is charged through C_1, and V_{in} receives current through L_1.
2) *Second state (from t_1 to t_2):* As shown in Figs. 4(d) and 5(b), residual current of the L_2 charges C_1 and the residual current of L_1 goes to input through D_1.

The state-space variables (x) and the input vector (u) are the same as in the previous section and the state matric A and the input matric B are as follows:

$$A = \begin{bmatrix} \frac{(-1+d_3)r_d - d_3 r_s - d_3 r_{L1}}{L_1} & 0 & \frac{-d_3}{L_1} & 0 & 0 \\ 0 & -\frac{r_{L2}+r_s}{L_2} & \frac{1}{L_2} & \frac{-d_3}{L_2} & 0 \\ \frac{d_3}{C_1} & \frac{-1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{d_3}{C_O} & 0 & 0 & \frac{-1}{C_O} \\ 0 & 0 & 0 & \frac{1}{L_O} & \frac{-R}{L_O} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{-1}{L_O} \end{bmatrix}. \tag{7}$$

The dc answer of state-space in charge mode by assuming $r_d = r_s = 0$, is given as follows, where the fourth row shows relationship between the input and output voltages, and the voltage gain of charge (buck) mode is obtained as $M_{\text{buck}} = \frac{V_{\text{in}}}{V_O}$

[21]:

$$X_{\rm dc}=\begin{bmatrix} i_{\rm in}\\ i_{L2}\\ V_{C1}\\ V_O\\ i_O\end{bmatrix}=\begin{bmatrix} \frac{V_{\rm in}-d_3^2E}{Rd_3^4+r_{L1}d_3+r_{L2}d_3^2}\\ \frac{d_3V_{\rm in}-d_3^3E}{Rd_3^4+r_{L1}d_3+r_{L2}d_3^2}\\ \frac{(d_3^2R+r_{L2})V_{\rm in}+d_3r_{L1}E}{Rd_3^4+r_{L1}d_3+r_{L2}d_3^2}\\ \frac{d_3^2RV_{\rm in}+d_3(r_{L1}+r_{L2}d_3)E}{Rd_3^4+r_{L1}d_3+r_{L2}d_3^2}\\ \frac{d_3^2V_{\rm in}-d_3^4E}{Rd_3^4+r_{L1}d_3+r_{L2}d_3^2}\end{bmatrix}. \tag{8}$$

Neglecting ESR of inductors ($r_{L1}=r_{L2}=0$), (8) is simplified as

$$X_{\rm dc}=\begin{bmatrix} i_{\rm in}\\ i_{L2}\\ V_{C1}\\ V_O\\ i_O\end{bmatrix}=\begin{bmatrix} \frac{V_{\rm in}}{Rd_3^4}-\frac{E}{Rd_3^2}\\ \frac{V_{\rm in}}{Rd_3^3}-\frac{E}{Rd_3}\\ \frac{V_{\rm in}}{d_3}\\ \frac{V_{\rm in}}{d_3^2}\\ \frac{V_{\rm in}}{Rd_3^2}-\frac{E}{R}\end{bmatrix}. \tag{9}$$

Fig. 6(b) shows voltage gain with respect to d_3 considering different values of r_{L1} and r_{L2} and using fourth row of (8) and (9). It is obvious that taking the losses into account (practical condition) brings limitation in voltage gain.

By neglecting losses (ideal condition) and considering different motor-side voltage values, $V_{\rm in}$ with respect to d_3 is shown in Fig. 7(b). In the extended converter with n cells, the relation between $V_{\rm in}$ and V_O is as follows:

$$M_{\rm buck}=\frac{V_{\rm in}}{V_O}=d_3^{n+1} \tag{10}$$

Where $M_{\rm buck}$ is the voltage gain in buck (charging) mode. The variations of $M_{\rm buck}$ with respect to d_3 is shown in Fig. 8(b). It is obvious that, given a certain d_3, the voltage gain decreases in line with the number of cells (n).

III. Voltage Stress of Semiconductors

One of the important parameters in the competency of the power electronic devices is voltage stress of the components. This parameter for the utilized diodes and switches in the proposed converter in charge and discharge modes are indicated in Table III, where the voltage stresses on the power diodes and switches are obtained by applying the KVL law on the equivalent circuits of the proposed converter in Fig. 4 in both charge and discharge modes. The voltage stresses in Table III is expressed as functions of $M_{\rm boost}$ and $M_{\rm buck}$ using (6) and (10). Also, normalized total voltage stresses of semiconductors (NTVS) and NTVS per semiconductors number (NTVSN) is indicated in Table III. The values of normalized voltage stresses on each diodes and switches with respect to voltage gain in both charging and discharging modes are shown in Fig. 9.

IV. Components Sizing

Using steady-state equations of first state in charge and discharge modes, inductances, and capacitors values by assuming $R_d=R_s=0$ can be obtained

$$C_1=\frac{-d_1i_{L2}}{\Delta V_{C1}f_S}=\frac{d_3\left(i_{\rm in}-i_{L2}\right)}{\Delta V_{C1}f_S} \tag{11}$$

TABLE III
Voltage Stress of the Components

	Discharge mode	Charge mode
D_1	$(1-d_1)V_O=\frac{1}{\sqrt{M_{boost}}}V_O$	$d_3V_O=V_O\sqrt{M_{buck}}$
D_2	$d_1V_O=(1+\frac{1}{\sqrt{M_{boost}}})V_O$	$(1-d_3)V_O=V_O(1-\sqrt{M_{buck}})$
S_1	V_O	V_O
S_2	$(1-d_1)V_O=\frac{1}{\sqrt{M_{boost}}}V_O$	$d_3V_O=V_O\sqrt{M_{buck}}$
S_3	V_O	V_O
NTVS	$(4-d_1)V_O=(3+\frac{1}{\sqrt{M_{boost}}})V_O$	$(3+d_3)V_O=V_O(3+\sqrt{M_{buck}})$
NTVSN	$\frac{(4-d_1)}{5}V_O=\frac{(3+\frac{1}{\sqrt{M_{boost}}})}{5}V_O$	$\frac{(3+d_3)}{5}V_O=\frac{(3+\sqrt{M_{buck}})}{5}V_O$

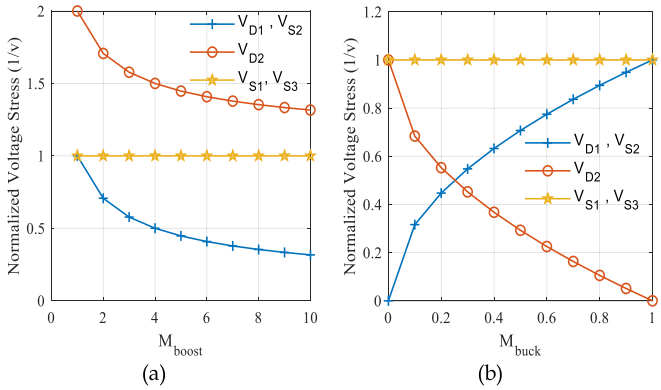


Fig. 9. NTVS in (a) discharge (boost) mode and (b) charge (buck) mode.

$$C_O=\frac{-d_1i_O}{\Delta V_Of_S}=\frac{d_3\left(i_{L2}-i_O\right)}{\Delta V_Of_S} \tag{12}$$

$$L_1=\frac{d_1V_{\rm in}}{\Delta i_{\rm in}f_S}=\frac{d_3\left(V_{\rm in}-V_{C1}\right)}{\Delta i_{\rm in}f_S} \tag{13}$$

$$L_2=\frac{d_1V_{C1}}{\Delta i_{L2}f_S}=\frac{d_3\left(V_{C1}-V_O\right)}{\Delta i_{L2}f_S} \tag{14}$$

Where ΔV_{C1}, ΔV_{C2} and $\Delta i_{\rm in}$, Δi_{L2} are capacitors voltage and inductances current ripples, respectively. Inductances value with respect to their currents ripples and d (d_1 or d_3) are shown in Fig. 10. It is obvious that decreasing in current ripple necessitates using large inductance. Capacitors values variation with respect to their voltage ripples and d (d_1 or d_3) are shown in Fig. 11. It is evident that decreasing in voltage ripple value necessitates using large capacitor. In Figs. 9 and 10, d is d_1 and d_3 in discharge and charge modes, respectively.

Based on (11) to (14), considering 10 kHz as switching frequency, $V_{\rm in}=36$ V, $V_O=155$ V, and maximum current and voltage ripple 1 A and 4 V, respectively, the value of passive components are $L_1=2$ mH, $L_2=500$ μH, $C_1=220$ μF, and $C_O=470$ μF.

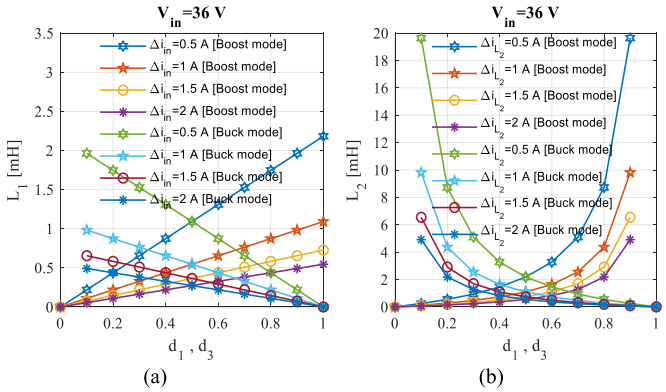


Fig. 10. Relationship between inductance and duty cycle in boost (discharging) and buck (charging) modes: (a) L_1 and d (d_1 or d_3) for different Δi_{in} and (b) L_2 and d (d_1 or d_3) for different Δi_{L2}.

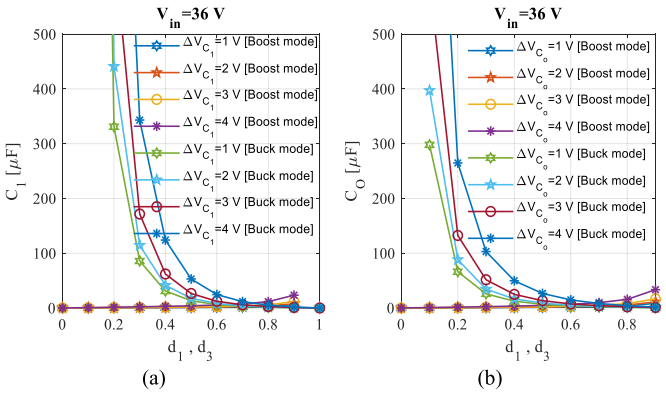


Fig. 11. Relationship between capacitor and duty cycle in boost (discharging) and buck (charging) modes: (a) C_1 and d (d_1 or d_3) for different ΔV_{C1} and (b) C_O and d (d_1 or d_3) for different ΔV_{Co}.

V. Nonlinear Control of Proposed Converter Based on Input–Output Linearization

In this section, dynamic nonlinear model of the proposed dc–dc converter is used to design a nonlinear controller by using IOFL [20], [22]. The nonlinear controller must be able to control the output voltage in discharge and the input current in charge modes by modulating the duty cycle, d_1 and d_3.

A. Design of Nonlinear Controller for Discharge Mode

The designed control scheme consists of inner and outer loops in discharge mode. The inner loop is to control the inductor current i_{in} (input current) and the outer loop is to control the output voltage V_O. These two loops are thoroughly described in the following subsections.

1) Design of Nonlinear Controller of Inner Loop in Discharge Mode: With reordering (1) to (3), the state equations are rewritten as

$$x' = f(x) + g(x)u, y = h(x) \tag{15}$$

Where $f(x)$, $g(x)$, and u are obtained as

$$f(x) = \begin{bmatrix} \frac{-1}{L_1}x_3 + \frac{1}{L_1}V_{\text{in}} \\ \frac{1}{L_2}x_3 - \frac{1}{L_2}x_4 \\ \frac{1}{C_1}x_1 - \frac{1}{C_1}x_2 \\ \frac{1}{C_O}x_2 - \frac{1}{C_O}x_5 \\ \frac{1}{L_O}x_4 - \frac{R}{L_O}x_5 - \frac{1}{L_O}E \end{bmatrix}, g(x) = \begin{bmatrix} \frac{1}{L_1}x_3 \\ \frac{1}{L_2}x_4 \\ -\frac{1}{C_1}x_1 \\ -\frac{1}{C_O}x_2 \\ 0 \end{bmatrix}, u = d_1. \tag{16}$$

As mentioned above, the purpose of the first loop in the controller is to control the current of L_1, (i_{in}). Therefore, $y = x_1$ and $\psi_1(x) = h(x) = y$. The relative degree of the output in the inner loop is $r = 1$.

In order to design the inner loop a new coordinate should be defined as

$$Z = T(x) = \begin{bmatrix} h(x) \\ x_2 \\ x_3 \\ x_4 \\ x_5 \end{bmatrix} = \begin{bmatrix} \xi_1 \\ \eta_1 \\ \eta_2 \\ \eta_3 \\ \eta_4 \end{bmatrix} \tag{17}$$

Where $\xi_1' = x'_1 = \frac{-1}{L_1}x_3 + \frac{1}{L_1}V_{\text{in}} + \frac{1}{L_1}x_3 u$.

In (17), ξ_1 is used to define the control law and η is zero dynamics. In IOFL, η' must be asymptotically stable at the point that is indicated by the following expressions, in this case the system is called minimum phase:

$$Z^* = \{x \in R^5 | \xi_1 = 0\}, \; u(x) = u^*(x) = -\frac{\xi'_1 f(x)}{\xi'_1 g(x)}\Big|_{x=Z^*}. \tag{18}$$

Referring to (18) by substituting u in (17), η' will be stable and minimum phase. A linear controller must be designed using the pole placement method to ensure that ξ_1 reaches the desired value of Y_r. New control inputs are given as

$$e_1 = \xi_1 - Y_r \Rightarrow e'_1 = \xi'_1 - Y'_r = V_1 = k_1 e_1. \tag{19}$$

By substituting ξ'_1 in (19), this equation can be rewritten as

$$V_1 = \frac{-1}{L_1}x_3 + \frac{1}{L_1}V_{\text{in}} + \frac{1}{L_1}x_3 u \Rightarrow u = \frac{L_1 V_1 + x_3 - V_{\text{in}}}{x_3} \tag{20}$$

Where V_1 is the control law in inner loop. To design a stable controller and ensure left-side poles, the coefficient k_1 must be negative.

2) Design of Nonlinear Controller of Outer Loop in Discharge Mode: If the inner loop correctly responds, e_1 and V_1 will be zero and $x_1 = x_{1\text{ref}}$. Referring to (16), the value of u in inner loop is d. Equation (14) is rewritten as

$$f(x) = \begin{bmatrix} \frac{1}{L_1}V_{\text{in}} + \frac{d_1 - 1}{L_1}x_3 \\ \frac{1}{L_2}x_3 + \frac{d_1 - 1}{L_2}x_4 \\ -\frac{1}{C_1}x_2 \\ \frac{1-d_1}{C_O}x_2 - \frac{1}{C_O}x_5 \\ \frac{1}{L_O}x_4 - \frac{R}{L_O}x_5 - \frac{1}{L_O}E \end{bmatrix}, g(x) = \begin{bmatrix} 0 \\ 0 \\ \frac{-d_1+1}{C_1} \\ 0 \\ 0 \end{bmatrix}, u = x_1 \tag{21}$$

Where d in the inner loop is obtained. As stated before, the purpose of the outer loop is to obtain the desired i_{in} where this current is the input of the controller.

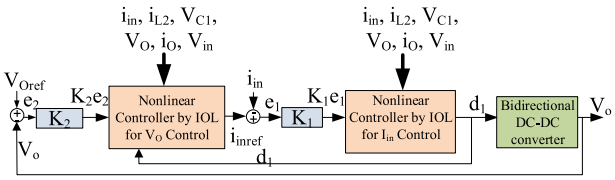


Fig. 12. Block diagram of the nonlinear controller using the IOFL method in discharge mode.

Whereas, the purpose of the outer control loop is to control V_o, the following equation is assumed, $\psi_1(x) = h(x) = y = x_4$. The relative degree of the output in the outer loop is $r = 3$. The controller input u is obtained as

$$u = \frac{1}{\frac{\partial \Psi_3}{\partial x} g(x)} \left(-\frac{\partial \Psi_3}{\partial x} f(x) + V_2 \right) \tag{22}$$

Where V_2 is the control law that is obtained as

$$V_2 = k_2 e_2 = k_2 (Y_2 - Y_{2\text{ref}}). \tag{23}$$

To preserve stability, the coefficient k_2 must be negative.

The block diagram of the nonlinear controller with the IOFL method in discharge mode is shown in Fig. 12. This figure shows how the duty cycle can be controlled by input–output linearization to obtain the desired output voltage.

B. Design of Nonlinear Controller for Charge Mode

The designed control scheme consists of one loop in charge modes. The loop is to control the inductor current i_{in} (input current) and described in the following.

With reordering (1) to (2) and (7), the state equations are rewritten as (15), where *f(x)*, *g(x)*, and *u* are obtained as

$$f(x) = \begin{bmatrix} \frac{1}{L_1} V_{\text{in}} \\ \frac{1}{L_2} x_3 \\ -\frac{1}{C_1} x_2 \\ -\frac{1}{C_O} x_5 \\ \frac{1}{L_O} x_4 - \frac{R}{L_O} x_5 - \frac{1}{L_O} E \end{bmatrix}, g(x) = \begin{bmatrix} -\frac{1}{L_1} x_3 \\ -\frac{1}{L_2} x_4 \\ \frac{1}{C_1} x_1 \\ \frac{1}{C_O} x_2 \\ 0 \end{bmatrix}, u = d_3. \tag{24}$$

As mentioned above, the purpose of the controller is to control the current of L_1, (i_{in}). Therefore, $y = x_1$ and $\psi_1(x) = h(x) = y$. The relative degree of the output in the inner loop is $r = 1$. In order to design, a new coordinate should be defined as (17) again.

Where, $\xi_1' = x'_1 = \frac{1}{L_1} V_{\text{in}} - \frac{1}{L_1} x_3 u$ ξ_1 is used to define the control law, η is zero dynamics, and η' must be asymptotically stable at the point that is indicated by the (18), in this case the system is called minimum phase. Again referring to (18) by substituting u in (17), η' will be stable and minimum phase.

A linear controller must be designed using the pole placement method to ensure that ξ_1 reaches the desired value of Y_r. New control inputs are given as

$$e = \xi_1 - Y_r \Rightarrow e' = \xi_1' - Y_r' = V = k_1 e. \tag{25}$$

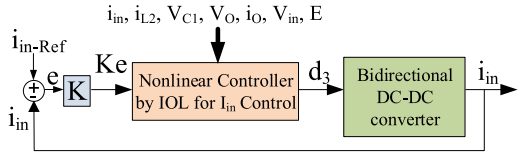


Fig. 13. Block diagram of the nonlinear controller using the IOFL method in charge mode.

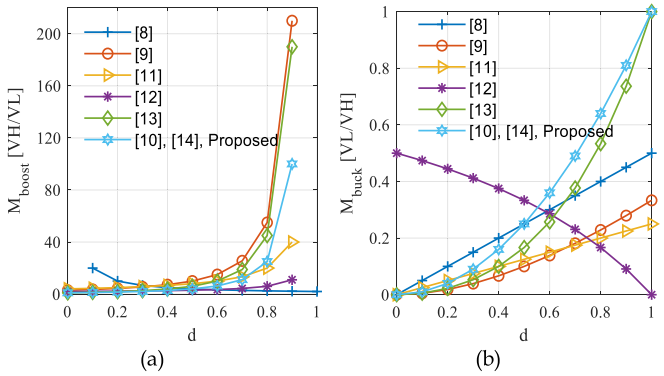


Fig. 14. Voltage gain curve comparison during (a) discharging (boost) and (b) charging (buck) modes.

By substituting ξ_1' in (19), this equation can be rewritten as

$$V = \frac{1}{L_1} V_{\text{in}} - \frac{1}{L_1} x_3 u \Rightarrow u = \frac{-L_1 V + V_{\text{in}}}{x_3} \tag{26}$$

Where V is the control law. To design a stable controller and ensure left-side poles, the coefficient k_1 must be negative.

The block diagram of the nonlinear controller with the input–output linearization method in charge mode is shown in Fig. 13. This figure shows how the duty cycle can be controlled by input–output linearization to obtain the desired input current.

VI. Literature Review of the High-Gain Converters

In this section, the proposed nonisolated bidirectional high-gain dc–dc converter is compared with the state-of-the-art nonisolated bidirectional dc–dc converters. To this end, the converters in [8], [9], [10], [11], [12], [13], and [14] are taken into consideration to be compared with the proposed converter. Different electrical parameters and required components of the considered converters along with the proposed one are listed in Table IV.

One of the most important parameters in dc–dc converters utilized in EVs is voltage gain. Ideally, the range of voltage gain in boost (discharge) mode is 1 to infinity, this parameter for buck (charge) mode is 0 to unity. In order to compare the considered converters from voltage gain and its limitation point of views, their voltage gain in both buck and boost modes is indicated in Fig. 14 and Table IV. As it is observed, the voltage gain and limitations of the proposed converter and the converters in [10], [13], and [14] can theoretically meet the abovementioned ideality. Moreover, referring to Table IV, it is seen that the proposed converter together with the converters in [10] and [14]

TABLE IV
COMPARISON OF THE CONSIDERED BIDIRECTIONAL DC–DC CONVERTERS

Compared converters		[8]	[9]	[10]	[11]	[12]	[13]	[14]	Proposed Converter
Utilized Component		**Number**							
Diode		0	0	0	0	0	0	2	2
Switch		4	6	4	6	3	5	4	3
Inductor		2	2	2	2	2	2	2	2
Capacitor		4	5	2	5	2	2	2	2
Parameters		**Values**							
Voltage gain	Boost mode	2/d	$(3-d)/(1-d)^2$	$1/(1-d)^2$	4/(1-d)	(2-d)/(1-d)	$(1+d)/(1-d)^2$	$1/(1-d)^2$	$1/(1-d)^2$
	Buck mode	d/2	$d^2/(2+d)$	d^2	d/4	(1-d)/(2-d)	$(d^2)/(2-d)$	d^2	d^2
Voltage gain range	Boost mode	2- ∞	3- ∞	1- ∞	4- ∞	2- ∞	1- ∞	1- ∞	1- ∞
	Buck mode	0-1/2	0-1/3	0-1	0-1/4	0-1/2	0-1	0-1	0-1
NTVS	Boost mode	2	(9-5d)/(3-d)	2	2.5	3/(2-d)	(6-2d)/(1+ d)	4-d	4-d
	Buck mode	2	(4+5d)/(2+d)	2+2d	2.5	3/(2-d)	$(4+2d)/d^2$	2	3+d
NTVC	Boost mode	(3+ d)/2	$(d^2-4d+5)/(3-d)$	2-d	(7-d)/4	2/(2-d)	$(d^2+4-3d)/(1+d)$	2-d	2-d
	Buck mode	(3+ d)/2	$(d^2+2d+3)/(2+d)$	d^2+d	(6+d)/4	2/(2-d)	$(d^2-d+2)/(2-d)$	1+d	1+d
Efficiency (%) @ Power(kW)	Boost mode	95@0.4	96@1	96 @0.5	97 @1.2	91 @0.04	96@0.5	88@0.2	95.9@0.16
	Buck mode	96@0.6	97@1	97 @0.5	97 @1.2	92 @0.04	97@0.5	88@0.2	97.2@0.27
Common ground		Yes	No	Yes	No	Yes	Yes	Yes	Yes

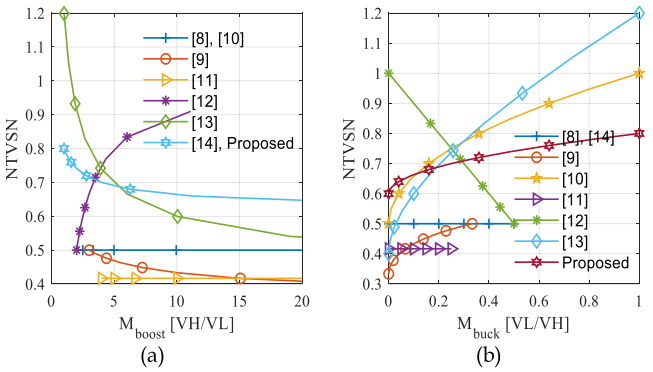


Fig. 15. NTVSN: (a) discharging (boost) and (b) charging (buck) modes.

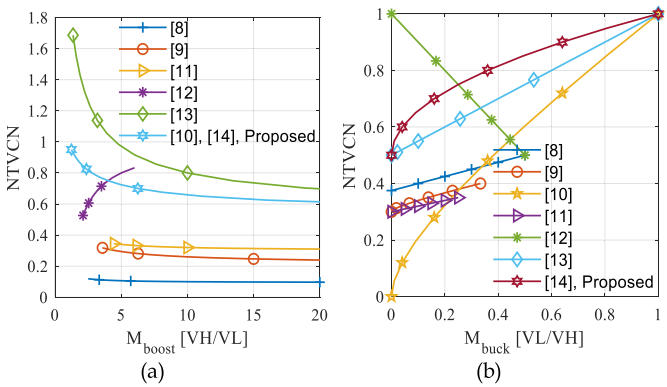


Fig. 16. NTVCN: (a) discharging (boost) and (b) charging (buck) modes.

offer the same voltage gain and can be considered as high-gain converters. Comparing the voltage gain to duty cycle curve in buck and boost modes of the converters, which are shown in Fig. 14, it is evident that the voltage gain of converters in [10] and [14] is the same as that of the proposed converter. Although the voltage gain curve of converter in [13] in boost mode is higher than that of the proposed converter, in buck mode, the voltage gain curve of converter in [13] is lower than that of the proposed converter. As a drawback the converter in [13] needs higher number of switches compared to the proposed converter.

Sharing a common ground between the input and output can be a significant merit of dc–dc converters. This feature can effectively alleviate the EMI. As indicated in Table IV, except the converters in [9] and [11], all the compared converters including the proposed one are common ground.

NTVSN and normalized total voltage stresses of capacitors per capacitors number (NTVCN) are the other important competence factors in dc–dc converters. The NTVSN and NTVCN curves with respect to voltage gain in both boost and buck modes are exhibited in Figs. 15 and 16.

As shown in Figs. 15 and 16, although the converters of [8], [9], and [11] have low NTVSN and NTVCN in boost mode compared to the proposed converter, their voltage gain range is limited. Furthermore, even though the converters in [8], [9], [11], and [12] have low NTVSN and [8], [9], and [11] have low NTVCN in buck mode compared to the proposed converter, their voltage gain range is limited, as well. For example, voltage gain of converter in [9] in boost mode is not between 0 and infinity, and in buck mode is not between 0 and unity. In other words, as indicated in Table IV, the voltage gain of the boost mode cannot be lower than 3 and for buck mode it cannot be higher than 1/3. Thus, it has limitation in both buck and boost modes.

Although the voltage gain of converter in [13] in buck and boost modes is better than that of the proposed one, the NTVSN and NTVSN of converter in [13] are higher than that of the proposed converter considering voltage gain ranged between 1 and 5, the NTVSN of the converter in [13] is higher than that of the proposed converter.

One of the most prominent advantages of the proposed converter, according to the Table IV, is the number of switches that is lower the compared converters. This can result in reduction in cost volume and complexity.

In this part, the proposed converter is compared with the dc–dc converter in [14]. The converter in [14] consists of a quadratic boost and a quadratic buck converters. The mentioned boost and quadratic converters are suggested in [18] and [23] and shown in Fig. 16(a) and (b), respectively. In converter in [14], this quadratic boost converter is restructured with an additional

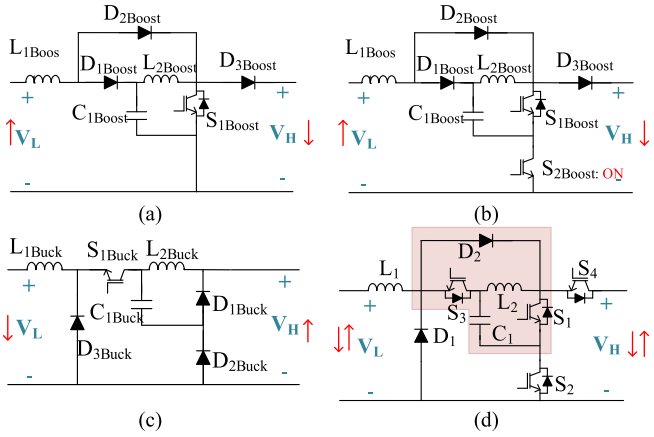


Fig. 17. Ingredient of converter in [14]: (a) quadratic boost converter in [18], (b) quadratic boost converter with an additional switch, (c) quadratic buck converter in [23], and (d) overall configuration quadratic bidirectional DC–DC converter.

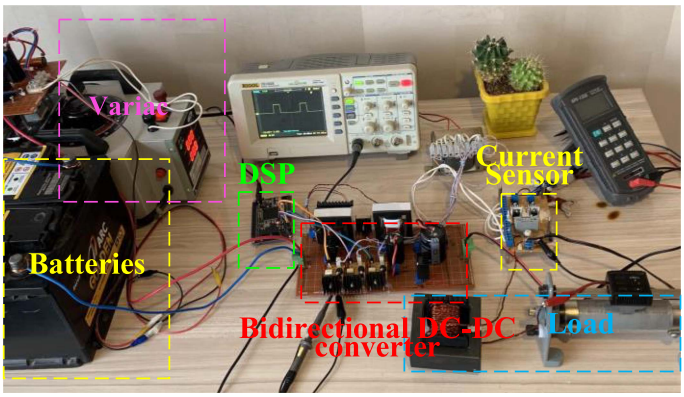


Fig. 18. Prototype of the proposed DC–DC converter.

switch ($S_{2\mathrm{Boost}}$) to combine it with a quadratic buck converter, as seen in Fig. 17(b). The resultant configuration is shown in Fig. 17(c). The mentioned switch ($S_{2\mathrm{Boost}}$) is always on in the boost mode. Finally, the overall configuration of the combined converter in [14] is depicted in Fig. 17(d).

The main difference of the proposed converter and converter in [14] is the buck mode of the quadratic converters. In the proposed converter, the quadratic buck converter, which is shown in Fig. 2(b), consists of two cascaded buck converters. However, the quadratic converter in [14] is a quadratic buck suggested in [23]. As an advantage, in the proposed converter, it is not necessary to add an extra switch to the quadratic boost converter to combine it with the buck converter. Thus, one switch can be reduced making the proposed converter simpler, cheaper, smaller, and efficient than the converter in [14].

VII. Experimental and Simulation Verification

A prototype of the proposed bidirectional dc–dc converter is employed to extract the experimental results and verify the theoretical analysis. The prototype is exhibited in Fig. 18 and the components utilized in the prototype are listed in Table V.

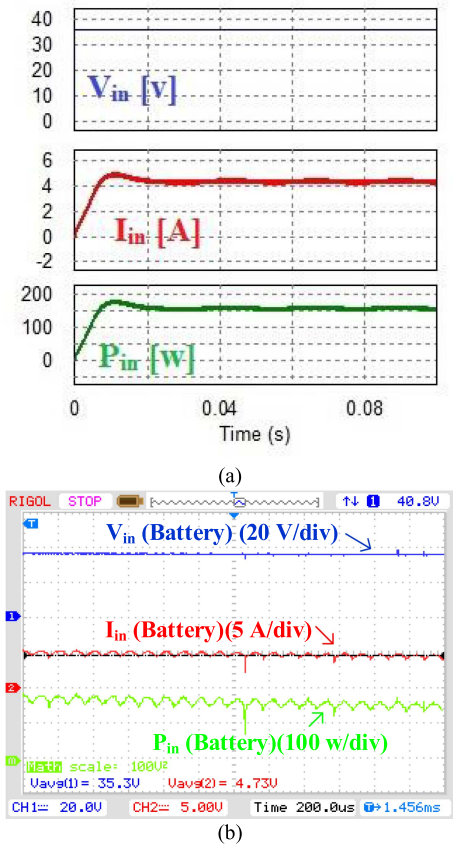


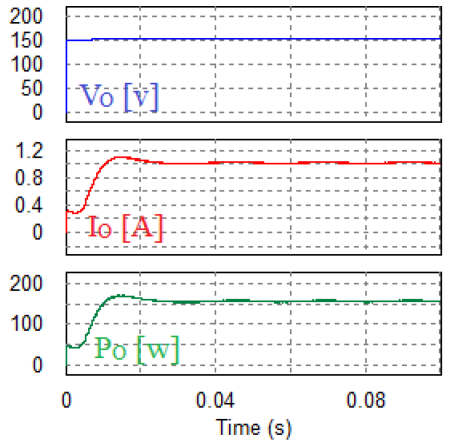
Fig. 19. Simulation and experimental results of input voltage, current, and instantaneous active power in discharge (boost) mode. (a) Simulation results. (b) Experimental results.

TABLE V
Proposed DC–DC Converter Parameters and Device Type

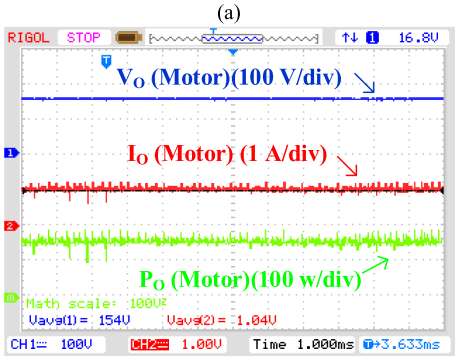
Device label	Definition
D_1, D_2	SFF508G 5A,600V
S_1~S_3	IRFP450
C_1 (μF)	220
C_O (μF)	470
L_1 (mH)	2
L_2 (mH)	0.5
Microcontroller	DSP-TMSF28335
Battery-side source	Three series connected batteries
Batteries characteristics	Lead-acid Calcium- 12 V-55 Ah

Fig. 19 shows the simulation and experimental results of the input current, voltage, and instantaneous power, and Fig. 20 shows the simulation and experimental results of the output current, voltage, and instantaneous power in discharge (boost) mode. According to this figure, the values of the input and output powers are 166.96 and 160.16 W, respectively, this means the efficiency of the proposed converter is 95.92% in discharge (boost) mode. As shown in these figures, with duty cycle of 0.52 and battery-side voltage of 36 V, the motor-side voltage is 155 V in discharge mode.

The experimental results of the V_{C1} are exhibited in Fig. 21. Considering the battery-side voltage is 36 V and the duty cycle



(a)



(b)

Fig. 20. Simulation and experimental results of output voltage, current, and power in discharge (boost) mode. (a) Simulation results. (b) Experimental results.

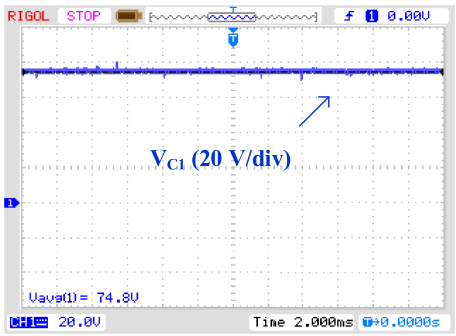


Fig. 21. Experimental result of voltage across C_1 (V_{C1}) in discharge (boost) mode.

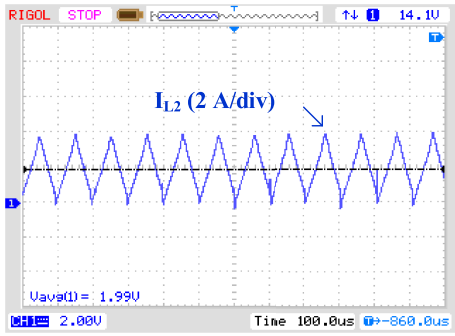
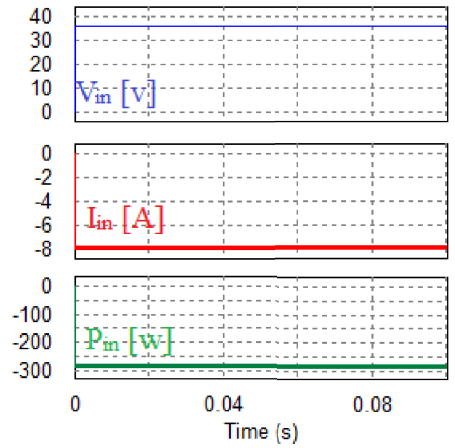
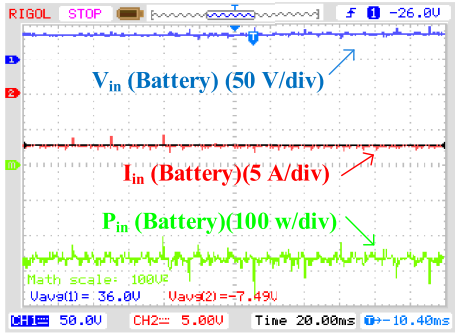


Fig. 22. Experimental result of current passing through L_2 (I_{L2}) in discharge (boost) mode.



(a)



(b)

Fig. 23. Simulation and experimental results of input voltage, current, and instantaneous active power in charge (buck) mode. (a) Simulation results. (b) Experimental results.

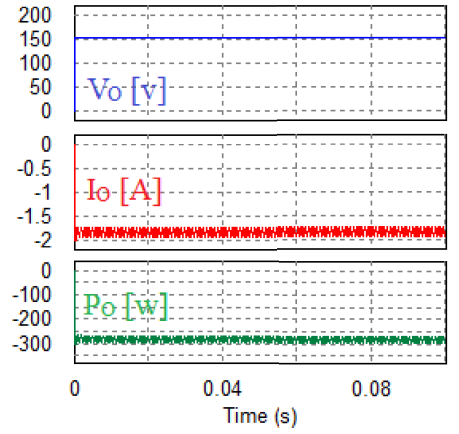
is 0.52, the shown value of voltage across C_1 (V_{C1}) verifies the third row of (4).

Since the current passing through L_2 goes through the active switches, this current is recorded and shown in Fig. 22.

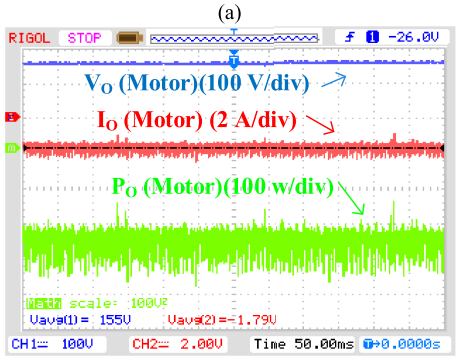
Fig. 23 shows the simulation and experimental results of the input current, voltage, and instantaneous power, and Fig. 24 shows the simulation and experimental results of the output current, voltage, and instantaneous power in charge (buck) mode. According to this figure, the values of the input and output powers are 277.45 and 269.64 W, respectively, this means the efficiency of driver is 97.2% in charge mode. Moreover, as shown in these figures, with duty cycle of 0.48 and motor-side voltage of 155 V, the battery-side voltage is 36 V in charge mode.

The experimental results of the V_{C1} are exhibited in Fig. 25. Considering the motor-side voltage is 155 V and the duty cycle is 0.48, the shown value of voltage across C_1 (V_{C1}) verifies the third row of (4).

Since the current passing through L_1 and L_2 go through the active switches, these currents are recorded and shown in Fig. 26.



(a)



(b)

Fig. 24. Simulation and experimental results of output voltage, current, and power in charge (buck) mode: (a) simulation results and (b) experimental results [the shown output power (P_O) is obtained by multiplying the output voltage and current into scope].

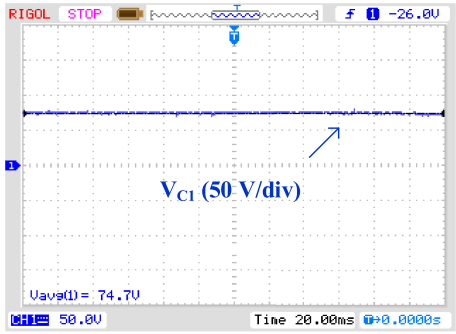
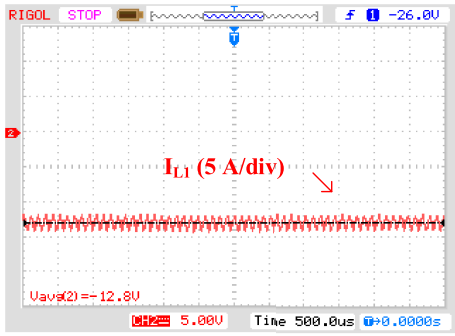
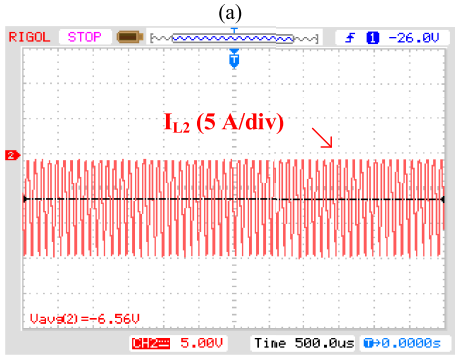


Fig. 25. Experimental result of voltage across C_1 (V_{C1}) in charge (buck) mode.

One of the most important parameters in any power electronics devices is the current stress of the utilized semiconductors. In order to scrutinize the mentioned parameter in the proposed dc–dc converter, the current stress of all the employed semiconductors along with the gate signal of the active switch *(S_1)* in discharge (boost) mode and *(S_3)* in charge (buck) mode are indicated in Figs. 27 and 28. According to these figures, S_1 and D_2 tolerate the highest and lowest current stress, respectively.

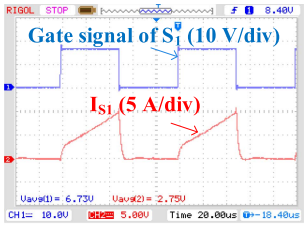


(a)

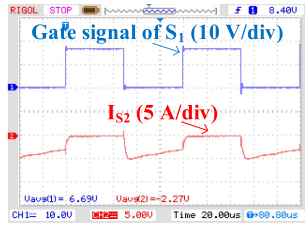


(b)

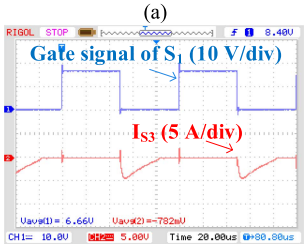
Fig. 26. Experimental result of current passing through inductors in charge (buck) mode: (a) L_1 (I_{L1}) and (b) L_2 (I_{L2}).



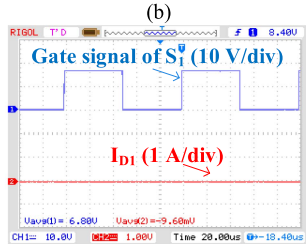
(a)



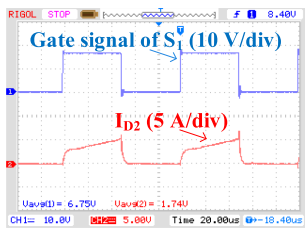
(b)



(c)



(d)



(e)

Fig. 27. Experimental results. (a) Gate signal of the switch S_1 and current of D_1. (b) Gate signal of the switch S_2 and current of D_2. (c) Gate signal of the switch S_1 and current of S_3. (d) Gate signal of the switch S_1 and current of D_1. (e) Gate signal of the switch S_1 and current of D_2 in discharge (boost) mode.

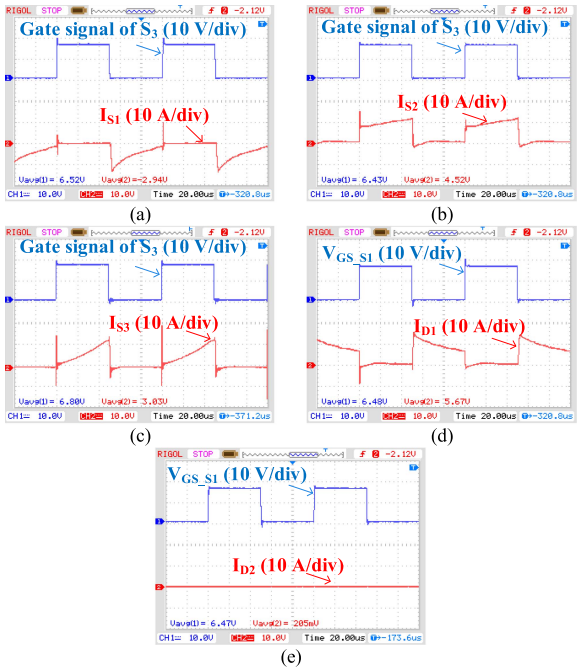


Fig. 28. Experimental results. (a) Gate signal of the switch S_1 and current of D_1. (b) Gate signal of the switch S_2 and current of D_2. (c) Gate signal of the switch S_1 and current of S_3. (d) Gate signal of the switch S_1 and current of D_1. (e) Gate signal of the switch S_1 and current of D_2 in charge (buck) mode.

VIII. Conclusion

In this article, a new extendable common-ground high-gain quadratic dc–dc converter for EVs applications was proposed. The proposed dc–dc converter has a nonisolated structure with bidirectional power supplying capability. It uses fewer switches and reduces voltage stress across the utilized semiconductors. Since in the proposed converter the input and output share the same ground (common-ground configuration), the EMI effects are alleviated. From the charging mode of view, the proposed converter is like two cascaded buck converters and from the discharging mode of view this converter is like a quadratic boost dc–dc converter. In comparison with prior-art dc–dc converters, the proposed converter has low NTVSN and NTVCN with high buck and boost voltage gain. Furthermore, the range of voltage gain in both buck and boost mode is not limited in the mentioned converter. In order to reach fast response, a nonlinear IOFL was designed for the proposed converter. The performance of this converter and designed nonlinear controlling approach were analyzed and verified through simulation and experimental results. The provided results validated the versatility of the proposed dc–dc converter and designed control approach.

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Tina Sojoudi received the B.Sc. degree in electrical engineering from the Tabriz Branch, Islamic Azad University, Tabriz, Iran, in 2012, and the M.Sc. degree in electrical engineering from the University of Tabriz, Tabriz, Iran, in 2015. She is currently working toward the Ph.D. degree in electrical engineering with the Department of Electrical Engineering, Kish International Branch, Islamic Azad university, Kish Island, Iran.

Her research interests include power electronic converters, electric vehicles, distribution networks, transmission lines, high-voltage substations, and renewable energy systems.

Mitra Sarhangzadeh received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the University of Tabriz, Tabriz, Iran, in 2001, 2004, and 2011, respectively.

She is currently an Assistant Professor with the Department of Electrical Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran. Her research interests include power electronic application in renewable energy systems, energy management in power electronic systems, modeling and control of power electronic systems, electrified railway systems, inverters, electric vehicles, and power quality compensation systems, such as SVC, UPQC, and FACTS devices.

Javad Olamaei (Senior Member, IEEE) received the B.S. degree from the Tabriz University, Tabriz, Iran, in 1988, the M.S. degree from the Amirkabir University of Technology, Tehran, Iran, in 1992, and the Ph.D. degree from the Islamic Azad University-Science and Research Branch, Tehran, Iran, in 2008, all in electrical engineering.

He was holding the Lecturer position from 1997 to 2009, an Assistant Professor Position to 2017, and has been an Associate Professor with the Department of Electrical Engineering, South Tehran Branch, Islamic Azad University, Tehran, Iran, since 2017. He has authored more than 120 journal and conference papers. His research interests include power distribution system, distribution automation system, microgrids, renewable energy, and VAR planning.

Jaber Fallah Ardashir received the B.Sc. degree from the Electrical Engineering Department, Azerbaijan Shahid Madani University, Tabriz, Iran, in 2010, the M.Sc. degree from the Electrical Engineering Department, Zanjan University, Zanjan, Iran, in 2012, and the Ph.D. degree from the Electrical Engineering Department, Tabriz University, Tabriz, Iran, in 2017, all in electrical engineering.

He also served as a Visiting Ph.D. Scholar with the Department of Energy, Aalborg University, Aalborg, Denmark from 2015 to 2016. He is currently an Assistant Professor of electrical power engineering with the Department of Electrical Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran. His research interests include power electronic converters, renewable energy systems, and reliability.