Adaptive Level-Shift Gate Driver With Indirect Gate Oxide Health Monitoring for Suppressing Crosstalk of SiC MOSFETs

Ho-Tin Tang, *Student Member, IEEE*, Henry Shu-Hung Chung, *Fellow, IEEE*, and Kevin Jing Chen, *Fellow, IEEE*

***Abstract*—An adaptive level-shift gate driver with indirect gate oxide health monitoring for suppressing crosstalk of bridge-leg configured SiC MOSFETs is proposed. This article firstly presents a holistic assessment of the changes in major intrinsic parameters before and after aging SiC MOSFETs with repetitive short-circuit tests. Gate leakage is found to be an appropriate precursor to reflect gate oxide degradation. Then, the structure, operation, and design of the proposed gate driver are given. The working principle is based on using a digitally controlled variable resistor in a resistor-capacitor-based voltage divider network to adjust the OFF-state gate-source voltage. Then, the peak OFF-state gate-source voltage caused by the spurious voltage is regulated at a level that can avoid shoot-through and reduce OFF-state voltage stress on the gate. Besides suppressing crosstalk, an optimal OFF-state gate-source voltage can also improve the life expectancy of SiC MOSFET. By utilizing the loading effect of the gate leakage current on the proposed gate driver output, the gate oxide degradation is indirectly monitored by observing the change in the value of the variable resistor. The proposed gate driver has been evaluated on a 1-kW inverter prototype under various intrinsic parameter variations. Performance comparisons between proposed and traditional gate drivers are given.**

***Index Terms*—Bridge-leg configuration, diagnosis, gate driver, level shifter, SiC MOSFETs, spurious voltage pulses.**

I. Introduction

BRIDGE-LEG configuration, constructed by two series-connected switching devices, is widely used in modern power electronic systems, from low-power dc/dc converters with synchronous rectification to high-power multilevel systems. The two devices are switched alternately with a dead time introduced to prevent shoot-through. Depending on the current direction at the midpoint of the bridge leg, each device operates either as a *control* switch or as a *synchronous* switch. However, due to the parasitic elements of the switch and circuit layout, crosstalk occurs when the control switch is turned ON while the synchronous switch is turned OFF. The mechanism is briefly described as follows. First, upon turning ON the control switch, the drain-source voltage of the synchronous switch rises abruptly. A displacement current is induced and injected into the gate of the synchronous switch through gate-source capacitance. Second, when the synchronous switch transits to the blocking state, its drain current reduces abruptly. A negative voltage is induced across the inductance associated with the source of the synchronous switch, such as source inductance of the switch and printed circuit board trace inductance.

The above phenomena lead to unwanted spurious voltage pulses on the gate-source voltage of the synchronous switch that might cause false triggering and result in excessive switching losses, network oscillations, and even intermittent shoot-through [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17]. The influence of intrinsic elements on the *crosstalk* mechanism is discussed in detail in [1] and [2]. A large body of literature has been devoted to addressing the crosstalk effect. The techniques can be classified into two main approaches. The first one is based on limiting the magnitude of the spurious voltage pulses on the gate-source voltage. As the induced voltage can be approximated by $R_g C_{gd} dv/dt$, where R_g is gate resistance, C_{gd} is gate-drain capacitance, and dv/dt is the rate of change of the gate-source voltage of the synchronous switch, its magnitude can be lowered by using a small turn-OFF gate resistor [18], [19], [20], [21], [22], [23], paralleling a capacitor [18], [19], [24] or a diode [25], [26], [27] across the gate resistor, or introducing a low impedance path between gate and source terminals with a bipolar junction transistor (BJT) or MOSFET at turn OFF [19], [20], [21], [22], [24], [30], [31], [32], [33]. When the switching device is in synchronous mode, a low OFF-state impedance path can help reduce the spurious voltage. However, when it is in control mode, the use of a small gate driving resistor will cause ringing on the gate-source voltage and a high spurious voltage on the other switching device in the phase leg and electromagnetic interference issue. It also requires a gate driver, which allows a high sinking current. Thus, as discussed in [34], the selection of the external gate resistor will affect drive current, gate-driver power dissipation, and rise and fall times.

Manuscript received 21 July 2022; revised 4 November 2022 and 12 February 2023; accepted 11 April 2023. Date of publication 18 April 2023; date of current version 21 June 2023. This work was supported in part by the Research Grants Council of the Hong Kong Special Administrative Region, China under Grant #R6008-18, and in part by the Innovation and Technology Fund of the HKSAR, China under Grant #ITS/051/20. Recommended for publication by Associate Editor D. Dong. *(Corresponding author: Henry Shu-Hung Chung.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3268129.

Digital Object Identifier 10.1109/TPEL.2023.3268129

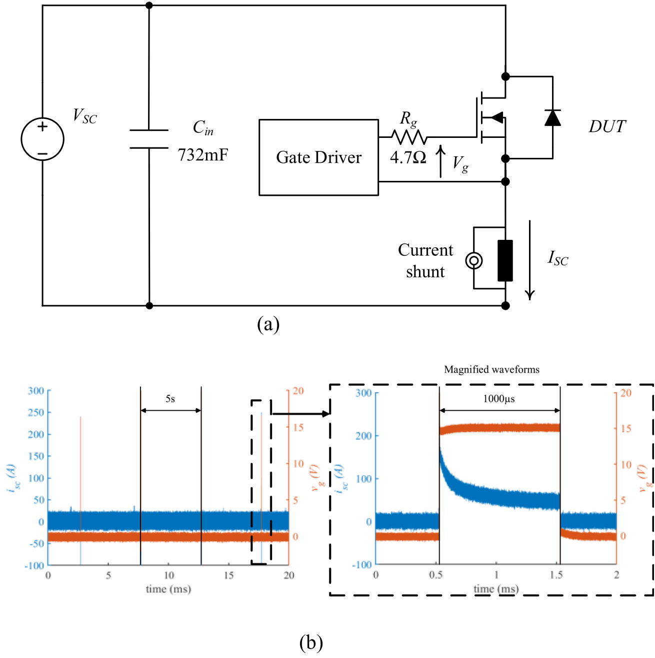


Fig. 1. SC-current stress test. (a) Circuit schematic. (b) Waveforms of v_g and i_{SC}.

The tradeoff between the fast rise and fall times versus oscillations is why the external gate resistor element of the gate-drive design is so valuable. Hence, the crosstalk phenomenon can only be mitigated, but not eliminated, by using a gate resistor. More importantly, the design value for the gate resistor is applicable to the nominal condition of the switching device. Upon aging, the gate resistance value has to be varied because the intrinsic parameters of the switching device have changed.

The second approach is based on superimposing a negative offset voltage onto the gate-source voltage to counteract the impact of the spurious voltage pulses. Many methods have been proposed to generate such negative offset voltage. They include an additional voltage source for the totem pole driver output [6], [20], [25], [26], [27], [35], [36], [37], [38], passive circuits [7], [8], [9], [10], [11], [24], [28], [29], [39], [40], [41], [42], active circuits [20], [23], [25], [26], [27], [30], [35], [36], [37], [43], [44], [45], [46], [47], [48], [49], [50], or charge pump circuits [23], [28], [43], [44]. However, high negative gate-source voltage would shorten the lifespan of the switching device. In particular, SiC MOSFETs have a thin gate oxide layer. The electric field within the gate oxide and between the drain and the source will increase if the SiC MOSFET is subject to a high negative gate-source voltage. As stated in [50] and [51], negative voltages may reduce the lifetime of the gate oxide. In addition, the forward voltage drop of the body diode increases with the magnitude of the gate-source voltage during reverse conduction [53]. Several multilevel gate-driving technologies [50], [51], [52] have been proposed. The key concept is based on applying a large, short-duration negative gate-source voltage to counteract the spurious voltage pulse caused by the crosstalk phenomena and then applying a small static gate-source voltage at the steady state to reduce gate oxide stress and lower the forward voltage drop of the body diode. However, additional power supply, fast-switching devices, and controllers are required.

As the magnitude of the spurious voltage pulses depends on several intrinsic and extrinsic factors, such as parasitic elements, drain current, and aging condition of switches, a gate driver, which can adaptively change the OFF-state negative gate-source voltage to minimize voltage stress of the gate oxide, can extend the lifetime of the switching device. Section II presents the experimental results of the drift of intrinsic parameters of eight different SiC MOSFETs before and after going through short-circuit-current stress cycling for 4000 times. The results show that the magnitude of the spurious voltage pulses diminishes after aging. In Section III, a gate driver that can adjust the OFF-state gate-source voltage dynamically to counteract the spurious voltage pulses is presented. Based on observing the change of the introduced OFF-state gate-source voltage, the gate oxide degradation of the switch is monitored indirectly. The proposed gate driver is evaluated on a 1-kW H-bridge inverter in Section IV. Experimental results are in close agreement with the theoretical prediction. Finally, Section V concludes this article.

II. Overview of the Drift of Intrinsic Parameters After Repetitive SC Cycling

This section summarizes the drift of seven parameters of eight different SiC MOSFETs after completing repetitive short-circuit (SC) tests. The devices are labeled from A to H. The parameters include threshold voltage V_{th}, ON-state resistance $R_{ds,\text{on}}$, drain-source leakage current I_{dss}, gate-source leakage current I_{gss}, gate-source capacitance C_{gs}, drain-source capacitance C_{ds}, and drain-source capacitance C_{ds}. Each test is stopped after repeating 4000 SC stress cycles due to a significant increase in gate leakage current. The authors in [57], [58], [61], [62], [63], [64], [66], [67], and [68] have reported aging studies of SiC MOSFETs under repetitive SC pulses. The authors in [54], [55], [56], [59], [60], and [65] have reported the parameter changes under power cycling for a few hundred hours. Comparing the results obtained by repetitive SC test and normal power cycling, the variation trend of V_{th}, $R_{ds,\text{on}}$, I_{dss}, and I_{gss} is similar.

The cycling procedure is based on the one described in [69], [70], [71], and [72]. Each device under test (DUT) is evaluated on a setup shown in Fig. 1. In each cycle, it is turned ON for 1000 μs and then turned OFF for 4.999 s to lower the effect of self-heating. In other words, each DUT takes 5.56 h to complete a cycling test. The parameters before and after the cycling are recorded.

V_{th} is measured by recording the gate-source voltage and drain current when the drain-source voltage $V_{ds} = 10$ V and drain current $I_d = 5$ mA. Fig. 2(a) shows the changes, ranging from 2.7% to 19%. A similar trend is reported in [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64], [65], and [69]. $R_{ds,\text{on}}$ is measured indirectly by measuring the voltage and current of the SiC MOSFET when $V_{gs} = 15$ V and $I_d = 20$ A. Fig. 2(b) shows the changes, ranging from 11.7% to 33.1%. A similar trend is reported in [54], [55], [56], [57], [58], [59], [60], [66], and [67]. I_{dss} is measured under $V_{ds} = 100$ V. Fig. 2(c) shows the changes of I_{dss}. A similar trend is reported

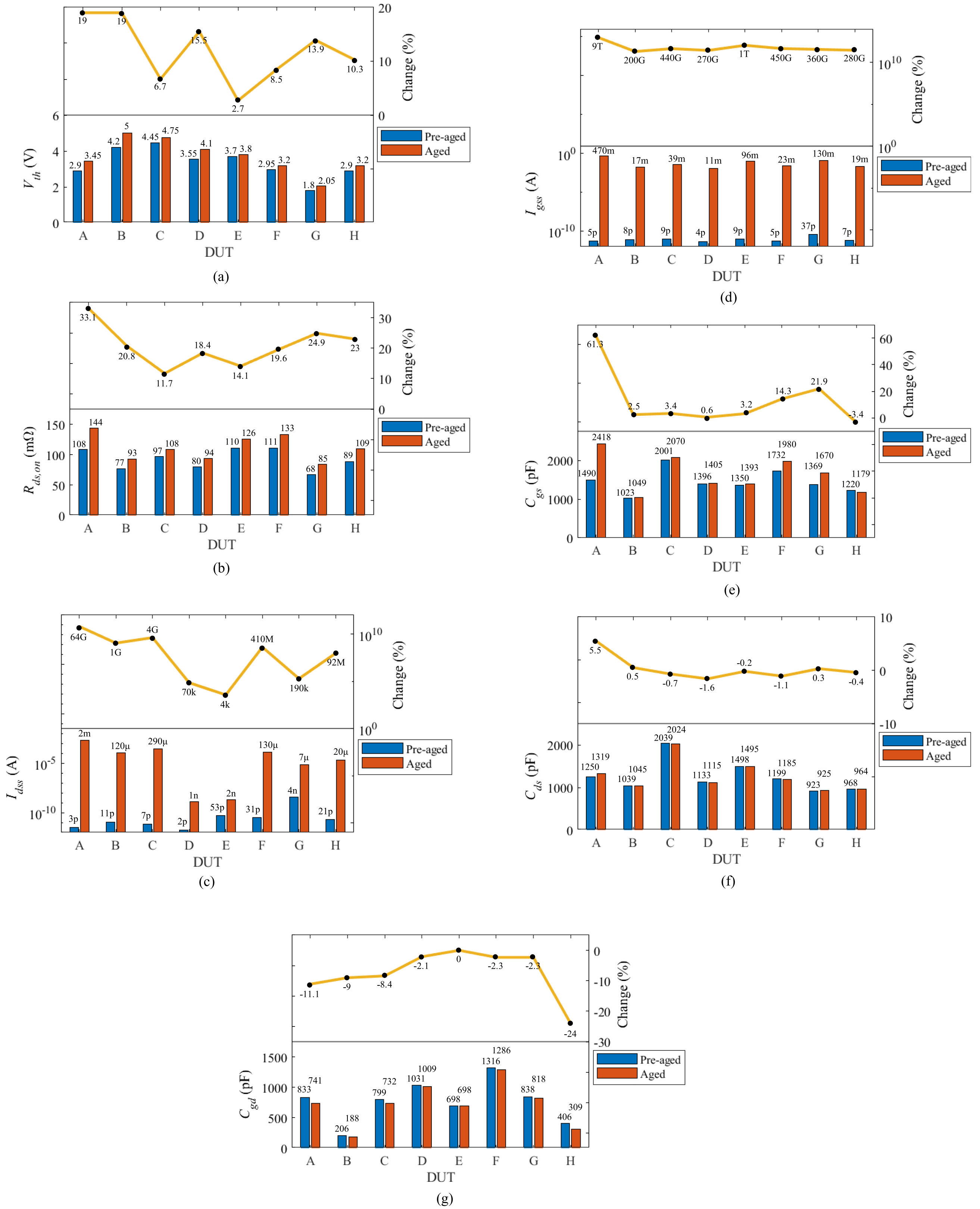


Fig. 2. Variation of various intrinsic parameters. (a) V_{th}. (b) $R_{ds,\text{on}}$. (c) I_{dss}. (d) I_{gss}. (e) C_{gs}. (f) C_{ds}. (g) C_{gd}.

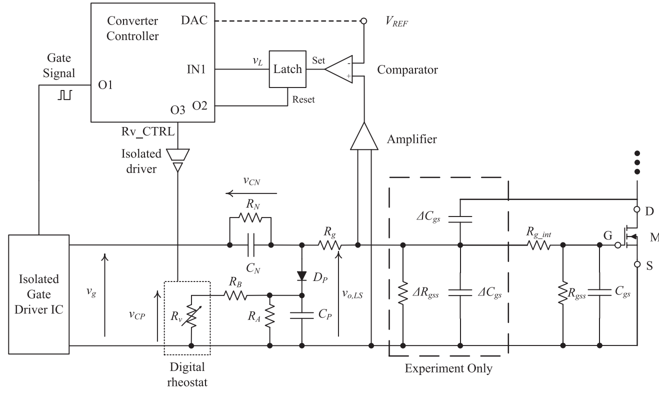


Fig. 3. Proposed adaptive level shifter with gate voltage detection.

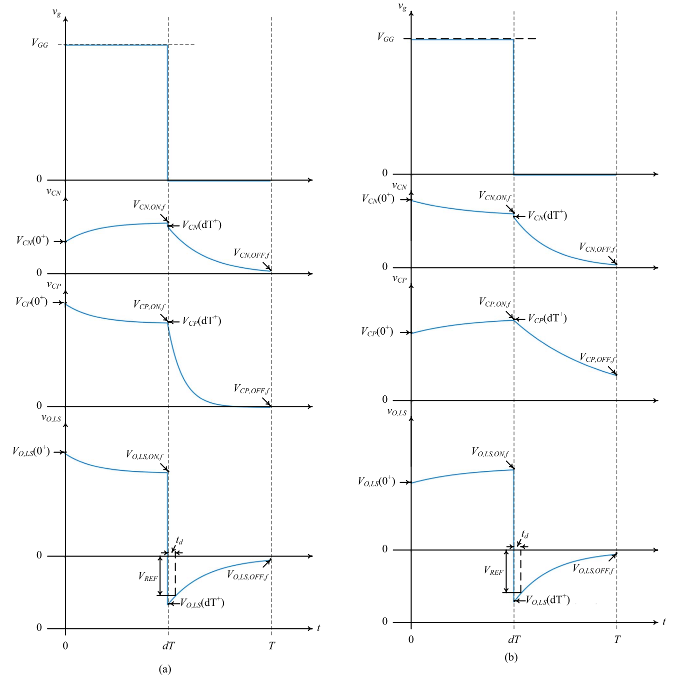


Fig. 4. Waveforms of the proposed circuit. (a) Case I. (b) Case II.

in [54], [55], [56], [57], and [66]. The increment is found to be more than 36 times. I_{gss} is measured when $V_{gs} = 15$ V. Fig. 2(d) shows a significant percentage increment. A similar trend is reported in [54], [55], [56], [58], [61], [62], [66], and [68]. C_{gs} is measured by a power device analyzer - Keysight B1506A, when $V_{ds} = 0$ V. Fig. 2(e) shows the changes of C_{gs}, ranging from –3.4% to 61%. C_{ds} is also measured by the power device analyzer when $V_{ds} = 0$ V. Fig. 2(f) shows the changes of C_{ds}, ranging from –1.6% to 5.5%. However, if the change of device A is excluded, the changes of the rest of the devices dominantly vary between –1.6% and 0.5%. A similar trend is reported in [54] and [55]. Finally, C_{gd} is also measured by the power device analyzer when $V_{ds} =$ 0V. Fig. 2(g) shows the changes of C_{gd}, ranging from 0% to –24%. A similar trend is reported in [63] and [69].

Based on the above observations, all parameters have different levels of changes after the cycling. Device aging can thus be monitored on the power handling side or the gate driving side. However, if it is done on the power handling side, sophisticated circuits, such as high-voltage and high-current sensing circuits, are required. If done on the gate driving side, sophisticated circuits will also be needed for extracting individual parameters. This article provides another perspective by utilizing the combined effects of the gate-related parameter changes on the magnitude of spurious voltage to monitor device aging. The parameters include I_{gss}, C_{gd}, and C_{gs}. As I_{gss} increases, and C_{gd} and C_{gs} decrease after the cycling, the magnitude of the spurious voltage reduces. As discussed in Section III, such information is used to adjust the negative OFF-state voltage and monitor device aging.

III. Proposed Adaptive Level Shifter

The architecture of the proposed adaptive level shifter is shown in Fig. 3. It consists of one diode D_P, two capacitors, C_N and C_P, three fixed resistors, R_N, R_A, and R_B, and one digital rheostat R_v. The converter controller dictates the gate signal via the port O1, senses the presence of peak OFF-state voltage higher than the threshold voltage v_{REF} via the port IN1, and generates the control command to R_v via the port O3. The total resistance across C_P and R_P, equals

$$R_P = \frac{R_A\left(R_B + R_v\right)}{R_A + R_B + R_v}. \quad (1)$$

With R_v varying between zero (short-circuit condition) and infinity (open-circuit condition), R_P varies between $R_{P,\min}$ and $R_{P,\max}$. Based on (1)

$$R_{P,\min} = \frac{R_A R_B}{R_A + R_B} \quad (2)$$

$$R_{P,\max} = R_A. \quad (3)$$

The gate driver IC output v_g is switched between 0 and V_{GG}. For the sake of simplicity in the analysis, the gate of the switching device M is modeled by an R_{gss}-C_{gs} network. As reported in Section II, R_{gss} is large initially and reduces upon aging. Thus, the impedance of the R_{gss}-C_{gs} network is typically larger than the gate resistance R_g and the internal gate resistance R_{g_int}, which is neglected in the following analysis. Let d and T be the duty cycle and switching period of M, respectively. The waveforms of v_g, the voltage across C_N, v_{CN}, the voltage across C_P, v_{CP}, and the output voltage of the level shifter $v_{o,LS}$ are shown in Fig. 4. The equivalent circuits in ON- and OFF-state operations of M are given in Fig. 5. They are denoted by Mode-1 and Mode-2 operations, respectively.

Some additional components are included in Fig. 3. ΔC_{gd} is used to vary the effective gate-drain capacitance that affects the magnitude of the spurious voltage, and then study the capability of the proposed gate driver in regulating the peak OFF-state gate-source voltage. ΔR_{gss} is used to provide an additional gate leakage path and thus study the capability of the proposed gate driver in monitoring the gate oxide condition. ΔC_{gs} is used to

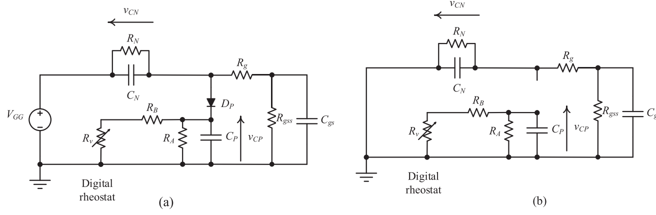


Fig. 5. Operation of the adaptive gate driver. (a) Mode 1 - ON-state. (b) Mode 2 - OFF-state.

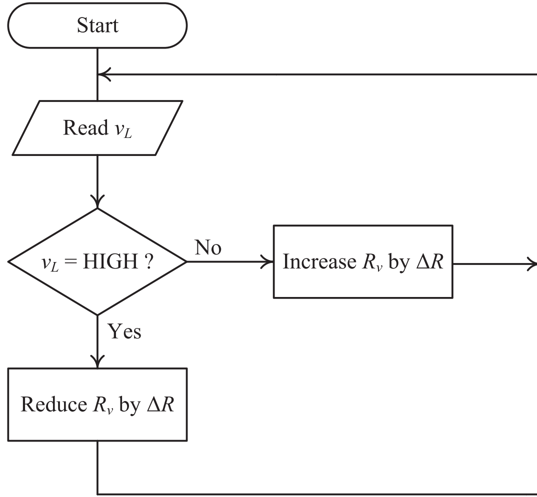


Fig. 6. Flowchart of the control mechanism.

vary the effective gate-source capacitance and thus study the driving capability of the proposed gate driver.

A. Mode 1-ON-State Operation

When M is turned ON, $v_g = V_{GG}$ and D_P conducts. Let the forward drop of D_P be zero. The equivalent circuit is shown in Fig. 5(a). v_{CN}, v_{CP}, and $v_{o,LS}$ are expressed as

$$v_{CN}(R_v,\, t) \;= v_{CN,ON}(R_v,\, t) =$$

$$\frac{(C_N+C_{P,ON})R_N+(C_{P,ON}\,R_{P,ON}-C_N\,R_N)\,e^{-\frac{t}{\tau_{ON}}})}{(C_N+C_{P,ON})(R_N+R_{P,ON})}\,V_{GG}$$

$$-\frac{C_{P,ON}\,e^{-\frac{t}{\tau_{ON}}}}{C_N+C_{P,ON}}\,V_{CP}(0^+)+\frac{C_N\,e^{-\frac{t}{\tau_{ON}}}}{C_N+C_{P,ON}}V_{CN}(0^+) \qquad (4)$$

$$v_{CP}(R_v,\, t) \;= v_{CP,ON}(R_v,\, t) =$$

$$\frac{(C_N+C_{P,ON})R_{P,ON}+(C_N R_N-C_{P,ON}\,R_{P,ON})\,e^{-\frac{t}{\tau_{ON}}})}{(C_N+C_{P,ON})(R_N+R_{P,ON})}\,V_{GG}$$

$$+\frac{C_{P,ON}\,e^{-\frac{t}{\tau_{ON}}}}{C_N+C_{P,ON}}\,V_{CP}(0^+)-\frac{C_N\,e^{-\frac{t}{\tau_{ON}}}}{C_N+C_{P,ON}}V_{CN}(0^+) \qquad (5)$$

$$v_{o,LS}(R_v,\, t) = v_{o,LS,ON}(R_v,\, t) = v_{CP,ON}(R_v,\, t) \qquad (6)$$

where $t \in [0 \quad dT]$, $V_{CN}(0^+)$ and $V_{CP}(0^+)$ are the initial voltages of C_N and C_P, respectively, $\tau_{ON} = C_{eq,ON}\,R_{eq,ON}$,

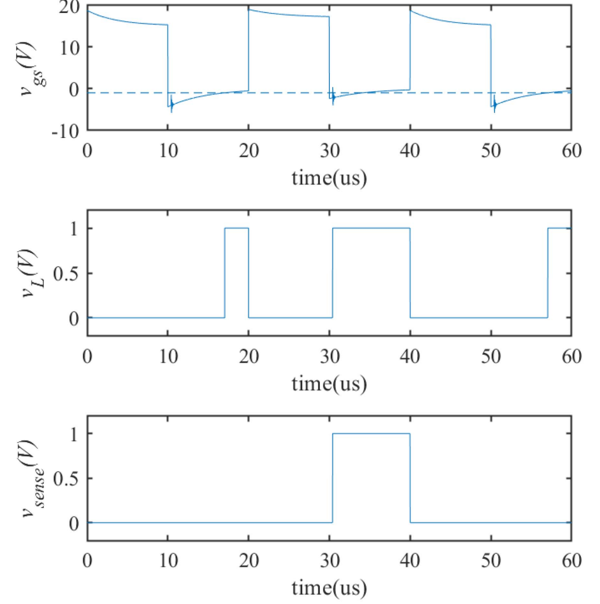


Fig. 7. Time sequences of three cycle of v_{gs}.

$C_{eq,ON} = C_N + C_{P,ON}$, $R_{eq,ON} = \frac{R_N\,R_{P,ON}}{R_N+R_{P,ON}}$, $C_{P,ON} = C_P + C_{gs}$, and $R_{P,ON} = \frac{R_P\,R_{gss}}{R_P+R_{gss}}$.

At the end of this mode, $v_{CN} = V_{CN,ON,f}$, $v_{CP} = V_{CP,ON,f}$, and $v_{o,LS} = V_{o,LS,ON,f}$. They can be expressed as

$$V_{CN,ON,f} = v_{CN,ON}(R_v,\, dT) \qquad (7)$$

$$V_{o,LS,ON,f} = V_{CP,ON,f} = v_{CP,ON}(R_v,\, dT). \qquad (8)$$

Based on (4) and (5), if $C_N > C_{P,ON}$(i.e., C_P is small), C_N undergoes charging while C_P undergoes discharging. Thus, $V_{CN}(0^+) < V_{CN,ON,f}$. The waveforms are shown in Fig. 4(a) (Case I). Conversely, if $C_N < C_{P,ON}$ (i.e., C_P is large), C_N undergoes discharging while C_P undergoes charging. Thus, $V_{CN}(0^+) > V_{CN,ON,f}$. The waveforms are shown in Fig. 4(b) (Case II). In both cases, the output voltage of the level shifter, $v_{o,LS}$, follows the voltage of C_P.

B. Mode 2 - OFF-State Operation

When M is turned OFF, $v_g = 0$ and D_P blocks. The equivalent circuit is shown in Fig. 5(b). v_{CN}, v_{CP}, and $v_{o,LS}$ are expressed as

$$v_{CN}(t) \;= v_{CN,OFF}(t) = e^{-\frac{t-dT}{\tau_{OFF}}}\,V_{CN}(dT^+) \qquad (9)$$

$$v_{CP}(R_v,\, t) \;= v_{CP,OFF}(R_v,\, t) = e^{-\frac{t-dT}{\tau_{CP}}}\,V_{CP}(dT^+) \qquad (10)$$

$$v_{o,LS}(t) = v_{o,LS,OFF}(t) = -v_{CN,OFF}(t) \qquad (11)$$

where $t \in [dT \quad T]$, $V_{CN}(dT^+)$ and $V_{CP}(dT^+)$ are the initial voltages of C_N and C_P, respectively, $\tau_{OFF} = C_{eq,OFF}$

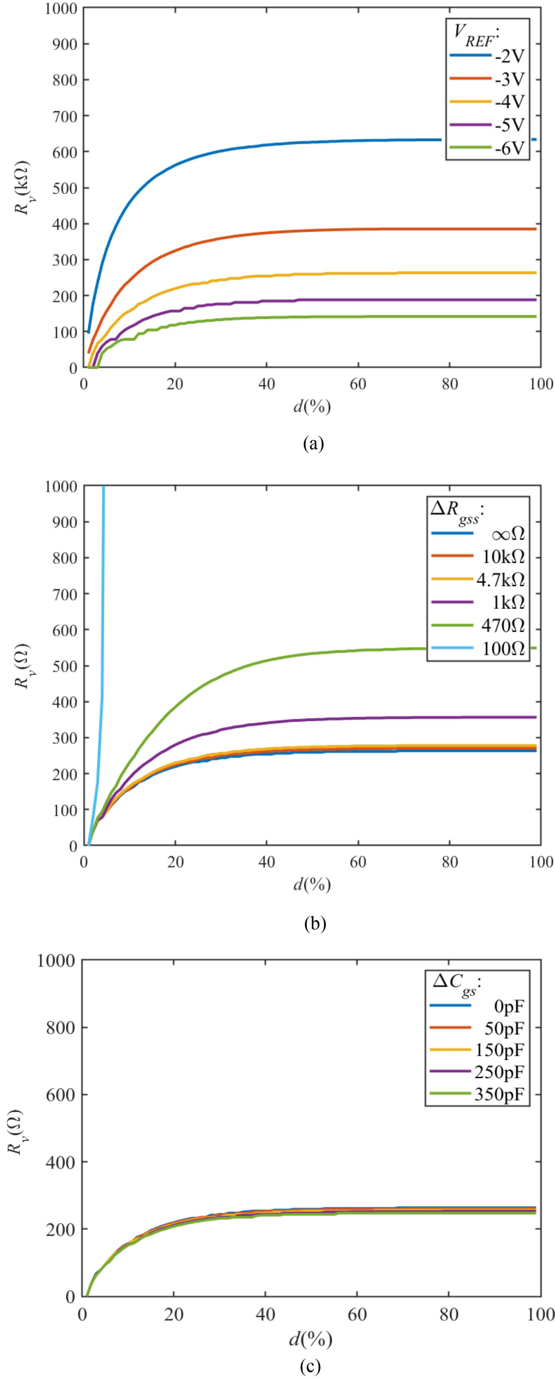
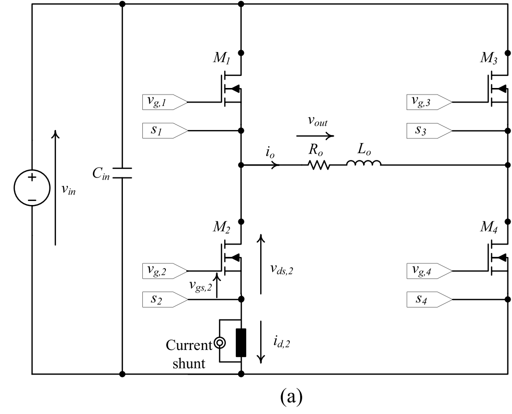


Fig. 8. Relationships between the duty cycle d and R_v. (a) With different values of V_{REF}. (b) With different values of ΔR_{gss}. (c) With different values of ΔC_{gs}.

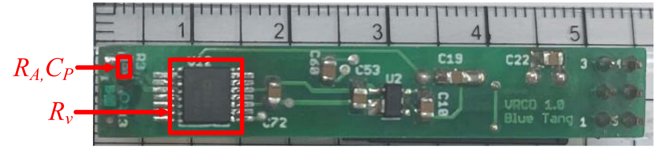
$R_{eq,OFF}$, $C_{eq,OFF} = C_N + C_{gs}$, $R_{eq,OFF} = \frac{R_N R_{gss}}{R_N + R_{gss}}$, and $\tau_{CP} = C_P R_P$.

At the end of this mode, $v_{CN} = V_{CN,OFF,f}$, $v_{CP} = V_{CP,OFF,f}$, and $v_{o,LS} = V_{o,LS,OFF,f}$. They can be expressed as

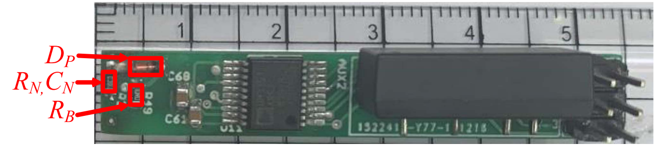
$$V_{o,LS,OFF,f} = -V_{CN,OFF,f} = -v_{CN,OFF}(R_v, (1-d)T) \tag{12}$$



(a)



(b)



(c)

Fig. 9. Testing schematic and proposed circuit prototype. (a) Circuit schematic. (b) Proposed circuit - top view. (c) Proposed circuit - bottom view.

$$V_{CP,OFF,f} = v_{CP,OFF}(R_v, (1-d)T). \tag{13}$$

Both C_N and C_P undergo discharging in this mode. The output voltage of the level shifter, $v_{o,LS}$, follows the voltage of C_P.With small C_P in Case I, C_P discharges quickly [Fig. 4(a)]. With large C_P in Case II, C_P discharges slowly [Fig. 4(b)].

C. Initial and Final Conditions Upon Switching

Fig. 4 shows the initial and final conditions of the capacitor voltages. The initial conditions of one mode are obtained from the final conditions of its previous mode. In Mode 1, when v_g is switched from 0 to V_{GG}, the charges stored in C_N and C_P are redistributed. By applying the law of conservation of charge, the voltage of C_N after the charge redistribution, $V_{CN}(0^+)$, and the voltage of C_P after the charge redistribution, $V_{CP}(0^+)$ can be expressed as

$$V_{CN}(0^+) = \frac{(C_P + C_{gs})V_{GG} + (C_N + C_{gs})V_{CN,OFF,f} - C_P V_{CP,OFF,f}}{C_N + C_P + C_{gs}} \tag{14}$$

$$V_{o,LS}(0^+) = V_{CP}(0^+) = V_{GG} - V_{CN}(0^+) = \frac{C_N V_{GG} - (C_N + C_{gs}) V_{CN,OFF,f} + C_P V_{CP,OFF,f}}{C_N + C_P + C_{gs}} \tag{15}$$

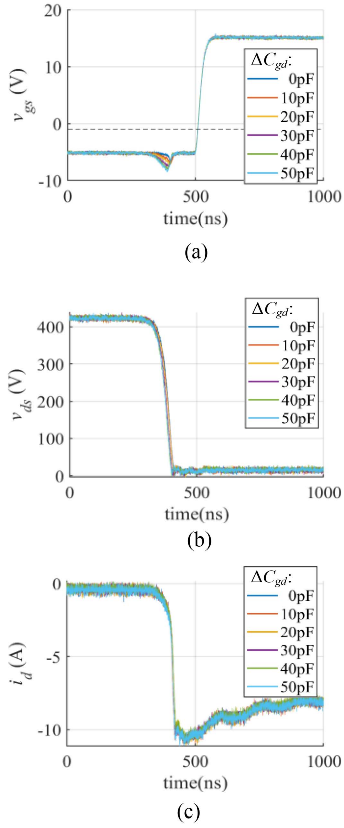


Fig. 10. Turn-ON waveforms of M_2 with the traditional gate driver. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

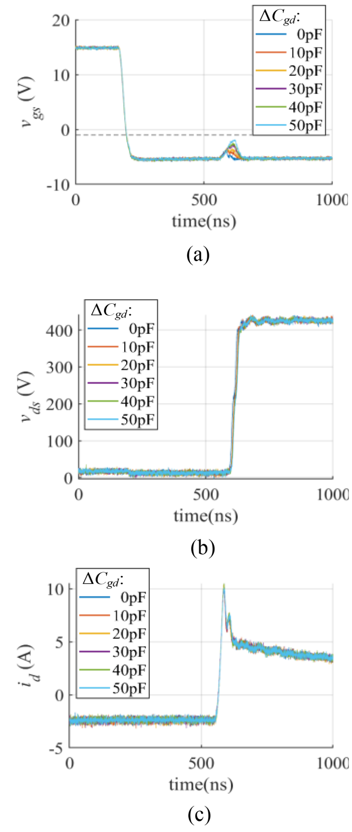


Fig. 11. Turn-OFF waveforms of M_2 with the traditional gate driver. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

where $V_{o,LS}(0^+)$, which is the same as $V_{CP}(0^+)$, is the initial output voltage of the level shifter in Mode 1.

In Mode 2, when v_g is switched from V_{GG} to 0, the charge stored in C_N is redistributed again. C_P discharges via R_P. The voltage of C_N after the charge redistribution, $V_{CN}(dT^+)$, and the voltage of C_P, $V_{CP}(dT^+)$, can be expressed as

$$V_{o,LS}(dT^+) = V_{CN}(dT^+) = \frac{C_N\, V_{CN,ON,f} - C_{gs}V_{CP,ON,f}}{C_N + C_{gs}} \tag{16}$$

$$V_{CP}(dT^+) = V_{CP,ON,f} \tag{17}$$

where $V_{o,LS}(dT^+)$, which is the same as $V_{CN}(dT^+)$, is the initial output voltage of the level shifter in Mode 2.

Since the value of C_P is chosen to be small, Case I operation is dominant.

D. Regulation of OFF-State Voltage

The shifting level of $v_{o,LS}$ is varied by changing the value of R_v, so that the spurious voltage is less than a threshold voltage of M. A spurious voltage typically occurs when the complementary power device is turned ON. That is, it appears after M has entered Mode 2 with a deadtime of t_d. In order to ensure that the spurious voltage will not trigger the switching device to turn ON, $v_{o,LS}$ at t_d should be no higher than V_{REF}. Based on (9)

$$v_{o,LS}(t_d) \leq V_{\text{REF}}$$

$$-e^{-\frac{t_d}{\tau_{OFF}}} V_{CN}(dT^+) \leq V_{\text{REF}}. \tag{18}$$

As illustrated in Fig. 3, when M has entered Mode 2, the gate-source voltage v_{gs} is sensed and compared with a reference voltage V_{REF}. The comparator output is latched to give the signal v_L. The peak spurious voltage is regulated around V_{REF} via a peak voltage control. Fig. 6 shows the flowchart of the control mechanism. Since the voltage will be discharged, after two deadtime intervals, i.e., $2\,t_d$, the controller will check the input pin IN1 for v_L once. If v_L is HIGH, it implies that $v_{gs} > V_{\text{REF}}$. The controller will decrease the value of R_v by ΔR_v, which is equal to unit change of R_v. For example, the eight-bit dual channel rheostat used in the experiment has a maximum value of 20 kΩ. The resolution of ΔR_v can achieve around 5 Ω, resulting in a change of v_{gs} in step of 0.1 V. If v_L is LOW, $v_{gs} < V_{\text{REF}}$. The controller will increase the value of R_v by ΔR_v. As a result, V_{CN} will be regulated to provide a minimum OFF-state voltage.

To illustrate the regulation mechanism, Fig. 7 shows the waveforms of v_{gs} and v_L in three switching cycles. In every switching cycle, the controller will check the signal v_L at $t = 2\,t_d$. In the 1st switching cycle, the OFF state v_{gs} is below V_{REF} at $t = 2\,t_d$. The voltage sensed by the controller is LOW. Then, the controller increases the value of R_v in the 2nd switching cycle. The OFF state v_{gs} is then higher than V_{REF} at $t = 2\,t_d$. The voltage sensed by the controller is HIGH. The controller decreases the value of R_v in the 3rd switching cycle.

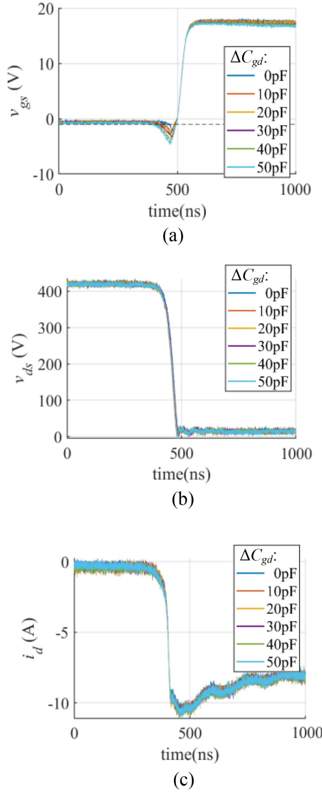


Fig. 12. Turn-ON waveforms of M_2 with the proposed gate driver. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

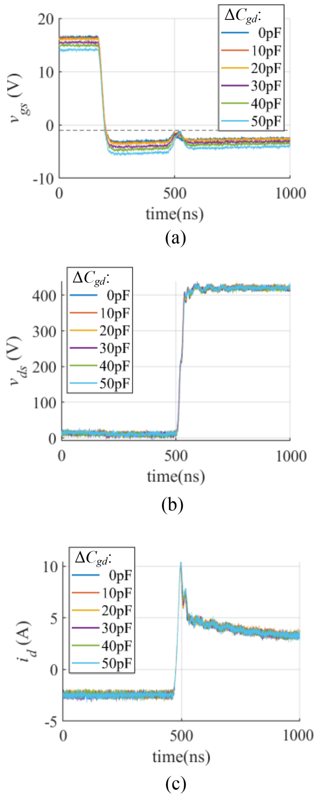


Fig. 13. Turn-OFF waveforms of M_2 with the proposed gate driver. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

TABLE I
LIST OF COMPONENTS

Parameter	Part no. / Value	Parameter	Part no. / Value
C_N	47 nF	R_N	100 Ω
C_P	4.7 nF	R_A	47 kΩ
C_{gs}	660 pF	R_B	10 Ω
V_{GG}	15 V	$R_{v,\max}$	10 kΩ
t_d	400 ns	R_g	4.7 Ω
D_P	1N4148		

E. Condition Monitoring of Switching Device

As the controller has information about the operating condition of the converter, such as the duty cycle of switching devices, supply and load conditions, and temperature, thus, the controller can keep tracking the change in the value of R_v under the same operating condition. By comparing the value of R_v with its value at the unaged condition, the health condition of the switch is monitored.

Fig. 8(a) shows the relationships between the duty cycle d and R_v with different values of V_{REF}. The value of R_{gss} is assumed to be infinite under the healthy condition. The component values are tabulated in Table I. The value of R_v can adjust the OFF-state voltage so that the condition of (18) can be satisfied. For the same duty cycle and loading condition, R_v increases as the magnitude of the spurious voltage decreases. For example, an aged switching device has a smaller value of C_{gd} than that in the healthy condition, giving a lower spurious voltage.

Fig. 8(b) shows the relationships between d and R_v with R_{gss} equal to infinity, 10 kΩ, 5 kΩ, 1 kΩ, and 100 Ω to represent different levels of degradation. The value of V_{REF} is set at –4 V. Since R_{gss} is in parallel with C_P, under the same duty cycle, the required values of R_v will increase as R_{gss} decreases.

Fig. 8(c) shows the relationships between d and R_v with additional capacitance ΔC_{gs} connected across gate and source terminals. ΔC_{gs} equals 0 pF, 50 pF, 150 pF, 250 pF, and 350 pF to represent different levels of degradation. The value of V_{REF} is set at –4 V and R_{gss} is infinity. The required values of R_v increase as C_{gs} decreases.

Therefore, based on Fig. 8, by observing the change of R_v at the considered duty cycle and loading condition, the condition of the switching device is monitored.

Compared with the traditional gate driver, the conduction loss of the SiC MOSFET can be reduced with the proposed gate driver. For example, the two gate driver ICs have the same total supply voltage of 20 V. The traditional gate driver requires two separate sources, i.e., +15 and –5 V, to make the gate-source voltage switch between +15 and –5 V. Using the proposed circuit, only a single +20 V supply is needed. The initial turn-ON gate-source voltage is fixed at 18 V at turn ON

and can be varied between 14.5 and 18 V at the steady state to adapt the required OFF-state voltage for counteracting spurious voltage pulses. Then, the maximum achievable OFF-state voltage is –5 V. Thus, the effective ON-state gate-source voltage is higher with the proposed gate driver. The conduction loss is lowered. The gate-source voltage level is within the device specification.

IV. Design Procedure

The values of C_N, C_P, R_N, R_A, and R_B, are designed by considering the following design criteria:

1) $V_{o,LS,\inf}(dT^+)$: Initial OFF-state gate-source voltage when $R_v \to \infty$, i.e., upon open-circuit fault in R_v
2) $V_{o,LS,\max}(dT^+)$: Initial OFF-state gate-source voltage when $R_v = R_{v,\max}$(maximum value of R_v)
3) $V_{o,LS,\min}(dT^+)$: Initial OFF-state gate-source voltage when $R_v = 0$ (minimum value of R_v)

A. Step 1 - Design of R_N, R_A, and R_B

By considering the steady-state gate-source voltage with different values of R_v

$$\frac{R_A}{R_A + R_N} = \frac{V_{GG} + V_{o,LS,\inf}(dT^+)}{V_{GG}} \tag{19}$$

$$\frac{R_A \parallel (R_B + R_{v,\max})}{R_N + R_A \parallel (R_B + R_{v,\max})} = \frac{V_{GG} + V_{o,LS,\max}(dT^+)}{V_{GG}} \tag{20}$$

$$\frac{R_A \parallel R_B}{R_N + R_A \parallel R_B} = \frac{V_{GG} + V_{o,LS,\min}(dT^+)}{V_{GG}}. \tag{21}$$

R_N, R_A, and R_B are determined by solving (19), (20), and (21).

B. Step 2 - Design of C_P

The value of C_P is chosen to be at least ten times larger than C_{gs}, so that the operation of the level shifter will not be dominated by C_{gs} in Mode-1 operation.

C. Step 3 - Design of C_N

The value of C_N is determined by considering the designed nominal value of R_v, $R_{v,norm}$. Thus, the time constants of the two *RC* networks are designed to be the same. Thus

$$C_N = \frac{(R_{v,norm} + R_B) \parallel R_A}{R_N} C_P. \tag{22}$$

V. Experimental Verification

The performances of the proposed level shifter are evaluated on a 1-kW, 400-Vdc/115-Vac full-bridge inverter with the proposed gate driver and traditional gate drivers. The output *LC* filter is constructed by an inductor $L_o = 0.7$ mH and a capacitor $C_o = 1$ μF. The circuit schematic and the photo of the proposed circuit are shown in Fig. 9. The nominal value of the load resistance R_L is 13.7 Ω. The switching frequency is 45 kHz. All switching devices are CREE C3M0065090J with the threshold voltage of 2.1 V and maximum allowable reverse gate-source voltage of –8 V. All gate driver ICs used are Skywork SI8233 [73], which can provide a peak output current of 4 A. When v_g is changed from 0 to V_{GG}, the capacitor charging current is not only limited by the diode, but also the gate driver. The supply voltages for the proposed gate driver are $V_{CC} = +20$ V and $V_{EE} = 0$ V. The supply voltages for the traditional gate driver are $V_{CC} = +15$ V and $V_{EE} = -5$ V.

The switching device M_2 has the proposed level shifter connected, while the rest of switching devices are driven by traditional gate drivers with the gate-source voltage switched between +15 and –5 V. The level shifter for M_2 is designed by following the design procedure described in Section IV. The component values are listed in Table I.

Different levels of crosstalk effect are emulated by using external components to vary the equivalent gate-drain capacitance, gate-source resistance, and gate-source capacitance. The observations are discussed as follows.

A. Effects of C_{gd}

To study the ability of the proposed gate driver to respond to different spurious voltages, a capacitor ΔC_{gd} is connected between the gate and drain terminals. It can vary the magnitude of the spurious voltage. Fig. 10 shows the turn-ON waveforms of the gate-source voltage, $v_{gs,2}$, drain-source voltage, $v_{ds,2}$, and drain current, $i_{d,2}$, of M_2 with the traditional gate driver. The value of the capacitor ΔC_{gd} includes 0 pF, 10 pF, 20 pF, 30 pF, 40 pF, and 50 pF. Fig. 11 shows the turn-OFF waveforms. The magnitude of the spurious voltage is 1.2 V, 1.5 V, 1.7 V, 2.3 V, 2.9 V, 3.5 V. Thus, when $\Delta C_{gd} = 50$ pF, the OFF-state gate-source voltage is –2 V. With the gate-drain capacitance further increased, undesired shoot through might occur.

Using the proposed gate driver, the spurious voltage is regulated below –1 V, i.e., $V_{\text{REF}} = -1$ V. Figs. 12 and 13 show the corresponding turn-ON and turn-OFF waveforms, respectively. Comparing Fig. 12 with Fig. 10, the gate-source voltage delivered by the proposed gate driver is close to zero near the end of the switching cycle while the one delivered by the traditional gate driver is kept at –5 V. Fig. 13 shows that, depending on the value of ΔC_{gd}, $v_{gs,2}$ varies between –3 and –5.7 V immediately after turning OFF. The peak OFF-state gate voltage caused by the crosstalk is kept at –1 V. It gradually increases until the end of the switching cycle. Hence, this can reduce the average voltage stress on the gate oxide.

Table II compares the measured power losses of M_2 using the proposed gate driver with that using the traditional one. When $\Delta C_{gd} = 50$ pF, the two drivers give the same gate-source voltage under this worst-case condition. The results show that the proposed one gives a lower power loss than the traditional one because of three reasons. First, as discussed above, the effective ON-state gate-source voltage is higher. Second, the ON-state gate-source voltage can dynamically change with C_{gd}. Upon the reduction of C_{gd}, the gate-source voltage is increased. Thus, the power loss reduces as the ON-state resistance reduces. Third,

TABLE II
POWER LOSSES OF M UNDER DIFFERENT ΔC_{gd}

ΔC_{gd} (pF)	$P_{L,act}$ *(W)	$P_{L,deact}$ *(W)	ΔP_L (%)
0	12.1	12.4	3
10	12.6	12.8	1.8
20	12.8	13	1.3
30	13.2	13.3	0.8
40	13.6	13.7	1.2
50	13.9	13.9	0.2

*Note: $P_{L,act}$ - Power loss of M_2 with the proposed dynamic gate-source voltage control activated.
$P_{L,deact}$ - Power loss of M_2 with the traditional gate driver.
ΔP_L - Percent difference, $\Delta P_L = (P_{L,deact} - P_{L,act}) \times 100\% / P_{L,act}$.

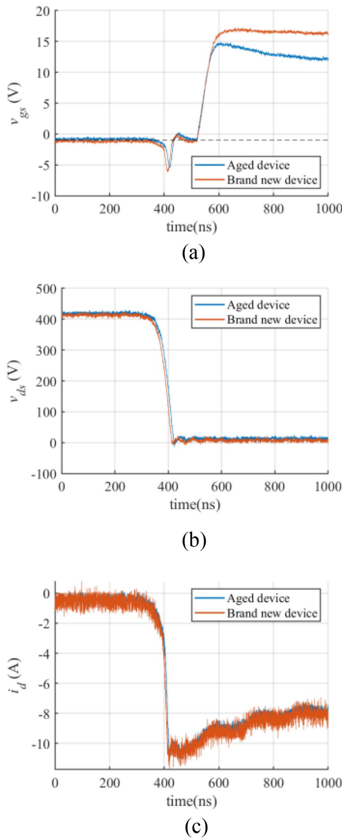


Fig. 14. Turn-ON waveforms of M_2. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

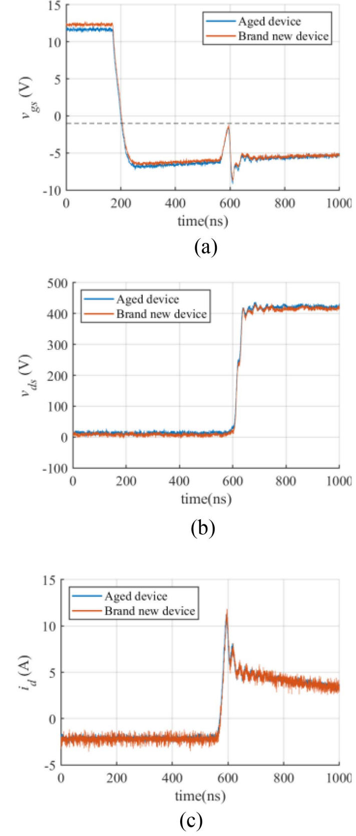


Fig. 15. Turn-OFF waveforms of M_2. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

as the OFF-state gate-source voltage is reduced dynamically, the reverse conduction loss can also be reduced [53].

B. Effect of R_{gss}

To demonstrate the health condition monitoring of the proposed gate driver, an experiment for illustrating the health monitoring function has been conducted. A brand-new device and an aged device are separately applied to the converter prototype. The switching performances are compared. Figs. 14 and 15 show the turn-ON and turn-OFF switching transients, respectively. The steady-state ON-state gate-source voltage with the brand-new device is 12.3 V and that with the aged device is 11.6 V. The value of R_v is 141 kΩ with the brand-new device and 10 kΩ with the aged device, showing that R_v can reflect the health condition.

Fig. 16 shows the turn-ON waveforms with the traditional gate driver, when a resistor ΔR_{gss} is connected between the gate and source. The value of ΔR_{gss} is 10 kΩ, 4.7 kΩ, 1 kΩ, 470 Ω, and 100 Ω. The magnitude of the spurious voltage slightly reduces with reducing ΔR_{gss}. Fig. 17 shows the turn-OFF waveforms. When $\Delta R_{gss} = 100$ Ω, the ON-state gate-source voltage drops to 11 V while the OFF-state gate-source voltage is kept at –5 V. It is mainly due to the loading effect of ΔR_{gss} on the gate driver.

With the proposed gate driver, Figs. 18 and 19 show the corresponding turn-ON and turn-OFF waveforms, respectively. Comparing Fig. 18 with Fig. 16, the gate-source voltage under different ΔR_{gss} is close to zero near the end of the switching cycle with the proposed gate driver. Fig. 18 shows that the proposed gate driver keeps the OFF-state gate-source voltage $v_{gs,2}$ at –3 V immediately after turning OFF the switch with ΔR_{gss} varying between 1 and 10 kΩ, giving rise a lower OFF-state voltage on the gate oxide. The peak OFF-state gate-source voltage caused by the crosstalk is also regulated at –1 V by reducing R_v. With $\Delta R_{gss} = 470$ Ω, the proposed control is unable to perform the regulation and the ON-state gate source voltage drop from 16.7

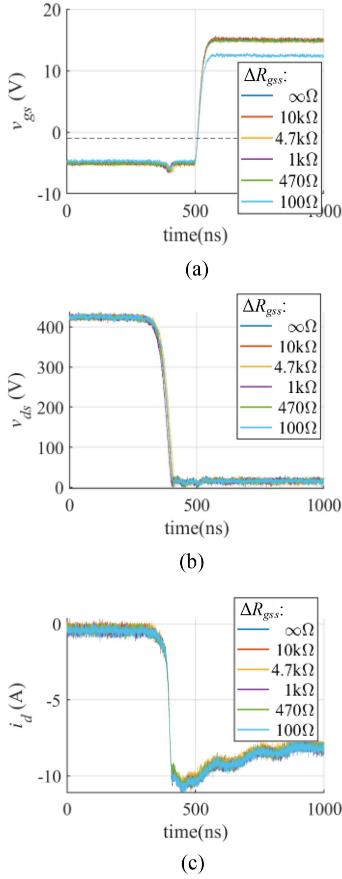


Fig. 16. Turn-ON waveforms of M_2 with the traditional gate driver. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

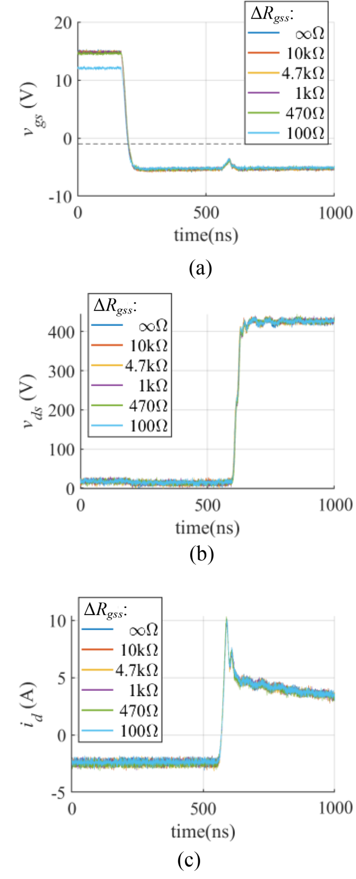


Fig. 17. Turn-OFF waveforms of M_2 with the traditional gate driver. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

TABLE III
POWER LOSSES OF M UNDER DIFFERENT R_{gss}

R_{gss} (Ω)	$P_{L,act}$ *(W)	$P_{L,deact}$ *(W)	ΔP_L (%)
∞	12.1	12.4	3.2
10k	12.1	12.3	1.9
4.7k	12.1	12.3	2.4
1k	11.9	12.7	6.1
470	12.6	12.9	2
100	14.5	15.2	4.7

*Note: $P_{L,act}$ - Power loss of M_2 with the proposed dynamic gate-source voltage control activated.
$P_{L,deact}$ - Power loss of M_2 with the proposed dynamic gate-source voltage control deactivated
ΔP_L - Percent difference, $\Delta P_L = (P_{L,deact} - P_{L,act}) \times 100\% / P_{L,act}$

to 15.8 V is observed. With $\Delta R_{gss} = 100\ \Omega$ (an extreme case), the proposed control fails to perform the regulation. Thus, based on observing the value of R_v, it is possible to monitor the change of R_{gss}.

Table III shows a comparison of the measured power losses of M2 with the proposed gate driver and traditional gate driver,, respectively, when ΔR_{gss} is reduced from ∞ to 100 Ω. The proposed gate driver one gives a lower power loss than the fixed one for three main reasons. First, as discussed above, the effective ON-state gate-source voltage is higher than that with the traditional gate driver. Second, the ON-state gate-source voltage is dynamically changed with spurious voltage. R_v is increased to regulate the gate-source voltage. The ON-state gate-source voltage is higher. Thus, the power loss is lower. Third, as the OFF-state gate-source voltage is reduced dynamically, the reverse conduction loss can also be reduced [53].

C. Effect of C_{gs}

To demonstrate the ability of the proposed circuit to drive a range of C_{gs}, an external capacitor is connected between the gate and source. Figs. 20 and 21 show the turn-ON and turn-OFF waveforms, respectively, with the traditional gate driver, when a capacitor of different values is connected between the gate and source terminals. The value of ΔC_{gs} includes 0 pF, 50 pF, 150 pF, 250 pF, and 350 pF. It has a little effect on the magnitude of the spurious voltage.

With the proposed gate driver, Figs. 22 and 23 show the turn-ON and turn-OFF waveforms, respectively. The spurious voltage is regulated below –1 V. Comparing Fig. 22 with Fig. 20, the profiles of gate-source voltage of the proposed gate driver are close to zero near the end of the switching cycle and higher than 15 V at the beginning of ON state. Comparing Fig. 20 with

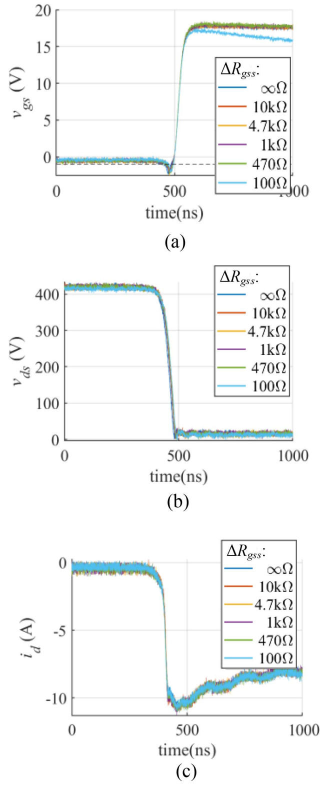


Fig. 18. Turn-ON waveforms of M_2 with the proposed gate driver. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

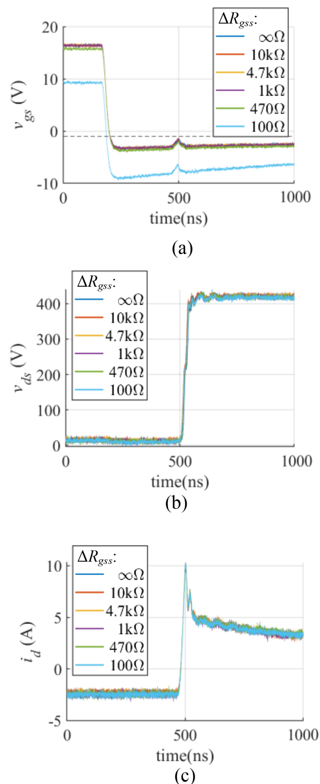


Fig. 19. Turn-OFF waveforms of M_2 with the proposed gate driver. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

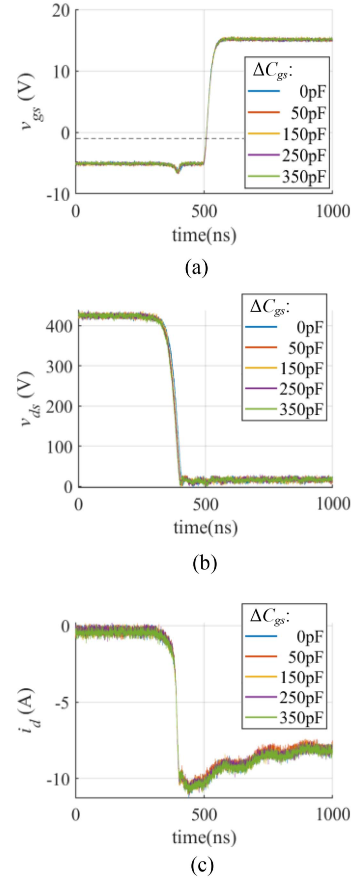


Fig. 20. Turn-ON waveforms of M_2 with the traditional gate driver. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

TABLE IV
POWER LOSS ON THE SWITCH FOR VARIABLE C_{gs}

ΔC_{gs} (pF)	$P_{L,act}$ *(W)	$P_{L,deact}$ *(W)	ΔP_L (%)
0	12.1	12.5	3.3
50	12.2	12.4	2.1
150	12.3	12.7	3.4
250	12.4	12.6	1.4
350	12.5	12.7	1.5

*Note: $P_{L,act}$ - Power loss of M_2 with the proposed dynamic gate-source voltage control activated.

$P_{L,deact}$ - Power loss of M_2 with the proposed dynamic gate-source voltage control deactivated.

ΔP_L - Percent difference, $\Delta P_L = (P_{L,deact} - P_{L,act}) \times 100\% / P_{L,act}$

Fig. 18, the profiles of the gate-source voltage are all similar, irrespective to ΔC_{gs}, showing that ΔC_{gs} has limited loading effect on the proposed circuit.

Table IV shows a comparison of the measured power losses of M2 with the dynamic and fixed OFF-state voltage control. As ΔC_{gs} increases, the turn-ON and turn-OFF times are both increased, resulting in a higher switching loss. As the proposed gate driver does not change the turn-ON and turn-OFF waveforms,

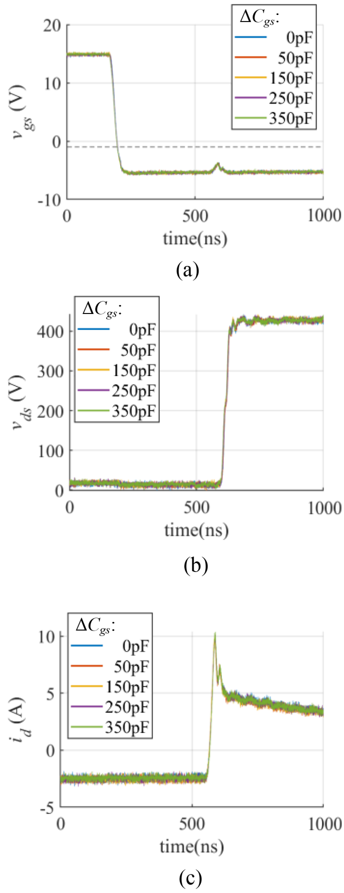


Fig. 21. Turn-OFF waveforms of M_2 with the traditional gate driver. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

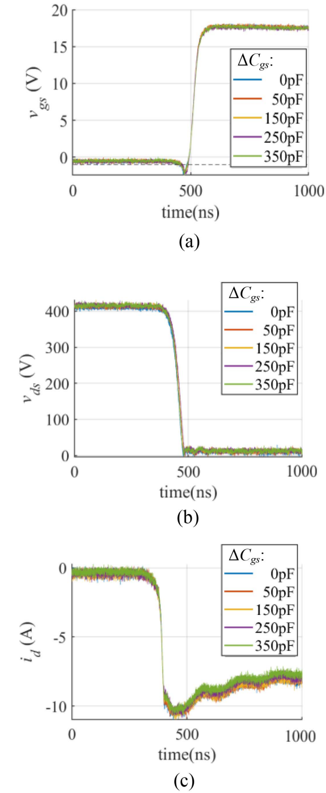


Fig. 22. Turn-ON waveforms of M_2 with the proposed gate driver. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

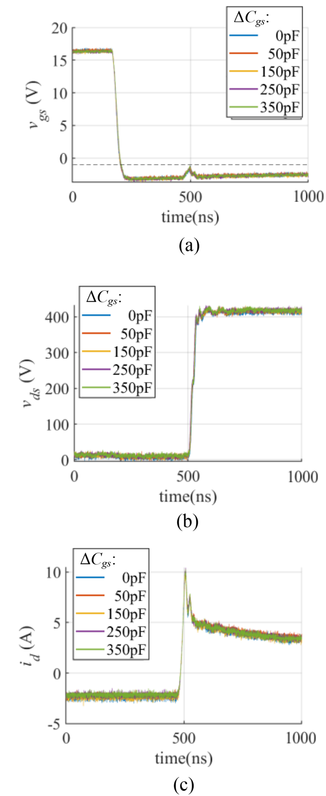


Fig. 23. Turn-OFF waveforms of M_2 with the proposed gate driver. (a) $v_{gs,2}$. (b) $v_{ds,2}$. (c) $i_{d,2}$.

the power losses with the dynamic and fixed OFF-state voltage control are not affected much.

D. Effect of L_s

As discussed in [74], some aging, such as the liftoff of the bond wire will increase the total parasitic inductance of the parallel bond wires. To study the response of the proposed gate driver to the change of the source inductance ΔL_s, a 1.1-nH inductor is added in series with the source of M_2. Figs. 24 and 25 show the waveforms of $v_{gs,2}$ and i_o with the traditional gate driver and the proposed one over one line- cycle, respectively. M_2 is in the synchronous mode in the positive half cycle and is in the control mode in the negative half cycle. Figs. 24(a) and 25(a) show the waveforms with $\Delta L_s = 0$. Figs. 24(b) and 25(b) show the waveforms with $\Delta L_s = 1.1$ nH. When M_2 is in the synchronous mode, the negative envelope of $v_{gs,2}$ increases with i_o because the spurious voltage caused by turning OFF the upper device M_1 increases with i_o. With the traditional gate driver, the ON-state value of $v_{gs,2}$ is fixed at 15 V. With the proposed gate driver, $v_{gs,2}$ is dynamically varied and its instantaneous value upon turning ON increases with i_o. It is because the duty cycle of M_2 reduces with the increase in i_o. C_N has a long time to discharge before the end of a switching cycle.

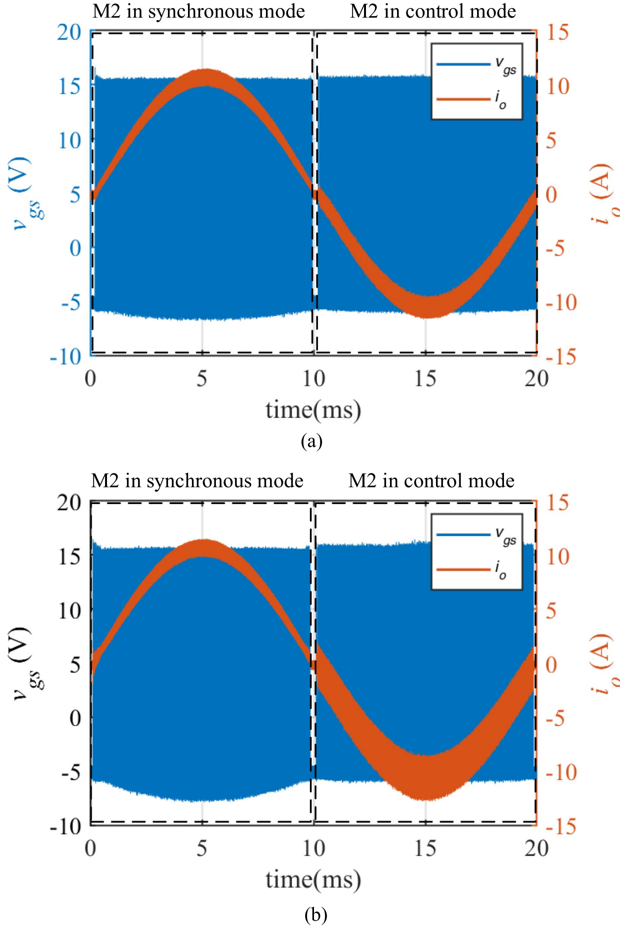


Fig. 24. $v_{gs,2}$ and i_o with the traditional gate driver over one line cycle. (a) $\Delta L_s = 0$. (b) ΔL_s = 1.1 nH.

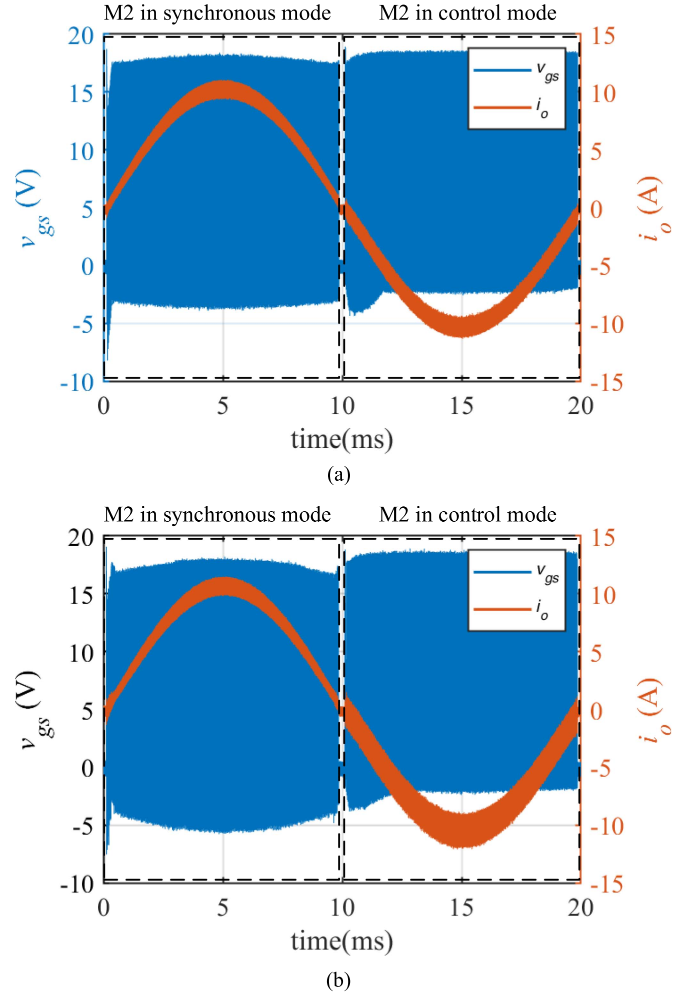


Fig. 25. $v_{gs,2}$ and i_o with the proposed gate driver over one line cycle. (a) $\Delta L_s = 0$. (b) ΔL_s = 1.1 nH.

When M_2 in the control mode, no spurious voltage is induced in $v_{gs,2}$. Thus, $v_{gs,2}$ varies between +15 and –5 V with the traditional gate driver and varies between +18 and –2 V with the proposed gate driver. By comparing Fig. 25(a) with Fig. 25(b), the added inductor will cause $v_{gs,2}$ in the synchronous mode to shift downward because of the increase in the spurious voltage. It has no impact on $v_{gs,2}$ in the control mode.

Fig. 26 shows the detailed waveforms when i_o equals 10 and 2 A. M_2 is in the synchronous mode. With the proposed gate driver, the peak OFF-state value of $v_{gs,2}$ is -1.3 V when i_o = 10 A, and is –1.38 V when i_o = 2 A. When i_o = 10 A, R_v reduces from 225 to 164 Ω when ΔL_s is changed from 0 to 1.1 nH. When i_o = 2 A, R_v reduces from 291Ω to 243 Ω when ΔL_s is changed from 0 to 1.1 nH. With the traditional gate driver, the waveform of $v_{gs,2}$ is almost the same in both cases, except that the amplitude of the spurious voltage increases with i_o.

Fig. 27 shows the detailed waveforms when i_o equals –10 and –2 A, and M_2 is in the control mode. With the traditional gate driver, the OFF-state voltage of $v_{gs,2}$ is –5 V in both cases. With the proposed gate driver, the OFF-state voltage of $v_{gs,2}$ is –1.42 and –1.22 V, which can reduce the stress on the gate of M_2. R_v remains unchanged even if ΔL_s is changed from 0 to 1.1 nH.

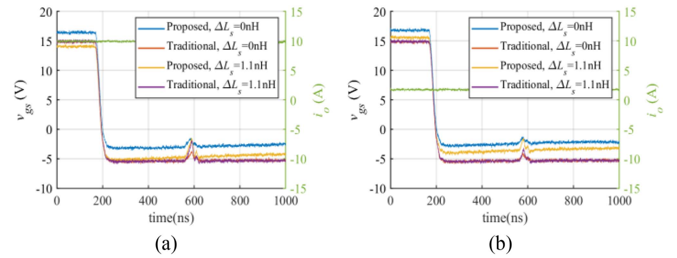


Fig. 26. $v_{gs,2}$ and i_o in the synchronous mode. (a) $i_o \cong$ 10 A. (b) $i_o \cong$ 2 A.

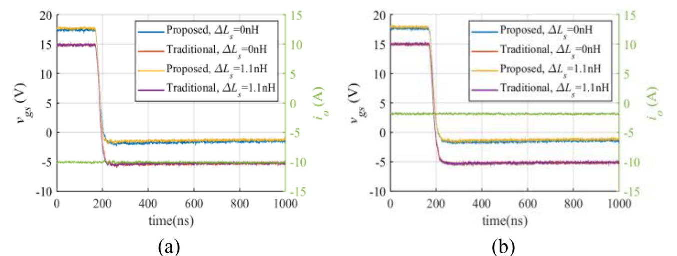


Fig. 27. $v_{gs,2}$ and i_o in the control mode. (a) $i_o \cong$ –10 A. (b) $i_o \cong$ –2 A.

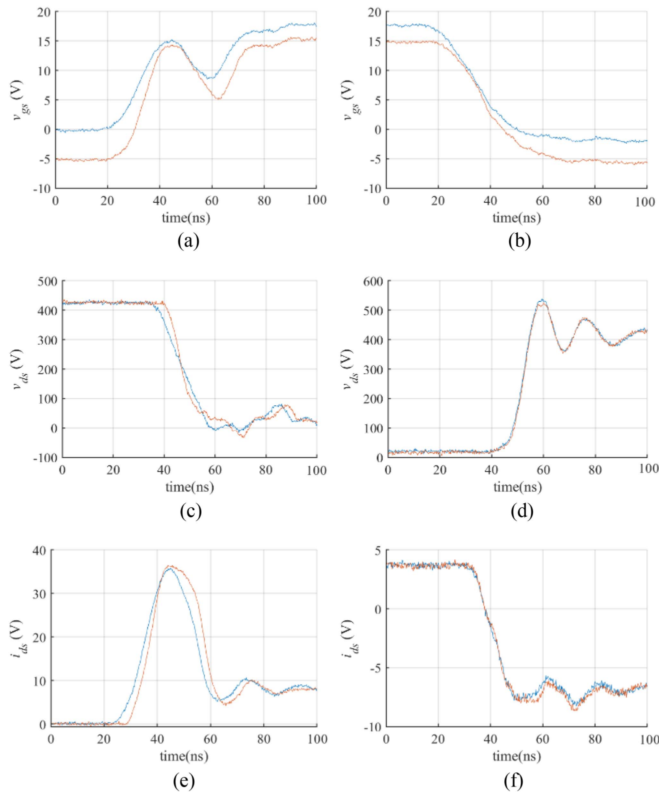


Fig. 28. Switching transients with the proposed gate driver (blue curves) and the traditional gate driver (orange curves). (a) Turn-ON waveforms of $v_{gs,2}$. (b) Turn-OFF waveforms of $v_{gs,2}$. (c) Turn-ON waveforms of $v_{ds,2}$. (d) Turn-OFF waveforms of $v_{ds,2}$. (e) Turn-ON waveforms of $i_{d,2}$. (f) Turn-OFF waveforms of $i_{d,2}$.

The above tests show that the proposed gate driver can still regulate the peak OFF-state gate-source voltage even if the source inductance increases. However, the liftoff of bond wire causes a reduction in R_v, which might counteract the effect of gate-oxide degradation on increasing R_v. The use of R_v to reflect device health can become ambiguous if both aging effects, including gate oxide degradation and bond wire stripping, are present at the same time. Further research will be dedicated to identifying different types of aging with R_v.

The value of C_P is designed to be larger than the gate-source capacitance of the SiC MOSFET, so that the gate-source voltage upon turning ON is determined by the ratio between C_N and C_P. Detailed analysis can be found in [11]. The impact of C_P on the switching transients of the SiC MOSFET, M_2, in the prototype converter has been studied. The results of the proposed gate driver and the traditional gate driver are compared. The results are shown in Fig. 28. It can be observed from the profiles of the drain-source voltage $v_{ds,2}$ and drain current $i_{d,2}$ that C_P has slightly lengthened the turn-ON time, but the change is negligible.

The application range of the proposed gate driver lies in the magnitude of the gate leakage current. The proposed gate driver can maintain the gate-source voltage with the gate leakage current less than 20 mA.

The added level shifter introduces an average power loss around 0.6 W, mainly on the resistors R_P, R_N, and R_v, as well as energy dissipation of C_P and C_N at the switching instants due to the initial inconsistent initial conditions. As reported in Section V, the power loss of the SiC MOSFET is reduced with the proposed gate driver and the reduction ranges between zero and 0.7 W. Then, combined with the power loss of the gate driver, the overall power loss is slightly higher than that of the traditional gate driver, but the difference is negligible. As the SiC MOSFET has a lower power dissipation, its temperature rise is reduced, resulting in lower ON-state resistance and slower degradation.

VI. Conclusion

An adaptive gate driver that can adjust the OFF-state gate-source voltage to counteract the spurious voltage caused by crosstalk effect has been presented. It can also be used to monitor the health condition of the switch directly by observing the change of the voltage level without imposing additional cost on the overall hardware implementation. Apart from resolving the crosstalk issue, an optimal OFF-state gate-source voltage can also improve the life expectancy of the switching device. The proposed technique has been evaluated on a 1-kW inverter. By introducing different values of gate-drain capacitance, gate-source resistance, and gate-source capacitance, the measurement results show that the peak spurious voltage caused by crosstalk is regulated. In addition, the power loss is found to be less than the driver with a fixed OFF-state gate-source voltage. Finally, as reported in [75], one of the main reliability issues of power electronic converters is the reliability of the switching devices. The proposed gate oxide health monitoring feature can track the degradation of switching devices. It also reduces system downtime and reactive maintenance calls, assists with inspection planning, and avoids costly emergency repairs.

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