Letters

A Simultaneous Wireless Power and High-Rate Data Transfer System Based on Transient Responses Regulation

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***Abstract*—In this letter, a simultaneous wireless power and data transfer (SWPDT) method for wireless power transfer systems is proposed. Data and power are transferred via the same coupler. To achieve a high transfer power and a high data transfer rate, double-side *LCC* compensation topology with bandpass filtering is adopted to create a favorable condition for data transfer. An inductor fully compensated at the power carrier frequency and connected serially with the coupled coil is used to inject and extract the data carrier and multiplexed to conduct the power carrier. In addition, the duration time of the transient responses of the data transfer channel is regulated based on the complex frequency-domain analysis. Finally, a 1.1 kW SWPDT experimental prototype with a data transfer rate of 1 Mbps and a data transfer delay of 0.4 μs is built to verify the feasibility of the proposed method.**

***Index Terms*—Data transfer, ON–OFF keying (OOK), simultaneous wireless power and data transfer (SWPDT), wireless power transfer (WPT).**

I. Introduction

RELIABLE communication between the transmitter side and receiver side plays an important role in a wireless power transfer (WPT) system. Compared with the conventional communication technologies, such as Bluetooth, ZigBee, Wi-Fi, and radio frequency, simultaneous wireless power and data transfer (SWPDT) technologies have the advantages of simpler paring, lower transmission delay, and lower cost [1], [2], [3], [4], [5], [6].

According to whether the power transfer coupled coils are shared with data transfer, the methods that have been proposed to transfer power and data simultaneously can be roughly divided into two categories. In the first category, extra coupled coils are added to transfer data [7], [8]. The power and data are transferred in two independent physical channels and can be controlled separately. Therefore, the parameters of the two transfer channels can be designed separately, which greatly simplifies the design of the SWPDT systems. Besides, it has a little impact on power transfer and can achieve a high data rate. Owing to these advantages, it has been applied to practical applications. However, the extra coils increase the coupler size and cost and make it not applicable to applications with limited operating space.

In the second category, power and data are transferred over the same coupler. To realize data transmission sharing the inherent power transfer channel of a WPT system can not only eliminate the data transmission cables or wireless signal transmitters but also has the advantage of flexibility [1]. Two methods are mainly adopted in this category. In the first method, data are directly modulated on power carriers [9], [10]. However, the power transfer of this method may be affected when data are simultaneously transferred, and the data transfer rate is limited by the relatively low-frequency power carrier. To improve the performance of the SWPDT systems, the method using frequency-division multiplexing is proposed. Instead of modulating data on power carriers, high-frequency data carriers whose frequencies are at least one order of magnitude higher than that of power carriers are employed and transferred along with power carriers via the same pair of coupled coils [1], [2], [3], [4], [5], [6]. Compared with the method modulating on power carriers, this method has less impact on power transfer and increases the data transmission rate. However, in the previous works, tapped coils [2] or wave trappers [3], [4] to block the data carrier from being weakened by power compensation networks are utilized, which may introduce a cross-coupling problem or cause relatively high power loss. Besides, methods to improve the data transfer rate have not been analyzed in these research articles.

A high data transfer rate SWPDT system is proposed in this letter, where the high-frequency data carrier is conducted by the power compensation networks and transferred simultaneously with the power carrier via the same coupler. The method proposed has the following features.

1) Double-side *LCC* compensation topology with bandpass filtering characteristic is adopted for power transfer, creating a favorable condition for data transfer.
2) Inductors (i.e., L_{pp}, L_{ss}) multiplexed for power and data transfer are connected in series with the coupled coils

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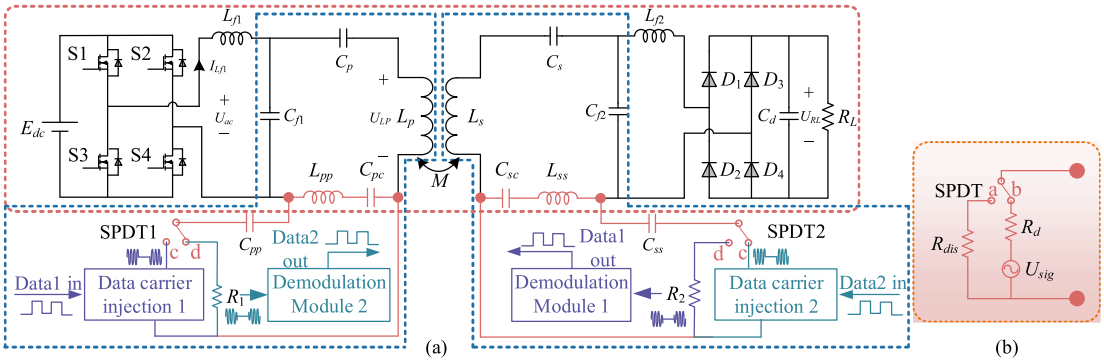


Fig. 1. (a) SWPDT system topology. (b) Data carrier injection circuits.

and fully compensated at power carrier frequency, which makes the power carrier voltage between the two ends of the serial *LC* network (i.e., $L_{pp}C_{pc}$, $L_{ss}C_{sc}$) almost zero, suppressing the interference of power carrier significantly, and is suitable for high-power transfer.

3) To achieve high-rate data transfer, the transient responses of the data transfer channel are analyzed based on the complex frequency-domain model and regulated by two regulating resistors.
4) An effective demodulation method featuring high data rate, interference filtering, and waveform reshaping is proposed.

Finally, an experimental prototype with a power transfer of 1.1 kW and a data transfer rate of 1 Mbps is built to verify the feasibility of the proposed method.

II. System Operation Principles

A. Operation Principles of Power Transfer Channel

For the proposed SWPDT system, as shown in Fig. 1, to achieve a constant-current output of the power transfer channel, the following equations should be satisfied [2]:

$$\begin{cases} 1 = \omega_r^2 L_{pp} C_{pc} = \omega_r^2 L_{ss} C_{sc} \\ 1 = \omega_r^2 \left(L_p - L_{f1}\right) C_p = \omega_r^2 \left(L_s - L_{f2}\right) C_s \\ 1 = \omega_r^2 L_{f1} C_{f1} = \omega_r^2 L_{f2} C_{f2} \\ \omega_r = 2\pi f_r \\ 1 = \omega_1^2 L_{pp} C_{pp} = \omega_1^2 L_{ss} C_{ss} \\ \omega_1 = 2\pi f_1 \end{cases} \tag{1}$$

where f_r and f_1 are the operating frequencies of the full-bridge inverter and the data carrier voltage source, respectively. f_1 is selected much greater than f_r. Therefore, the capacitors of the data transfer channel (i.e., C_{pp} and C_{ss}) show high impedance to the power carrier and can be treated as open circuits to the power carrier. Besides, the serial *LC* networks (i.e., $L_{pp}C_{pc}$ and $L_{ss}C_{sc}$) can be treated as short circuits to the power carrier. The equivalent topology of the power transfer channel is the same as the original *LCC–LCC* compensated topology.

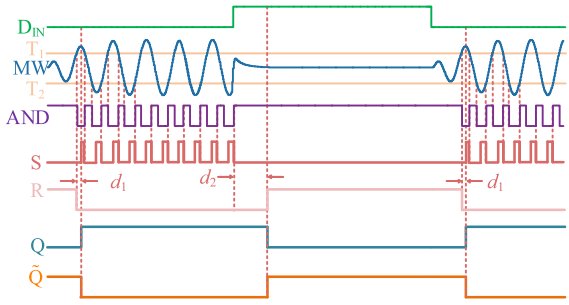


Fig. 2. Process of data demodulation.

B. Operation Principles of Data Transfer Channel

At f_1, the compensation capacitors of the power transfer channel (i.e., $C_{f1}, C_{f2}, C_p, C_s, C_{pc}$, and C_{sc}) can be treated as short circuits and the equivalent topology of the data transfer channel is the same as the original *CLL–LLC* topology.

1) Data Carrier Injection and Modulation: The data carrier injection circuits are shown in Fig. 1(b). R_{dis} is the discharge resistor of the data injection circuits and R_d represents the total resistance of the serial equivalent resistance of the inductor L_{pp}, the ON-resistance of the switch single-pole-double-throw (SPDT), and the extra regulating resistor added. The ON–OFF keying (OOK) is adopted for data modulation. When the data to be transferred are "1" and "0," the switch is connected to *a* and *b*, respectively.

2) Data Carrier Extraction and Demodulation: When the data are transferred, the switch on the transmitting side is connected to *c* and the switch on the receiving side is connected to *d*. Finally, the data are demodulated from the voltage of the sampling resistor. In addition, R_1 and R_2 are also used for the transient waveform shaping of the data transfer channel.

To meet the demand for high-rate data transfer, a demodulation method is proposed in this letter and the demodulation process is shown in Fig. 2. D_{IN} is the data transmitted and MW is the signal received. MW is compared with two thresholds (i.e., *T*1 and *T*2) and AND signal is obtained by AND operation of a field-programmable gate array (FPGA) on the comparison results. Then, the AND signal is further processed by the FPGA

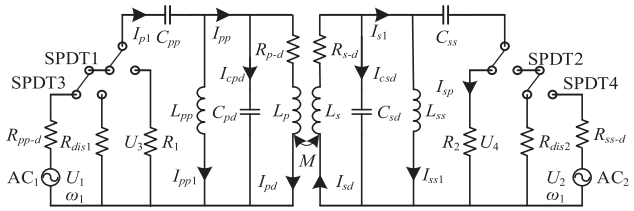


Fig. 3. Data transfer channel with internal resistances and parasitic capacitances.

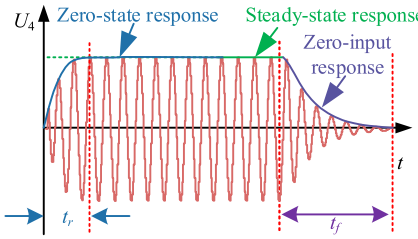


Fig. 4. Curves and approximate envelope of U_4.

module to obtain S and R signals with operations expressed by the following equations:

$$S = \begin{cases} '1' & t_L \geq d_1 \\ '0' & \text{AND} =' 1' \end{cases} \quad R = \begin{cases} '1' & t_H \geq d_2 \\ '0' & \text{AND} = '0' \end{cases} \tag{2}$$

where t_H and t_L are the duration times of the high level and the low level of the AND signal, respectively. S and R signals are the S input and the R input of the SR flip-flop, respectively. Finally, $\tilde{Q}$ is the data demodulated. The comparator is used to preliminarily reshape the received data carrier and filter out the interference to a certain extent. d_1 and d_2 are set to filter the unexpected pulse interference and regulate the pulsewidth.

III. Transient Response of Data Transfer Channel

At data carrier frequency, the internal resistances and parasitic capacitances (i.e., C_{pd} and C_{sd}) of the coupled coils cannot be neglected and the forward data transfer channel is shown in Fig. 3.

As shown in Fig. 4, when the sinusoidal data carrier is modulated by OOK, there is an approximate envelope for U_4, where t_r and t_f are the times when the zero-state response reaches its steady value for the first time and the time when zero-input response reaches zero, respectively. To achieve a high data transfer rate, t_r and t_f should be as short as possible.

To analyze the transient process of the proposed system, the complex frequency-domain analyzing method is utilized. When the state of the system is zero, and based on the complex frequency-domain form of Kirchhoff's voltage and current laws, the Laplace image function of the data transfer channel can be

TABLE I
Main Parameters for Analysis

Symbols	Value	Symbols	Value	Symbols	Value
L_p L_s	30 μH	L_{pp} L_{ss}	5 μH	f_1	4 MHz
C_{pp} C_{ss}	316.6 pF	$R_{pp\text{-}d}$ $R_{ss\text{-}d}$	30 Ω	M	15 μH
R_1 R_2	100 Ω	$R_{p\text{-}d}$ $R_{s\text{-}d}$	15 Ω	C_{pd}	90 pF
U_1(peak)	6 V	U_2(peak)	6 V	C_{sd}	90 pF

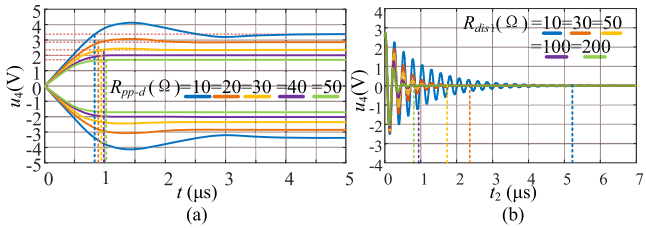


Fig. 5. (a) Zero-state and (b) zero-input responses of the data transfer channel.

deduced

$$\begin{cases} U_4(s) = I_{s1}(s) \cdot \frac{sL_{ss}}{sL_{ss}+1/(sC_{ss})+R_2} \cdot R_2 \\ I_{s1}(s) = I_{sd}(s) \cdot \frac{1/(sC_{sd})}{\frac{(1/(sC_{ss})+R_2)sL_{ss}}{sL_{ss}+1/(sC_{ss})+R_2}+1/(sC_{sd})} \\ I_{sd}(s) = sMI_{pd}(s)/Z_s(s) \\ I_{pd}(s) = I_{pp}(s) \cdot \frac{1/(sC_{pd})}{sL_p+Z_r(s)+R_{p-d}+1/(sC_{pd})} \\ I_{pp}(s) = \frac{U_1(s)}{Z_p(s)} \cdot \frac{sL_{pp}}{\frac{(sL_p+Z_r(s)+R_{p-d})\cdot 1/(sC_{pd})}{sL_p+Z_r(s)+R_{p-d}+1/(sC_{pd})}+sL_{pp}} \\ Z_p(s) = \frac{\frac{(sL_p+Z_r(s)+R_{p-d})sL_{pp}}{sL_p+Z_r(s)+R_{p-d}+sL_{pp}} \cdot \frac{1}{sC_{pd}}}{\frac{(sL_p+Z_r(s)+R_{p-d})sL_{pp}}{sL_p+Z_r(s)+R_{p-d}+sL_{pp}}+\frac{1}{sC_{pd}}} + \frac{1}{sC_{pp}} + R_{pp-d} \\ Z_r(s) = \frac{-s^2M}{Z_s(s)} \\ Z_s(s) = \frac{\frac{(R_2+\frac{1}{sC_{ss}})sL_{ss}}{R_2+\frac{1}{sC_{ss}}+sL_{ss}} \cdot \frac{1}{sC_{sd}}}{\frac{(R_2+\frac{1}{sC_{ss}})sL_{ss}}{R_2+\frac{1}{sC_{ss}}+sL_{ss}}+\frac{1}{sC_{sd}}} + sL_s + R_{s-d}. \end{cases} \tag{3}$$

The time-domain expression of U_4 can be obtained by the inverse Laplace transform of $U_4(s)$

$$u_4(t) = \mathcal{L}^{-1}[U_4(s)]. \tag{4}$$

When R_{pp-d} varies, $u_4(t)$ is calculated with (4) and the parameters listed in Table I, and the results are shown in Fig. 5(a). To make the figures tight, only the envelopes of the waveforms are drawn. It can be seen from Fig. 5(a) that the steady-state gain and the transient responses of the data transfer channel can be improved by adjusting R_{pp-d} reasonably.

For zero-input response, when the input is connected to R_{dis1}, the complex frequency-domain model of the forward data transfer channel is shown in Fig. 6. Based on Fig. 3, the initial values of the electrical parameters at time t can be calculated by applying input $\dot{U}_1 = Ae^{j\omega_1 t}$ and taking the imaginary parts of the results, where A is the amplitude of $\dot{U}_1$. Based on Fig. 6, the Laplace image function of the data transfer channel can also be obtained. With the parameters, as listed in Table I, taking the values of the electric parameters at $t_1 = 1\text{e}^{-5}$ s (when the input voltage reaches zero) as the initial values and when R_{dis1} varies,

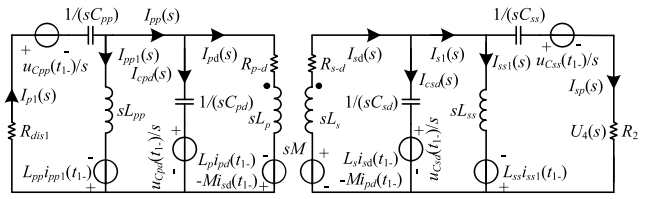


Fig. 6. Complex frequency-domain model of the data transfer channel.

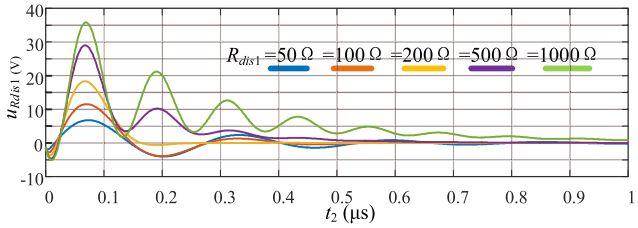


Fig. 7. Time-domain curves of the voltage of different R_{dis1}.

TABLE II
MAIN PARAMETERS FOR EXPERIMENTAL VERIFICATION

Symbols	Value	Symbols	Value	Symbols	Value
E_{dc}	140 V	M	18 μH	L_p L_s	30 μH
L_{f1} L_{f2}	20 μH	C_{f1} C_{f2}	175.3 nF	C_p C_s	350.6 nF
L_{pp} L_{ss}	5 μH	C_{pc} C_{sc}	701.2 nF	f_r	85 kHz
C_{pp} C_{ss}	316.6 pF	$R_{pp\text{-}d}$ $R_{ss\text{-}d}$	15 Ω	f_1	4.2 MHz
R_L	16 Ω	R_{dis1} R_{dis2}	100 Ω	R_1 R_2	100 Ω
U_2(peak)	6 V	U_1(peak)	6 V	C_{pd} C_{sd}	90 pF

the zero-input responses $u_4(t_2)$ are shown in Fig. 5(b). It can be seen from Fig. 5(b) that t_f decreases with the increase of the discharging resistor R_{dis1}.

However, the value of R_{dis1} cannot be infinitely increased. With the same method, $u_{R\mathrm{dis1}}(t_2)$ can also be calculated. When R_{dis1} varies, the time-domain curves of the voltages of R_{dis1} are shown in Fig. 7. It can be seen from Fig. 7 that the peak value of the voltage of R_{dis1} increases sharply as R_{dis1} increases, which may break down the electronic components of the data transfer channel.

With the same method, the responses of the data transfer channel under other parameters (i.e., R_1, R_2, L_{pp}, L_{ss}, $R_{p\text{-}d}$, $R_{s\text{-}d}$, M, L_p, L_s, and f_1) can also be calculated.

IV. EXPERIMENTAL VERIFICATION

By analyzing the responses, the parameters, as shown in Table II, are adopted for experimental verification. An experimental prototype, as shown in Fig. 8, is built based on Fig. 1 to verify the feasibility of the proposed method. An amplifier (THS6002) is used to amplify the data carrier and drive the coupled coils, an analog switch (TMUX6219) is used to modulate the data carrier according to the data transmitted, and an FPGA module (EPM240T100C5N) is used to demodulate the signal received.

When power and data are transferred simultaneously, the waveforms of the power and data transfer channel are shown

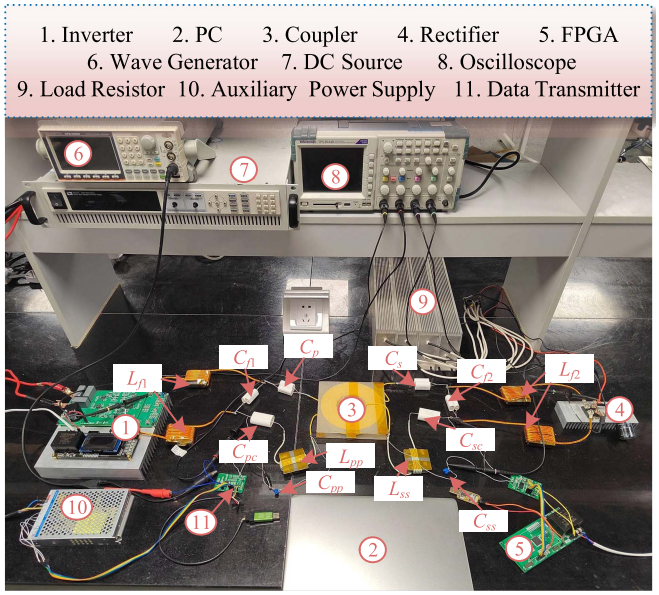


Fig. 8. Schematic diagram of the experimental prototype.

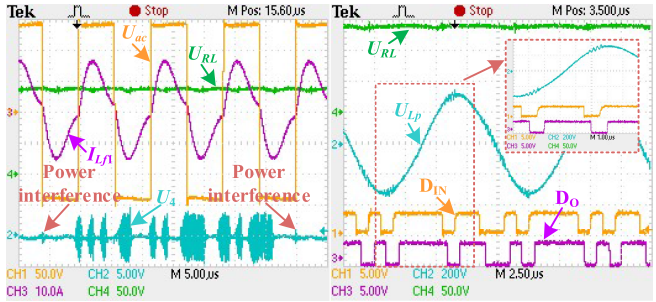


Fig. 9. Waveforms of the power transfer channel and data transfer channel.

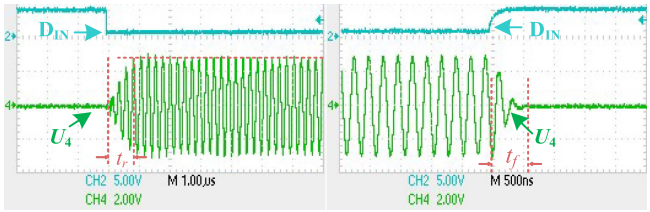
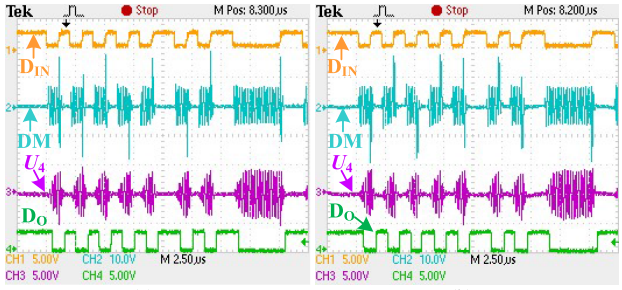


Fig. 10. Transient responses of the data transfer channel.

in Fig. 9, where D_{IN} is the data transmitted, D_O is the data demodulated, and U_{RL} is the voltage of the load. The measured U_{RL} is 133 V and when the load is 16 Ω, the output power is 1105 W. The input power is 1198 W and the efficiency is about 92.2%.

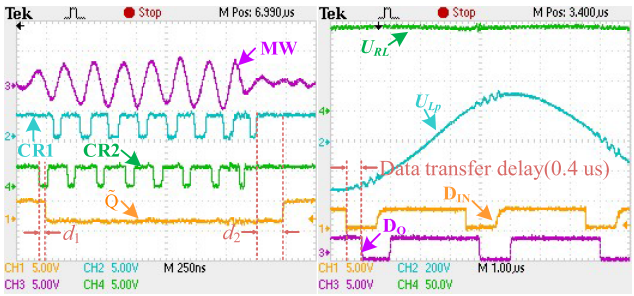
Fig. 10 shows the transient responses of the data transfer channel; it can be seen from Fig. 10 that t_r and t_f are less than 1 μs, which is consistent with the theoretical analysis, as shown in Fig. 5.

Fig. 11 shows the waveforms of the data transfer channel with and without power transfer, where DM is the data modulated. It can be inferred from the waveform of DM that when the analog



(a) (b)

Fig. 11. Waveforms of data transfer channel (a) without and (b) with simultaneous power transfer.



(a) (b)

Fig. 12. Waveforms of (a) data demodulation and (b) power transfer channel and data transfer channel.

TABLE III
PERFORMANCE COMPARISON

Reference	Power	Data rate	Efficiency
proposed	1.1 kW	1 Mbps	92.2%
[1]	354 W	19.2 kbps	52%
[2]	300 W	500 kbps	90.1%
[3]	500 W	600 kbps	84%
[4]	600 W	80 kbps	86.8%
[5]	500 W	20 kbps	86%
[6]	3.3 kW	64 kbps	N/A

switch is connected to a, spike voltage is generated on DM, which is consistent with the theoretical analysis. Comparing Fig. 11(a) with (b), it can be inferred that power transfer has little influence on data transfer.

The waveforms of the data demodulation process are shown in Fig. 12(a), where MW is the signal received, CR1 and CR2 are the comparison results, and $\tilde{Q}$ is the output of the SR flip-flop. It can be inferred from Fig. 12(b) that a high-frequency data carrier wave appears on the waveform of the voltage of the primary coil, which indicates that power and data are transferred simultaneously. In addition, it can also be inferred from Fig. 12(b) that the data transfer rate is 1 Mbps and the transfer delay is about 0.4 μs.

Table III summarizes the performance of the proposed system and the previous research articles. Compared with the previous research articles, with the method proposed, a data transfer of Mbps level is achieved along with a power transfer of kW level.

V. CONCLUSION

In this letter, an SWPDT system with a high data rate is proposed and the feasibility of this method is verified by experiment. The power and data are transmitted simultaneously via the same coupled coils. Inductors fully compensated at power carrier frequency are multiplexed for data carrier injection and extraction, creating a favorable condition for data transfer. To achieve a high data rate, the transient responses of the data transfer channel are analyzed based on the complex frequency-domain model and resistors are added to regulate the transient responses. Besides, an effective demodulation method is also proposed. With the method proposed in this letter, a 1.1 kW SWPDT prototype with 1 Mbps data transfer is achieved.

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