A Region-Folding Electromagnetic Transient Simulation Approach for Large-Scale Power Electronics System

Cheng Jin, *Student Member, IEEE*, Zhendong Ji, *Member, IEEE*, Kangli Liu, *Member, IEEE*, Wenzhe Chen, *Student Member, IEEE*, and Jianfeng Zhao

***Abstract*—This article proposes a region-folding electromagnetic transient simulation approach for large-scale power electronics systems to boost simulation speed. In the region-folding approach, the loop tear method is proposed to decouple the connections among power electronics blocks, the grouping and pre-calculating method of identical structural blocks is proposed to avoid computing the inverse of matrices repeatedly, and the global simultaneous response procedure is proposed to handle the simultaneous and multiple switching events. The implementation of the proposed approach is combined with high-performance parallelization technology to shorten the simulation time. The modular multilevel converter based high voltage direct current model and dc photovoltaic power station model are simulated respectively to validate the accuracy and efficiency. Simulation results indicate that the proposed approach has the same accuracy as other electromagnetic transients commercial software with better efficiency.**

***Index Terms*—Electromagnetic transients program (EMTP), loop tear method, modified nodal analysis (MNA), multiarea Thévenin equivalent (MATE), parallel computing, power electronics, region-folding, simulation.**

I. Introduction

LARGE-SCALE power electronics converters are being employed in the power system to meet the rising demand for clean energy generation and high voltage direct current (HVdc) power transmission. However, the complex interconnection among the power electronics converters and transmission networks leads to a decrease in safety margin and an increase in unpredictability. Hence, the power electronics simulation tool plays an essential role in designing and verifying the coordination and stability of power electronics control strategies.

However, the increasing number of power electronics switches, such as high-voltage silicon rectifier stack, GTO, IGBT, etc., and higher switching frequency challenge the efficiency and accuracy of the present simulation tools. Due to the fast nonlinear switching process and high-dimensional system matrix, the large-scale power electronics system is slow to simulate. Thus, based on the structural homogeneity of power electronics blocks, this article proposes the loop tear decoupling method to split the high-dimensional matrix into smaller pieces and calculate them in parallel to accelerate the electromagnetic transient simulation process.

Much work and studies have been done in large-scale power electronics simulation to identify the necessity and importance [1]. The discrete state event-driven approach is proposed to improve the simulation efficiency [2], [3], [4], achieving 1000-fold acceleration. The ideal transformer decoupling method is adopted to realize efficient parallelization [5], [6]. The HVdc power transmission widely takes MMC equivalent models to reduce matrix dimensions [7], [8], [9], [10]. Besides, the coarse and fine simulation step control algorithm is also a research direction, achieving progress in multitime scale electromagnetic transient parallel computation [11], [12].

According to the above research, system partition is inevitable in large-scale power electronics systems, coping with the dimensions, computational burden, etc. The state-variable-interfaced decoupling strategy partitions the large-scale circuit into smaller subsystems with state variables as interfaces so that the numerical integration can be performed in a decoupled manner [2]. The ideal transformer decoupling method, represented by a pair of controlled voltage and current sources, exchanges the controlled voltage and current value and divides the system into smaller subsystems [5], [6]. The multiarea Thévenin equivalent algorithm (MATE) decoupling method, including the multilevel simulation method [13], [14], the branch tear method [13], [14], [15], [16], [17], the node splitting method [18], and the multirate simultaneous solution [19], subdivides the system into

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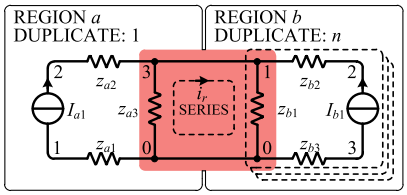


Fig. 1. Loop tear method applied to power electronics blocks in series.

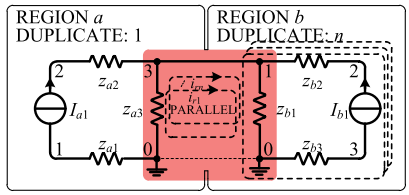


Fig. 2. Loop tear method applied to power electronics blocks in parallel.

kindred subnetworks. The propagation delay decoupling method is usually adopted in long-distance networks [20], [21]. Some researchers also developed the matrix-level partitioning method by regrouping the large system matrix into the bordered block diagonal form [22], [23], [24].

However, most partition schemes are raised initially to settle the traditional ac power grid, leading to low efficiency in handling the power electronics systems. Specifically, whether the branch tear method or the node splitting method of the MATE is offered to solve parallel power grids in different areas, it is reasonable since under no circumstances can the grids be connected in series. Nevertheless, the series connection, such as MMC and input series output parallel, is a typical structure to bear high-voltage stress in power electronics. Thus, based on the MATE, the loop tear method is proposed to overcome such defects. This method can accommodate parallel partitions, series partitions, and a combination of both. With the help of the proposed loop tear decoupling method, the power electronics blocks with identical structures can be grouped as a region, and the blocks in a region share the same set of precalculated admittance and impedance matrices, which avoids a lot of matrix computation time. Besides, the simulation of large-scale power electronics devices is characteristic of repetitive power electronics blocks. This article turns such repetitive structure into batched homogeneous calls in Basic Linear Algebra Subprograms (BLAS) library, boosting simulation efficiency. Moreover, the global simultaneous response procedure (GSRP) is proposed to handle switching events accurately and timely.

This article contributes to the loop tear method, the region group method, and the GSRP to implement the electromagnetic transient simulation for large-scale power electronics systems in a multiple-core high-performance computer. Case analysis indicates that the proposed simulation approach achieves a 765-fold acceleration compared with state-space-based EMT commercial software and achieves a 20-fold acceleration compared with MNA-based EMT commercial software, with the same accuracy.

II. Region-Folding Approach

In the published literature, several methods are proposed to divide large power systems into smaller ones. Among these algorithms, the MATE has the advantages of no calculation error, no time delay, no structure-specific, and precise physical mechanisms. Thus we choose it as the partitioning scheme. However, almost all the published research concerning the MATE, including the branch tear method and node splitting method, is built for the traditional power grid, [13], [14], [15], [16], [17], [18], [19], [20]. Hence, the loop tear method is proposed based on the MATE mechanism to accommodate power electronics blocks in series. According to structural repetition, the decoupled power electronics blocks with identical structures, linked by the loop current, share the same precalculated admittance and impedance matrices. The loop tear method and the shared matrices together comprise the region-folding approach.

A. Loop Tear Method

To simulate the power electronics system, we need to describe the circuit in the form of mathematics quantitatively

$$A_m X_m = H_m - I_m. \tag{1}$$

Usually, the MATE is represented in nodal equations, so the circuit following is modeled in MNA [28], [29], yields (1). m is the unique block number, A_m is the hybrid admittance matrix, X_m is the hybrid nodal voltage vector, H_m is the hybrid current source vector, and I_m is the injection current vector from the system loop currents. The injection current vector I_m is introduced to represent the coupling relationship with the global system.

To demonstrate the loop tear concept, let us consider the simplified series interconnection of the power electronics blocks in Fig. 1 and parallel in Fig. 2. They are the structures that most power electronics converters employ. We consider the blocks with the same structure and parameters as a region.

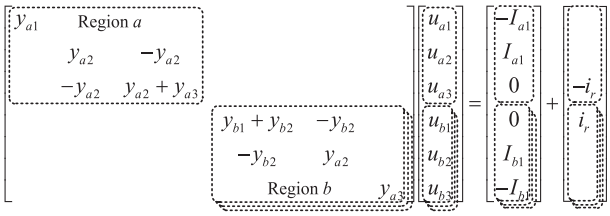
Fig. 1. shows the series connection of power electronics blocks. Regions a and b are structurally different power electronics blocks, and region b consists of a series of blocks head to tail. Voltage $u_{a1\text{-}3}$ and $u_{b1\text{-}3}$ are referenced to respective node 0 inside the partition. Regions a and b are coupled by loop current i_r

$$\begin{bmatrix} y_{a1} & 0 & 0 \\ 0 & y_{a2} & -y_{a2} \\ 0 & -y_{a2} & y_{a2}+y_{a3} \end{bmatrix} \begin{bmatrix} u_{a1} \\ u_{a2} \\ u_{a3} \end{bmatrix} = \begin{bmatrix} -I_{a1} \\ I_{a1} \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ -i_r \end{bmatrix}. \tag{2}$$

Region a can be modeled by MNA in (2). y_{ai} is the branch admittance of z_{ai} and u_{ai} is the node voltage $(i = 1, 2, 3)$

$$\begin{bmatrix} y_{b1}+y_{b2} & -y_{b2} & 0 \\ -y_{b2} & y_{a2} & 0 \\ 0 & 0 & y_{a3} \end{bmatrix} \begin{bmatrix} u_{b1} \\ u_{b2} \\ u_{b3} \end{bmatrix} = \begin{bmatrix} 0 \\ I_{b1} \\ -I_{b1} \end{bmatrix} + \begin{bmatrix} i_r \\ 0 \\ 0 \end{bmatrix}. \tag{3}$$

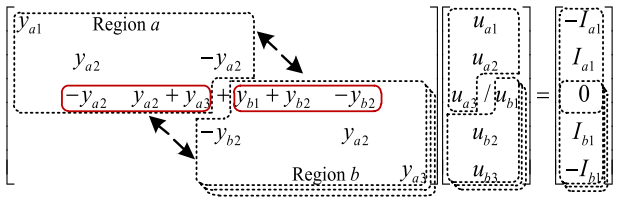
MNA can model all blocks in region b with the same (3). y_{bi} is the branch admittance of z_{bi} and u_{bi} is the node voltage ($i = 1, 2, 3$).



(4)

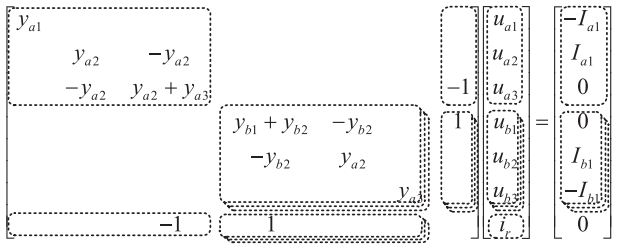
As i_r is the interface variable in both (2) and (3), they are put into the same MNA matrix to solve the circuit in Fig. 1.

The loop tear method treats the interaction with neighbor partitions as the loop current. Compared to the original nodal analysis (5), the off-diagonal conductance elements, linking nodes to other blocks, are represented by the loop current i_r. Specifically, if the boundary u_{a3}/u_{b1} is considered in the region a, the sum of $(y_{b1} + y_{b2})u_{b1}$ and $-y_{b2}u_{b2}$ equals i_r. So is it in region b



(5)

It can be seen in (4) and (5) that boundary u_{a3}/u_{b1} is the same node accounted for twice in neighbored blocks, and an extra variable i_r is introduced into the MNA matrix. In other words, the combination matrix (4) is rank-deficient, which cannot get the numerical solution. The augmented equations describing the branch voltage, branch current, and branch impedance are supplemented in the branch tear method. The augmented equations describing the same voltage of boundary pair nodes are supplemented in the node-splitting method



(6)

While in the proposed loop tear method, the voltage sum 0 of all the elements cycling around, based on Kirchhoff's Voltage Law (KVL), is supplemented, as presented in the last line in (6).

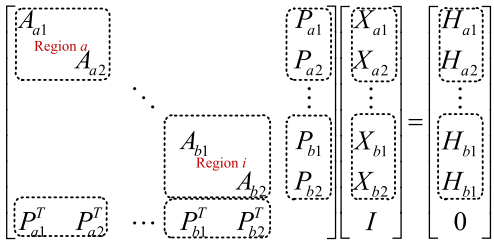
We define the matrices demonstrating the relationship between the loop voltage and current as incidence matrices P_m. P_m is an $n \times r$ matrix, n is the size of the hybrid vector X_m in block m, and r is the size of all loop currents in the global power electronics system. $P_m(i, j)$ yields to

$$P_m(i,j) = \begin{cases} 1 & \text{if loop current } j \text{ into block node } i \\ -1 & \text{if loop current } j \text{ from block node } i \\ 0 & \text{if loop current } j \text{ and block node } i \text{ are unrelated} \end{cases}. \tag{7}$$

The above analysis is raised based on 1:n between region a and region b, and it is also applicable to the quantitative relationships of 1:1 and n:n.

Fig. 2 illustrates the parallel power electronics blocks. Regions a and b are structurally different power electronics blocks, and node 3 in region a and all nodes 1 in region b are connected. It is a typical topology researched in almost all papers concerning MATE. Further, we view it from the perspective of loop current to get a consistent simulation process following the loop tear method. The parallel nodes and the reference ground make up the cycles, considered virtual loops. Each parallel power electronics block has its loop current. The rest modeling process follows (2)–(6).

After tearing the large-scale power electronics system into smaller subsystems, the power electronics system can be described in the bordered block diagonal form in (8). $H_{a1\text{-}2}$ and $H_{b1\text{-}2}$ are the hybrid vectors of current and voltage sources. I is an $r \times 1$ vector that contains all loop currents in the system



(8)

Several handling methods can be used to calculate the hybrid vectors X_m. Some works [22], [23] solve the system by LU decomposition to improve solution efficiency. At the same time, some works, [17], take a two-step method to solve it. The global loop current is calculated and substituted into each small system solving X_m. Considering several hundreds of blocks in large-scale power electronics systems, the LU decomposition of bordered block diagonal form for (8) is still time-consuming. So the latter method is adopted in this article

$$\begin{cases} A_m X_m + P_m I = H_m \\ \sum P_m^T X_m = 0 \end{cases}. \tag{9}$$

Equation (8) is rewritten in (9). According to the nodal analysis, the hybrid voltage X_m in the subsystem can be expressed as

$$X_m = A_m^{-1} H_m - A_m^{-1} P_m I. \tag{10}$$

Substituting (10) in the second equation of (9), Z_m is the block impedance matrix, the inverse of A_m, $Z_m = A\text{-}1\ m$. The stacked voltages around loops $\Sigma PT\ mX_m = 0$. And the global

loop current I can be expressed

$$\sum P_m^T Z_m H_m = \left(\sum P_m^T Z_m P_m\right) \times I. \tag{11}$$

Equation (11) is further simplified as (12) and calculated as (13)

$$\begin{cases} E_{\text{loop}} = P_m^T Z_m H_m \\ Z_{\text{loop}} = P_m^T Z_m P_m \end{cases} \tag{12}$$

$$I = \left(\sum Z_{\text{loop}}\right)^{-1} \sum E_{\text{loop}}. \tag{13}$$

Equation (12) and (13) are precisely the loop current analysis, in which the unknown I are loop currents, ΣE_m are the total voltages, and ΣZ_m are the total impedances across all related blocks in loops. After obtaining the loop currents, take them into (10), and solve node voltages in blocks by MNA.

Compared with other methods of solving (8), the adopted method does not need to store or manipulate the whole matrix of all partitions. Equation (8) is presented conceptually just as a matter of analysis method. The actual solving process goes following (12), (13), and (10), with the benefits of scalability and parallelization.

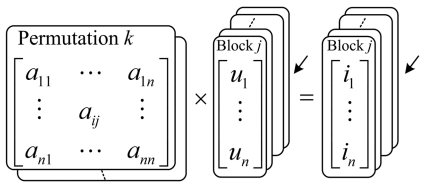
The loop current tear method implements the Diakoptics [30], [31]. It solves the extensive system by tearing and turning the interconnections into loop currents. It is much more efficient to solve smaller subsystems. Besides all, (12), (13), and (10) are highly parallelized. So the solving process can be accelerated by high-performance multiple-core computers or clusters.

B. Region Group Method

In the above section, the extensive system has been modeled as the loop current tear model (9), and subsystems with different kinds of connections can be calculated separately. However, the maddening situation, slowing electromagnetic transient simulation speed, is that the impedance matrix Z_m and admittance impedance A_m change with the switch states of the power electronics devices in the subsystem. Some software precalculates all switch-state permutations to boost the simulation process. However, in the simplest case of a two-valued resistor imitating a switch device, n switches produce 2^n switch-state permutations, leading to the difficulties of enumerating all combinations. It is forced to calculate the inverse of the matrices during each simulation step, which slows the simulation speed.

The unique feature of the proposed decoupling method is that the power electronics blocks with an identical structure produce precisely the same impedance and admittance matrices as the series blocks in (6). The boundary node is split into the neighbor blocks, and each block can form its diagonal block matrix without admittance interference, as in (5), from neighbors. In other words, not the whole system, but the minimum repetition structure needs to enumerate impedance and admittance matrices. Specifically, in an MMC arm, all submodules share the same set of four pairs of precalculated impedance and admittance matrices. In the calculating following process (12), (13), (10), the solver only needs to pick the submodule's precalculated impedance and admittance according to its switch state. In this article, the minimum repetition structure is called the block, and the identical power electronics blocks are grouped into the same region. The repeated number is the *duplicate* attribute of the region.

The impedance and admittance sharing mechanism is described in (14). All the impedance and admittance matrices of the region are precalculated based on switch-state permutations before the simulation starts, assigned with switch-state permutation numbers, and each block calculates the permutation number k to pick the impedance/admittance pair out of the matrices to calculate E_{loop}, Z_{loop}, and X_m in the simulation process



(14)

The switch device and other nonlinear elements, such as saturable inductors, can be assembled by combining linear elements and switches, [32]. So the proposed linear precalculated method can also get accurate simulation results with nonlinear devices.

Since the impedance and admittance are associated with discrete step size in electromagnetic transient simulation, the fix-step simulation is more efficient than the variable-step simulation due to keeping constant impedance and admittance matrices. So the fix-step solver is preferable in the proposed region-folding approach.

III. Global Simultaneous Response Procedure

The simultaneous switching, multiple switching events, and numerical oscillations [33], [34] are peculiar problems in power electronics systems different from traditional power systems, bothering the accuracy and efficiency. In most proposed handling methods [35], problems are coped with interpolation, extrapolation, and critical damping adjustment [36].

However, compared to traditional small-scale simulations, things are almost totally different in an extensive power electronics system. If the power electronics system is large enough, hundreds of simultaneous and multiple switching events occur in a simulation step in different regions with coupling. The global solver will tire of coping events and degenerate into the series computation. Furthermore, interpolation and extrapolation change the simulation step, leading to the precalculation failure of impedance/admittance matrices.

The GSRP is then proposed based on the simultaneous response procedure [37] to solve the above problems. The GSRP consists of two stages 1) forward switching detection and 2) backward switching propagation.

Fig. 3 illustrates the switching event process. In Fig. 3(a), IGBT1 is turned off by the control signal, and the simultaneous switching is hard to predict since the coupling relationships across several partitions are complex. So we calculate all the node voltages, detect switching events in parallel and find that D1 and D2 are forced to open at t_2. Then in Fig. 3(b), all the affected devices, D1 and D2, are turned on, and the simulation step goes back to t_1 from t_2. IGBT1, D1, and D2 change switch

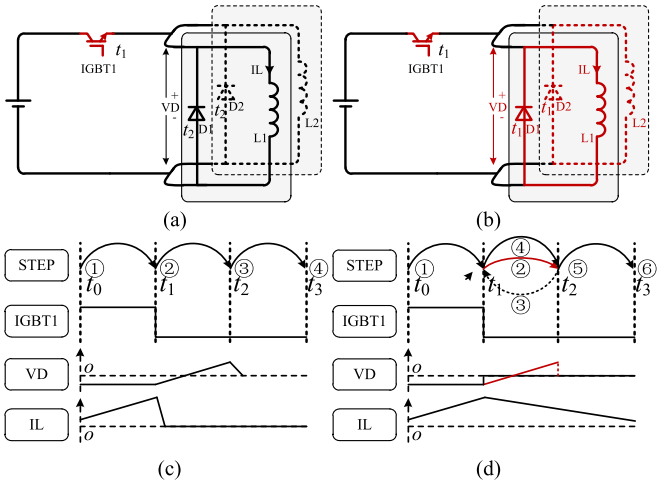


Fig. 3. GSRP. (a) Forward switching detection. (b) Backward switching propagation. (c) Switching events without handling. (d) Switching events with GSRP.

states simultaneously at t_1, solving simultaneous and multiple switching problems. The GSRP ignores the switching order and aligns them to the previous step. In electromagnetic transients (EMT), such an error is too minute to affect accuracy. Since all the nonstate variables are recalculated at ④ in Fig. 3(d) after solving simultaneous switching dependencies, no numerical oscillations should occur.

If the simultaneous switching is not dealt with properly, as in Fig. 3(c), the inductor current IL of L1 and L2 will go to zero and fail to open diodes D1 and D2 at t_2, leading to the simulation failure. The detailed algorithm steps are the following.

Step 1: Change the active switch device's state according to the control signal.
Step 2: Calculate the node voltages by (12), (13), and (10). Store the voltage of every device.
Step 3: Detect switching events in all regions. If no switching event occurs, go to the next simulation step. Otherwise, go to Step 4.
Step 4: Change the passive switch device's switch state according to the detection result from Step 3.
Step 5: Recalculate the loop-current voltage and loop-current impedance affected by switching events and calculate the difference values between step 5 and Step 2.
Step 6: Add the difference value of the loop-current voltage and impedance from affected switching event blocks to the original global loop-current voltage $\Sigma P_m^T Z_m H_m$ and the global loop-current impedance $\Sigma P_m^T Z_m P_m$.
Step 7: Recalculate global loop currents according to (13).
Step 8: Recalculate node voltages according to (10).
Step 9: Advance simulation time.

The switching event detecting and handling algorithms are necessities for the power electronics simulation approach and are closely related to the simulation mechanism. The GSRP calculates the variables in the changed partition, not the whole system, to boost simulation efficiency. The GSRP is a fixed-step switching event dealing method that fully uses the precalculated

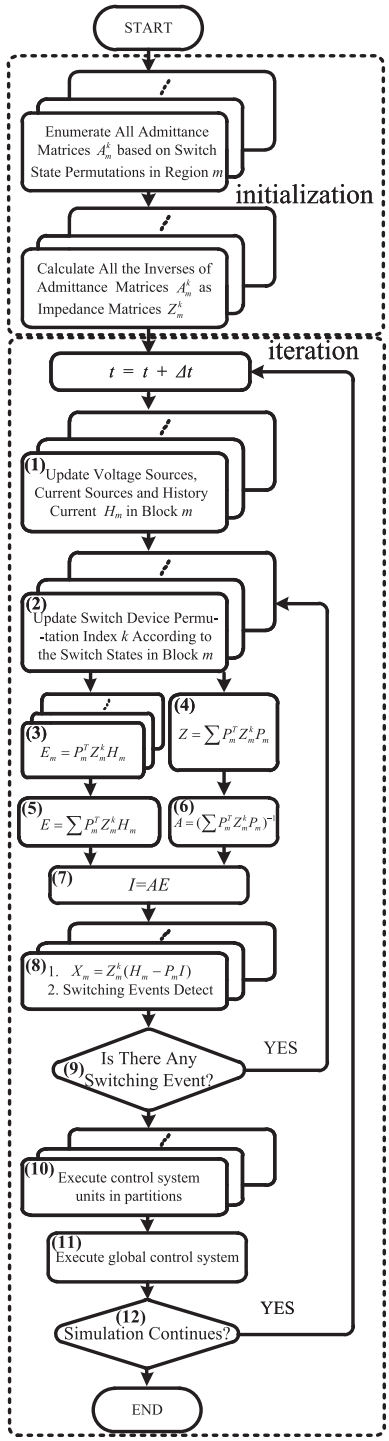


Fig. 4. Flowchart of the proposed simulation approach.

impedance/admittance matrices in parallel instead of interpolation and extrapolation, accelerating the simulation speed.

IV. Implementation Method

The implementation of the proposed electromagnetic transient simulation approach is depicted in Fig. 4.

Fig. 4 consists of the initialization stage and the iteration stage. In the initialization stage, the simulation program parses

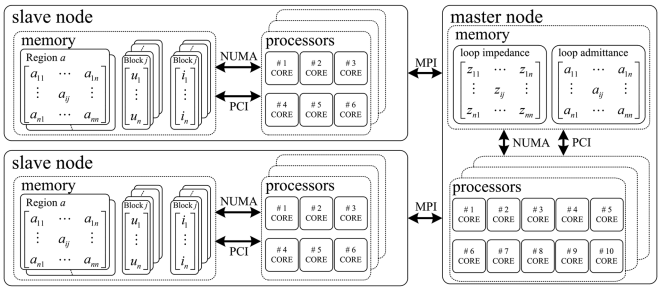


Fig. 5. Distributed memory implementation for proposed simulation approach.

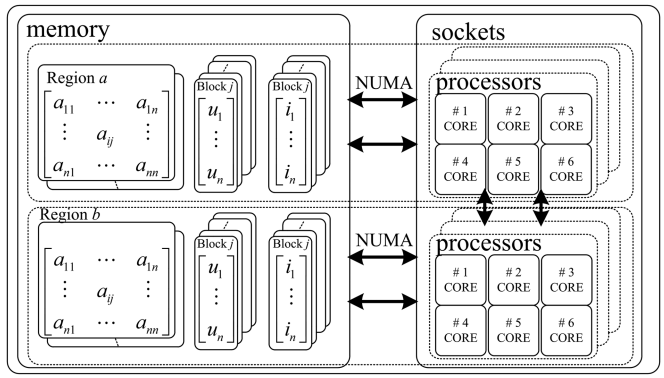


Fig. 6. Shared memory implementation for proposed simulation approach.

the simulation file, such as Figs. 8 and 15, and precalculates all switch-state permutations of the impedance and admittance matrices in regions. In the iteration stage, the simulation program repeatedly executes the nodal analysis in regions and loop-current analysis among regions to get the node voltages.

It should be pointed out that $\Sigma P_m^T Z_m P_m$ is the sum of loop impedance, and $(\Sigma P_m^T Z_m P_m)^{-1}$ is the sum of loop admittance around blocks. Essentially, they can also be enumerated with all the switch permutations around the loop. However, different from the region's situation, the loop-current concerns many more switches with exponentially increased topologies. Therefore it is not realistic to calculate all of them in advance. Instead, A can be computed as encountered during the simulation and cached. Usually, the simulation step is much smaller than the switching period so that the same loop-current admittance may be kept in several simulation steps. Moreover, different switch state combinations may result in the same loop-current impedance as the loop-current impedance across an MMC arm. Thus, the cached loop-current admittance saves much simulation time.

As depicted in Fig. 4, most parts of the proposed simulation flowchart are parallelizable, and the precalculated impedance and admittance matrices have an affinity with the corresponding computation cores. Thus, the flowchart applies to the distributed and shared memory programming models.

Fig. 5 is the implementation of the distributed memory architecture for the proposed simulation approach. This architecture applies to high-performance computer clusters, presented as supercomputers. In this architecture, the solver consists of the master node solver and the slave node solver, the master node solver is designed to solve the loop currents linking all partitions, and the slave node solver is designed to solve the node voltages in each block. The precalculated impedance and admittance matrices are stored on the slave nodes so that the calculation of E_{loop}, Z_{loop}, and X_m can access the on-site memory. The cached loop-current impedance and admittance matrices are stored in the master node, boosting the speed of calculating loop currents.

Fig. 6 illustrates the shared memory architecture, and all matrices are stored and computed in the same high-performance computer.

The detailed implementation for the distributed memory is addressed in Fig. 7(a), and only the E_{loop}, Z_{loop}, and I vectors are transmitted between the master and slave nodes. So the time delay for transmitting MPI messages is short. There are five

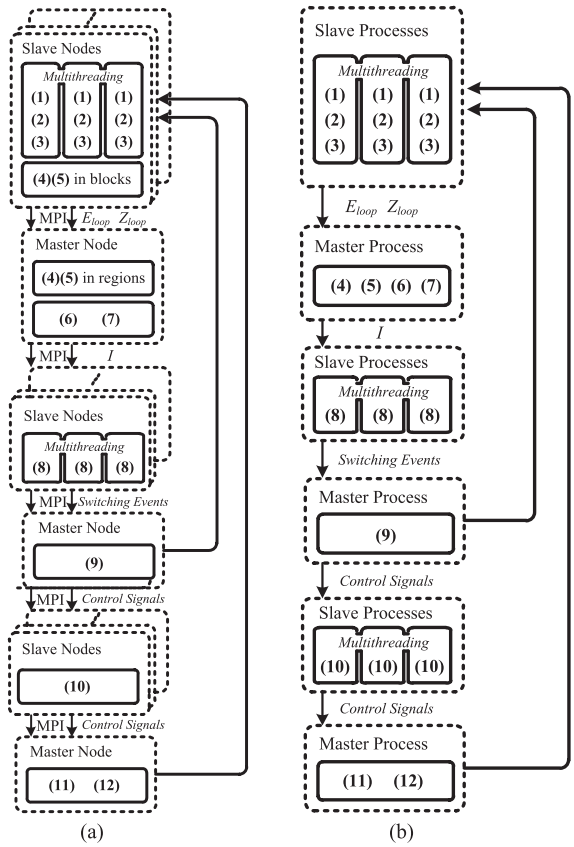


Fig. 7. Detailed implementation of the proposed simulation approach for different architectures. (a) Implementation for the distributed memory. (b) Implementation for the shared memory.

implicit barriers to synchronizing in a simulation step. The most obvious benefit of adopting the distributed memory architecture is that it has almost infinite memory capacity and computing power, which can enlarge the simulation scale of the power electronics system to meet almost any demand. The deficiency is that though the MPI messages are short, synchronization of IO between nodes is still time-consuming in high-performance computation. Hence the distributed memory architecture is extremely cumbersome but highly scalable.

Fig. 7(b) is the detailed implementation of the shared memory architecture. It consists of master and slave processes, which

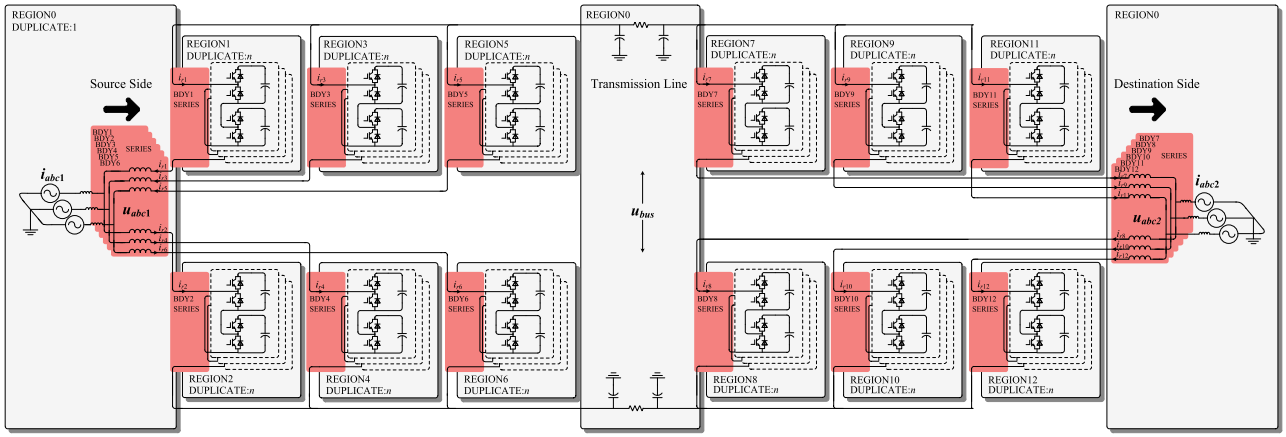


Fig. 8. Simulation model of the MMC-based HVDC described in region-folding.

almost have the same functions as in the distributed memory architecture. The benefit is that each simulation step is executed without IO operations to other nodes, and both the master and slave processes can access all the variables on shared memory. Thus, the synchronization is time-saving, and this implementation is more efficient than the distributed memory architecture with the same simulation model. The deficiency is that a single node's memory and computation power is limited. Thus, the hardware confines the simulation scale of the power electronics systems. The following cases are implemented on shared memory to compare the accuracy and efficiency of the proposed simulation approach with the popular state-space-based EMT commercial software 1 and the famous MNA-based EMT commercial software 2. Since a large-scale power electronics system is a complex and coupling system, all the following simulations are carried out by the backward Euler method to ensure numerical stability. The max iteration is 300. As the simulation scale grows, the convergence tolerance in MMC-based HVdc increases from 1e-8 to 1e-6, and the max tolerance 1e-6 is in the simulation of 1536 submodules. The convergence tolerance of 1e-8 meets all simulations in dc photovoltaic power station.

V. Case ①: MMC-Based HVDC

This article validates the accuracy and efficiency of the proposed region-folding simulation approach compared with the commercial software, sharing the same MMC-based HVdc power transmission simulation model.

As is known to all, the large-scale simulation of the MMC converter is complex and time-consuming due to the large amounts of cascaded submodules. Many papers [7], [8], [9], [10] have contributed to the equivalent model to simplify the topological complexity and accelerate the simulation speed. Fortunately, the proposed simulation approach is especially suitable for the MMC, as it is the typical topology connected by loop currents around arms. No matter how many submodules are cascaded in an arm, we only need to enumerate a submodule's impedance and admittance matrices based on the switch-state perturbations of two IGBTs and share the matrices with every submodule in this arm.

TABLE I
Simulation Parameters for MMC-Based HVDC Transmission

Symbol	Description	Value
u_{bus}	DC bus voltage	4800 V
N	Number of sub-modules in an arm	8
u_{sm}	Voltage of sub-module capacitor	600 V
i_d^{ref}	Instantaneous active current reference for the destination station	40 A
i_q^{ref}	Instantaneous reactive current reference for the destination station	0 A
L_a	MMC arm inductor	20 mH
L_s	MMC grid inductor	10 mH
D_{cable}	Cable distance	150 km
s_{cable}	Cable section area	1600 mm^2
r_{cable}	Cable resistance	2 Ω
c_{cable}	Cable capacitance	50 μF
t	Simulation time	5 s
h	Simulation step	1 μs
N	Number of sub-modules in a region	4
duplicate	Duplicates of blocks in an arm	2
regions	Regions in simulation	13
blocks	Blocks in simulation	25
switches	Switch devices in simulation	192
nodes	Nodes in simulation	796

The simulation model is depicted in Fig. 8, as the same model is built in both commercial software. They are given the same circuit, control, and simulation parameters. The detailed parameters are in Table I. The MMC converters are controlled according to the instantaneous reactive power theory and modulated with the nearest level modulation. On the source side, the MMC maintains the voltage of the dc bus. On the destination, the MMC operates following the active and reactive current references.

In Fig. 8, the ac power grid and the transmission line are placed in REGION 0, and each arm of the MMC is a separate region, named from REGION 1 to REGION 12. These regions are connected by boundary (BDY). There are two kinds of boundaries: the series boundary and the parallel boundary.

Theoretically, a submodule in a block is the most memory-saving method, with the fewest switch-state permutations. However, the modern CPU is designed and manufactured with the single instruction multiple data (SIMD) instruction set. Hence, matrix computation is optimized with the dot product of vectors, and a bit larger matrix will enhance computational efficiency. It

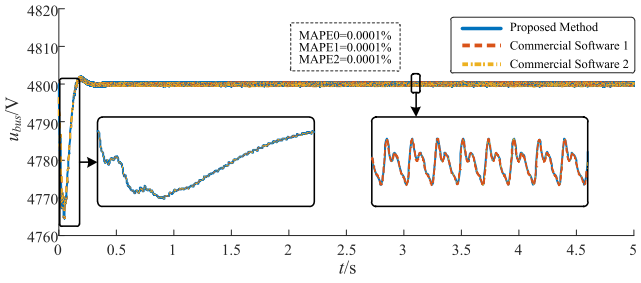


Fig. 9. Comparison of the DC bus voltage u_{bus} waveforms.

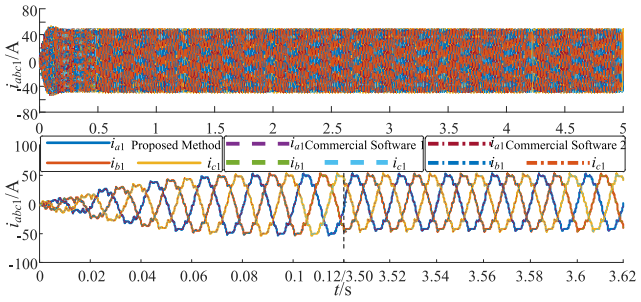


Fig. 10. Comparisons of the AC grid current i_{abc1} on the source side.

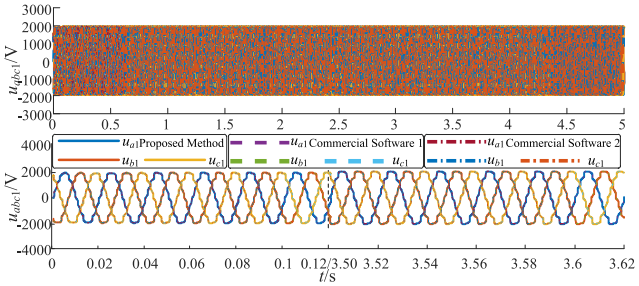


Fig. 11. Comparisons of the AC output voltage u_{abc1} on the source side.

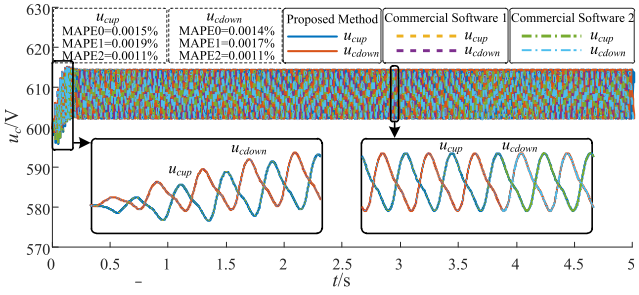


Fig. 12. Comparisons of the capacitor voltages from the upper and lower arm on the source side.

is a tradeoff between memory and efficiency. Thus, each block has four submodules, eight switches, and nine nodes.

A. Comparison of Simulation Accuracy

As a comparison, the same simulation model with eight submodules in each arm is carried out separately by the region-folding approach, the commercial software 1 and the commercial software 2. We introduce the mean absolute percentage error (MAPE) as the general accuracy indicator to conduct quantitative comparisons among them. Due to the MAPE defect of enlarging error near zero, the MAPE is calculated solely on dc variables away from zero, excluding ac variables and i_{q2}. MAPE0 is the value of commercial software 1 and 2, calculated as a reference of tolerant error. MAPE1 is the value of commercial software 1 and the proposed method, and MAPE2 is the value of commercial software 2 and the proposed method. Simulation results indicate that the proposed approach has almost the same simulation accuracy as commercial software 1 and 2.

Fig. 9 is the waveforms of the dc bus voltage u_{bus}. The model has eight submodules in each arm, and each submodule voltage is 600 V. So the reference voltage of the dc bus is 4800 V. It can be seen that the proposed method has an identical dynamic process and switch-level ripple with commercial software 1 and commercial software 2 in the bus voltage waveforms. The MAPE1 and MAPE2 are negligible, which guarantees accuracy.

Fig. 10 is the ac grid current i_{abc1} on the source side. Since the instantaneous active current is 40 A and the instantaneous reactive current is 0 A, controlled on the destination side. The current reference values are reflected on the source side in Fig. 10. The proposed approach and the commercial software 1

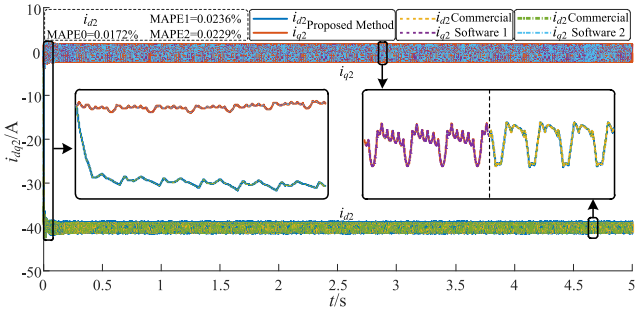


Fig. 13. Comparisons of the instantaneous current on the destination side.

and 2 share the same dynamic adjustment process and distortion on i_{abc1}.

Fig. 11 compares the MMC output ac voltage u_{abc1} on the source side. Since each arm only has eight submodules, the voltage distortion is noticeable. Accordingly, the waveforms indicate the consistency between the proposed method and the commercial software.

Fig. 12 illustrates the capacitor voltages from the upper arm and lower arm, respectively. The simulation results show identical voltage fluctuations caused by phase current.

The MMC has the same structure and modulation method on the destination side, so i_{abc2}, u_{abc2}, and capacitor voltage fluctuations are similar to those on the source side. The MAPE1 and MAPE2 of u_{cup} and u_{cdown} are small, consistent with the wave-to-wave comparisons.

Fig. 13 compares instantaneous active i_{d2} and reactive current i_{q2} waveforms from different simulation tools. The results show

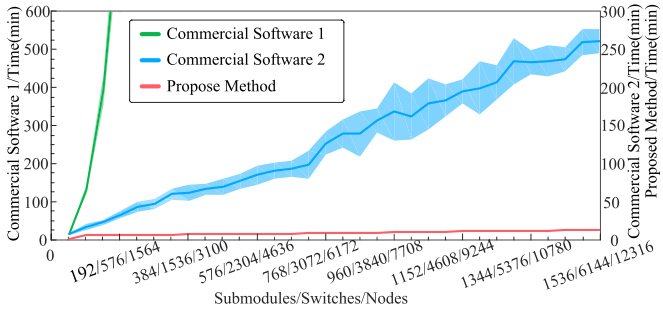


Fig. 14. Statistics of simulation time in commercial software 1, 2, and proposed approach.
Note: All the simulations are on the same computer with 2 Intel Xeon E5-2680 2.50 GHz CPUs, a total of 24 cores.

the same current fluctuations. The MAPE1 and MAPE2 of i_{d2} validate the accuracy.

The comparisons of simulation accuracy between the proposed region-folding approach and commercial software prove that though adopting different simulation mechanisms, the proposed simulation approach is still as accurate as the other simulation software.

B. Comparison of Simulation Efficiency

The proposed region-folding EMTP simulation approach is designed for large-scale power electronics systems, so the proposed approach's simulation efficiency is tested with thousands of switch devices and tens of thousands of nodes. This section compares the simulation times with the commercial software. Different scale and dc bus voltage models are simulated by increasing the *duplicate* attribute of REGION 1–REGION 12 in Fig. 8.

The max scale in the popular state-space-based simulation software is 192 submodules since it already takes too much time to simulate, equivalent to the *duplicate* 4 of REGION 1–REGION 12 in Fig. 8. The proposed simulation approach can quickly extend the simulation scale by changing the duplicate attribute, avoiding the trouble of connecting each node with its neighbors.

Fig. 14 shows the mean and standard error statistics of simulation time, in which the same model is simulated four times. The simulation time is 0.5 s, and other parameters are the same as in Table I. The X-axis is the total number of submodules, switches, and nodes in the arm regions from REGION 1 to REGION 12. The left Y-axis is the simulation time of the state-space-based EMT commercial software, and the right Y-axis is the simulation time of the MNA-based EMT commercial software and the proposed approach. The max scale model simulated in the state-space-based EMT commercial software of 192 submodules consumes 558 minutes. While with the same model, the average time consumed by the proposed method with 24-core computation is 7 minutes, the results achieve an 80× speedup. The average time consumed by MNA-based EMT commercial software with 1563 submodules is 261 minutes, compared with 13.3 minutes by the proposed method. We achieve a 20× speedup.

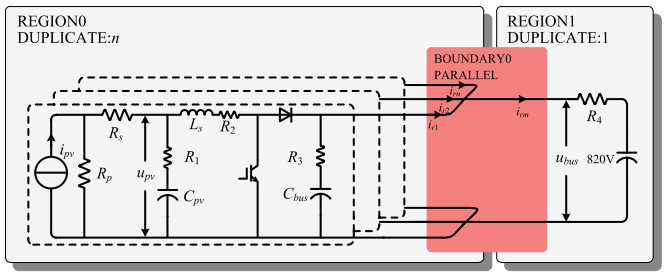


Fig. 15. Simulation model of the DC photovoltaic power station in region-folding.

In conclusion, the case analysis of MMC-based HVdc proves the accuracy and efficiency of the proposed region-folding simulation approach.

VI. Case ②: DC Photovoltaic Power Station

In this chapter, the accuracy and efficiency of the proposed region-folding simulation approach are verified by the typical parallel scene, where many converters are connected to the dc bus.

Fig. 15 is the simulation model of a dc photovoltaic power station depicted in region-folding, in which the current source i_{pv}, resistor R_s, and resistor R_p imitate the photovoltaic panel at a quiescent point.

Several converters are connected to the dc bus to collect the solar energy in the photovoltaic power station. Blocks in REGION 0 are the partitions that contain converters in parallel. The duplicate attribute of REGION 0 controls the scale of the connected photovoltaic converter. This kind of model is usually used to verify the stability of large-scale converters parallel connected at the point of common coupling.

The detailed parameters are in Table II. The control purpose of the boost converter employed is to stabilize the output voltage of the photovoltaic panel at u_{pv} and transmit electricity to the u_{bus}.

To fully utilize the SIMD instruction set optimizing the dot product of vectors, we put five converters in a block to enlarge the dimensions of the impedance/admittance matrices.

A. Comparison of Simulation Accuracy

As a comparison, the same simulation model with 240 converters is carried out separately by the commercial software and the region-folding approach. The simulation waveforms illustrate identical switch-level fluctuations.

Fig. 16 compares the dc bus voltage u_{bus}, whose reference value is 820 V. The simulation results give consistent ripple voltage on u_{bus}. The MAPE1 and MAPE2 of u_{bus} indicate accuracy.

Fig. 17 shows the photovoltaic panel's output voltage waveform from one of those converters. The dynamic process of adjusting u_{pv} by closed-loop control and the switch-level fluctuations are reflected on the voltage waveforms. In the simulations, a small simulation step of 1 μs is adopted, and the switching

TABLE II
SIMULATION PARAMETERS FOR LARGE-SCALE DC PHOTOVOLTAIC POWER STATION

Symbol	Description	Value
u_{bus}	DC bus voltage	820 V
u_{pv}	PV panel reference output voltage	620 V
i_{pv}	PV panel output current	10 A
R_p	PV panel parallel parasitic resistor	1 kΩ
R_s	PV panel series equivalent resistor	0.2 Ω
L_s	MPPT inductor	2 mH
R_2	Series resistor for L_s	10 Ω
f_s	IGBT frequency	10 kHz
C_{pv}	PV panel output capacitor	1000 μF
R_1	Equivalent resistor for C_{pv}	0.5 Ω
C_{bus}	MPPT output capacitor	1000 μF
R_3	Equivalent resistor for C_{bus}	0.5 Ω
R_4	Equivalent resistor for u_{bus}	1 mΩ
t	Simulation time	5 s
h	Simulation step	1 μs
converters	Total number of converters	240
N	Number of converters in a region	5
duplicate	Duplicates of MPPT region	48
regions	Regions in simulation	2
blocks	Blocks in simulation	49
switches	Switch devices in simulation	480
nodes	Nodes in simulation	720

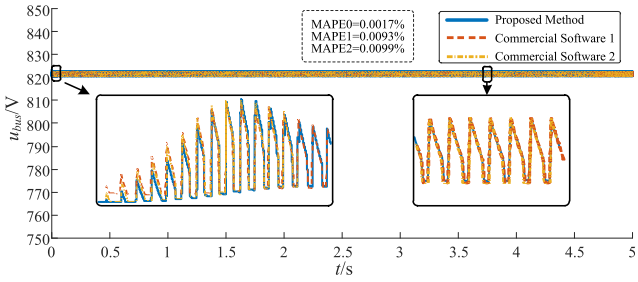


Fig. 16. Comparison of the dc bus voltage u_{bus}.

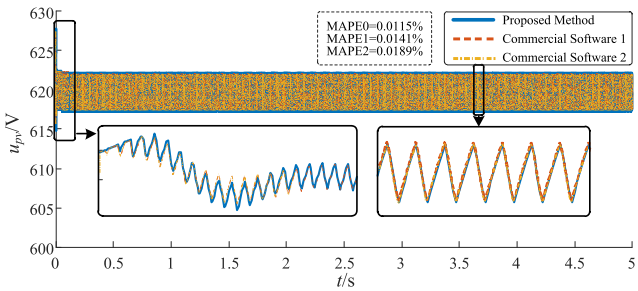


Fig. 17. Comparison of the PV panel output voltage u_{pv}.

process of 10 kHz is precisely portrayed. The MAPE1 and MAPE2 of u_{pv} validate the accuracy.

Fig. 18 demonstrates the waveform of inductor current i_L, which freewheels the output current to the high-voltage side. The simulation model in the commercial simulation software and the proposed approach share the same conducted and freewheeling process with a similar ripple wave. The MAPE1 and MAPE2 are larger than in other figures since i_L is a sharp changed curve near zero. It is in the range of tolerant error compared with MAPE0.

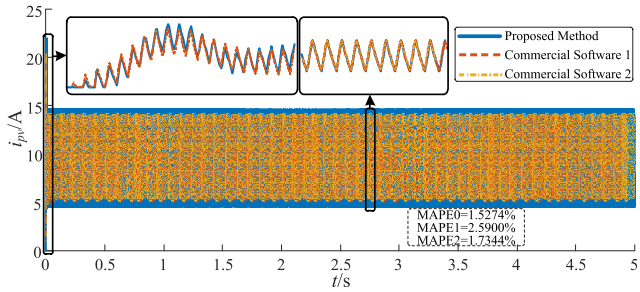


Fig. 18. Comparison of the inductor current i_L.

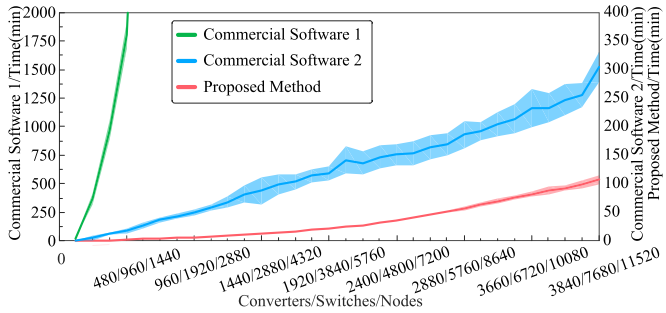


Fig. 19. Statistics of simulation time in commercial software 1, 2, and proposed approach.
Note: All the simulations are on the same computer with 2 Intel Xeon E5-2680 2.50 GHz CPUs, a total of 24 cores.

The comparisons of simulation accuracy between the proposed approach and the popular commercial simulation software driven by different mechanisms prove that they share the same accuracy in the scene of large-scale converters connected in parallel. The loop-current analysis between regions is accurate for different connection types in power electronics systems.

B. Comparison of Simulation Efficiency

Considering that the proposed simulation approach is designed for large-scale power electronics systems, the scale of the dc photovoltaic power station is enlarged by increasing the *duplicate* attribute of REGION 0 in Fig. 15.

With the same problem in the MMC-based HVdc, a large-scale simulation model in state-space-based commercial software is hard to build because the circuit is complex to connect thousands of nodes, and commercial software 1 is stuck to rendering the UI interface. Thus the max scale simulated in commercial software 1 is 480 boost converters in parallel, equivalent to the *duplicate* 96 in REGION 0.

Fig. 19 shows the mean and standard error statistics of simulation time, in which the same model is simulated four times. The simulation time is 0.5 s, and other parameters are the same as in Table II. The X-axis is the total number of converters, switches, and nodes. The left Y-axis is the simulation time of the state-space-based commercial EMT software, and the right Y-axis is the simulation time of the MNA-based commercial EMT software and the proposed approach.

The simulation acceleration is apparent in the max scale model simulated in the state-space-based EMT commercial software of 480 converters. The average time consumed is 1800 min.

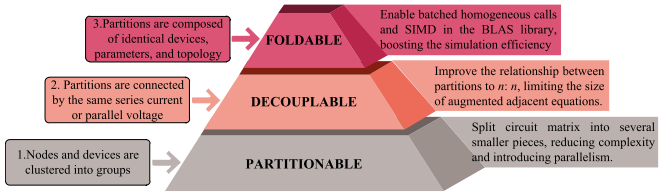


Fig. 20. Application scope and benefits of the proposed simulation approach.

While with the same model, the average time consumed by the proposed method with 24-core computation is 2.35 min, the results achieve a 765× speedup within the comparable system scale. The average time consumed by MNA-based EMT commercial software with 3840 converters is 305 min, compared with 107 min by the proposed method. We achieve a 2.85× speedup within the comparable system scale.

In conclusion, the case analysis of the dc photovoltaic power station proves the accuracy and efficiency of parallel topologies.

VII. Application Scope and Limitations

The application scope and limitations of the proposed region-folding simulation approach are described in Fig. 20.

Generally, the simulation efficiency is increased by three acceleration levels: partitionable, decouplable, and foldable. The higher a circuit locates, the more efficient simulation is.

A. Partitionable

First, a circuit is partitionable if the electrical nodes and devices are topologically clustered into several groups and several tie lines connect different groups. As is known, the computational complexity of matrix inversion is $O(n^3)$, and n is the size of the matrix. The computational complexity of a partitionable circuit matrix's inversion is far less than that of an unpartitionable circuit's.

B. Decouplable

Second, a circuit is decouplable if the circuit can be partitioned and partitions are coupled by series current or parallel voltage. The undecouplable circuit has an increasing size of augmented adjacent equations (matrix border), and the decouplable circuit has a fixed size of augmented adjacent equations (matrix border). The computational complexity of a decouplable circuit matrix's inversion is far less than that of an undecouplable circuit's.

C. Foldable

Furthermore, a circuit is foldable if the circuit can be decoupled and partitions share identical devices, parameters, and topology. The foldable circuit matrix contains a batch of small and identical matrices, which can be calculated in a batched call in BLAS library like Math Kernel Library. Such batched call in BLAS is optimized and takes full use of vector units and the cache of modern architecture in CPU. Foldable circuit matrices have better calculation efficiency than unfoldable circuit matrices calculated one by one, boosting simulation speed.

VIII. Conclusion

This article proposes a region-folding electromagnetic transient simulation approach for large-scale power electronics systems to boost simulation speed. In the region-folding approach, the loop tear method is proposed to decouple the connections among power electronics blocks, the grouping and precalculating method of identical structural blocks is proposed to avoid computing the inverse of matrices repeatedly, and the GSRP is proposed to handle the simultaneous and multiple switching events. The implementation of the proposed approach is combined with high-performance parallelization technology to shorten the simulation time. An MMC-based HVdc model and a dc photovoltaic power station are separately simulated to validate the accuracy and efficiency. Simulation results indicate that the proposed approach has the same accuracy as commercial software but with more than a 765× speedup compared with state-space-based EMT simulation software and a 20× speedup compared with MNA-based EMT simulation software.

The presented results demonstrate the proposed simulation approach's potential in power electronics systems and make the large-scale and small-step simulation of electromagnetic transients with thousands of switch devices efficient.

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