A Multi-Inverter Multi-Rectifier Wireless Power Transfer System for Charging Stations With Power Loss Optimized Control

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***Abstract*—Electric vehicles with different output power levels can use wireless power transfer (WPT) systems. Different vehicle assemblies (VAs) may be charged by different ground assemblies (GAs) in charging stations. However, the overall efficiency of the WPT system may drop significantly when the power class difference between GA and VA is large. To address this issue this article proposes a dc-link parallel ac-link series multi-inverter multirectifier architecture for high-power WPT systems. Modulation, power transfer capability, and power sharing from the design aspects are investigated. A detailed power loss analysis and an easy-to-implemented power loss optimized control method based on mutual inductance identification are presented in this article. Finally, experimental results are obtained from a 20-kW *LCC-LCC* WPT system to validate the analysis and proposed system operation.**

***Index Terms*—Multi-inverter multi-rectifier (MIMR), power loss optimized control (PLOC), wireless power transfer (WPT).**

I. Introduction

WIRELESS power transfer (WPT) can achieve automatic charging for electric vehicles (EVs) without user intervention [1], which provides a better user experience than conventional plug-in chargers. In recent years, academic research, industrial products, and international standards have been conducted, looking at optimal control methods, coil and circuit design, and power and efficiency improvements [2], [3], [4]. Fig. 1 shows the diagram of the EV WPT system which consists of the ground assembly (GA) and the vehicle assembly (VA). The power is supplied from the grid and a power factor corrector (PFC) turns the mains ac voltage into a stable dc voltage. DC/DC converters such as buck/boost can be added to the GA and VA to obtain a wide range of power regulations. Series, parallel, and compound circuits have been proposed to compensate for the reactance of the coils [5], and the *LCC-LCC* compensation circuit is widely used for EV WPT products [2].

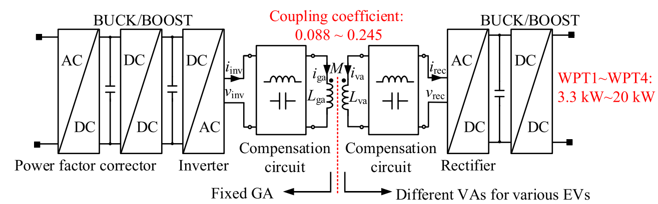

Fig. 1. Diagram of the conventional EV WPT system.

Due to the large range of the battery capacities in different EVs and variables such as the parking positions, power rating and coupling coefficient of the EV WPT system can change considerably. According to the definition of the international wireless charging standard SAE J2954 in [6], the output power ratings range from 3.3 kW to higher than 20 kW, and the coupling coefficient can range from 0.088 to 0.245. Although multiple transmitter (*Tx*) coils, multiple receiver (*Rx*) coils, and multiple cells are conducive to power level improvement [7], [8], [9], [10], original equipment manufacturers have strict restrictions on the size, weight, and cost of the GA and VA. For example, manufacturers like Hongqi for their E-HS9 model require the 10-kW VA to be less than 37 cm $\times$ 37 cm $\times$ 6 cm and weigh less than 17 kg. The required offsets defined in SAE J2954 [6] are $\pm$75 mm on the *X*-axis and $\pm$100 mm on the *Y*-axis. Since *Tx* coils larger than RX coils result in improved misalignment tolerance caused by different parking positions, the EV WPT system usually has a large *Tx* coil and a small Rx coil (one-to-one coil design). Considering the cost and the limited volume of

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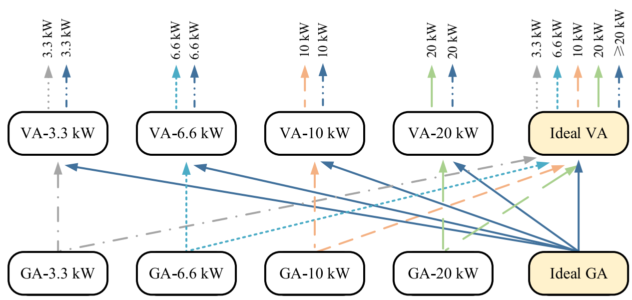

Fig. 2. Interoperability of different GAs and VAs in charging stations.

EVs, the high-power WPT system with one *Tx* coil and *RX* coil is more practical and has already been adopted by the EV WPT suppliers like WiTricity, ZTE, VIE, etc. Currently, the design of a WPT system usually provides customized parameters for different power ratings and power transfer distances. Various dc/dc converters [11], active rectifiers [13], phase-shifted capacitors [14], and variable inductors [15] have been proposed to achieve a wide output power range with a large coupling coefficient variation. In addition, different modulation schemes have been investigated including duty cycle control [16], phase shift control [17], frequency shift control [18], pulse density modulation [19], and ON-OFF keying [20]. Research reported in [11] and [12] shows the design of 50-kW and 100-kW coupling coils with a dc/dc efficiency higher than 95.5% under 160 mm power transfer distance, respectively. The customized WPT system has already achieved high efficiency and high power. However, this design of GA and VA is only feasible for domestic use where the interoperability is not considered.

A GA used as a public facility needs to be compatible with different VAs as shown in Fig. 2. When the GA and VA with different power ratings operate with each other, the equivalent impedance of the resonant tank deviates from the optimal region. This may result in a significant decrease in the output power and overall efficiency [21], [22]. For example, a 20-kW GA interoperating with a 20-kW VA should be able to deliver 20 kW efficiently, while the same GA interoperating with a 3.3-kW VA is also able to deliver 3.3 kW but with a significant loss in efficiency caused by impedance mismatch. As defined in SAE J2954 for interoperability, the overall efficiency decreases with the increase of the power class difference and it is only 75% when two power class difference exists. Since the industrialization of wireless charging technology for EVs is advancing rapidly, the interoperability requirement is becoming increasingly important, especially for the high-power WPT systems used in charging stations.

In high-frequency and high-power WPT systems, power loss optimized control (PLOC) is important where heat dissipation would otherwise become difficult [27], [28], [29], [30], [31]. The buck/boost converters or active rectifiers are used to regulate the inverting and rectifying voltages against system parameter variations through traversing algorithms, simulated annealing algorithms, perturbation and observation (P&O) algorithms, and online parameter identification algorithms. However, these additional circuits are difficult to achieve wide-range soft switching under all operating conditions. The switching power losses of these converters increase when hard switching occurs. In addition, these additional circuits increase the size and cost of the overall system. For the interoperability of the EV WPT systems with different power levels, a PLOC method is required to maximize the power transfer capability of the system to reduce the charging time and to obtain a high efficiency to ensure good heat dissipation simultaneously.

In summary, there is relatively little literature on the interoperability of the EV WPT systems, and no comprehensive design guidelines and control algorithms are available that simultaneously optimize both the power transfer capability and overall efficiency, especially for public wireless charging stations. The essential requirement for strong interoperability is that both GA and VA need to have strong power regulation abilities under soft-switching conditions. However, dual-side dc/dc converters increase the number of cascaded main circuits which may decrease power density and increase costs, and complex high-frequency synchronization of active rectifiers or phase-shifted capacitors reduces the charging reliability. To solve this problem, a dc-link parallel ac-link series (DPAS) multi-inverter multirectifier (MIMR) architecture is proposed in this article, whose contributions can be summarized as follows.

1) A modular DPAS-MIMR architecture with strong interoperability for the high-power WPT system used in charging stations.
2) A novel mutual inductance identification-based easy-to-implemented PLOC method.
3) Experimental validation of a 20-kW efficient, high-power, and flexible EV WPT system.

The rest of this article is organized as follows, in Section II the proposed DPAS-MIMR WPT system is introduced and its modulation, power transfer capability, and power sharing are studied. Section III presents the power loss analysis and the efficiency optimization of the system with large coupling coefficients and output power variations. Section IV proposes a simplified PLOC method where high efficiency and low complexity can be achieved simultaneously. The experimental validation is given in Section V, finally Section VI concludes this article.

II. Proposed DPAS-MIMR WPT System

This section presents the proposed DPAS-MIMR WPT system and its synchronization principle. In addition, the power transfer capability and power-sharing characteristics of the proposed DPAS-MIMR WPT system are discussed.

A. Proposed Topology

The schematic of the proposed system is shown in Fig. 3. V_{bus} and V_{bat} are the input and output dc-link voltages, respectively. *m* and *n* are the numbers of inverters and rectifiers, respectively. S_{1i}_S_{4i} are the MOSFETs of #*i* inverter. Q_{1j}_Q_{2j} and D_{1j}_D_{2j} are the MOSFETs and diodes of #*j* rectifier, respectively. v_{pi} and i_{pi} are the resonant voltage and current of #*i* inverter, respectively. v_{sj} and i_{sj} are the resonant voltage and current of #*j* rectifier, respectively. C_b is a dc blocking capacitor whose capacitive reactance should be small (less than 0.5 Ω), and it should withstand high inverting current at 85 kHz. When using symmetrical phase shift control methods, there is no dc component on $v_{pi,}$ and C_b

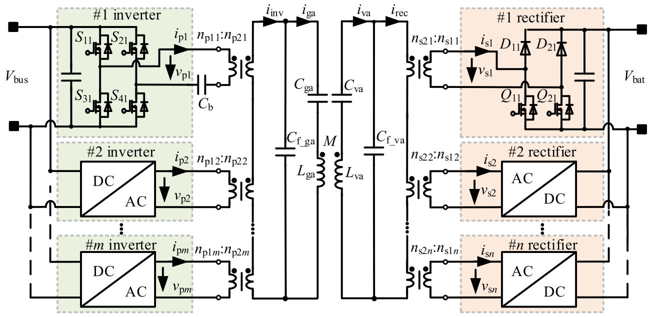

Fig. 3. Proposed DPAS-MIMR WPT system.

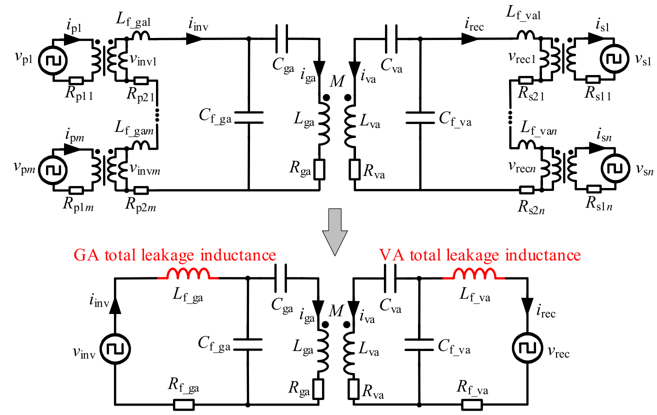

Fig. 4. Equivalent circuit of the proposed DPAS-MIMR WPT system.

is not needed. However, the regulation range is limited and hard switching occurs when the phase shift angle is large. Hence, an asymmetric control method is proposed and the half-bridge mode is introduced. Since there exists a dc component in this mode, a dc-blocking capacitor is required. The dc-blocking capacitors can be added to all the inverters and rectifiers. However, to reduce the number of these capacitors, only one capacitor needs to be added to #1 inverter, which enables it to be used with asymmetric modulation schemes, such as half-bridge duty cycle control. Since multiple inverters and active rectifiers are used, the controllers should be synchronized. In this article, #1 inverter acts as the master and generates a square-wave synchronization signal, and the other inverters act as the slaver. C_{f_ga}, C_{ga}, C_{va}, and $C_{\text{f\_va}}$ are the compensation capacitors of the *LCC-LCC* circuits. L_{ga} and L_{va} are the inductances of the coupling coils. $n_{p1i}\,(n_{s1i})$ and $n_{p2i}\,(n_{s2i})$ are the turns of primary and secondary windings of the resonant inductor integrated transformers (RIITs) on the GA and VA, whose turns ratios, m_i and n_j, are defined as

$$m_i = m_{p1i}/m_{p2i} \tag{1}$$

$$n_j = n_{s1j}/n_{s2j} \tag{2}$$

k and M are the coupling coefficient and mutual inductance between *Tx* and *Rx* coils

$$M = k\sqrt{L_{\text{ga}}L_{\text{va}}}. \tag{3}$$

Fig. 4 shows the equivalent circuit of the proposed DPAS-MIMR WPT system. R_{p1i} and R_{p2i} are the primary and secondary parasitic resistances of #*i* RIIT on the GA, respectively. R_{s1j} and R_{s2j} are the primary and secondary parasitic resistances of #*j* RIIT on the VA, respectively. R_{ga} and R_{va} are the parasitic resistances of the coupling coils. R_{f_ga} and R_{f_va} are the total equivalent parasitic resistances of the DPAS-based inverters and rectifiers, respectively. $L_{f\_\text{ga}i}$ and $L_{f\_\text{va}j}$ are the leakage inductances of #*i* and #*j* RIITs on the GA and VA, respectively. Although a very small leakage inductance can be achieved using a sandwich structure, additional resonant inductors are still needed. To reduce the size and cost, the leakage inductance of the RIITs is used as the resonant inductors. The total reactance can be calculated as conventional *LCC-LCC* topology and its accuracy can be within 5%. Thus, one can obtain the total leakage inductances of the GA and VA as

$$L_{f\_\text{ga}} = \sum_{i=1}^{m} L_{f\_\text{ga}i} \tag{4}$$

$$L_{f\_\text{va}} = \sum_{j=1}^{n} L_{f\_\text{va}j}. \tag{5}$$

For simplicity, their reactances are defined as X_{ga} and X_{va}, respectively,

$$X_{\text{ga}} = \omega L_{f\_\text{ga}} \tag{6}$$

$$X_{\text{va}} = \omega L_{f\_\text{va}}. \tag{7}$$

To ensure proper power sharing and modular design, the turns ratios of the primary and secondary RIITs are designed as follows:

$$m_1 = \cdots = m_m = m_p \tag{8}$$

$$n_1 = \cdots = n_n = n_s. \tag{9}$$

The required leakage inductance for each RIIT can be calculated as

$$L_{f\_\text{ga}1} = \cdots = L_{f\_\text{ga}m} = L_{f\_\text{ga}}/m_p \tag{10}$$

$$L_{f\_\text{va}1} = \cdots = L_{f\_\text{va}n} = L_{f\_\text{va}}/n_s. \tag{11}$$

The secondary windings of the RIITs are connected in series. $v_{\text{inv}i}$ is the secondary voltage of #*i* RIIT on the GA and $v_{\text{rec}j}$ is the secondary voltage of #*j* RIIT on the VA. Thus, one can obtain the total inverting and rectifying voltages v_{inv} and v_{rec} as

$$v_{\text{inv}} = \sum_{i=1}^{m} v_{\text{inv}i} = \sum_{i=1}^{m} v_{pi}/m_i \tag{12}$$

$$v_{\text{rec}} = \sum_{j=1}^{n} v_{\text{rec}j} = \sum_{j=1}^{n} v_{sj}/n_j. \tag{13}$$

B. Power Transfer Analysis

The power rating of the proposed topology can be expanded by adding more cells. In addition, it can adapt to large variations in coupling coefficient, output power, and battery voltage. This

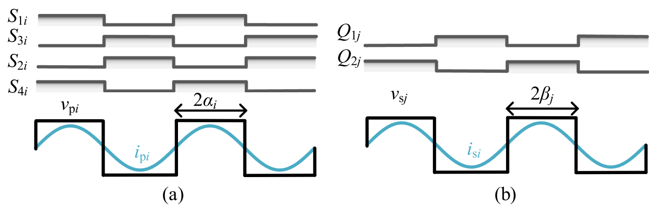

Fig. 5. Typical waveforms of phase shift control. (a) Waveforms of #i inverter; (b) Waveforms of #j rectifier.

section details the modulation schemes of this topology, the power transfer analysis, and the reasons for adapting to the abovementioned parameter variations.

Fig. 5 shows the modulation schemes of the inverters and rectifiers, where the inverters and rectifiers are synchronized. The phase shift control can be applied to the inverters and rectifiers, whose phase angles are defined as α_i and β_j, respectively. The larger the α_i and β_j, the easier it is to achieve soft switching for the inverters and rectifiers. The fundamental harmonic analysis (FHA) is widely used in the WPT system due to the strong filtering effect of the *LCC* resonant tank. The power transfer mainly depends on the fundamental harmonic voltages, whose RMS values can be expressed as [13]

$$V_{pi} = 2\sqrt{2}V_{\text{bus}} \sin \alpha_i / \pi \tag{14}$$

$$V_{sj} = 2\sqrt{2}V_{\text{bat}} \sin \beta_j / \pi. \tag{15}$$

To reduce the reactive power, the system operates at the resonant frequency according to [5]. The output power P_{o} is approximately equal to

$$P_o \approx \omega M I_{\text{ga}} I_{\text{va}}. \tag{16}$$

Furthermore, according to the FHA of the *LCC-LCC* WPT system in Fig. 4, the following relationships can be derived:

$$I_{\text{ga}} = V_{\text{inv}} / X_{\text{ga}} \tag{17}$$

$$I_{\text{va}} = V_{\text{rec}} / X_{\text{va}} \tag{18}$$

$$I_{\text{inv}} = \omega M I_{\text{va}} / X_{\text{ga}} \tag{19}$$

$$I_{\text{rec}} = \omega M I_{\text{ga}} / X_{\text{va}}. \tag{20}$$

To reduce the voltage regulation stress on the inverter and rectifier, the front-end PFC is involved in the voltage regulation. λ and $V_{\text{bus\_max}}$ are the voltage ratio and maximum V_{bus}, respectively,

$$V_{\text{bus}} = \lambda V_{\text{bus\_max}}. \tag{21}$$

The inverters and receivers are synchronized with each other to maximize the power transfer capability. One can obtain the output power P_o as (22) according to (12)–(21)

$$P_o = \frac{\omega M \sum_{i=1}^{m} V_{pi}/m_{pi} \sum_{j=1}^{n} V_{sj}/n_{sj}}{X_{\text{ga}} X_{\text{va}}} = P_{\text{ref}} G_p \tag{22}$$

where the power reference P_{ref} and the power gain G_p are defined as

$$P_{\text{ref}} = 8\omega M V_{\text{bus\_max}} V_{\text{bat}} / \pi^2 X_{\text{ga}} X_{\text{va}} \tag{23}$$

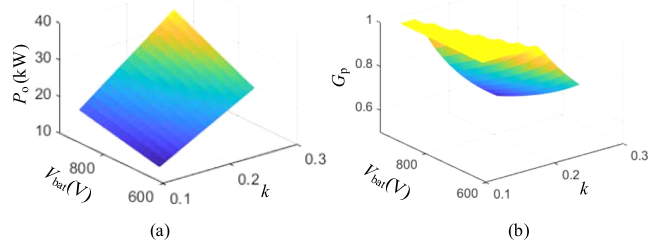

Fig. 6. 3-D plots of P_{ref} and G_p concerning V_{bat} and k for a 20-kW WPT system where $V_{\text{bus}} = 800$ V, $L_{f\_\text{ga}} = 20.6$ μH, $L_{f\_\text{va}} = 28$ μH, $L_{\text{ga}} = 39$ μH, $L_{\text{va}} = 140$ μH, $f = 85.5$ kHz, $m_p = m_s = 2$. (a) P_{ref} concerning V_{bat} and k; (b) G_p concerning V_{bat} and k.

$$G_p = \frac{P_o}{P_{\text{ref}}} = \lambda \sum_{i=1}^{m} \sin \alpha_i \sum_{j=1}^{n} \sin \beta_j / (m_p n_s). \tag{24}$$

P_{ref} is the basic unit representing the power transfer capability of the DPAS-MIMR WPT system. A higher power rating can be obtained by increasing m and n, i.e., increasing G_p.

According to (24), the selections of m, n, m_p, and n_s are important. m and n are determined by the power transfer capability of each converter and the desired output power. For example, if the power transfer capability of one inverter and one rectifier is 10 kW, which is related to the used semiconductors and the cooling conditions, m and n could be 2 for a 20-kW WPT system. According to (25) and (26), m_p and n_s are determined by the maximum resonant currents $I_{\text{ga\_max}}$ and $I_{\text{va\_max}}$, the maximum $V_{\text{bus\_max}}$, and $V_{\text{bat\_max}}$

$$m_p = 2\sqrt{2}mV_{\text{bus\_max}} / (\pi X_{\text{ga}} I_{\text{ga\_max}}) \tag{25}$$

$$n_s = 2\sqrt{2}nV_{\text{bat\_max}} / (\pi \omega L_{f\_\text{va}} I_{\text{va\_max}}). \tag{26}$$

In practice, the designer should consider constraints of output charging current and voltage. V_{bat} varies with the state of charge and the charging current is determined by the desired power. k varies with the parking position. Supposing that V_{bat} and k range from [650 V, 920 V] and [0.14, 0.26], respectively. The desired output power is 20 kW, which means the maximum charging current is 30.8 A. Fig. 6 shows the 3D plot of P_{ref} and G_{p} concerning V_{bat} and k for a 20-kW WPT system where $I_{\text{ga\_max}}$ = 65 Arms and $I_{\text{va\_max}} = 55$ Arms determined by system heat dissipation capability. P_{ref} increases with V_{bat} and k, and a higher P_{ref} corresponds to a stronger power transfer capability of the coils. When both V_{bat} and k are small, P_{ref} is smaller than 20 kW where G_p is set at 1. When both V_{bat} and k are maximum, P_{ref} approaches 37.4 kW where G_p should be set at the minimum value (0.54) to limit the output power to 20 kW.

Although V_{bat} and k vary, one can design proper m, n, m_p, n_s, α_i, β_j, and λ to achieve different G_p. Therefore, the proposed DPAS-MIMR architecture has strong interoperability and can adapt to various VAs with different power ratings.

C. Power Sharing Analysis

To avoid excessive current stresses on the modular converters, proper power sharing is required. In conventional topologies,

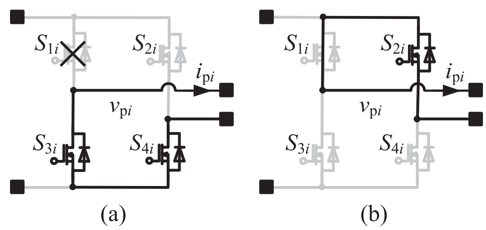

Fig. 7. FMEA of #i inverter. (a) Open-circuited fault. (b) Short-circuited fault.

complex control algorithm such as the droop loop control is used to realize desired power sharing. However, good power-sharing performances can be achieved by the proposed DPAS-MIMR architecture under open-loop control.

i_{mi} presents the magnetizing current of #i transformer. One can obtain (27) according to Kirchhoff's current law

$$i_{pi} = (i_{\text{inv}} + i_{mi})/m_p \approx i_{\text{inv}}/m_p. \tag{27}$$

Since L_{mi} is more than 2 mH, i_{mi} is smaller than 1 A at 85 kHz when V_{bus} is 840 V. Every i_{pi} is almost equal to i_{inv}/m_p, which means current sharing among different inverters can be realized naturally.

The input current of #i inverter is defined as $I_{\text{bus}i}$. According to (14) and the energy conservation law, one can obtain the input current for #1 - #m inverter

$$I_{\text{bus}i} = 2\sqrt{2}I_{\text{inv}}\sin\alpha_i/(\pi m_p). \tag{28}$$

The transferred power of each inverter can be expressed as

$$P_{\text{bus}i} = I_{\text{bus}i}V_{\text{bus}} = 2\sqrt{2}I_{\text{inv}}V_{\text{bus}}\sin\alpha_i/(\pi m_p). \tag{29}$$

Since V_{bus}, I_{inv}, and m_p are the same for all inverters, the power distribution can be realized by controlling α_i

$$P_{\text{bus}1} : P_{\text{bus}2} : \cdots : P_{\text{bus}m} = \sin\alpha_1 : \sin\alpha_2 : \cdots : \sin\alpha_m. \tag{30}$$

The output current of #j rectifier is defined as $I_{\text{bat}j}$. Similarly, according to (15), the transferred power of each rectifier can be expressed as

$$P_{\text{bat}j} = I_{\text{bat}j}V_{\text{bat}} = 2\sqrt{2}I_{\text{rec}}V_{\text{bat}}\sin\beta_j/(\pi n_s). \tag{31}$$

One can obtain the power distribution of the rectifiers as

$$P_{\text{bat}1} : P_{\text{bat}2} : \cdots : P_{\text{bat}n} = \sin\beta_1 : \sin\beta_2 : \cdots : \sin\beta_n. \tag{32}$$

The power distribution among different inverters and rectifiers can be easily regulated by the phase angles α_i and β_j, respectively.

D. Failure Mode and Effect Analysis

Reliability is of great importance in MIMR systems. The increase in the number of power semiconductor devices used may lead to an increase in the failure rate of the system. Therefore, the failure mode and effect analysis (FMEA) of the multiple inverters in the DPAS-MIMR system is presented.

For power semiconductor devices, there may be open-circuited and short-circuited faults. Fig. 7(a) and (b) show the open-circuited and short-circuited faults of a full-bridge inverter, respectively. When S_{1i} is open-circuited, S_{3i} and S_{4i} are turned on all the time while S_{2i} is turned OFF. #i inverter is bypassed and the other inverters can work normally. When S_{1i} is short-circuited, S_{3i} and S_{4i} are turned OFF while S_{2i} is turned ON permanently. The same strategy can be applied when these faults come to the other MOSFETs. Therefore, only #i inverter is bypassed under these open-circuited or short-circuited faults, and the other inverters can work normally.

According to (19), I_{inv} is determined by I_{va} which is related to the output power and not to the inverter types. When using multiple inverters, the current flows through each inverter decreases to $I_{\text{inv}}/m_{\text{p}}$. In high-power WPT systems, a single MOSFET with TO247 packaging cannot withstand the high conducting currents. For the same current capability, the same number of MOSFETs should be connected in parallel even if only using a full-bridge inverter as shown in Fig. 1. When the short-circuited fault occurs to this full-bridge inverter, it can only operate at the half-bridge mode which means the power transfer capability decreases by half. According to (24), the power transfer capability of the proposed system only decreases by 1/m during a single point of failure on the semi-conductors of the inverters. The larger the m, the smaller the impact of these faults.

III. Power Loss Analysis and Efficiency Optimization

Although both primary-side control and dual-side control can obtain the same desired output power, the overall efficiencies vary. This section presents a detailed power loss analysis for the DPAS-MIMR WPT system with primary-side control and dual-side control.

A. Power Loss Analysis With Primary-Side Control

Primary-side control is a conventional and easy-to-implemented method. The diode rectification can be adopted which means β_j is fixed at 90°. The output power is regulated by α_i. However, the overall efficiency is low at low power levels which will be studied here.

The core loss of #i RIIT is related to the operating frequency f, the magnetic flux density B_i, and the magnetic core volume V_{ei}. Thus, the total core loss P_{core} can be expressed as (33) where a, b, and c are determined by the materials

$$P_{\text{core}} = \sum_{i=1}^{m} af^bB_i^cV_{ei} + \sum_{j=1}^{n} af^bB_j^cV_{ej}. \tag{33}$$

Although P_{core} varies with the applied voltages, it represents only a small part of the total power loss and can be considered a constant for simplicity.

The forward voltage of the diode is defined as V_f. Since all the output current flows through two diodes, the total forward voltage loss P_{dio} can be derived as

$$P_{\text{dio}} = 2I_{\text{bat}}V_f = 2P_oV_f/V_{\text{bat}}. \tag{34}$$

The conduction resistance of the MOSFET is R_{dson}. The conduction losses of #i inverter and #j rectifier can be approximated as being generated by two R_{dson} and one R_{dson} according to

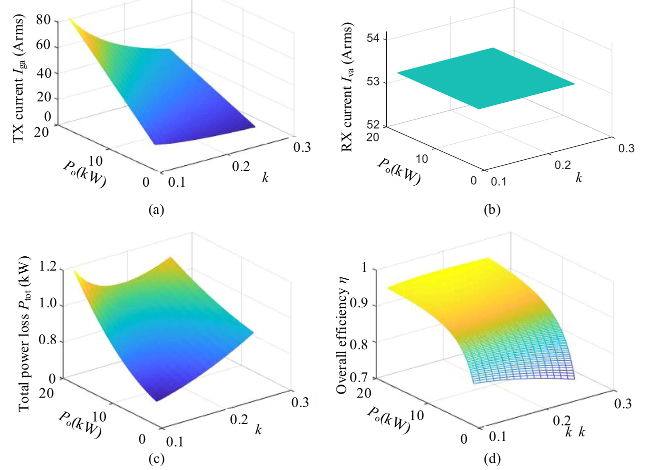

Fig. 8. 3-D plot of I_{ga}, I_{va}, P_{tot}, and η concerning k and P_{o} with diode rectifiers for a 20-kW WPT system where $V_{\mathrm{bat}} = 800$ V, $L_{f_\mathrm{ga}} = 20.6\ \mu$H, $L_{f_\mathrm{va}} = 28\ \mu$H, $C_{f\_\mathrm{ga}} = 168$ nF, $C_{f\_\mathrm{va}} = 123.6$ nF, $C_{\mathrm{ga}} = 178.8$ nF, $C_{\mathrm{va}} = 30.9$ nF, $L_{\mathrm{ga}} = 39\ \mu$H, $L_{\mathrm{va}} = 140\ \mu$H, $R_{\mathrm{ga}} = 60$ mΩ, $R_{\mathrm{va}} = 200$ mΩ, $m = 2$, $n = 2$, $R_{\mathrm{p11}} = 40$ mΩ, $R_{\mathrm{p21}} = 30$ mΩ, $R_{s11} = 40$ mΩ, $R_{s21} = 30$ mΩ, $R_{\mathrm{dson}} = 20$ mΩ, $V_{\mathrm{f}} = 1.6$ V, $f = 85.5$ kHz. (a) I_{ga}. (b) I_{va}. (c) P_{tot}. (d) η.

Fig. 5(a) and (b), respectively. Based on the resistance transformation of the transformer and Fig. 4, the total equivalent resistances, R_{f_ga} and R_{f_va}, can be expressed as

$$R_{f\_\mathrm{ga}} = \sum_{i=1}^{m}\left(\frac{R_{p1i} + 2R_{\mathrm{dson}}}{m_p^2} + R_{p2i}\right) \tag{35}$$

$$R_{f\_\mathrm{va}} = \sum_{j=1}^{n}\left(\frac{R_{s1j} + R_{\mathrm{dson}}}{n_p^2} + R_{s2j}\right). \tag{36}$$

According to (16) and (19), one can obtain the relationships among I_{va}, I_{inv}, and I_{ga} as

$$I_{\mathrm{va}} \approx P_o/(\omega M I_{\mathrm{ga}}) \tag{37}$$

$$I_{\mathrm{inv}} \approx P_o/(X_{\mathrm{ga}} I_{\mathrm{ga}}). \tag{38}$$

The total power loss of the proposed WPT system, P_{tot}, consists of the conduction loss of the MOSFETs, the core loss and copper loss of the RIITs, the loss of the *Tx* and *Rx* coils, and the forward voltage loss of the diodes. Combining (20), (37), and (38), P_{tot} can be derived as

$$\begin{aligned} P_{\mathrm{tot}} &= I_{\mathrm{inv}}^2 R_{f\_\mathrm{ga}} + I_{\mathrm{ga}}^2 R_{\mathrm{ga}} + I_{\mathrm{va}}^2 R_{\mathrm{va}} + I_{\mathrm{rec}}^2 R_{\mathrm{f\_va}} + P_{\mathrm{dio}} + P_{\mathrm{core}} \\ &= \frac{y_1}{I_{\mathrm{ga}}^2} + y_2 I_{\mathrm{ga}}^2 + \frac{2P_o V_f}{V_{\mathrm{bat}}} + P_{\mathrm{core}} \end{aligned} \tag{39}$$

where y_1 and y_2 are defined as follows

$$y_1 = \frac{P_{\mathrm{o}}^2 R_{f\_\mathrm{ga}}}{X_{\mathrm{ga}}^2} + \frac{P_{\mathrm{o}}^2 R_{\mathrm{va}}}{\omega^2 M^2},\ y_2 = R_{\mathrm{ga}} + \frac{\omega^2 M^2 R_{f\_\mathrm{va}}}{X_{\mathrm{va}}^2}. \tag{40}$$

Finally, one can obtain the overall efficiency η as

$$\eta = P_{\mathrm{o}}/(P_{\mathrm{o}} + P_{\mathrm{tot}}). \tag{41}$$

Fig. 8 shows the 3-D plot of I_{ga}, I_{va}, P_{tot}, and η concerning coupling coefficient and power variations under conventional primary-side control for a 20-kW WPT system. I_{ga} increases with the increase of P_o, whereas decreases with the increase of k. Since only primary-side control is used, I_{va} remains unchanged despite different P_o and k. Generally, P_{tot} increases with the increase of k and P_o. η increases with the increase of M when P_o is large, whereas decreases with the increase of M when P_o is small. In addition, η decreases significantly at light loading. The maximum efficiency approaches 95% at 20 kW, whereas the minimum efficiency decreases to only 75% at 3.3 kW. The reason is that the constant power loss caused by I_{va} accounts for a large portion of P_o at light loading.

B. Efficiency Improvement With Dual-Side Control

Although primary-side control can obtain the desired output power, the overall efficiency decreases significantly when P_o decreases to a certain value. Dual-side control can optimize the distribution of resonant currents which benefits efficiency improvement. The parasitic resistances, mutual inductance, output power, and battery voltage are determined by the application scenario. Both α_i and β_j can be used to regulate I_{ga} and I_{va} against the variations in mutual inductance and power. The overall efficiency can be optimized while achieving the desired output power.

The minimum P_{tot} is defined as $P_{\mathrm{tot\_min}}$. Since $y_1 + y_2 \geq 2\sqrt{y_1 y_2}$, one can obtain (42) according to (39)

$$\begin{aligned} P_{\mathrm{tot\_min}} = 2P_o &\sqrt{\left(\frac{R_{f\_\mathrm{ga}}}{X_{\mathrm{ga}}^2} + \frac{R_{\mathrm{va}}}{\omega^2 M^2}\right)\left(R_{\mathrm{ga}} + \frac{\omega^2 M^2 R_{f\_\mathrm{va}}}{X_{\mathrm{va}}^2}\right)} \\ &+ \frac{2P_o V_f}{V_{\mathrm{bat}}} + P_{\mathrm{RIIT\_Fe}} \end{aligned} \tag{42}$$

where I_{ga} is regulated at its optimal value $I_{\mathrm{ga\_opt}}$ as

$$I_{\mathrm{ga\_opt}} = \sqrt[4]{\left(\frac{P_o^2 R_{f\_\mathrm{ga}}}{X_{\mathrm{ga}}^2} + \frac{P_o^2 R_{\mathrm{va}}}{\omega^2 M^2}\right) \Big/ \left(R_{\mathrm{ga}} + \frac{\omega^2 M^2 R_{\mathrm{f\_ga}}}{X_{\mathrm{va}}^2}\right)}. \tag{43}$$

The maximum overall efficiency $\eta_{\max}$ for a fixed system can be derived accordingly

$$\eta_{\max} = P_o/(P_o + P_{\mathrm{tot\_min}}). \tag{44}$$

Fig. 9 shows the optimal conditions with coupling coefficient and power variations. Generally, both $I_{\mathrm{ga\_opt}}$ and $I_{\mathrm{va\_opt}}$ decrease with the increase of k and increase with the increase of P_o. Different from primary-side control, P_{tot} almost remains the same for a certain P_{o} despite different k. The minimum calculated efficiency can be still higher than 93%, which is 18% higher than that of Fig. 8(d).

According to (42), smaller R_{f_ga}, R_{ga}, R_{va}, and R_{f_a} contribute to a smaller $P_{\mathrm{tot\_min}}$ for a certain output power. Although using high-performance semiconductors and low on-resistance transformers and coupling coils can improve $\eta_{\max}$, it also increases the cost or volume. When designing a WPT system, engineers need to find a balance between cost, volume, and maximum efficiency.

In addition, $P_{\mathrm{tot\_min}}$ is related to mutual inductance. The optimal M_{opt}, i.e., the optimal k_{opt}, and $P_{\mathrm{tot\_min\_opt}}$ can be

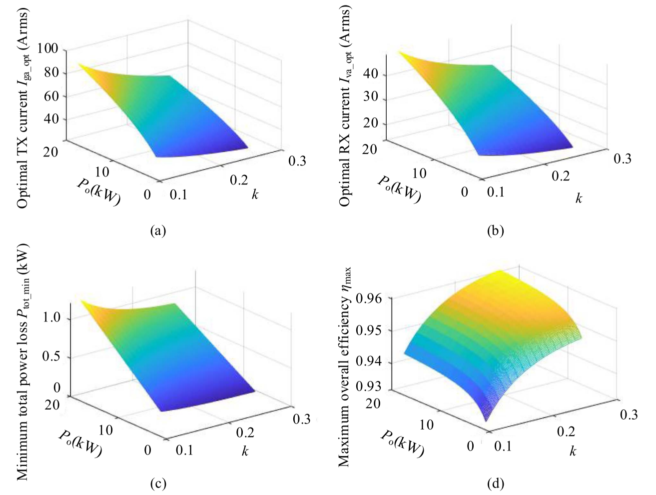

Fig. 9. 3-D plot of $I_{\text{ga\_opt}}$, $I_{\text{va\_opt}}$, $P_{\text{tot\_min}}$, and $\eta_{\max}$ concerning k and P_o for a 20-kW WPT system where $V_{\text{bat}} = 800$ V, $L_{f\_\text{ga}} = 20.6$ μH, $L_{\text{f\_va}} = 28$ μH, $C_{f\_\text{ga}} = 168$ nF, $C_{f\_\text{va}} = 123.6$ nF, $C_{\text{ga}} = 178.8$ nF, $C_{\text{va}} = 30.9$ nF, $L_{\text{ga}} = 39$ μH, $L_{\text{va}} = 140$ μH, $R_{\text{ga}} = 60$ mΩ, $R_{\text{va}} = 200$ mΩ, $m = 2$, $n = 2$, $R_{\text{p11}} = 40$ mΩ, $R_{\text{p12}} = 30$ mΩ, $R_{s11} = 40$ mΩ, $R_{s12} = 30$ mΩ, $R_{\text{dson}} = 20$ mΩ, $V_f = 1.6$ V, $f = 85.5$ kHz. (a) $I_{\text{ga\_opt}}$. (b) $I_{\text{va\_opt}}$. (c) $P_{\text{tot\_min}}$. (d) $\eta_{\max}$.

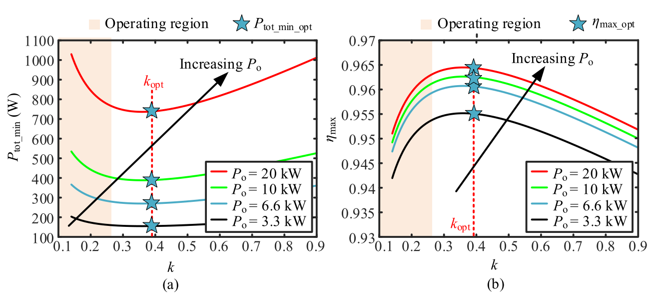

Fig. 10. Plot of $P_{\text{tot\_min}}$ and $\eta_{\max}$ versus k. (a) $P_{\text{tot\_min}}$; (b) $\eta_{\max}$.

deduced as

$$M_{\text{opt}} = \sqrt[4]{\frac{R_{\text{ga}} R_{\text{va}} X_{\text{ga}}^2 X_{\text{va}}^2}{\omega^4 R_{f\_\text{ga}} R_{f\_\text{va}}}} = k_{\text{opt}} \sqrt{L_{\text{ga}} L_{\text{va}}} \tag{45}$$

$$P_{\text{tot\_min\_opt}} = 2P_o \times \sqrt{2\sqrt{\frac{R_{f\_\text{ga}} R_{\text{ga}} R_{f\_\text{va}} R_{\text{va}}}{X_{\text{ga}}^2 X_{\text{va}}^2}} + \frac{R_{f\_\text{ga}} R_{\text{ga}}}{X_{\text{ga}}^2} + \frac{R_{\text{f\_va}} R_{\text{va}}}{X_{\text{va}}^2}} + \frac{2P_o V_f}{V_{\text{bat}}} + P_{\text{RIIT\_Fe}}. \tag{46}$$

Therefore, the optimized $\eta_{\text{max\_opt}}$ can be expressed as

$$\eta_{\text{max\_opt}} = P_o/(P_o + P_{\text{tot\_min\_opt}}). \tag{47}$$

Fig. 10 shows $P_{\text{tot\_min}}$ and $\eta_{\max}$ versus k. $\eta_{\max}$ increases with the increase of k at first, and then decreases. k_{opt} is independent of P_o, which is about 0.4. Generally, k ranges from 0.088 to 0.245 as defined in [6]. Therefore, a higher k may correspond to a higher $\eta_{\max}$ in practice, which can be observed in Fig. 9(d).

IV. Proposed PLOC Method

The total power loss is related to both the hardware and control methods. The maximum efficiency can be obtained when I_{ga} equals $I_{\text{ga\_opt}}$ by varying α_i and β_j as analyzed in Section III-B. However, accurate regulation of β_j requires a complex synchronization technique, as the dual-side controllers are physically separated. In addition, hard switching may occur in both inverters and rectifiers when α_i and β_j are small. It poses great challenges to the control of inverters and rectifiers. This section presents an easy-to-implemented mutual inductance identification-based PLOC method with ZVS operation for the proposed DPAS-MIMR architecture where the challenging secondary synchronization is avoided. High efficiency can also be achieved with a significant reduction in control complexity.

A. Mutual Inductance Identification

Various methods not requiring the knowledge of mutual inductance can be applied to this system and achieve the desired power by using a PID controller. In addition, maximum efficiency point tracking can be realized by the traversal algorithms or P&O methods. However, the dynamic performances need to be improved or it may be trapped in local efficiency optimizations. The power reference P_{ref}, which is important for the interoperability of different GAs and VAs, is a function of mutual inductance M as derived in (23). The desired G_p can be determined only when M is identified. There are some parameter identification-based control methods for output regulation or efficiency optimization. In [32] and [33], the primary phase angle is utilized to estimate the mutual inductance of the series-series WPT system. However, high-frequency phase angle detection is difficult. In [29], a high-order harmonic current is used to identify the mutual inductance of the series-parallel WPT system. However, this method is unsuitable for the *LCC-LCC* topology. This section provides a simple mutual inductance identification for the proposed *LCC-LCC* WPT system.

One can calculate M by sampling I_{inv}, I_{ga}, I_{va}, and I_{rec} according to (19) and (20) during main power transfer. However, high-order harmonic currents of I_{inv} and I_{rec} caused by the *LCC* resonant tank and the power losses can affect the identification accuracy. Although M changes with the relative positions of coupling coils, it is fixed once the EV parks. To avoid overvoltage protection, Q_{1n} - Q_{2n} remain ON state before the main power transmission starts, during which period the proposed mutual inductance identification method is implemented to minimize the influence of the power loss and high-order currents on the identification accuracy.

#1 inverter works to provide necessary I_{ga}, whereas the other inverters remain in by-pass mode. Due to the parallel resonant tank, I_{va} almost equals zero. Thus, the equivalent circuit can be further simplified as shown in Fig. 11. v_{induced} is the induced voltage in the receiving voltage, which can be calculated as

$$V_{\text{induced}} = \omega M I_{\text{ga}} = \omega M V_{\text{inv}}/(\omega L_{f\_\text{ga}}) = M V_{\text{inv}}/(L_{f\_\text{ga}}). \tag{48}$$

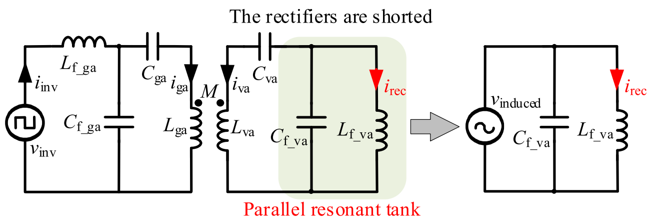

Fig. 11. Simplified equivalent circuit of the WPT system during mutual inductance identification mode.

v_{induced} is applied to the parallel resonant tank, and one can derive the following equation:

$$I_{\text{rec}} = V_{\text{induced}}/(\omega L_{f\_\text{va}}) = MV_{\text{inv}}/(\omega L_{f\_\text{ga}} L_{f\_\text{va}}). \quad (49)$$

According to (49), the voltage transformation between V_{bus} and V_{inv}, and the current transformation between I_{rec} and I_{s1}, the mathematical model for the mutual inductance identification can be obtained

$$\begin{aligned} M &= \omega L_{f\_\text{ga}} L_{f\_\text{va}} I_{\text{rec}}/(V_{\text{inv}}) \\ &= \pi \omega m_p n_s L_{f\_\text{ga}} L_{f\_\text{va}} I_{s1} / \left(2\sqrt{2} V_{\text{bus}}\right). \end{aligned} \quad (50)$$

The proposed mutual inductance identification implements once before the main power transfer, and it helps the system settle around the optimum point quickly. This method is based on the samplings of V_{bus} and I_{s1} which are also used for the control and protection system. Therefore, no additional hardware is required, making it a cost-effective solution.

B. Proposed PLOC

Although the number of inverters and rectifiers can be increased for power improvement, the two-inverter two-rectifier configuration is the fundamental cell of the DPAS-MIMR topology and the other configurations can be regarded as the superposition of several cells. Therefore, without the loss of generality, a DPAS-MIMR WPT system with two inverters and two rectifiers is used to intuitively illustrate the principle of the proposed simplified PLOC method.

The maximum resonant currents, $I_{\text{ga\_max}}$ and $I_{\text{va\_max}}$, are limited by the heat dissipation of the coils. When M is identified, one can obtain the minimum currents $I_{\text{ga\_min}}$ and $I_{\text{va\_min}}$ according to (37)

$$I_{\text{va\_min}} \approx P_o/(\omega M I_{\text{ga\_max}}) \quad (51)$$

$$I_{\text{ga\_min}} \approx P_o/(\omega M I_{\text{va\_max}}). \quad (52)$$

Once the desired output power P_o is determined, I_{ga} and I_{va} range in $[I_{\text{ga\_min}}, I_{\text{ga\_max}}]$ and $[I_{\text{va\_min}}, I_{\text{va\_max}}]$, respectively.

$I_{\text{ga\_max}}$ and $I_{\text{va\_max}}$ are obtained when $\alpha_1 = \alpha_2 = 0.5\pi$ and when $\beta_1 = \beta_2 = 0.5\pi$, respectively. I_{ga} and I_{va} can be re-expressed as

$$\begin{aligned} I_{\text{ga}} &= \frac{2\sqrt{2}(\sin\alpha_1 + \sin\alpha_2)\lambda V_{\text{bus\_max}}}{\pi X_{\text{ga}}} \\ &= \lambda(\sin\alpha_1 + \sin\alpha_2) I_{\text{ga\_max}} \end{aligned} \quad (53)$$

$$\begin{aligned} I_{\text{va}} &= \frac{2\sqrt{2}(\sin\beta_1 + \sin\beta_2)V_{\text{bat}}}{\pi X_{\text{va}}} \\ &= (\sin\beta_1 + \sin\beta_2) I_{\text{va\_max}}. \end{aligned} \quad (54)$$

TABLE I
DIFFERENT OPERATING MODES OF DIFFERENT G_{P}

Mode	λ	α_1	α_2	β_1	β_2	$I_{\text{ga}}/I_{\text{ga\_max}}$	$I_{\text{va}}/I_{\text{va\_max}}$	G_{p}
1	0.75-1	0.5π	0.5π	0.5π	0.5π	0.75-1	1	0.75-1
2	0.75-1	50%*	0.5π	0.5π	0.5π	0.5625-0.75	1	0.563-0.75
3	0.75-1	0	0.5π	0.5π	0.5π	0.375-0.5	1	0.375-0.5
4	0.75-1	50%*	0	0.5π	0.5π	0.1875-0.25	1	0.188-0.25
5	0.75-1	0.5π	0.5π	0	0.5π	0.75-1	0.5	0.375-0.5
6	0.75-1	50%*	0.5π	0	0.5π	0.5625-0.75	0.5	0.281-0.375
7	0.75-1	0	0.5π	0	0.5π	0.375-0.5	0.5	0.188-0.25
8	0.75-1	50%*	0	0	0.5π	0.1875-0.25	0.5	0.094-0.125

Note: * indicates that #1 inverter is switched to the half-bridge topology with a 50% duty cycle.

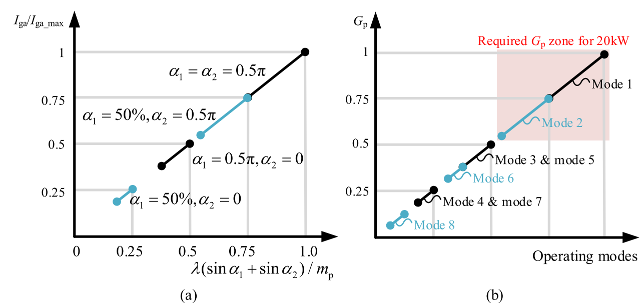

Fig. 12. I_{ga} and G_p with respect to α_1, α_2, β_1, β_2, and λ. (a) I_{ga}. (b) G_p.

Therefore, α_i, β_j, and λ can be used to optimize the current distribution to improve η as analyzed in Section III-B.

The three-phase Vienna PFC is used for the high-power WPT system. When it is applied by the 380-V grid, its bus voltage should be higher than 380 V × 1.414 × (1+20%) considering a ±20% fluctuation in grid voltage. Therefore, V_{bus} ranges from 640 V to 840 V, where λ belongs to [0.75, 1]. Thus, G_p can be regulated by λ when it falls within this range. The schematic and experimental results for a 22-kW Vienna are discussed in Section V-D and Appendix, respectively.

As for α_i, it equals 0.5 π or 0 to avoid hard switching. In addition, #1 inverter can be also switched to the half-bridge topology to expand the regulation range of G_p. To avoid secondary side synchronization, #2 rectifier only works at the diode rectification or the by-pass mode where β_j equals 0.5 π and 0, respectively.

Table I shows eight operating modes with different α_1, α_2, β_1, β_2, and λ. Furthermore, the relationship of I_{ga} and G_p with respect to these variables is plotted in Fig. 12. Although α_i and β_j are discrete, one can obtain a continuous G_p in most zones. According to Fig. 12, G_{p} almost covers the regulation range for the 20-kW VA. The G_p zones of modes 3 and 5 are the same as that of modes 4 and 7, respectively. It indicates that there exist

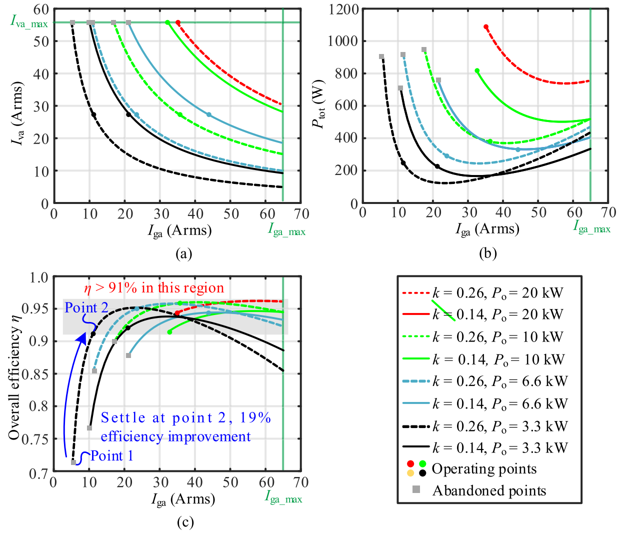

Fig. 13. Possible I_{ga} with coupling coefficient and power variations with proposed simplified PLOC method where $V_{\mathrm{bat}} = 800$ V, $L_{f\_\mathrm{ga}} = 20.6$ μH, $L_{f\_\mathrm{va}} = 28$ μH, $C_{f\_\mathrm{ga}} = 168$ nF, $C_{f\_\mathrm{va}} = 123.6$ nF, $C_{\mathrm{ga}} = 178.8$ nF, $C_{\mathrm{va}} = 30.9$ nF, $L_{\mathrm{ga}} = 39$ μH, $L_{\mathrm{va}} = 140$ μH, $R_{\mathrm{ga}} = 60$ mΩ, $R_{\mathrm{va}} = 200$ mΩ, $m = 2$, $n = 2$, $R_{\mathrm{p11}} = 40$ mΩ, $R_{p12} = 30$ mΩ, $R_{s11} = 40$ mΩ, $R_{s12} = 30$ mΩ, $R_{\mathrm{dson}} = 20$ mΩ, $V_f = 1.6$ V, $f = 85.5$ kHz. (a) I_{va}. (b) P_{tot}. (c) η.

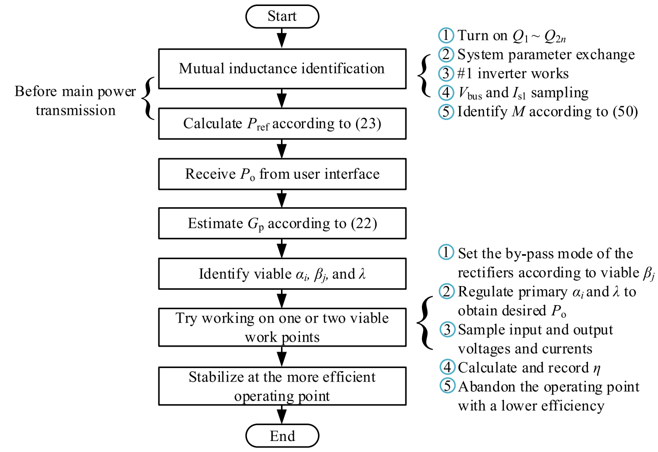

Fig. 14. Flowchart of the proposed simplified PLOC method.

two viable operating points. However, their overall efficiencies vary due to different current distributions.

To intuitively show the process of settling at the optimal point, Fig. 13 shows the operating points of a two-inverter two-rectifier WPT system with different P_{o} and k. There may be one or two viable operating points. As shown in Fig. 13(c), points 1 and 2 are marked for 3.3 kW at $k = 0.26$. I_{va} equals 55 Arms when $\beta_1 = \beta_2 = 0.5\pi$, and I_{va} equals 27.5 Arms when β_1 changes to 0. The corresponding I_{ga} is 5.5 and 11 Arms, respectively. Although both two operating points can achieve the desired P_o, P_{tot} and η vary a lot due to different current distributions. The proposed system can traverse these two viable operating points and distinguish the one with the higher efficiency. The operating points are marked in color, while abandoned points are marked in grey. As can be seen in Fig. 13(c), all the operating points fall within the dashed box. Although I_{va} is discrete and may not equal $I_{\mathrm{va\_opt}}$, the overall efficiencies are still greater than 91% under large variations in k and P_{o}, which theoretically verifies the validity of the proposed method.

Fig. 14 further summarizes the flowchart of the simplified PLOC method, which can be divided into six steps as follows.

Step 1: Mutual inductance identification. Before main power transmission, Q_1 - Q_{2n} are turned ON for overvoltage protection. The GA and VA establish the communication link through WiFi and exchange system parameters including resonant parameters, power rating, battery voltage range, etc. #1 inverter starts to work to provide a resonant voltage. Meanwhile, V_{bus} and I_{s1} are sampled. Then, the controllers identify M according to (50).

Step 2: Power reference calculation. According to the system parameters and the identified M, one can obtain P_{ref} according to (23).

Step 3: Controller receives the desired P_{o} from the user interface and then calculates the required G_p according to P_{ref} and (22).

Step 4: Controller identifies viable α_i, β_j, and λ according to the calculated G_{p} and (24).

Step 5: System tries to work on one or two viable operating modes and records their overall efficiencies. As shown in Fig. 12, there are two operating points for a given P_o in modes 3 & 5 and modes 4 & 7, and only one operating point in modes 1, 2, 6, and 8. The controllers receive the command of P_o, calculate the desired G_p, and then set the operating modes of all inverters and rectifiers. Because of the difference between the calculated G_p and the actual value, a proportional-integration control can be used to regulate α_i and λ slightly. When the system stabilizes, the input and output voltages and currents are sampled and the overall efficiency is calculated and recorded. If there exists only one viable operating point, the regulation is finished. Otherwise, the system turns to step 6. Since the charging power almost remains unchanged and the battery voltage increases slowly, the regulation time is enough.

Step 6: if there exist two viable operating points, the system compares their efficiencies and then stabilizes at the more efficient operating point.

The rectifiers operate at by-pass mode or diode rectification mode. Thus, all the MOSFETs on the VA can achieve soft switching. The inverters operate with 90°. The system operates at the resonant frequency which means the fundamental current and voltage of the inverter are in phase. Because of the high-order components of the inverting current, I_{pi} lags V_{pi} by some degrees which helps to achieve ZVS operation during different conditions.

The proposed PLOC method does not require high-frequency accurate synchronization on the VA which makes it easy-to-implemented. The system may not operate at the maximum efficiency point, but its overall efficiency is still higher than that using primary-side control. In addition, the charging time is long and the controller can settle around the optimal region after a quick calculation once the desired P_{o} is given. Although the parasitic resistances of the RIITs are slightly higher than that of

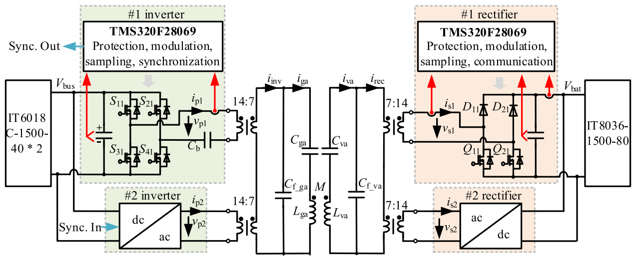

Fig. 15. Diagram of the 20-kW WPT prototype.

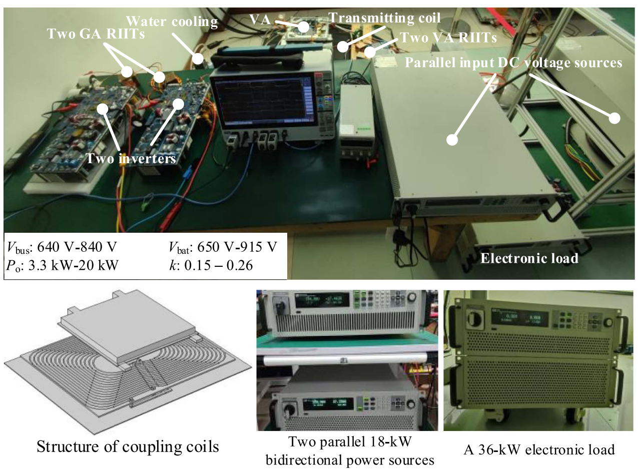

Fig. 16. 20-kW DPAS-MIMR *LCC-LCC* WPT prototype.

the conventional resonant inductors, the DPAS-MIMR topology with the proposed PLOC method can realize a wide range of voltage regulation under ZVS operation without adding additional BUCK/BOOST converters. Thus, the proposed system can have advantages in higher efficiency, higher power density, and lower cost than conventional WPT systems.

V. Experimental Verification

A 20-kW EV WPT system is built to verify the proposed DPAS-MIMR topology and the simplified PLOC method. Figs. 15 and 16 show the diagram and experimental prototype consisting of two parallel inverters and two parallel rectifiers. The key parameters of the system are given in Table II. The waveforms are obtained from Tektronix MSO56 5-BW-1000 six-channel oscilloscope. The input power is supplied by two IT6018C-1500–40 bidirectional power sources with a total power rating of 36 kW and the load is consumed by a 36-kW electronic load IT8036-1500–80. Independent digital signal processors (TMS320F28069) are used for the inverters and rectifiers. #1 inverter acts as the master inverter. The AC sides of the inverters and rectifiers are connected in series through four RIITs whose turns ratios are 14:7. Each RIIT consists of four EE70B ferrite magnetic cores whose size is 65 mm × 80 mm × 65 mm with a total weight of 1.28 kg. Their leakage inductances are 10.3, 10.4, 13.4, and 13.9 μH, respectively. Thus, the total leakage inductances of the GA and the VA are 20.7 and 27.3 μH, respectively. C3M0021120K and STTH75S12W are used as the

TABLE II
Key Parameters of the Proposed Prototype

Symbol	Parameter	Value
P_o	Output power	3.3 kW- 20 kW
V_{bat}	Output voltage	650 V-915 V
V_{bus}	Input voltage	640 V - 840 V
f	Operating frequency	85.5 kHz
C_b	DC blocking capacitor	5.0 µF
$C_{f\ ga}$	Filtering capacitor	168 nF
C_{ga}	Resonant capacitor	175 nF
L_{ga}	Self-inductance of Tx coil	39 µH
L_{va}	Self-inductance of Rx coil	140 µH
C_{va}	Resonant capacitor	30.7 nF
$C_{f\ va}$	Filtering capacitor	124.0 nF
m	Number of inverters	2
n	Number of rectifiers	2
m_p	Turns ratios of RIITs on the GA	14:7
n_s	Turns ratios of RIITs on the VA	14:7
$L_{f\ ga}$	Total leakage inductance of GA RIITs	20.7 µH
$L_{f\ va}$	Total leakage inductance of VA RIITs	27.3 µH
R_{ga}	Parasitic resistance of Tx coil	60 mΩ
R_{va}	Parasitic resistance of Rx coil	200 mΩ
R_{p12},R_{p11}	Primary resistances of GA transformers	40 mΩ
R_{p21},R_{p22}	Secondary resistances of GA transformers	30 mΩ
R_{s12},R_{s11}	Primary resistances of VA transformers	40 mΩ
R_{s21},R_{s22}	Secondary resistances of VA transformers	30 mΩ
R_{dson}	Parasitic resistance of the MOSFET	20 mΩ
V_f	Forward voltage of the MOSFET	1.6 V

MOSFETs and the diodes, respectively. The dc-blocking capacitor C_b is 5 μF. The filtering capacitances C_{f_ga} and C_{f_va} are 168 and 14.4 nF, respectively. The resonant capacitances C_{ga} and C_{va} are 175 and 30.6 nF, respectively. The OEM has strict requirements on the size and weight of the VA. To obtain a smaller VA and an improved misalignment tolerance caused by different parking positions, the *Tx* coil is larger than the Rx coil. The outer dimension of the *Tx* coil is 800 mm × 700 mm × 60 mm with a self-inductance of 39 μH to meet the dimensions specified in SAE J2954. The Rx coil has an outer dimension of 480 mm × 370 mm × 55 mm and a self-inductance of 140 μH, which is dictated by the power transmission requirements and the size constraints of the OEM. I_{ga_max} and I_{va_max} are 65 and 55 Arms, respectively. The system operates at 85.5 kHz. To satisfy the heat dissipation requirements, the current flowing through each MOSFET is set below 35 Arms. In addition, a forced air-cooling system is used on the GA, and a water-cooling system is used on the VA.

A. Mutual Inductance Identification

Mutual inductance is one of the most important parameters of the WPT system which are strongly related to the power transfer capability and efficiency. This section provides the experimental study of the proposed online mutual inductance identification method.

Fig. 17(a) shows the typical waveforms of the proposed method including V_{bus}, v_{p1}, v_{p2}, i_{s1}, and the identified M. #1 inverter works at the phase shift control with 90°. #2 inverter and two rectifiers operate at the by-pass mode where S_{32}, S_{42}, Q_{11}, Q_{21}, Q_{12}, and Q_{22} remain ON state all the time. V_{bus} remains at 640 V. I_{rec} is 9.05 Arms. Since i_{rec} is a sinusoidal waveform, one can use its amplitude to calculate the mutual inductance for

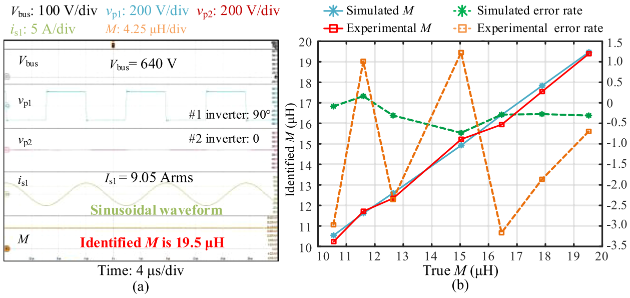

Fig. 17. Mutual inductance identification. (a) Typical waveforms. (b) Simulated and experimental identified M and error rates.

simplification. According to (50), the identified M is 19.4 μH corresponding to a real value of 19.5 μH.

Fig. 17(b) further shows the simulated and experimental identified M with respect to k at different coil positions. Since the rectifiers are short-circuited, the influence of power loss is very small. High accuracy can be obtained both in the experimental and simulated results. It can be seen that the identification errors of the simulated and experimental results are within 1% and 5% when M changes from 10.5 to 19.5 μH. Since the proposed PLOC method aims to operate in an optimized region, this experimental error is acceptable. This verifies the effectiveness of the proposed mutual inductance identification method in Section IV-A.

B. DPAS-MIMR Architecture With Primary-Side Control

Fig. 18 shows the experimental study of the proposed DPAS-MIMR architecture with primary-side control under different battery voltages and output power levels. Both β_1 and β_2 are 90°. The battery voltages in the left and right figures are 650 and 915 V, respectively. The power transfer distance is 21 cm and the coupling coefficient is 0.155. In Fig. 18(a), the output power is 3.3 kW. #1 inverter operates at half-bridge mode with a 50% duty cycle, and #2 inverter is bypassed. V_{bus} is regulated from 840 to 680 V to obtain the same power at different V_{bat}. In Fig. 18(b), the output power is increased to 6.6 kW. #1 inverter operates at full-bridge mode with a 90° phase angle. #2 inverter is still bypassed. V_{bus} decreases from 800 to 600 V when V_{bat} increases from 650 to 915 V. In Fig. 18(c), the expected output power is 10 kW. When V_{bat} is 650 V, #1 inverter operates at half-bridge mode with a 50% duty cycle and #2 inverter operates at full-bridge mode with a 90° phase angle. When V_{bat} increases to 915 V, V_{bus} decreases from 780 to 640 V. In Fig. 18(d), the expected output power increases to 20 kW. Both #1 and #2 inverters operate at full-bridge mode with 90° phase angles, where V_{bus} increases to 800 V. The measured output power increases from 14.4 to 19.3 kW when V_{bat} increases from 650 to 915 V. This phenomenon agrees well with Fig. 6(a). Small coefficients and low battery voltages can result in an output power of less than 20 kW. It can be observed from Fig. 18 that the zero-crossing point of the inverting current always lags the inverting voltage at the transitions. ZVS operation has been achieved by all MOSFETs.

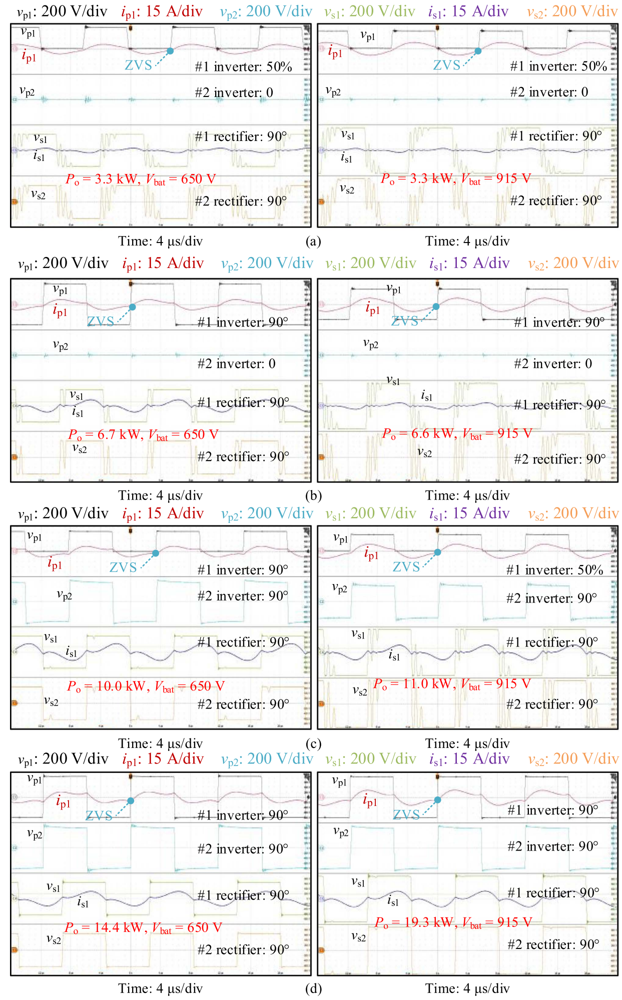

Fig. 18. Typical waveforms of the DPAS-MIMR architecture with primary-side control under different power levels and battery voltages where $k = 0.155$. (a) $P_o = 3.3$ kW, $V_{\mathrm{bat}} = 650$ V and 915 V. (b) $P_o = 6.6$ kW, $V_{\mathrm{bat}} = 650$ V, and 915 V. (c) $P_{\mathrm{o}} = 10$ kW, $V_{\mathrm{bat}} = 650$ V, and 915 V. (d) $P_o = 20$ kW and $V_{\mathrm{bat}} = 650$ V and 915 V.

Table III further shows the output power and overall efficiencies under different conditions. Although primary-side control can achieve different output power levels ranging from 3.3 to 20 kW at different battery voltages, the overall efficiency decreases significantly when operating at a low output power. When V_{bat} is 915 V and P_{o} is 3.3 kW, the measured overall efficiency η is only 78.6%. Thus, a better control method is required.

C. DPAS-MIMR Architecture With PLOC

Fig. 19 shows the experimental study of the proposed DPAS-MIMR architecture with a simplified PLOC method under different battery voltages, coupling coefficients, and output power levels. The battery voltages on the left and right figures are 650 and 915 V, respectively. The power transfer distance ranges from 16 cm to 21 cm where the coupling coefficient decreases from 0.26 to 0.155. In Fig. 19(a), P_{o} increases from 2.8 to 3.3 kW when V_{bat} increases from 650 to 915 V, respectively. #1 inverter

TABLE III
EXPERIMENTAL RESULTS OF DPAS-MIMR ARCHITECTURE WITH PRIMARY-SIDE CONTROL

k	V_{bat} (V)	V_{bus} (V)	α_1	α_2	β_1	β_2	P_o (kW)	η
	650	840	50%	0	90°	90°	3.3	84.3%
0.155	780	740	50%	0	90°	90°	3.3	82.0%
	915	680	50%	0	90°	90°	3.3	78.6%
	650	800	90°	0	90°	90°	6.7	89.9%
0.155	780	680	90°	0	90°	90°	6.6	88.6%
	915	600	90°	0	90°	90°	6.6	86.7%
	650	780	50%	90°	90°	90°	10.0	93.1%
0.155	780	680	50%	90°	90°	90°	10.2	92.1%
	915	640	50%	90°	90°	90°	11.0	91.0%
	650	800	90°	90°	90°	90°	14.4	93.6%
0.155	780	800	90°	90°	90°	90°	16.9	93.4%
	915	800	90°	90°	90°	90°	19.3	92.8%

TABLE IV
EXPERIMENTAL RESULTS OF DPAS-MIMR ARCHITECTURE WITH THE PLOC METHOD

k	V_{bat} (V)	V_{bus} (V)	α_1	α_2	β_1	β_2	P_o (kW)	η
	650	720	90°	0	90°	0	3.3	90.2%
0.155	780	640	90°	0	90°	0	3.4	90.3%
	915	640	90°	0	90°	0	3.8	90.3%
	650	840	50%	0	90°	0	2.8	88.9%
0.26	780	840	50%	0	90°	0	3.3	89.1%
	915	750	50%	0	90°	0	3.3	88.4%
	650	800	90°	0	90°	90°	6.7	89.9%
0.155	780	680	90°	0	90°	90°	6.6	88.6%
	915	700	50%	90°	90°	0	6.6	94.0%
	650	650	50%	90°	90°	0	6.6	95.1%
0.26	780	820	90°	0	90°	0	6.6	92.8%
	915	700	90°	0	90°	0	6.5	92.7%
	650	780	50%	90°	90°	90°	10.1	93.1%
0.155	780	680	50%	90°	90°	90°	10.2	92.1%
	915	640	50%	90°	90°	90°	11.1	91.0%
	650	740	90°	90°	90°	0	10.1	94.4%
0.26	780	820	50%	90°	90°	0	10.0	95.0%
	915	710	50%	90°	90°	0	10.1	95.1%
	650	800	90°	90°	90°	90°	14.4	93.6%
0.155	780	800	90°	90°	90°	90°	16.9	93.4%
	915	800	90°	90°	90°	90°	19.3	92.8%
	650	760	90°	90°	90°	90°	20.1	94.4%
0.26	780	640	90°	90°	90°	90°	20.1	94.0%
	915	740	50%	90°	90°	90°	20.1	93.0%

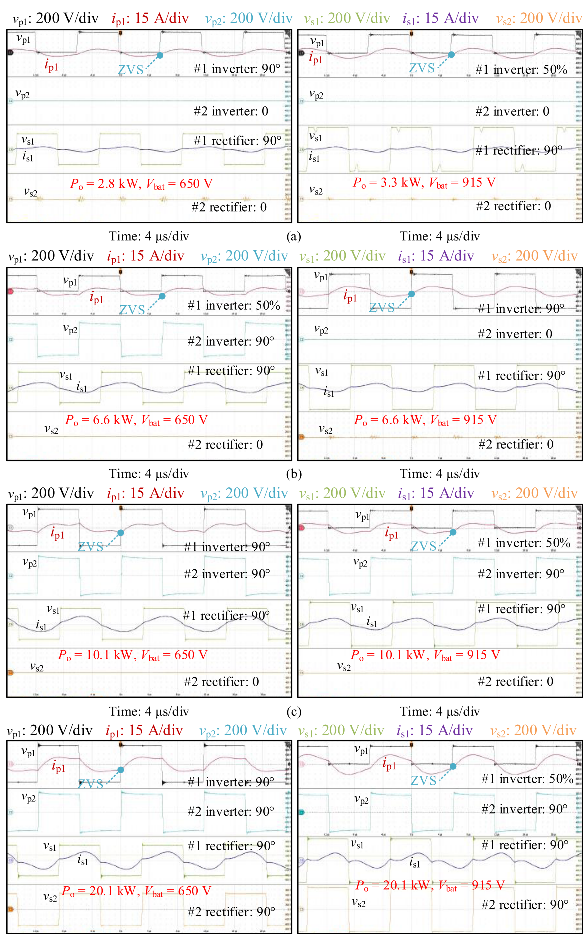

Fig. 19. Typical waveforms of the DPAS-MIMR architecture with simplified PLOC method at different power ratings and battery voltages where $k = 0.26$. (a) $P_o = 3.3$ kW and $V_{bat} = 650$ V and 915 V. (b) $P_o = 6.6$ kW and $V_{bat} = 650$ V and 915 V. (c) $P_o = 10$ kW and $V_{bat} = 650$ V and 915 V. (d) $P_o = 20$ kW and $V_{bat} = 650$ V and 915 V.

operates at half-bridge mode while V_{bus} decreases from 840 to 750 V. #2 inverter is bypassed. β_1 is 90° while β_2 is 0. In Fig. 19(b), the output power is increased to 6.6 kW. When V_{bat} is 650 V, #1 inverter operates at half-bridge mode with a 50% duty cycle and #2 inverter operates at full-bridge mode with a 90° phase angle. When V_{bat} increases to 915 V, #1 inverter is changed to full-bridge mode with a 90° phase angle, while #2 inverter is bypassed. β_1 is 90° while β_2 becomes 0. In Fig. 19(c), the output power is 10 kW. When V_{bat} is 650 V, both #1 and #2 inverters operate at full-bridge mode with 90° phase angles. When V_{bat} increases from 650 to 915 V, #1 inverter is changed to the half-bridge mode, while V_{bus} decreases from 740 to 710 V. β_1 is 90° while β_2 is 0. In Fig. 19(d), the output power is finally increased to 20 kW. The operating modes of the inverters almost remain the same as that in Fig. 19(c). However, both β_1 and β_2 are 90°. It can be observed from Fig. 19 that ZVS operation has been achieved under all conditions. Due to the by-pass mode of #2 rectifier, i_{s1} and i_{s2} can increase at low power levels. The voltage distortions of v_{s1} and v_{s2} disappear compared with Fig. 18, which can reduce the interferences and switching losses.

Table IV summarizes the transferred power and overall efficiencies under different conditions. P_o changes from 3.3 to 20 kW, V_{bat} increases from 650 to 915 V, and the coupling coefficient changes from 0.155 to 0.26. The maximum efficiency is 95.1%, and all the efficiencies are greater than 88% under three large parameter variations.

Fig. 20 compares the overall efficiencies of the proposed DPAS-MIMR architecture with primary-side control and PLOC method. Although the maximum efficiencies of the two methods are close, the minimum efficiencies differ significantly. Using the primary-side control, the minimum efficiency at 3.3 kW is only 78.6%. However, by using the proposed simplified PLOC, it approaches 88.4%, i.e., a 10% increase in efficiency is achieved.

The power losses of *Tx* and *Rx* coils are produced by the resonant currents. These currents are determined by the inverting and rectifying voltages which may not be strongly related to the output power. The power losses of the inverters and rectifiers only account for a small portion of the total power losses. For

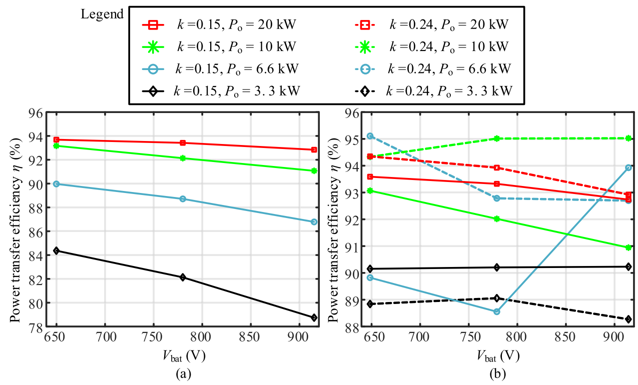

Fig. 20. Efficiency comparison between primary-side control and simplified PLOC at different k, V_{bat}, and P_o. (a) DPAS-MIMR architecture with primary-side control. (b) DPAS-MIMR architecture with PLOC.

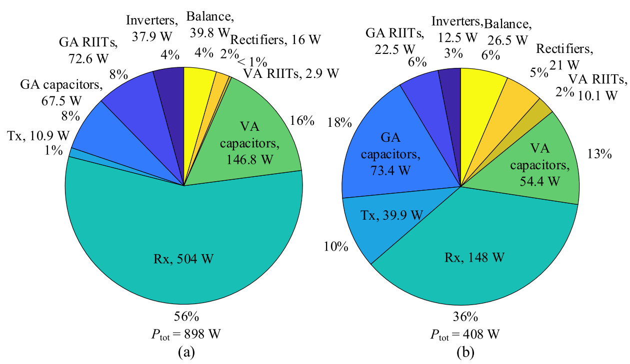

Fig. 21. Power loss breakdowns of a 20-kW WPT system operating at low power levels with two control methods. (a) $P_o = 3.3$ kW with diode rectification, $\eta = 78.6\%$. (b) $P_o = 3.8$ kW with the proposed PLOC method, $\eta = 90.3\%$.

example, the power losses of the *Rx* coil at 3.3 kW with a high V_{bat} may be higher than that at 20 kW with a low V_{bat}.

To investigate the power loss distribution intuitively, Fig. 21 shows the power loss breakdown of the 20-kW MIMR WPT system operating at low power levels with a coupling coefficient of 0.155 and a battery voltage of 915 V. In Fig. 21(a), a diode rectification is used and the output power is 3.3 kW. I_{va} is around 55 Arms and the power loss of the *Rx* coil and VA capacitors approaches 650 W. The total power loss is 898 W, corresponding to an efficiency of only 78.6%. Although the multi-inverter GA can provide a wide range of V_{inv}, the efficiency is still low at low power levels with a diode rectification. In Fig. 21(b), β_1 is 90° and β_2 is 0. I_{va} becomes 27.5 Arms. The power losses of the Rx coil and VA capacitors are decreased to only 202 W. By allocating I_{ga} and I_{va} properly, the efficiency is increased to 90.3%, where an 11.7% efficiency improvement is achieved. Only by combining the multi-rectifier topology with the proposed PLOC method can we obtain high efficiency against large system variations.

Table V compares the SAE J2954 interoperability class I system efficiency requirement and the dc/dc efficiency of the proposed system while operating at different power levels. Supposing the efficiency of the Vienna PFC is 97% whose measured results are presented in Appendix, the minimum system

TABLE V
COMPARISON BETWEEN THE CONVENTIONAL AND PROPOSED ARCHITECTURES

WPT class of tested VA	Minimum system efficiency requirement by SAE J2954: At centered position	Minimum system efficiency requirement by SAE J2954: In alignment tolerance area	DC/DC efficiency of the proposed system (In alignment tolerance area)
WPT1	80%	75%	88%
WPT2	82%	77%	88.5%
WPT3	85%	80%	91%
WPT4	/	/	92.5%

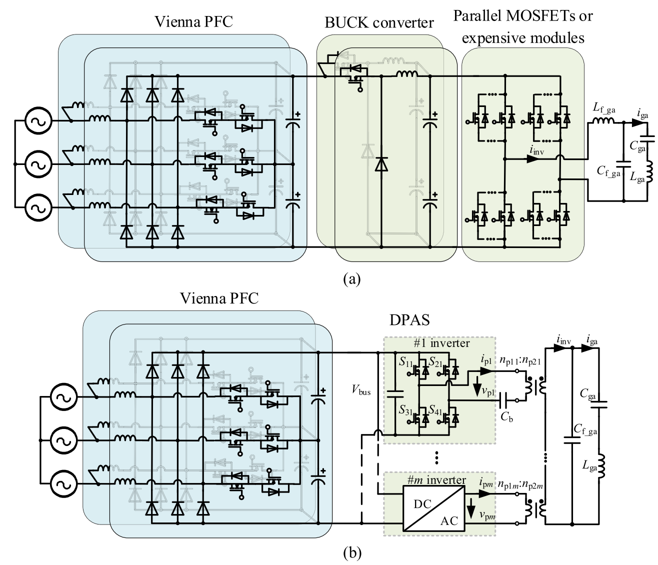

Fig. 22. Comparison between conventional GA and proposed GA for high-power WPT systems. (a) Conventional GA. (b) Proposed GA.

efficiency of the proposed system in the alignment tolerance area is at least 8% higher than the interoperability requirement.

These experiments and comparisons confirm the analysis in Section IV and validate the effectiveness of the proposed DPAS-MIMR architecture with a simplified PLOC method.

D. Comparison and Discussions

The GA and VA can have a symmetrical topology with dc/dc converters for power regulation. As shown in Fig. 22, the GA is used as an example to clearly show the advantages and disadvantages of the conventional and proposed architectures.

The differences between the BUCK converters and inverters of the two systems are given in Table VI. More components including 3m-4 driver circuits, m transformers, and a dc blocking capacitor are used in the proposed GA. However, two resonant inductors are removed. The current ratings of these two inductors increase with the increase in power level, as well as their size and cost. In addition, m diodes, m MOSFETs, m BUCK inductors, m filtering capacitors, and 1 voltage sampling and m current sampling circuits are removed. The size and cost of m transformers are just slightly higher than those of m buck inductors. In summary, fewer components are used in the proposed topology which contributes to a lower cost and a higher power density.

There are several advantages of the proposed DPAS-MIMR topology as given in Table VII. First, the modular architecture

TABLE VI
COMPARISON BETWEEN THE CONVENTIONAL TOPOLOGY AND PROPOSED TOPOLOGY

		GA with BUCK converters	Proposed topology
BUCK converters	Diodes	m	0
	MOSFETs	m	0
	Driver circuits	m	0
	Inductors	m	0
	Filtering capacitors	m	0
	Current sampling circuits	m	0
	Voltage sampling circuits	1	0
Inverters	MOSFETs	$4m$	$4m$
	Driver circuits	4	$4m$
	Filtering capacitors	m	m

Note: supposing that the rated power of a BUCK converter and a full bridge inverter is 10 kW.

TABLE VII
COMPARISON BETWEEN THE CONVENTIONAL AND PROPOSED ARCHITECTURES

	Conventional topology in Fig. 1	Proposed topology
Interoperability	Weak	Strong
Modular design	×	√
Resonant inductors	Required	No need
Front-end DC/DC converter	Required	No need
Back-end DC/DC converter	Alternative	No need
Efficiency optimization	Possible (with a back-end DC/DC converter)	√
Cost	High	Lower
Power density	Low	Higher
Overall efficiency	Low	Higher
Control complexity	Easy	Simplified
Transformers	No need	Required
DC blocking capacitor	No need	One

benefits the improvement of the high-power WPT system. Second, the interoperability of both GA and VA is strong which suits the industrialization requirements of the EV WPT system, especially in public charging applications. Third, wide-range power regulation can be achieved and the conventional front-end and back-end dc/dc converters are no longer required. The proposed system can have a higher power density and higher overall efficiency. Fourthly, the leakage inductances of the RIITs replace the conventional resonant inductors of the *LCC-LCC* circuit, which helps to reduce the cost and size. Finally, a simplified PLOC method based on accurate and easy-to-implemented mutual inductance identification is proposed, which achieves high efficiency at low power levels.

As for the power losses in the single full-bridge inverter in Fig. 22, they have the same value as that of the proposed topology under a given operating condition. The total numbers of MOSFETs used in the two systems are the same for the same power level as analyzed in Section II-D. Supposing that all MOSFETs achieve soft-switching ON, $P_{\text{single\_inverter}}$ and $P_{\text{multi\_inverters}}$ present the total conduction and simplified switching-off losses of the inverters used in the conventional and proposed systems as shown in (55) and (56). To ensure the same $I_{\text{ga\_max}}$ under different configurations, m_{p} can be the same as m, both of which are 2 in this article. Therefore, $P_{\text{single\_inverter}}$ is equal to $P_{\text{multi\_inverters}}$

$$P_{\text{single\_inverter}} = I_{\text{inv}}^2 \bullet 2\frac{R_{\text{dson}}}{m} + 0.5V_{\text{bus}}I_{\text{inv\_off}} \tag{55}$$

$$\begin{aligned} P_{\text{multi\_inverters}} &= \left(\frac{I_{\text{inv}}}{m_{\text{p}}}\right)^2 \bullet 2R_{\text{dson}} \bullet m + 0.5V_{\text{bus}}\frac{I_{\text{inv\_off}}}{m_{\text{p}}} \bullet m \\ &= P_{\text{single\_inverter}}. \end{aligned} \tag{56}$$

Admittedly, this proposed system is not perfect and there are some shortcomings in voltage gain and volume and loss of some devices. Each converter requires an additional transformer whose power losses may be a little larger than that of a resonant inductor with the same inductance. #1 inverter requires one dc blocking capacitor. As shown in Fig. 12, G_p is discontinuous and in some cases may lead to some power derating when interoperating with other devices. To compensate for these discontinuous regions, the duty cycle control or the phase shift control can be applied to the half-bridge and full-bridge converters, respectively. Besides, frequency shift control may be introduced as well.

VI. CONCLUSION

To improve the power and interoperability of the EV WPT systems, this article proposes a DPAS-MIMR architecture. Furthermore, a simplified mutual inductance identification-based PLOC method is proposed to minimize the power loss with large coupling coefficients and power variations. The conventional dc/dc regulators and resonant inductors of the *LCC-LCC* compensation circuit can be eliminated. Owing to the inherent characteristic of the proposed topology, power sharing among different converters can be realized without a complex closed-loop control. The system is efficient, cost-effective, compact, and has strong interoperability, which makes it suitable for the industrialization of EV WPT products. A two-inverter two-rectifier 20-kW WPT platform has been built where the maximum overall efficiency approaches 95%. The minimum efficiency is still higher than 88% when the output power, battery voltage, and coupling coefficient vary in [2.8 kW, 20 kW], [650 V, 915 V], and [0.155 to 0.26], respectively.

APPENDIX

The key waveforms and experimental results of a 22-kW Vienna PFC are presented in this part.

Fig. 23 shows the typical waveforms of the Vienna PFC operating at different power levels, which are recorded by a power analyzer PA5000H. v_a, v_b, and v_c are the input three-phase voltages. i_a, i_b, and i_c are the input three-phase currents. NVHL027N65S3F and B2D20120HC1 are used as the MOSFETs and diodes. In Fig. 23(a), the output voltage is 640 V and the output current is 15.6 A. The ac/dc conversion efficiency measured by the power analyzer is 97.5%. The total harmonic distortion of the currents is smaller than 3.6%. The dc-link voltage is stable and the input currents are sinusoidal. In Fig. 23(b), the output current is 33.6 A, corresponding to an input power of 22.1 kW. The ac/dc conversion efficiency becomes 97.1%. The total harmonic distortion of the currents is only 1.8%.

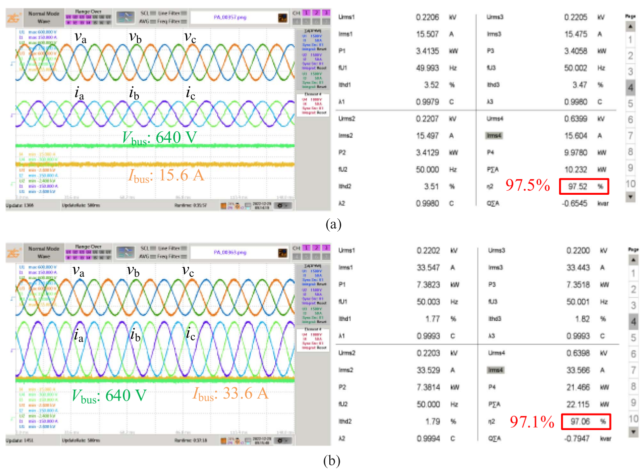

Fig. 23. Typical waveforms of a 22-kW Vienna PFC. (a) Input power is 10.3 kW. (b) Input power is 22.1 kW.

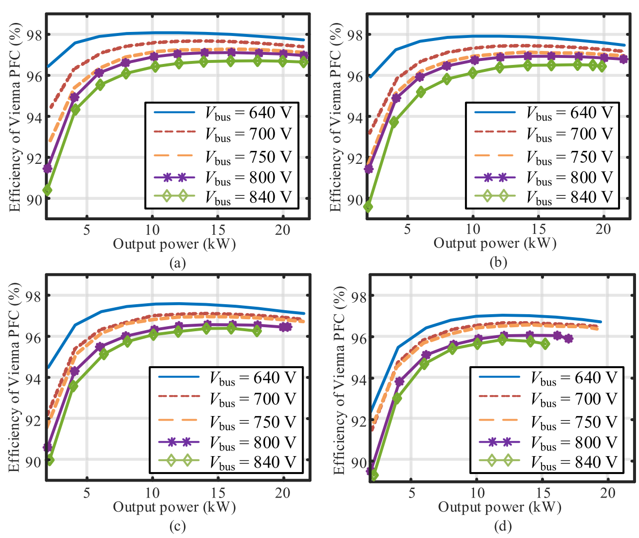

Fig. 24. Efficiencies of a 22-kW Vienna PFC with respect to grid voltages, bus voltages, and output power. (a) $V_a = V_b = V_c = 250$ Vrms. (b) $V_a = V_b = V_c = 240$ Vrms; (c) $V_a = V_b = V_c = 220$ Vrms. (d) $V_a = V_b = V_c = 200$ Vrms.

To validate the performance of the PFC under different conditions, Fig. 24 shows the ac/dc conversion efficiencies when the input voltages, dc-link voltages, and output power level range in [200 Vrms, 250 Vrms], [640 V, 840 V], and [2 kW, 22 kW], respectively. The input three-phase voltages in Fig. 24(a)–(d) are 250 Vrms, 240 Vrms, 220 Vrms, and 200 Vrms, respectively. The conversion efficiency increases quickly with the increase of the power level at first. It reaches the maximum efficiency around half loading. Then, it decreases slowly. For the same input voltages and output power, a higher V_{bus} requires a larger duty cycle of the PFC which results in a smaller conversion efficiency. The efficiency difference caused by different bus voltages is smaller than 2% when the power level is higher than 10 kW. A higher input three-phase voltages can also obtain a higher efficiency due to a smaller duty cycle. The maximum efficiency is higher than 98.0% when the input and output voltages are 250 Vrms and 640 V, respectively. All the efficiencies are higher than 94% when the output power is higher than 5 kW, after which the efficiency difference caused by parameter variations is small.

It can be found that the conversion efficiency is related to the input volages, output voltages, and output power levels. The optimization of the PFC itself under different conditions is complex. Therefore, the design of the PFC and dc/dc stage of the WPT system are conducted separately.

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