A Digital Twin System of Capacitive DC Bank Using Rogowski Coil to Monitor Individual Capacitors

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***Abstract*—The reliability of dc link capacitors is closely related to the operational safety of the whole power electronic system. To meet the application requirements, it is usually necessary to use a series or parallel structure of multiple capacitors to increase the capacity and withstand voltage, which also makes it difficult to monitor the individual capacitors in the capacitor bank. This article proposed a digital twin system for dc-link capacitor banks with PCB integrated Rogowski coils as sensors. The system uses highly integrated Rogowski coils to obtain the operating currents of individual capacitors in order to realize parameter correction of the digital twin system and ensure that the digital twin system can accurately reflect the electrothermal behavior of the dc-link capacitor bank. In addition, the effect of operating temperature on capacitor parameters is also considered, and the capacitor parameters and the operating temperature monitored by the digital twin system simultaneously are used to standardize the parameters. The standardized parameters are used as indicators to realize the health status assessment of each capacitor in the capacitor bank, which further provide an important basis for operation and maintenance.**

***Index Terms*—DC-link capacitor bank, digital twin system, health assessment, integrated Rogowski coils.**

I. Introduction

AS AN important role in the harmonic filtering, voltage regulation, energy storage, etc., the capacitive dc bank is the key component of the converter [1]. In the operation of the capacitive dc bank, the reliability of the dc link capacitors has rose concern [2], [3], [4], [5].

According to [6], the inside thermal stress that deteriorates the electrolyte and reduces the lifetime is one of the main failure mechanisms of the capacitors. The deteriorated electrolyte will increase the equivalent series resistance (ESR) of the capacitor and increase the inside temperature of the capacitor in return, which is a positive feedback process.

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The transient voltage shock and current shock are the other two main causes of the failure of the capacitor. A high voltage shock wills breakdown the electrolyte of the capacitor [7]. The huge current shock will transfer into the temperature shock of the capacitor, further leading to the operation of the vent or cracking at the terminal or the connections of the inside parts for the capacitor [8], [9].

To be aware of the operation condition status of the capacitor is an effective way to improve the reliability of the capacitor. Based on this idea, massive capacitor online monitoring method has been proposed [10], [11], [12], [13], [14], [15], [16], [17], [18].

But the online monitoring of capacitors still has following challenges.

1) Due to individual differences in the manufacturing process of capacitors and the spatial distribution of each capacitor in a dc bank, the electrical and thermal stresses of each capacitor in the bank are not uniformly distributed, and the degree of damage varies under the same operating hours. Even for capacitors of the same model and batch, the parameter characteristics between different capacitors are not completely the same.
2) The characteristic parameter values such as ESR and capacitance (C) of the capacitor will change with the change of the capacitor temperature. Therefore, it is not very accurate to judge the health status of the capacitor simply by only using the values of ESR and C. It is necessary to find a way to eliminate the influence of temperature.

The proposal of the digital twin concept provides a new solution for the condition monitoring of the capacitive dc bank. Digital twin is a digitally created virtual model of a physical entity, which can simulate the behavior of the physical entity in the real environment. The virtual model can be numerical function model [19], [20], [21], [22], [23], [24], probabilistic model [25], or simulations in the software [26]. As a digital representation of a real-world entity or system, digital twin plays the role of bridges connecting the physical world and the digital world [27], [28].

According to the data acquisition approach, the modeling of data twin can be classified into two types: the historical data based type and the real-time data based type. The historical data based digital twin model is trained from the historical data by the intelligent algorithm. For example, in a digital twin based evaluation method of the inverter-dominated power grid proposed in [19], the historical data is used to train the digital

twin model through a neural network, so that the model can accurately simulate the running state of the physical entity using the data collected by the phasor measurement unit. The real-time data based digital twin modeling established the interface algorithm for the resolution of the working conditions. In [20], a digital twin model of photovoltaic system has been designed based on the measurable characteristic output of PV energy conversion unit in real-time. An error residual evaluator has been designed as the interface algorithm. Condition monitoring and fault diagnosis of photovoltaic systems have been achieved by comparing the estimated input of the digital twin model with the measured output of the sensors. Similarly, applied Kalman filter as the interface algorithm, a thermal analysis digital twin model of a three-phase inverter has been built in [21]. [22] designed the digital twin model of Buck converter and Boost converter by using Bayesian Optimization on the basis of analyzing the variation law of output voltage and inductor current of dc–dc converter. [23], [24] proposed a modeling method of the digital twin of Buck converter based on particle swarm optimization algorithm. This method is used to monitor the working state of capacitors, MOSFETs and other devices in the circuit, and to judge deterioration degree of these devices. The influence of environmental temperature and other factors on the accuracy of the digital twin model is also considered.

In order to establish a capacitor bank digital twin model that can reflect the individual differences of capacitors, it is necessary to obtain the current data of each capacitor in the capacitor bank. However, traditional current sensors are difficult to meet this demand. The sensors used to measure the current of dc bank include sampling resistance [29], Hall current sensor [30], tunnel magneto resistance (TMR) [31], traditional Rogowski coil [32] and so on. However, limited by the volume, these sensors are usually only installed at the terminal of dc bank to measure the total current, and cannot measure the current of a single capacitor in the capacitor bank.

It is worth noting that the parameters of the capacitor have obvious temperature characteristics, and in the real operation of the capacitive dc bank, the electrical and thermal stress of the capacitor often couples with each other [33]. This type of characteristics will affect the accuracy of data twin models, but these characteristics have been rarely discussed.

This article aims to fill the above research gaps and proposes a digital twin system of dc link capacitor banks that can reflect individual differences of capacitors. The system uses PCB Rogowski coil to obtain the working current of each capacitor, and combines the recursive least squares (RLSs) algorithm to realize the parameter correction of digital twin. At the same time, the thermal network model is used to reflect the thermal behavior of the capacitor bank. Combining electro-thermal coupling algorithm and unscented particle filter (UPF) algorithm, a condition monitoring method considering the temperature characteristics of capacitor parameters is proposed, and the correctness of the algorithm is verified by experiments. The contributions of this article are as follows.

1) *Improvement of Capacitor Bank Digital Twin System*: The proposed digital twin model can reflect the individual differences of different capacitors in the capacitor bank. The digital twin model uses sensor data to update and correct the parameters of each capacitor and calculate the internal temperature, so that the digital twin can reflect the differences in parameters and temperature of each capacitor. Combined with the corresponding parameter values at different times and different temperatures in historical operating data, the temperature characteristic identification method based on UPF algorithm is used to reflect the temperature characteristic difference of each capacitor.
2) *Parameter Standardization*: A standardization method of capacitor bank health parameters based on digital twin monitoring results is proposed, which eliminates the influence of temperature on health assessment. The UPF algorithm is used to identify the temperature characteristics of each capacitor parameter, and the monitoring results are converted to a unified temperature to eliminate the influence of temperature on the health status indicators, so as to achieve more accurate health assessment.

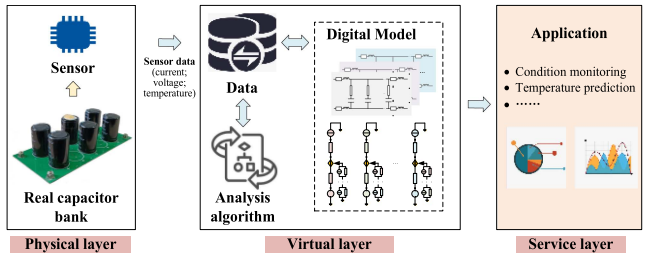

Fig. 1. Digital twin system structure.

The rest of this article is organized as follows: In Section II, the overall structure and design steps of the digital twin system of dc link capacitor bank are introduced. The digital twin system consists of physical layer, virtual layer, and service layer, which are introduced in detail in Sections III–V respectively. In Section VI, the monitoring effect of the digital twin system is verified through experiments. The conclusion of this article is drawn in Section VII.

II. General Structure of Digital Twin System

The digital twin system structure of dc-link capacitor bank established in this article is shown in Fig. 1. The data sampled by the sensor in the physical layer of the digital twin system is transmitted to the database in real-time. After being processed by the analysis algorithm in the virtual layer, the processing results are transmitted to the application layer to realize some applications related to status monitoring. The specific development of the digital twin system can be divided into the following six parts.

1) *Physical entity*: DC-link capacitor bank device.
2) *Sensors*: Sensors are used to sample the operating data of the dc-link capacitor bank.
3) Digital model: Equivalent model of the dc-link capacitor bank in the virtual layer, including the equivalent circuit model and the thermal network model.
4) *Database*: The database stores real-time operation data collected by sensors, historical operation data, digital twin

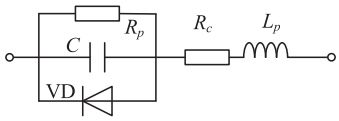

Fig. 2. Equivalent circuit of electrolytic capacitor.

parameter data, and condition monitoring results calculated by the analysis algorithm.

5) *Analysis Algorithm*: The analysis algorithms include the RLS-based digital twin parameter identification and calibration algorithm, and the UPF-based electro-thermal coupling health status assessment algorithm, in order to realize the calibration of the capacitor parameter degradation phenomenon and the condition monitoring of the capacitor bank.
6) *Applications*: The digital twin provides services such as capacitor bank operation monitoring, health status assessment, etc. and generates corresponding reports for technicians to study and provide reliability recommendations.

The details of each part are described in detail below.

III. Physical Layer of Digital Twin

A. Physical Entity

The dc-link capacitor bank is composed of several capacitors in series or parallel. Take the aluminum electrolytic capacitor as an example, the typical structure diagram of aluminum electrolytic capacitor mainly includes lead wire, aluminum pad lead wire, cathode aluminum foil, dielectric and electrolyte.

The equivalent circuit model of electrolytic capacitor is shown in Fig. 2, where R_p represents the dielectric (metal oxide film) loss resistance, L_p represents the lead parasitic inductance, diode VD reflects the unidirectional conductivity of the capacitance of aluminum oxide dielectric *PN* junction effect, C represents the ideal capacitance, and R_C represents the ESR of electrolytic capacitor. Because the working frequency of aluminum electrolytic capacitor is usually low, the influence of parasitic inductance L_p can be ignored; in addition, the value of R_p is much smaller than that of R_C, so its equivalent circuit can be simplified as a model of ideal capacitor C in series with ESR R_C.

In fact, R_C and C are not fixed, and their values are affected by frequency and temperature [31].

B. Sensor

Using the digital twin model to realize the state monitoring of capacitors requires the operating voltage, current and ambient temperature data of capacitors.

The dc-link capacitor bank is usually a parallel structure of multiple capacitors, and the voltage of each capacitor is the same. Therefore, the voltage of each capacitor can be obtained by measuring the overall voltage of the dc link. The dc bank usually has terminals that connected to the dc link input, which can be applied as the measurement terminal of Hall voltage sensors.

Temperature sensors are used to measure the case temperature and ambient temperature of the dc-link capacitor bank, and an SMD T-type thermocouple is used as the temperature sensor in this article.

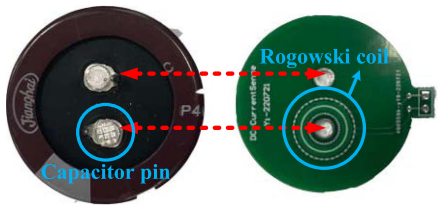

Fig. 3. PCB-type Rogowski coil.

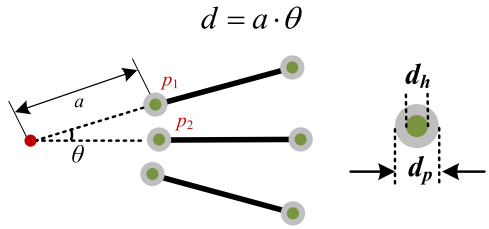

Fig. 4. Illustration of the Rogowski coil turns calculation.

The measurement of individual current of capacitors in capacitor banks is one of the difficulties to be overcome, since the traditional Hall current sensor is difficult to meet the measurement requirements in terms of size. A PCB Rogowski coil installed on the capacitor pin is designed as a current sensor, as shown in Fig. 3, to realize the acquisition of the operating current of each capacitor.

The output voltage expression of Rogowski coil is

$$V = N_r \frac{\mu h}{2\pi} \cdot \ln \frac{D_b}{D_a} \cdot \frac{dI}{dt} \tag{1}$$

where μ is the relative permeability, which can be approximated to the vacuum permeability; N is the number of coil turns; h represents the height of the nonmagnetic framework, D_a and D_b represent the outer and inner diameters of the non-magnetic framework of the coil, respectively, and I represents the instantaneous current passing through the coil.

In order to improve the anti-interference ability of Rogowski coil, this article adopts fishbone winding mode and adds shielding layer to the outermost layer of PCB to improve the signal-to-noise ratio of Rogowski coil. In addition to the winding method, the factors that need to be considered when designing the Rogowski coil include the number of turns, inner diameter, and outer diameter of the Rogowski coil. It can be seen from (1) that in order to improve the output voltage of the Rogowski coil, we hope that the number of turns of the Rogowski coil is as much as possible, but for a limited PCB area, too many turns means that the distance between turns is very small, resulting in inter-turn insulation is difficult to guarantee. Therefore, it is necessary to design the winding turns reasonably.

Fig. 4 is a schematic diagram of winding parameter calculation of PCB integrated Rogowski coil. The diagram is shown as the top view of the winding part of the coil, d_p is the diameter of the pad, d_h is the diameter of the via hole, a is the inner diameter of the coil, and θ is the angle between the two adjacent winding

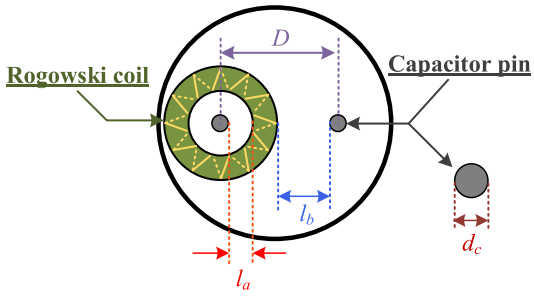

Fig. 5. Illustration of the safe distance for insulation.

lines. The distance d between p_1 and p_2 can be approximated as

$$d = a \cdot \theta. \tag{2}$$

According to the Texas Instruments PCB Rogowski coil design requirements [34], the distance between the two vias needs to be at least three times the width of the pad. The minimum distance between the two holes is

$$d_{\min} = 3\left(d_p - d_h\right). \tag{3}$$

Considering the limitation of the safe space between windings, for the Rogowski coil with inner diameter a, the maximum number of turns of the winding cannot exceed the limit value $N_{\max}$, as follows:

$$N_{\max} = \frac{2\pi a}{d_{\min}}. \tag{4}$$

It is not difficult to see that the number of windings N is limited by the inner diameter a. However, on the one hand, too large a will cause the Rogowski coil to occupy too much space on the dc link. On the other hand, if the size of the Rogowski coil is too large, the limitation of the distance between the positive and negative terminals of the capacitor will cause it to be unable to adapt [35]. In addition, as shown in Fig. 5 the insulation requirements between the coil and the capacitor terminal are also required

$$\begin{cases} l_a = a - 0.5d_c - 0.5d_p > l_{\lim a} \\ l_b = D - a - 0.5d_c - 0.5d_p > l_{\lim b} \end{cases}. \tag{5}$$

D is the distance between the positive and negative terminals of capacitor. d_c is the diameter of capacitor pin. $l_{\lim a}$ and $l_{\lim b}$ represent the minimum safe distance between the low voltage side (capacitor negative) and the high voltage side (capacitor positive), which can be obtained from the standard in [36].

The frequency characteristics of the designed Rogowski coil are shown in the Fig. 6. The measured current can be restored by amplifying and integrating the output voltage of Rogowski coil with an amplifier and an integrator. The integration circuit of Rogowski coil are shown in Fig. 7. The integral circuit adopts an improved noninverting active integral circuit. Because the gain and dc drift of the traditional in-phase integration circuit are very large at very low frequencies, the noise at low frequencies is amplified. Therefore, a resistor R_f is connected in parallel to the two sections of the integral capacitor to suppress this phenomenon. The integrated signal is input to the signal amplification circuit, and finally the current signal is restored.

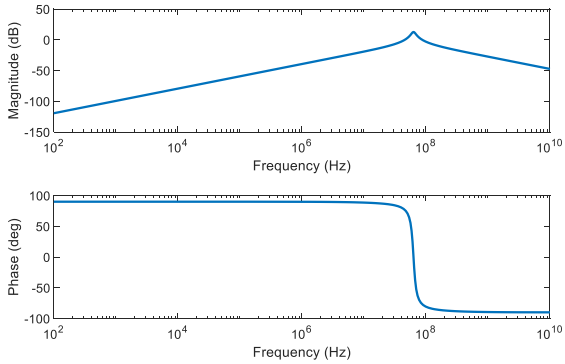

Fig. 6. Frequency characteristics of the designed Rogowski coil.

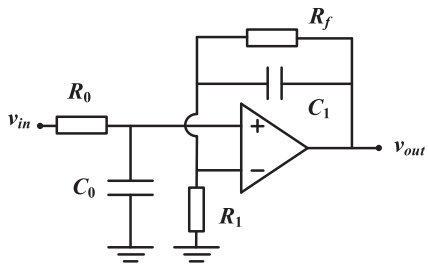

Fig. 7. Integration circuit circuit of Rogowski coil.

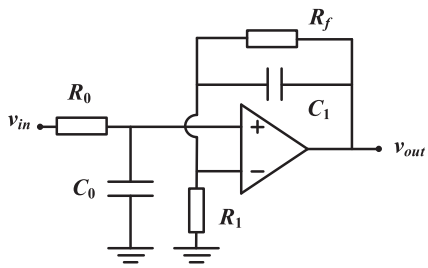

Fig. 8. Circuit model of DC link capacitor bank.

IV. Virtual Layer of Digital Twin

A. Digital Model

Considering that the capacitor parameters have temperature characteristics, the digital twin model established in this article contains a circuit model and a thermal network model.

The equivalent circuit of electrolytic capacitor can be further simplified to a series circuit with ideal capacitance and ESR. This results in the equivalent circuit model of a dc link capacitor bank consisting of multiple capacitors connected in parallel as shown in Fig. 8, where R_{Ci} and C_i represent the ESR and capacitance of capacitor i, respectively.

Using circuit theory to analyze the circuit in Fig. 8, the current distribution in the capacitor bank can be obtained by (6), where $Z_{ci} = R_{Ci} + 1/j\omega C_i$

$$I_{ci}(j\omega) = \frac{1}{Z_{ci}} \cdot V_{ci}(j\omega). \tag{6}$$

The capacitance and ESR of a capacitor change as the internal temperature of the capacitor changes. In order to reflect this characteristic of the capacitor in the digital twin model, a thermal

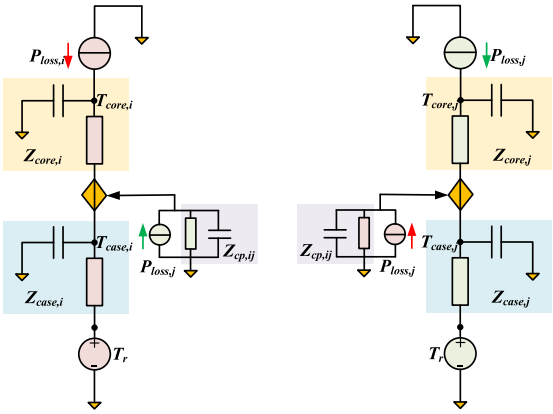

Fig. 9. Capacitor bank coupling thermal model.

network model is needed to obtain the internal temperature of the capacitor.

For the thermal network of the capacitor bank, according to the superposition theorem, the model of the aggregate thermal network considering the self-generated heat and thermal coupling effect of the capacitor bank can be obtained. Taking the two capacitors *i* and *j* in the capacitor bank as an example, the thermal network model is shown in Fig. 9. In this model, the thermal coupling phenomenon between capacitors is characterized by a controlled voltage source. $R_{cp,ij}$ and $C_{cp,ij}$ denotes the coupling thermal resistance and thermal capacity between the two capacitors. $R_{\mathrm{core},i}$ and $R_{\mathrm{case},i}$ denote the thermal resistance from the inner core to the case of capacitor *i* and the thermal resistance from the case to the external environment, respectively. $C_{\mathrm{core},i}$ and $C_{\mathrm{case},i}$ denote the thermal capacity from the inner core to the case of capacitor *i* and the thermal capacity from the case to the external environment, respectively. $T_{\mathrm{core},i}$, $T_{\mathrm{case},i}$, and T_a denote the internal temperature, the case temperature, and the ambient temperature of the capacitor *i*, respectively. $P_{\mathrm{loss},i}$ is the power loss on capacitor *i*.

The internal temperature of capacitor *i* can be calculated as

$$T_{\mathrm{case},i} = R_{\mathrm{case},i}[1 - e^{-t/R_{\mathrm{case},i}C_{\mathrm{case},i}}]P_{\mathrm{loss},i} + \sum_{j=1,j\neq i}^{N-1} R_{cp,i}[1 - e^{-t/R_{cp,i}C_{cp,i}}]P_{\mathrm{loss},j} + T_{a,i} \quad (7)$$

$$T_{\mathrm{core},i} = R_{\mathrm{core},i}[1 - e^{-t/R_{\mathrm{core},i}C_{\mathrm{core},i}}]P_{\mathrm{loss},i} + T_{\mathrm{case},i}. \quad (8)$$

The following describes how to obtain the initial parameters of the above model.

Because the equivalent circuit parameters have frequency characteristics and temperature characteristics, it is necessary to measure the equivalent circuit parameters of capacitors at different frequencies and temperatures. Put the capacitor into the thermostat, lead the pin out of the thermostat through the wire, and connect it with the LCR measuring instrument. The LCR measuring instrument controls the measurement frequency, the thermostat controls the measurement temperature, and measures the R_C and C values at different frequencies and temperatures, which are recorded as R_C (f, T_{core}) and C (f, T_{core}) and stored in the parameter database.

Different from the equivalent circuit parameters, the thermal impedance parameters in the thermal network cannot be directly measured by the instrument. In this article, the thermal network model parameters were obtained by the method introduced in the [37] using the temperature response test.

B. Database

The database of the digital twin model stores different kinds of data, include the following.

1) The operating voltage, current, ambient temperature and other data of the capacitor bank sampled in real-time by sensors.
2) The historical data of the parameters of the digital model, including the capacitance value, ESR, thermal impedance and other data at different times, of which the data at the initial time can be measured offline, and the data at different subsequent times can be calculated through the online parameter update algorithm.
3) The output data of the digital twin, including the operating temperature monitoring and prediction results of each capacitor, and the health state parameters after temperature standardization and so on.

C. Analysis Algorithm

During the long-term operation of the capacitor, due to the evaporation of electrolyte caused by heat generation, the ESR R_C increases and the capacitance C decreases as the contact area between the electrolyte and the oxide layer decreases.

At this time, if the previous parameters are still used as the digital twin parameters, the digital twin system will have a large error and cannot accurately reflect the operating state of the dc-link capacitor bank. Therefore, when the digital twin system deviates from the dc-link capacitor bank, the digital twin parameters need to be updated and calibrated.

During the synchronous operation of the digital twin system and the actual circuit of the dc-link capacitor bank, the input matrix $\mathbf{E_k}$ and the operation state matrix $\mathbf{X_k}$ of the dc-link capacitor bank are constructed using the voltage, current and temperature data of the capacitor bank monitored by the sensor; Input $\mathbf{E_k}$ into the digital model to obtain the state matrix $\mathbf{Y_k}$ of the digital model under the same operating conditions. $\mathbf{E_k}$, $\mathbf{X_k}$ and $\mathbf{Y_k}$ are defined as

$$\mathbf{E_k} = [u_c \quad T_a]_k^T \quad (9)$$

$$\mathbf{X_k} = [i_{c1}\ i_{c2}\cdots i_{cN}\ T_{\mathrm{core},1}\ T_{\mathrm{core},2}\cdots T_{\mathrm{core},N}]_k^T \quad (10)$$

$$\mathbf{Y_k} = [i_{c1^*}\ i_{c2^*}\cdots i_{cN^*}\ T_{\mathrm{core},1^*}\ T_{\mathrm{core},2^*}\cdots T_{\mathrm{core},N^*}]_k^T \quad (11)$$

where u_c is the operating voltage of the dc link; T_a is the ambient temperature; $i_{c1}, i_{c2}\cdots i_{cN}$ and $T_{\mathrm{core},1}, T_{\mathrm{core},2}\cdots T_{\mathrm{core},N}$ respectively represent the current and case temperature of each capacitor in the capacitor bank; $i_{c1^*}, i_{c2^*}\cdots i_{cN^*}$ and $T_{\mathrm{core},1^*}, T_{\mathrm{core},2^*}\cdots T_{\mathrm{core},N^*}$, respectively, represent the current

and case temperature of each capacitor in the digital model, and the subscript k represents the kth sampling.

Calculate the error between the state data matrix $\mathbf{X_k}$ and $\mathbf{Y_k}$. When the error between the two is less than the error determination threshold, that is, if condition (12) is met, it can be considered that the reflection of the digital model to the physical device is accurate within the tolerance error range. If the condition (12) is not met, the parameters of the digital model need to be corrected

$$|\mathbf{X_k} - \mathbf{Y_k}| < \varepsilon. \tag{12}$$

As C and R_C of capacitor are related to frequency, fast Fourier transform is used to obtain the working frequency of capacitor bank and separate the corresponding frequency component from the voltage and current data of capacitor bank collected by sensor. Then, according to the voltage and current data of different frequencies, the RLS algorithm is used to identify the parameters of C and ESR.

By bilinear transformation of (2), we can get

$$u_{i,k} - u_{i,k-1} = \left(\frac{T_s}{2C_i} + R_{ci}\right) i_{i,k} + \left(\frac{T_s}{2C_i} - R_{ci}\right) i_{i,k-1} + e_k \tag{13}$$

T_s is the sampling interval, the subscript k represents the kth sampled data, and e_k is the error signal.

Write in the form of least squares

$$y_k = \varphi_k^T \cdot \theta + e_k \tag{14}$$

$$\begin{cases} y_k = u_{i,k} - u_{i,k-1},\ \varphi_k^T = [i_{i,k} \quad i_{i,k-1}]^T \\ \theta = [T_s/(2C_i) + R_{Ci} \quad T_s/(2C_i) - R_{Ci}] \end{cases}. \tag{15}$$

The objective of RLS is to minimize the error cost function:

$$J(\theta) = \sum_k e_k^2 = \sum_k [y_k - \varphi_k^T \theta]. \tag{16}$$

The recursive formula of RLS can be solved as follows:

$$\begin{cases} \hat{\theta}_k = \hat{\theta}_{k-1} + K_k[y_k - \varphi_k^T \hat{\theta}_{k-1}] \\ K_k = P_{k-1}\varphi_k / \left[1 + \varphi_k^T P_{k-1} \varphi_k\right] \\ P_k = [I - K_k \varphi_k^T] P_{k-1} \end{cases} \tag{17}$$

where $\hat{\theta}_k$is the kth parameter identification result, K_k is the kth correction gain vector, P_k is the kth error covariance matrix.

When the parameters of the capacitor change, RLS will track this change. Input the sampled capacitor voltage and current data to solve (17), then the parameter collection θ which contains the information of R_C and C can be obtained. With the continuous sampling of the sensors, k is constantly updated, and parameter collection θ are also updated. Fig. 10 shows the parameter updating process of the RLS algorithm when the temperature of the capacitor changes from 25 °C to 30 °C. It can be seen that RLS can accurately identify the parameter changes of the capacitor.

After solving C_i and R_{Ci} with (17), mark the operating frequency and internal temperature of the capacitor, namely C_i (f, $T_{\text{core},i}$) and R_{Ci} (f, $T_{\text{core},i}$), and replace the original numerical twin parameters C_i (f, $T_{\text{core},i}$) and R_{Ci} (f, $T_{\text{core},i}$) in the database.

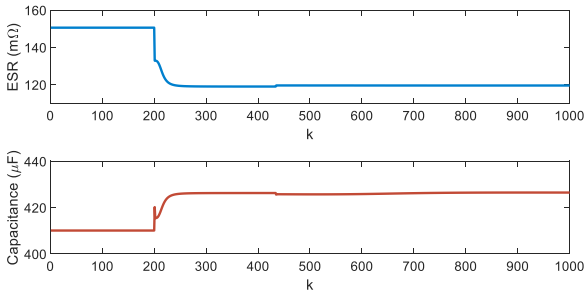

Fig. 10. Parameter update process.

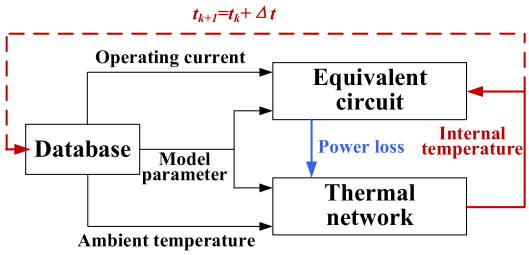

Fig. 11. Temperature monitoring method based on digital twins.

V. Service Layer of Digital Twin

A. Internal Operating Temperature Monitoring

The ESR of the capacitor has a temperature characteristic, therefore, during the operation of the capacitor, the change of the internal operating temperature of the capacitor will cause the change of power loss, namely

$$P_{\text{loss},i}(T_{\text{core},i}) = \sum_{m=1}^{\infty} I_{ci,m}^2 R_{ci}(mf_0, T_{\text{core},i}) \tag{18}$$

where m is the harmonic order and f_0 is the fundamental frequency.

According to (8), it can be seen that the internal temperature of the capacitor also changes with the change of the power loss. The combination of (8) and (18) can be found that the power loss of the capacitor and the internal temperature have a mutual coupling relationship. Therefore, in order to accurately monitor the operating temperature of each capacitor, the loss calculated by the circuit model needs to be injected into the thermal network model, and the internal temperature of each capacitor calculated by the thermal network model needs to be fed back to the circuit model to update the loss calculation results, so as to realize the bidirectional coupling of loss and internal operation temperature calculation. The specific process is shown in Fig. 11.

B. Health Assessment

Research has been shown that the relationship between R_C and temperature is approximately a double exponential relationship, while the relationship between C and temperature is linear [31], as shown in

$$R_C(f, T_{\text{core}}) = R_{C\_25°\text{C}}(f) \cdot [a \exp(bT_{\text{core}}) + c \exp(dT_{\text{core}})] \tag{19}$$

$$C\left(f, T_{\text{core}}\right) = C_{25^\circ\text{C}}(f) \cdot \left(\gamma T_{\text{core}} + \lambda\right) \tag{20}$$

where $R_{C\_25^\circ C}(f)$ and $C_{25^\circ C}(f)$ are the ESR and capacitance of the capacitor under frequency f at 25 °C, and a, b, c, d, γ, and λ are the model parameters.

If the characteristic parameters obtained from monitoring at a certain moment are directly used to assess the health condition of a capacitor without considering the effect of temperature, there is a possibility that the operating temperature of the capacitor may lead to deviation of the characteristic parameters and an incorrect assessment of the health condition of the capacitor. Therefore, when assessing the health status of a capacitor using R_C and C as degraded characteristic parameters, it is necessary to standardize the degraded characteristic parameters with the operating temperature, so as to eliminate the influence of the operating temperature for an accurate health assessment. Fortunately, the internal temperature of individual capacitors in a capacitor bank can be directly monitored using the digital twin model constructed in this article, without the need for additional temperature sensors.

Although the characteristic parameters of components of the same specification and model change with temperature in a consistent manner, the characteristic parameters of components and model parameters of temperature are not fixed values due to individual differences. Moreover, there are factors such as noise interference in the measurement process. In order to accurately evaluate the health status of capacitors, the state transition equation and measurement equation considering noise factor are constructed, and the UPF algorithm is used to solve them. In this article, 25 °C is taken as the standardized temperature, and the measurement equation of standardized characteristic parameter value at time k is

$$R_{\text{C\_25}^\circ\text{C}}\left(f, T_{\text{core},k}\right) = \frac{R_C\left(f, T_{\text{core},k}\right)}{a_k \exp\left(b_k T_{\text{core},k}\right) + c_k \exp\left(d_k T_{\text{core},k}\right)} + v_{R_C} \tag{21}$$

$$C_{25^\circ\text{C}}\left(f, T_{\text{core},k}\right) = \frac{C\left(f, T_{\text{core}}\right)}{\gamma_k T_{\text{core},k} + \lambda_k} + v_{\text{C}}. \tag{22}$$

The state transfer equation is

$$\begin{cases} a_k = a_{k-1} + e_a & b_k = b_{k-1} + e_b \quad c_k = c_{k-1} + e_c \\ d_k = d_{k-1} + e_d & \gamma_k = \gamma_{k-1} + e_\gamma \quad \lambda_k = \lambda_{k-1} + e_\lambda \end{cases} \tag{23}$$

where v_{R_C} and v_C are measurement noises, and e are process noises, which obey normal distribution.

After the standardized degradation characteristic parameters are obtained, the current health status of the capacitor can be evaluated. It is generally believed that when the capacitance value of the capacitor decreases to 80% of the initial value, or the ESR increases to twice the initial value, the capacitor will lose its ability to work normally. Thus, the health degree (HD) of capacitor can be defined

$$\text{HD}_{R_C} = \left[\left(2 \cdot R_{C0\_25^\circ\text{C}} - R_{C\_25^\circ\text{C}}\right) / R_{C0\_25^\circ\text{C}}\right] \times 100\% \tag{24}$$

$$\text{HD}_C = \left[1 - \left(C_{0\_25^\circ\text{C}} - C_{25^\circ\text{C}}\right) / \left(20\% \cdot C_{0\_25^\circ\text{C}}\right)\right] \times 100\% \tag{25}$$

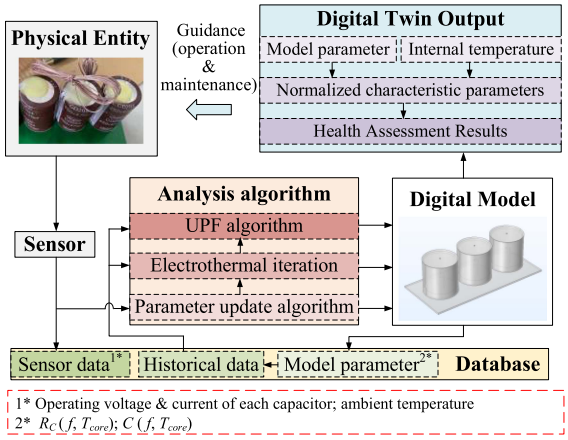

Fig. 12. Health assessment of capacitor banks based on digital twins.

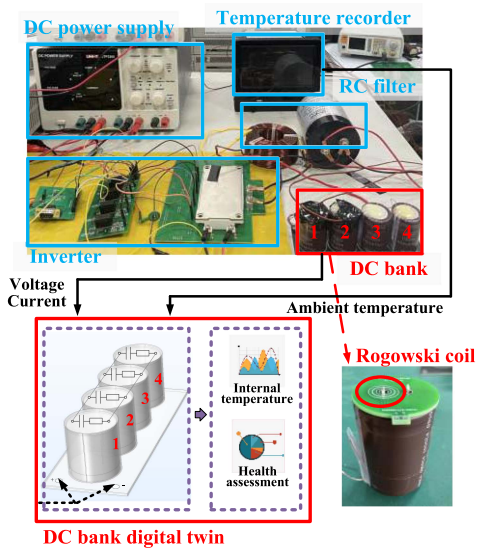

Fig. 13. Experimental setup.

where $R_{C0\_25^\circ C}$ and $R_{0\_25^\circ C}$ represents the initial value of R_C and C at 25 °C.

When HD = 100%, it indicates that the capacitor is completely healthy without parameter degradation; When HD = 0, it means that the capacitor has lost its ability to work normally. At this time, a new capacitor needs to be replaced in time to avoid more serious system failures.

To sum up, based on the method of dynamic updating model parameters by UPF, the estimated values of characteristic parameters at 25 °C can be accurately obtained, so as to assess the health status of devices at the current time, as shown in Fig. 12.

VI. Verification

This article takes the dc link capacitor bank in single-phase inverter as the experimental object, and verifies the condition monitoring method based on digital twins. The experimental apparatus is shown in Fig. 13. The switching frequency is 1000 Hz, fundamental frequency is 50 Hz, dc voltage is 50 V and load is 15 Ω. The dc-link capacitor bank is composed of four capacitors in parallel, and the CD294 electrolytic capacitor produced by

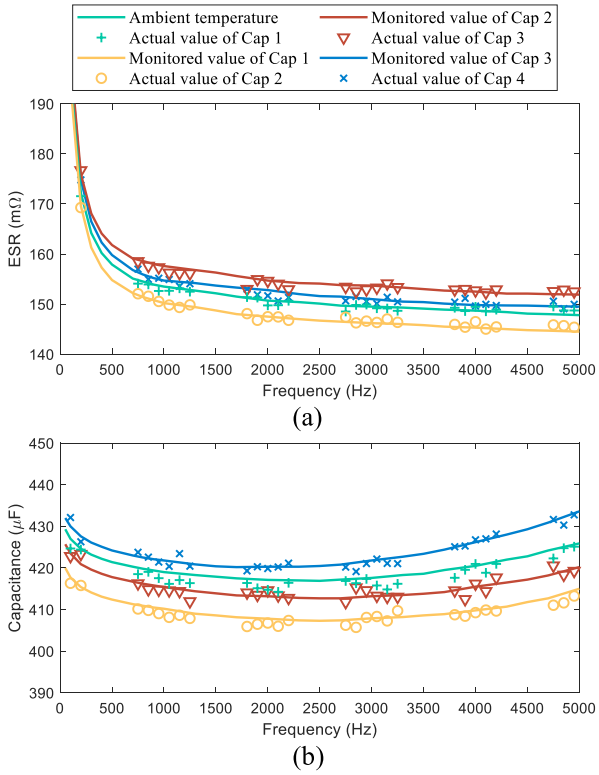

Fig. 14. Parameter update results.

Jianghai is used in the experiment. In order to obtain the thermal network parameters of the capacitor and verify the accuracy of the temperature detection results, we contacted the capacitor manufacturer to customize and produce some capacitors with a thermocouple inside the capacitor to monitor the actual internal temperature of the capacitor.

The parameter update results of each capacitor are shown in Fig. 14. It can be seen that the digital twin model established in this article can accurately update the parameters and reflect the frequency characteristics of the parameters.

During the operation of the capacitor bank, the digital twin model is used to obtain the operating temperature and characteristic parameters of the capacitor at different times. Because the operating temperature at different times is different, the characteristic parameter values of the capacitor at different times are also different. Therefore, it is necessary to standardize the characteristic parameters according to the corresponding operating temperature at different times. The temperature of the thermostat is controlled to simulate the ambient temperature change of the capacitor bank, and the internal temperature and parameter changes of the capacitor monitored by the digital twin system at different times are recorded. The experimental results are shown in Fig. 15. The actual value of temperature is measured by the thermocouple inside the capacitor, and the actual value of R_C and C is measured by LCR measuring instrument at different temperatures. The abscissa in the figure represents the corresponding test number at different times.

To verify the health status assessment results, put the capacitor bank in the thermostat, gradually change the temperature of the

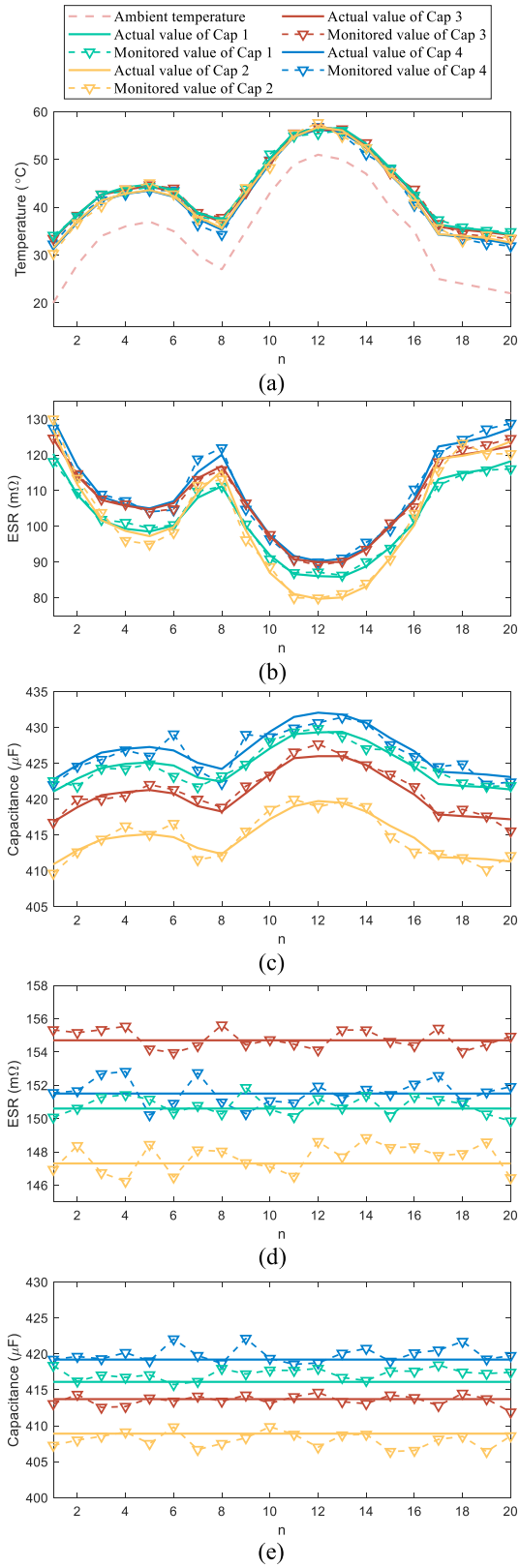

Fig. 15. Monitoring results of digital twin model. (a) Temperature monitoring results at different times. (b) Monitoring results of ESR at different times. (c) Capacitance monitoring results at different times. (d) Standardization results of ESR at different times. (e) Standardization results of capacitance at different times.

TABLE I
RESULTS OF HEALTH ASSESSMENT WITH R_C

Capacitor	Operating temperature	$R_{C\_25℃}$ (mΩ) DT value	$R_{C\_25℃}$ (mΩ) Measured value	$R_{C0\_25℃}$ (mΩ)	HD (%)
Cap 1	30℃	154.0	150.6	143.7	92.8
	40℃	156.5			91.1
	50℃	149.5			95.9
Cap 2	30℃	152.4	147.3	139.2	90.5
	40℃	149.8			92.3
	50℃	145.2			95.6
Cap 3	30℃	151.9	154.7	145.8	95.8
	40℃	149.2			97.6
	50℃	148.9			97.8
Cap 4	30℃	153.6	151.5	142.9	92.5
	40℃	154.9			91.6
	50℃	149.4			95.4

TABLE II
RESULTS OF HEALTH ASSESSMENT WITH C

Capacitor	Operating temperature	$C_{25℃}$ (μF) DT value	$C_{25℃}$ (μF) Measured value	$C_{25℃}$ (μF)	HD (%)
Cap 1	30℃	414.5	416.1	421.9	91.1
	40℃	415.6			92.4
	50℃	411.4			87.4
Cap 2	30℃	406.7	408.9	417.8	86.7
	40℃	410.9			91.7
	50℃	405.2			85.0
Cap 3	30℃	417.7	413.7	431.8	83.6
	40℃	416.3			82.1
	50℃	412.9			78.2
Cap 4	30℃	417.5	419.2	432.7	82.4
	40℃	421.6			87.1
	50℃	415.7			80.4

thermostat. The digital twin model is used to monitor the internal operating temperature of capacitors at different times, and the method in Section V is used to evaluate the health status of capacitors at corresponding times. When use R_C at 2000 Hz to evaluate the healthy state, the evaluation results are given in Table I. When use C at 2000 Hz to evaluate the healthy state, the evaluation results are given in Table II.

It can be seen that temperature has a great influence on the evaluation of capacitor health status, and if the temperature factor is ignored to make a rough evaluation of capacitor status directly, it is possible that the capacitors that have degraded to the limit will continue to be used as normal capacitors, which will affect the reliability and safety of the power system, and it is also possible that the capacitors that can continue to be used will be misjudged as having failed, which will increase the maintenance cost of the power system. By using the established digital twin model, the characteristic parameters of capacitors can be monitored simultaneously with the operating temperature, so that the characteristic can be further standardized to eliminate the influence of temperature on the parameters and achieve more accurate health status assessment.

VII. CONCLUSION

The development of digital twin technology for power equipment provides a new idea for condition monitoring of dc-link capacitor banks. This article studies the application of Rogowski coil and digital twin technology in the field of dc-link capacitor bank condition monitoring, and the structure of digital twin system for dc-link capacitor bank with the parameter updating method are proposed. The digital twin model established considers the frequency characteristics and temperature characteristics of capacitor parameters, realizes the mapping from physical space to virtual space, and can accurately simulate the operation of individual capacitors in dc bank. At the same time, based on the method of dynamic updating model parameters by the RLS and UPF algorithm, combined with the operating temperature monitored by the digital twin system, the digital twin characteristic parameters are estimated and standardized, so as to realize the health status assessment of capacitor banks under variable operating temperature. The experimental results prove the accuracy of the digital twin system and its application in the field of condition monitoring.

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