Variable Sampling Frequency-Based SM Power Loss Balancing Control for MMCs With Bypassed Faulty SMs

Huailong Li, Fujin Deng, *Senior Member, IEEE*, Jifeng Zhao, Jie Tian, Yu Lu, and Gang Li

***Abstract*—The modular multilevel converter (MMC) is one of the most appropriate topologies for high-power applications due to its high modularity and low harmonic distortion. As faulty submodules (SMs) are bypassed, the capacitor voltage and switching frequency of healthy SMs in the faulty arm will rise, which causes unbalanced power loss distribution among the arms of MMCs and affects the reliability of MMCs. This article proposes a variable sampling frequency-based power loss balancing control (VSF-PLBC), which can balance power loss distribution among the arms of MMCs through adjusting the sampling frequency for an arm inserted SM number to modify switching losses in power devices in the MMC with bypassed SMs. The proposed VSF-PLBC can effectively improve the reliability of the MMC with the balanced power loss distribution among the arms in the MMC with bypassed SMs. The proposed VSF-PLBC is simulated with the professional tool PSCAD/EMTDC and is validated on a down-scale MMC prototype. The simulation and experimental results confirm the effectiveness of the proposed VSF-PLBC.**

***Index Terms*—Modular multilevel converter (MMC), power loss balancing, submodule (SM) bypass, variable sampling frequency.**

I. Introduction

MODULAR multilevel converter (MMC), which was first introduced in 2003 [1], becomes one of the most promising topologies for high-power applications due to its modularity, scalability, high quality voltage, and high reliability [2], [3], [4].

The MMC consists of abundant submodules (SMs) and each SM may be a potential failure point [5], [6]. The bypass of faulty SMs will result in higher SM capacitor voltage and switching frequency in a faulty arm, which would cause unbalanced power loss distribution among arms in MMC, and therefore threaten the reliability of the MMC [7], [8].

So far, a few studies have paid attention to the power loss optimization for MMCs, which can be divided into modulation strategies optimization-based method, circulating current control-based method, and SM capacitor voltage control-based method. The modulation strategies optimization-based method has been proposed to optimize power loss of the power device in the SM of the MMC. Picas et al. [9] and [10] proposed the discontinuous pulsewidth modulation with low switching frequency to optimize power losses of the MMC. Kim et al. [11] presented a hybrid pulsewidth modulation to optimize power losses by operating with the fundamental frequency modulation scheme for some SMs. However, the modulation strategies optimization-based method would affect the power quality owing to the low switching frequency.

Circulating current control-based method can optimize the power losses of the MMC. Zhao et al. [12] presented a power loss optimization control method, where the maximum power loss in the switch/diode of each SM can be effectively reduced through injecting optimum second-order harmonic current into the circulating current of MMC. Merlin and Mitcheson [13] proposed a power loss distribution control method for MMC based on second-order harmonic circulating current control, which results in a lower power loss difference between the top power device and bottom power device in each SM of the MMC. Bakhshizadeh et al. [14] introduced a power loss optimization control method by controlling the second-order harmonic circulating current in the arm to maintain loss constant to improve the reliability of MMC under all operating conditions. However, the circulating current control-based method will increase total power loss of the MMC.

The SM capacitor voltage control-based method also plays an important role in power loss optimization of the MMC. Deng et al. [15] presented a power loss optimization method, which can realize balanced SM power loss distribution in the same arm of the MMC through the voltage-balancing control for the virtual capacitor voltages in the MMC. Wang et al. [16] proposed an active power loss control method for the switches in the MMC based on the tradeoff between the switching loss balance control and the capacitor voltage control to reduce degree of power loss imbalance among SMs. Picas et al. [17] presented a power loss optimization method by introducing a weighted function of voltage and power losses to achieve evenly distributed switching

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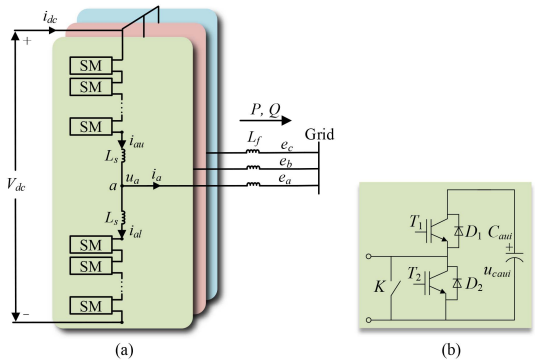

Fig. 1. (a) Circuit diagram of MMCs. (b) Structure of SM.

and conduction power losses of the SMs in the MMC. However, the aforementioned methods increase the differences in the capacitor voltage spread among the SMs.

In this article, the SM power loss distribution among the different arms of the MMC with bypassed SMs is analyzed in detail, where the SM faults would cause different SM capacitor voltage and switching frequency among the arms of MMC. It would result in unbalanced SM power loss distribution among the arms in the MMC, and therefore affect the reliability of the MMC. In this article, a variable sampling frequency-based power loss balancing control (VSF-PLBC) is proposed for the MMC under SM faults. Through adjusting the sampling frequency for arm inserted SM number (AISN), the proposed VSF-PLBC can balance the SM power losses among the arms in the MMC with bypassed SMs. The proposed VSF-PLBC eliminates the power loss difference among the arms in the MMC with bypassed SMs, and therefore, it imposes the reliability of the MMC.

The rest of this article is organized as follows. Section II describes the MMC. Section III analyzes the characteristics of the MMC with bypassed SMs. Section IV analyzes the power loss of the MMC with bypassed SMs. Section V proposes the VSF-PLBC for the MMC with bypassed SMs. The system simulation and experiment are conducted in Sections VI and VII, respectively, to show the effectiveness of the proposed VSF-PLBC for the MMC. Finally, Section VIII concludes this article.

II. Descriptions of MMCs

A. Structure of MMCs

A three-phase MMC is shown in Fig. 1(a), which is made up of six arms. Each arm consists of N_n half-bridge SMs and an inductor L_s. Fig. 1(b) shows the ith ($i = 1, 2, \ldots, N_n$) SM in the upper arm of phase A, which contains the switches/diodes (T_1/D_1 and T_2/D_2) and the capacitor C_{aui}. A bypass switch K is equipped to bypass the faulty SMs [18].

Normally, the ith SM is controlled by the ith switching signal S_{aui} as

$$S_{aui} = \begin{cases} 1, T_1 \text{ is on and } T_2 \text{ is off} \\ 0, T_1 \text{ is off and } T_2 \text{ is on.} \end{cases} \quad (1)$$

B. Voltage-Balancing Control for MMCs

Fig. 2 shows the balancing adjusting number (BAN)-based capacitor voltage-balancing control for MMCs in the upper arm of phase A [19]. In Fig. 2, the capacitor voltage sampling frequency can be set the same as the system control frequency, which is more than the sampling frequency f_s for AISN. The AISN N_m is obtained by the reference y_{au} and the modulation strategy. And then, the number N_{in} of ON-state SMs in the arm is obtained by the sampling of AISN N_m at the sampling frequency f_s. The incremental number ΔN_{incre} of the ON-state SMs in the arm can be calculated as the difference of the ON-state SMs number N_{in_new} at current sampling cycle and the ON-state SMs number N_{in_old} at previous sampling cycle, as

$$\Delta N_{\text{incre}} = N_{in\_\text{new}} - N_{in\_\text{old}}. \quad (2)$$

The adjusted number N_{adj} of the SMs to be switched ON or OFF within this sampling cycle is

$$N_{\text{adj}} = |\Delta N_{\text{incre}}| + N_{\text{ban}} \quad (3)$$

where the N_{ban} is the BAN.

The actual switching number of the SMs to be switched ON among the N_n-N_{in_old} OFF-state SMs and the actual switching number of the SMs to be switched OFF among the N_{in_old} ON-state SMs are decided based on the direction of the arm current i_{au} and the ΔN_{incre}, as follows.

1) $i_{au}>0$ and $\Delta N_{\text{incre}} = 0$: Switch ON N_{ban} SMs with the lowest voltages among the N_n-N_{in_old} OFF-state SMs. In addition, switch OFF N_{ban} SMs with the highest voltages among the N_{in_old} ON-state SMs.
2) $i_{au}>0$ and $\Delta N_{\text{incre}}>0$: Switch ON N_{adj} SMs with the lowest voltages among the N_n-N_{in_old} OFF-state SMs. In addition, switch OFF N_{ban} SMs with the highest voltages among the N_{in_old} ON-state SMs.
3) $i_{au}>0$ and $\Delta N_{\text{incre}}<0$: Switch ON N_{ban} SMs with the lowest voltages among the N_n-N_{in_old} OFF-state SMs. In addition, switch OFF N_{adj} SMs with the highest voltages among the N_{in_old} ON-state SMs.
4) $i_{au}<0$ and $\Delta N_{\text{incre}} = 0$: Switch ON N_{ban} SMs with the highest voltages among the N_n-N_{in_old} OFF-state SMs. In addition, switch OFF N_{ban} SMs with the lowest voltages among the N_{in_old} ON-state SMs.
5) $i_{au}<0$ and $\Delta N_{\text{incre}}>0$: Switch ON N_{adj} SMs with the highest voltages among the N_n-N_{in_old} OFF-state SMs. In addition, switch OFF N_{ban} SMs with the lowest voltages among the N_{in_old} ON-state SMs.
6) $i_{au}<0$ and $\Delta N_{\text{incre}}<0$: Switch ON N_{ban} SMs with the highest voltages among the N_n-N_{in_old} OFF-state SMs. In addition, switch OFF N_{adj} SMs with the lowest voltages among the N_{in_old} ON-state SMs.

III. Characteristics Analysis of MMCs With Bypassed Faulty SMs

A. Analysis of SM Capacitor Voltage of MMCs With Bypassed Faulty SMs

The tolerant operation of spinning reserve is used for the MMC, where the MMC is equipped with redundant SMs, such

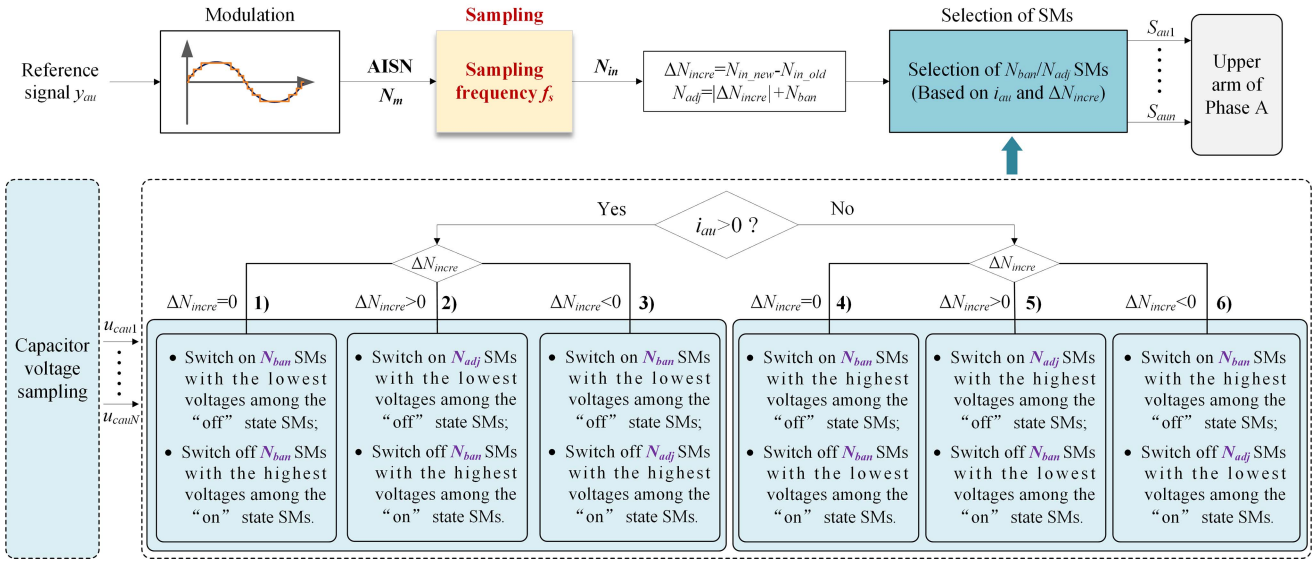

Fig. 2. BAN-based capacitor voltage-balancing control for MMCs.

as 10% redundant SMs [20]. When the MMC works normally, the redundant SMs operate in the same way as other SMs. When the SM fault occurs, only the faulty SM is bypassed from the arm. This tolerant operation of the MMC can achieve high SM utilization and high economic of the MMC system.

Assuming that all SM capacitor voltages are kept balanced by the voltage-balancing control [19], the rated SM capacitor voltage under normal operation condition is [21]

$$U_{cr} = \frac{V_{\rm dc}}{N_n} \tag{4}$$

where $V_{\rm dc}$ is the dc-link voltage, as illustrated in Fig. 1(a).

Taking the SM faults in the upper arm of phase A as an example, the faulty SMs will be bypassed from the faulty arm by the bypass switch [22], and then, the SM capacitor voltage U_{cf} in the faulty arm will be

$$U_{cf} = \frac{U_{cr}}{1-\lambda} \tag{5}$$

with

$$\lambda = \frac{N_{\rm fau}}{N_n} \times 100\% \tag{6}$$

where λ is the proportion of bypassed SM number. $N_{\rm fau}$ is the number of bypassed SMs in the faulty arm.

According to (4)–(6), it can be observed that the SM capacitor voltage U_{cf} under SM fault is determined by corresponding λ. The U_{cf} increases along with the increase of λ, and the U_{cf} reduces along with the reduction of λ. Fig. 3 shows the SM capacitor voltage under different λ, which is derived from the simulation system in Section VI. It shows that the SM capacitor voltage increases along with the increase of λ.

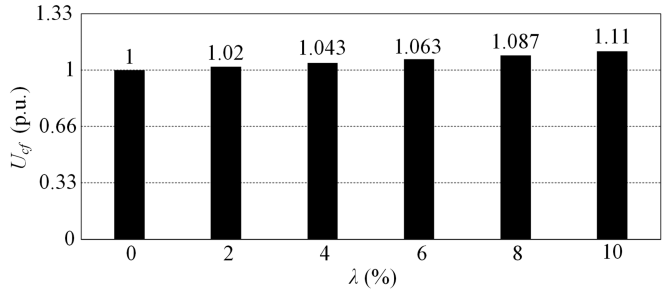

Fig. 3. SM capacitor voltage under various λ.

B. Analysis of SM Switching Frequency of MMCs With Bypassed SMs

For the BAN-based voltage-balancing control [19], the average switching frequency $f_{\rm sw}$ of each SM in the arm can be calculated, as shown in the Appendix, as

$$f_{\rm sw} = \frac{f_s}{1-\lambda} \cdot \frac{N_{\rm ban}}{N_n} + \frac{m}{T_f} \tag{7}$$

with

$$m = \frac{2\sqrt{(\omega LP)^2 + (3U_s^2 - \omega LQ)^2}}{3U_s V_{dc}} \tag{8}$$

where m is the modulation index. T_f is the fundamental cycle and $T_f = 2\pi/\omega$. ω is fundamental angular frequency and $\omega = 2\pi f$. f is the fundamental frequency. L_f is the filter inductor, as shown in Fig. 1. L is equivalent inductor as $L = L_f + L_s/2$. U_s is the phase voltage root mean square (rms) value of ac grid. P and Q are active and reactive power, respectively, as shown in Fig. 1(a).

From (7), it can be observed that the SM switching frequency $f_{\rm sw}$ is related to λ, where $f_{\rm sw}$ increases along with the increase of λ, and $f_{\rm sw}$ reduces along with the reduction of λ. Fig. 4 shows $f_{\rm sw}$ under different λ, which is derived from the simulation system

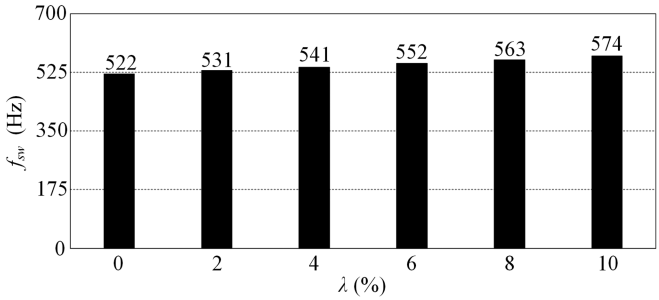

Fig. 4. SM switching frequency under various λ.

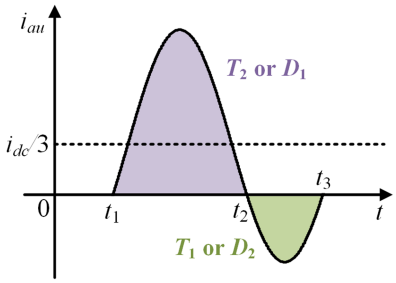

Fig. 5. Upper arm current i_{au} of MMCs.

in Section VI. It can be observed that the $f_{\rm sw}$ increases along with the increase of λ.

IV. Power Loss Analysis of MMCs With Bypassed SMs

A. Analytical Models of MMCs

In Fig. 1, based on the active power P, reactive power Q, and the phase voltage rms value U_s of the ac grid, the ac current in phase A can be obtained as [23]

$$i_a(t) = I_m \cdot \sin(\omega t + \varphi) \tag{9}$$

with

$$\begin{cases} I_m = \frac{\sqrt{2}}{3}\frac{\sqrt{P^2+Q^2}}{U_s} \\ \varphi = \arctan(\frac{Q}{P}) \end{cases}. \tag{10}$$

Suppose that the fundamental frequency circulating current is suppressed with the method [5] and the second-order harmonic circulating current is suppressed with the method [24], the upper arm current i_{au} in phase A can be described as

$$i_{au}(t) = \frac{i_a(t)}{2} + \frac{i_{\rm dc}}{3} \tag{11}$$

with

$$i_{\rm dc} = \frac{P}{V_{\rm dc}} \tag{12}$$

where $i_{\rm dc}$ is dc-link current of MMCs, as shown in Fig. 1(a).

B. Analysis of SM Device Current

Fig. 5 shows the upper arm current i_{au} in one period T_f. Combining (9)–(12), the zero crossing instants t_1, t_2, and t_3 of i_{au} in Fig. 5 can be obtained as

$$\begin{cases} t_1 = -\frac{\arcsin(\frac{2i_{\rm dc}}{3I_m})+\varphi}{\omega} + T_f \\ t_2 = \frac{\pi+\arcsin(\frac{2i_{\rm dc}}{3I_m})-\varphi}{\omega} + T_f \\ t_3 = t_1 + T_f. \end{cases} \tag{13}$$

In one period T_f, as shown in Fig. 5, when the arm current is $i_{au}>0$, i_{au} flows through T_2 or D_1, as shown in Fig. 1; when the arm current is $i_{au}<0$, i_{au} flows through T_1 or D_2, as shown in Fig. 1. According to [25], [26], (9)–(13), and Fig. 5, the current mean values $I_{\rm ave\_T1}$, $I_{\rm ave\_T2}$, $I_{\rm ave\_D1}$, and $I_{\rm ave\_D2}$ of T_1, T_2, D_1, and D_2 in the SM can be obtained, respectively, as

$$\begin{cases} I_{\rm ave\_T1} = \frac{1}{T_f}\int_{t_2}^{t_3}\frac{1-y_{au}(t)}{2}(-i_{au}(t))dt \\ I_{\rm ave\_T2} = \frac{1}{T_f}\int_{t_1}^{t_2}\frac{1+y_{au}(t)}{2}i_{au}(t)dt \\ I_{\rm ave\_D1} = \frac{1}{T_f}\int_{t_1}^{t_2}\frac{1-y_{au}(t)}{2}i_{au}(t)dt \\ I_{\rm ave\_D2} = \frac{1}{T_f}\int_{t_2}^{t_3}\frac{1+y_{au}(t)}{2}(-i_{au}(t))dt \end{cases}. \tag{14}$$

According to [25], [26], (9)–(13), and Fig. 5, the current rms values $I_{\rm rms\_T1}$, $I_{\rm rms\_T2}$, $I_{\rm rms\_D1}$, and $I_{\rm rms\_D2}$ of T_1, T_2, D_1, and D_2 in the SM can be obtained, respectively, as

$$\begin{cases} I_{\rm rms\_T1} = \sqrt{\frac{1}{T_f}\int_{t_2}^{t_3}\frac{1-y_{au}(t)}{2}i_{au}^2(t)dt} \\ I_{\rm rms\_T2} = \sqrt{\frac{1}{T_f}\int_{t_1}^{t_2}\frac{1+y_{au}(t)}{2}i_{au}^2(t)dt} \\ I_{\rm rms\_D1} = \sqrt{\frac{1}{T_f}\int_{t_1}^{t_2}\frac{1-y_{au}(t)}{2}i_{au}^2(t)dt} \\ I_{\rm rms\_D2} = \sqrt{\frac{1}{T_f}\int_{t_2}^{t_3}\frac{1+y_{au}(t)}{2}i_{au}^2(t)dt} \end{cases}. \tag{15}$$

C. Analysis of Device's Conduction Losses

According to [27], the conduction losses $P_{\rm con\_T1}$, $P_{\rm con\_T2}$, $P_{\rm con\_D1}$, and $P_{\rm con\_D2}$ of T_1, T_2, D_1, and D_2 in the SM can be obtained, respectively, as

$$\begin{cases} P_{\rm con\_T1/2} = V_{ce0}I_{\rm ave\_T1/2} + R_{ce0}I^2_{\rm rms\_T1/2} \\ P_{\rm con\_D1/2} = V_{d0}I_{\rm ave\_D1/2} + R_{d0}I^2_{\rm rms\_D1/2} \end{cases} \tag{16}$$

where V_{ce0} and V_{d0} are ON-state zero-current voltage drop of switch and diode, respectively. R_{ce0} and R_{d0} are ON-state resistance of switch and diode, respectively.

According to (8)–(16), the conduction losses $P_{\rm con\_T1}$, $P_{\rm con\_T2}$, $P_{\rm con\_D1}$, and $P_{\rm con\_D2}$ of T_1, T_2, D_1, and D_2 are nearly not affected by SM bypass. Fig. 6 shows the conduction losses of T_1, T_2, D_1, and D_2 under different proportion λ of bypassed SM number, which are derived from the simulation system

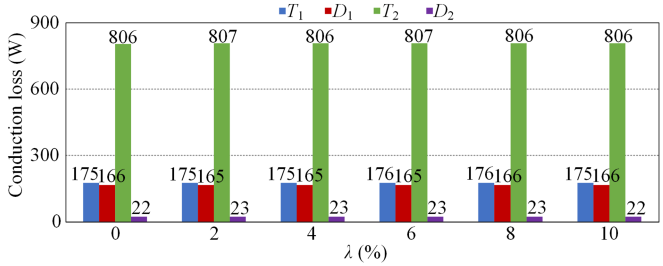

Fig. 6. Conduction losses of T_1, T_2, D_1, and D_2 under various λ.

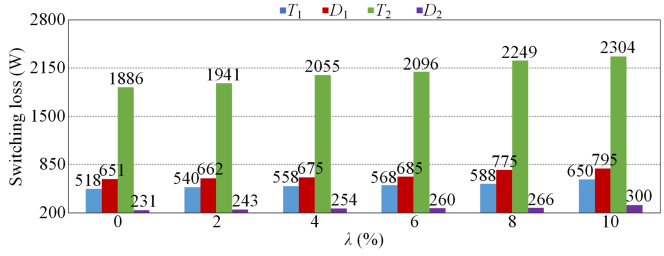

Fig. 7. Switching losses of the T_1, T_2, D_1, and D_2 under various λ.

in Section VI. It can be observed that the conduction losses of T_1, T_2, D_1, and D_2 under different λ are nearly close to each other.

D. Analysis of Device's Switching Losses

According to [27], the switching losses $P_{\mathrm{sw\_}T1}$, $P_{\mathrm{sw\_}T2}$, $P_{\mathrm{rec\_}D1}$, and $P_{\mathrm{rec\_}D2}$ of T_1, T_2, D_1, and D_2 in the SM can be calculated as

$$\begin{cases} P_{\mathrm{sw\_}T1/2} = f_{\mathrm{sw}} E_{\mathrm{sw}}(I_{\mathrm{ave\_}T1/2}, I_{\mathrm{rms\_}T1/2}) U_{cf}/U_{\mathrm{ref}} \\ P_{\mathrm{rec\_}D1/2} = f_{\mathrm{sw}} E_{\mathrm{rec}}(I_{\mathrm{ave\_}D1/2}, I_{\mathrm{rms\_}D1/2}) U_{cf}/U_{\mathrm{ref}} \end{cases} \tag{17}$$

where E_{sw} is the switching energy of the switch, E_{rec} is the reverse-recovery energy of the diode, and U_{ref} is the testing voltage in the datasheet.

Based on (17), it can be observed that the SM switching loss depends on the U_{cf} and f_{sw}. The switching loss increases along with the increase of U_{cf} or f_{sw}, and reduces along with the reduction of U_{cf} or f_{sw}. Based on Figs. 3 and 4, and (17), the relationship between λ and the devices' switching loss can be obtained. Along with the increase of λ, U_{cf} and f_{sw} will increase, which would increase the devices' switching loss. Along with the reduction of λ, U_{cf} and f_{sw} will reduce, which would reduce the devices' switching loss.

Fig. 7 shows switching loss of T_1, T_2, D_1, and D_2 under different λ, which is derived from the simulation system in Section VI. It can be observed that the switching losses of the T_1, T_2, D_1, and D_2 increase along with the increase of λ, and reduce along with the reduction of λ.

E. Analysis of Device's Total Power Losses

The total power loss P_{T1}, P_{T2}, P_{D1}, and P_{D2} of the T_1, T_2, D_1, and D_2 is the sum of their conduction loss and switching loss, respectively, as

$$\begin{cases} P_{T1/2} = P_{\mathrm{con\_}T1/2} + P_{\mathrm{sw\_}T1/2} \\ P_{D1/2} = P_{\mathrm{con\_}D1/2} + P_{\mathrm{rec\_}D1/2}. \end{cases} \tag{18}$$

Based on Figs. 6 and 7, and (18), it can be observed that the SM bypass would not affect the conduction loss, but cause the increase of the switching loss, which would lead to the increase of the total power loss of the device, as shown in Table I, as follows.

1) The increase of λ would cause increased switching losses $P_{\mathrm{sw\_}T1/2}$ and $P_{\mathrm{rec\_}D1/2}$, while the conduction losses $P_{\mathrm{con\_}T1/2}$ and $P_{\mathrm{con\_}D1/2}$ are nearly not affected. Consequently, the total power losses $P_{T1/2}$ and $P_{D1/2}$ would be increased along with the increase of λ.

TABLE I
RELATIONSHIP BETWEEN $P_{\mathrm{T1/2}}$, $P_{\mathrm{D1/2}}$ AND λ

λ	$P_{sw\_T1/2}$	$P_{rec\_D1/2}$	$P_{con\_T1/2}$	$P_{con\_D1/2}$	$P_{T1/2}$	$P_{D1/2}$
↑	↑	↑	—	—	↑	↑
↓	↓	↓	—	—	↓	↓

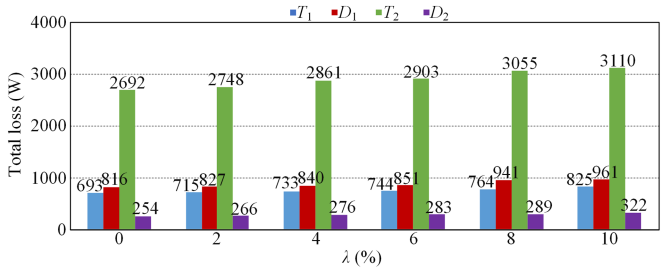

Fig. 8. Total losses of the T_1, T_2, D_1, and D_2 under various λ.

2) The reduction of λ would cause decreased switching losses $P_{\mathrm{sw\_}T1/2}$ and $P_{\mathrm{rec\_}D1/2}$, while the conduction losses $P_{\mathrm{con\_}T1/2}$ and $P_{\mathrm{con\_}D1/2}$ are nearly not affected. Consequently, the total power losses $P_{T1/2}$ and $P_{D1/2}$ would be decreased along with the decrease of λ.

Fig. 8 shows total power losses of T_1, T_2, D_1, and D_2 under various λ, which is derived from the simulation system in Section VI. From Fig. 8, it can be observed that the total power losses of T_1, T_2, D_1, and D_2 increase along with the increase of λ, and the total power losses of T_1, T_2, D_1, and D_2 reduce along with the reduction of λ, which is consistent with the total loss analysis in Table I.

F. Analysis of Reliability

According to power loss models in (18) and [28], the mean junction temperature T_{jm} and junction temperature fluctuation ΔT_j of switch T and diode D can be expressed as

$$\begin{cases} T_{jm\_T/D} = P_{T/D} \cdot \sum_{i=1}^{4} R_{\mathrm{th}jc\_T/D}(i) \\ \quad + P_{T/D} \cdot R_{\mathrm{th}ch} + T_h \\ \Delta T_{j\_T/D} = 2P_{T/D} \cdot \sum_{i=1}^{4} R_{\mathrm{th}jc\_T/D}(i) \\ \quad \cdot \frac{\left(1-e^{-t_{\mathrm{on\_}T/D}/\tau_{\mathrm{th}jc\_T/D}(i)}\right)^2}{1-e^{-T_f/\tau_{\mathrm{th}jc\_T/D}(i)}} \end{cases} \tag{19}$$

where $t_{\mathrm{on}\cdot T/D}$ represents the ON-state time within each fundamental cycle of the switch/diode, $R_{\mathrm{th}jc\cdot T/D}$ represents the thermal resistance from the junction to case, $R_{\mathrm{th}ch}$ represents the thermal resistance from case to heat sink, $P_{\mathrm{T/D}}$ represents the power loss of the switch/diode, T_h represents the sink temperature, and $\tau_{\mathrm{th}jc\cdot T/D}$ represents the thermal time constant.

The number of cycles to failure N_f of the power device is a function of the amplitude of thermal cycles ΔT_j and the mean junction temperature T_{jm} [25], which can be expressed as

$$N_f = A(\Delta T_j)^{\beta_1} \cdot e^{\left(\frac{\beta_2}{T_{jm\_T/D}+0.5\Delta T_{j\_T/D}+273}\right)} \cdot \left(\frac{t_{\mathrm{test}}}{1.5}\right)^{\beta_3} \tag{20}$$

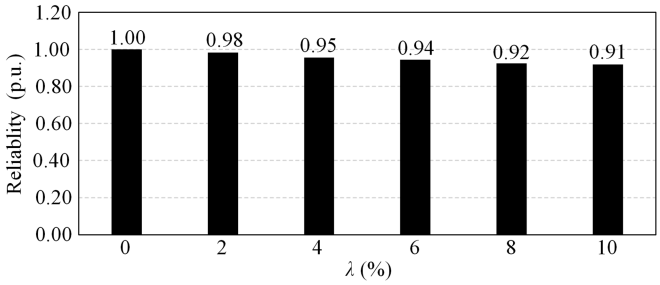

Fig. 9. Reliability of MMCs under various λ.

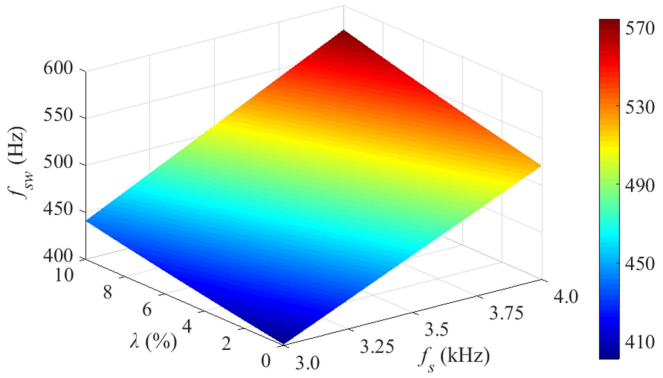

Fig. 10. SM switching frequency of MMCs under various λ and f_s.

where A, β_1, β_2, and β_3 are fitting parameters. $A = 1.42 \times 10^{12}$, $\beta_1 = -7.14$, $\beta_2 = 5154$, and $\beta_3 = -0.3$, t_{test} ranges from 0.1 to 60 s.

According to [29] and [30], the reliability of the power device is

$$R_{\text{com}}(t) = e^{-\frac{365^*24^*3600}{N_f \cdot T_f} t}. \tag{21}$$

According to [25], the reliability of the MMC is

$$R_{\text{MMC}}(t) = \left[\left[\prod_{i=1}^{4} R_{\text{comi}}(t)\right]^{N_n(1-\lambda)}\right]^{k} \cdot \left[\left[\prod_{i=1}^{4} R_{\text{comi}}(t)\right]^{N_n}\right]^{(6-k)} \tag{22}$$

where k is the number of faulty arms.

According to above analysis, the reliability of the MMC under different λ can be obtained as shown in Fig. 9, which is derived from the simulation system in Section VI. It shows that the reliability of the MMC reduces along with the increase of λ, and the SMs bypass affects the reliability of the MMC.

V. Proposed VSF-PLBC Strategy for MMCs With Bypassed Faulty SMs

A. Proposed VSF-PLBC Approach

Based on (7), it can be obviously observed that the switching frequency f_{sw} is not only affected by the corresponding λ but also affected by the sampling frequency f_s.

1) If f_s is increased, the f_{sw} is increased.
2) If f_s is reduced, the f_{sw} is reduced.

Fig. 10 shows f_{sw} under different λ and f_s, which is derived from (7) and the simulation system in Section VI. It can be obviously observed that f_{sw} increases along with the increase of f_s or λ, and f_{sw} reduces along with the reductions of f_s or λ.

Based on above analysis, a VSF-based power loss control is proposed, where the power device's power loss $P_{T1/2}$ and $P_{D1/2}$ in the MMC can be controlled by the sampling frequency f_s, as shown in Table II, as follows.

1) *Increase of f_s:* The switching losses $P_{\text{sw\_}T1/2}$ and $P_{\text{rec\_}D1/2}$ are increased, while the conduction losses $P_{\text{con\_}T1/2}$ and $P_{\text{con\_}D1/2}$ are nearly not affected. As a result, the power device's power losses $P_{T1/2}$ and $P_{D1/2}$ are increased.

TABLE II
Relationship Between $P_{\text{T1/2}}$, $P_{\text{D1/2}}$, and F_{S}

f_s	$P_{sw\_T1/2}$	$P_{rec\_D1/2}$	$P_{con\_T1/2}$	$P_{con\_D1/2}$	$P_{T1/2}$	$P_{D1/2}$
↑	↑	↑	—	—	↑	↑
↓	↓	↓	—	—	↓	↓

2) *Decrease of f_s:* The switching losses $P_{\text{sw\_}T1/2}$ and $P_{\text{rec\_}D1/2}$ are decreased, while the conduction losses $P_{\text{con\_}T1/2}$ and $P_{\text{con\_}D1/2}$ are nearly not affected. As a result, the power device's power losses $P_{T1/2}$ and $P_{D1/2}$ are decreased.

B. Proposed VSF-PLBC Strategy for MMCs Under SM Faults

Based on above VSF-based power loss control, a VSF-PLBC strategy is proposed to balance power loss distribution among the arms of the MMC with bypassed SMs, as shown in Fig. 11.

The maximum power loss of the devices in the ith SM is defined as $P_{\text{SM\_}jki} = \text{Max}\{P_{T1}, P_{T2}, P_{D1}, P_{D2}\}$ ($j = a,b,c$; $k = u,l$), where the power losses P_{T1}, P_{T2}, P_{D1}, and P_{D2} can be obtained by (18). The average power loss of $N_{\text{sel\_}jk}$ healthy SMs in each arm is defined as

$$P_{arm\_jk} = \sum_{i=1}^{N_{sel\_jk}} P_{SM\_jki}, (j = a,b,c; k = u,l) \tag{23}$$

where $N_{\text{sel\_}jk}$ is the number of selected healthy SMs in each arm. According to the power losses $P_{\text{arm\_}au}$, $P_{\text{arm\_}al}$, $P_{\text{arm\_}bu}$, $P_{\text{arm\_}bl}$, $P_{\text{arm\_}cu}$, and $P_{\text{arm\_}cl}$ in upper arm of phase A, lower arm of phase A, upper arm of phase B, lower arm of phase B, upper arm of phase C, and lower arm of phase C, respectively, the reference power loss $P_{\text{arm·ref}}$ of the MMC can be obtained as

$$P_{\text{arm\_ref}} = \text{Min} \times [P_{\text{arm\_}au}, P_{\text{arm\_}al}, P_{\text{arm\_}bu}, P_{\text{arm\_}bl}, P_{\text{arm\_}cu}, P_{\text{arm\_}cl}]. \tag{24}$$

For the three-phase MMC, the PI controller is used to regulate its sampling frequency f_s in the faulty arm to realize the power loss balancing among the six arms of the MMC based on VSF-based power loss control, as shown in Table II. f_{sr} is the rated sampling frequency of the VSF-PLBC for the MMC. The PI controller is used to produce the sampling frequency's

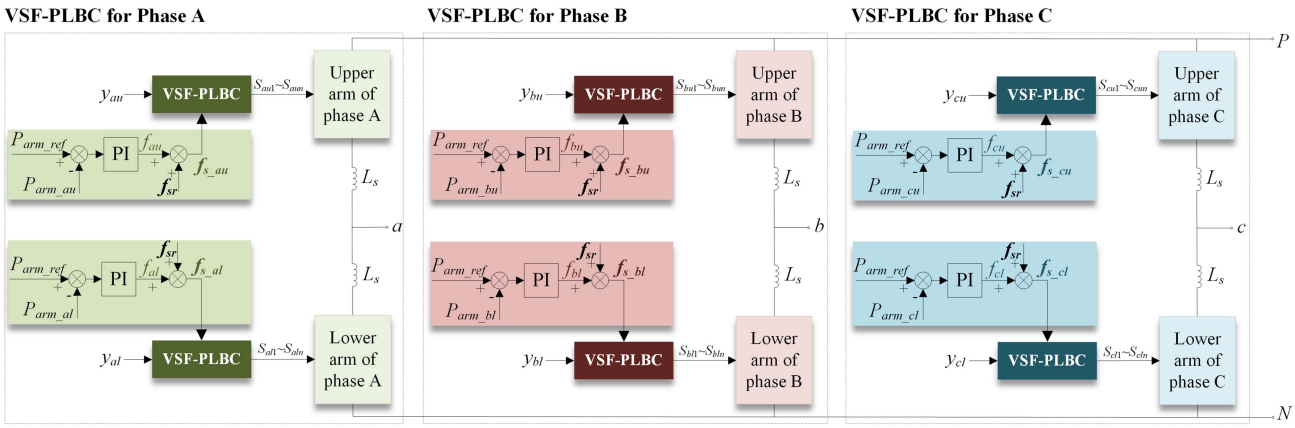

Fig. 11. Proposed VSF-PLBC strategy.

TABLE III
SIMULATION SYSTEM PARAMETERS

Parameters	Value
Active power P (MW)	100
DC-link voltage V_{dc} (kV)	150
Grid line-to-line voltage (kV)	75
Grid frequency (Hz)	50
Transformer rating voltage	75 kV/220 kV
Number of SMs per arm N_n	50
Rated number of redundant SMs N_{fN}	5
Balancing adjusting number N_{ban}	6
Nominal SM capacitance C (mF)	3
Inductance L_s (mH)	45
Inductance L_f (mH)	10
Rated sampling frequency f_{sr} (kHz)	4
Power device	FZ750R65KE3

compensation components f_{jk} ($j = a, b, c$; $k = u, l$) in phase j. If P_{arm_jk} in the faulty arm is more than $P_{\mathrm{arm'ref}}$, the PI controller would reduce the f_{jk}. As a result, the sampling frequency $f_{s'jk} = f_{sr} + f_{jk}$ in the arm is reduced, and the P_{arm_jk} is reduced to follow $P_{\mathrm{arm'ref}}$. As a result, the proposed VSF-PLBC strategy can effectively realize SM power loss balancing among six arms of the MMC with bypassed SMs.

C. Discussion of Proposed VSF-PLBC

Fig. 12 shows the worst faulty situation of the MMC, where 10% SMs are faulty and bypassed from the upper arm of phase A. The system parameters of the MMC are shown in Table III. In this situation, T_2 takes the maximum power loss among the power devices in the SM, as shown in Figs. 6–8. Fig. 12(a)–(d) show the switching frequency f_{sw_au}, conduction loss $P_{\mathrm{con}\_T2\_au}$, switching loss $P_{\mathrm{sw}\_T2\_au}$, and total loss $P_{T2\_au} = P_{\mathrm{arm}\_au}$ in the upper arm of phase A, respectively, under various sampling frequencies f_s. For the convenience of comparison, Fig. 12(a)–(d) also show the switching frequency f_{sw_al} (blue dot), conduction loss $P_{\mathrm{con}\_T2\_al}$ (blue dot), switching loss $P_{\mathrm{sw}\_T2\_al}$ (blue dot), and total loss $P_{T2\_al} = P_{\mathrm{arm}\_al}$ (blue dot) in the lower arm of phase A, respectively, where the

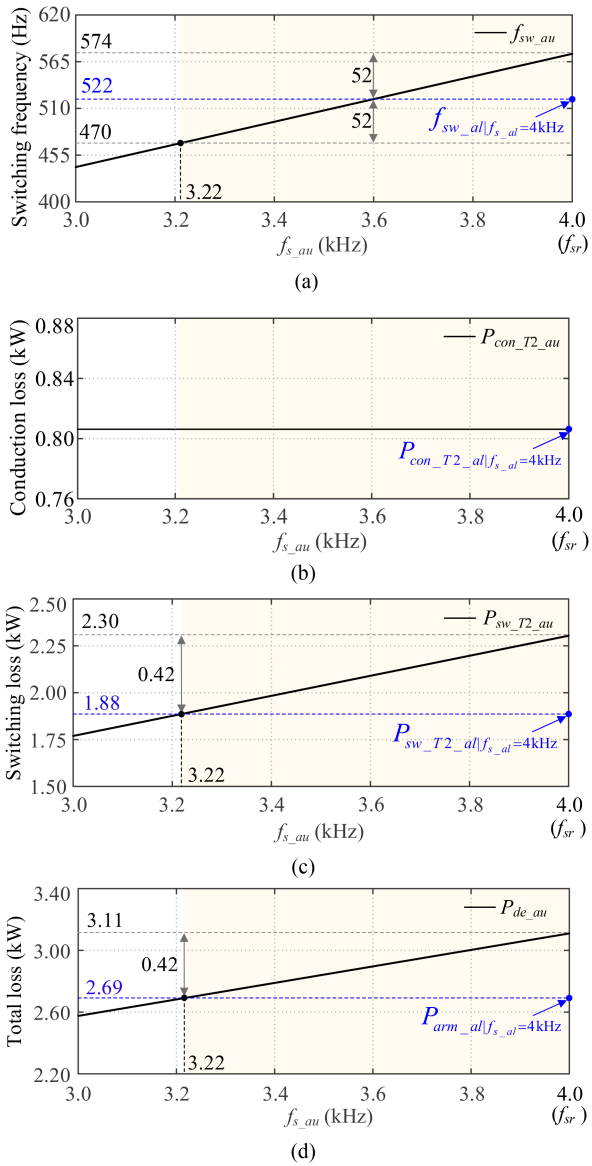

Fig. 12. MMC performance under various sampling frequencies. (a) Switching frequency. (b) Conduction loss. (c) Switching loss. (d) Total loss.

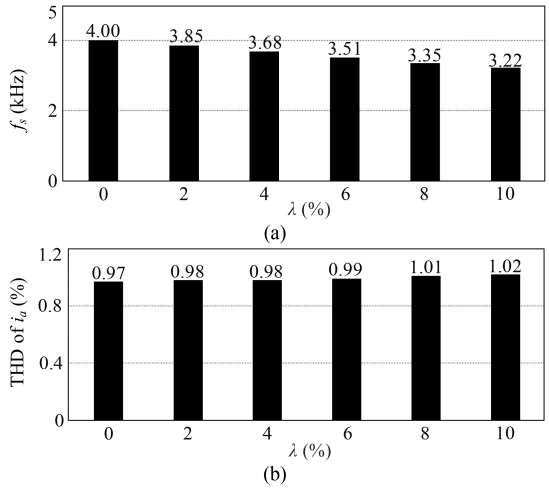

Fig. 13. (a) f_s under various λ. (b) THD of i_a under various f_s.

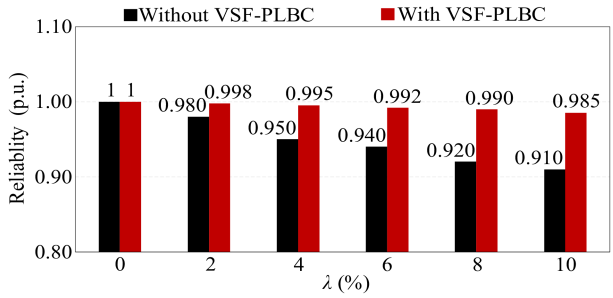

Fig. 14. Reliability of the MMC under various λ in two control methods.

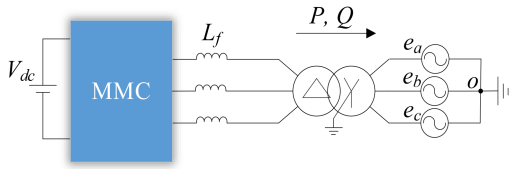

Fig. 15. Schematic diagram of the simulation system.

sampling frequency in the lower arm is at the rated value as $f_{sr} = 4$ kHz.

From Fig. 12, the switching frequency $f_{\mathrm{sw\_}au}$, switching loss $P_{\mathrm{sw\_}T2\_au}$, and power loss $P_{\mathrm{arm\_}au}$ in the upper arm of phase A are increased along with the increase of f_s, and vice versa. However, the conduction loss $P_{\mathrm{con\_}T2\_au}$ in the upper arm of phase A is almost not affected by the sampling frequency. At the rated sampling frequency as $f_{sr} = 4$ kHz, the switching frequency $f_{\mathrm{sw\_}au}$ is increased to 574 Hz in the upper arm, while the switching frequency $f_{\mathrm{sw\_}al}$ is 522 Hz in the lower arm; the switching loss $P_{\mathrm{sw\_}T2\_au}$ is increased to 2.30 kW in the upper arm, while the switching loss $P_{\mathrm{sw\_}T2\_al}$ is 1.88 kW in the lower arm; the power loss $P_{\mathrm{arm\_}au}$ is increased to 3.11 kW in the upper arm, while the $P_{\mathrm{arm\_}al}$ is 2.69 kW in the lower arm. With the proposed VSF-PLBC, through reducing the sampling frequency f_{s_au} to 3.22 kHz in the upper arm, the switching frequency $f_{\mathrm{sw\_}au}$ in the upper arm can be reduced to 470 Hz, where the switching loss $P_{\mathrm{sw\_}T2\_au}$ is reduced to 1.88 kW, and the total power loss in the upper arm is reduced to 2.69 kW, and is the same as that in the lower arm of phase A. Fig. 12(a) shows that the maximum difference of the switching frequency between normal situation and worst SM bypass situation is only 52 Hz, and the sampling frequency only varies between 3.22 and 4.0 kHz.

D. THD Analysis of MMCs

Fig. 13(a) shows the sampling frequency f_s corresponding to various faulty SM proportions λ with the proposed VSF-PLBC. Fig. 13(b) shows the total harmonic distortion (THD) of the MMC's output current i_a corresponding to various faulty SM proportions λ with the proposed VSF-PLBC. It can be observed that the THD of the i_a changes from 0.97% to 1.02%, which is quite small. Therefore, the proposed VSF-PLBC has little effect on the ac output current of the MMC.

E. Reliability Analysis of MMCs Under Proposed VSF-PLBC

Fig. 14 shows the reliability of the MMC under various λ in two control methods including without VSF-PLBC and with VSF-PLBC. It can be seen that the proposed VSF-PLBC can enhance the reliability of the MMC.

VI. Simulation Studies

To verify proposed VSF-PLBC, a three-phase MMC is built with professional tool PSCAD/EMTDC, as shown in Fig. 15. The simulation system parameters are shown in Table III.

A. Case I: Normal Situation

Fig. 16 shows the performance of the three-phase MMC under normal situation. Fig. 16(a) shows grid currents i_a, i_b, and i_c. Fig. 16(b) shows the upper arm SM capacitor voltages u_{cau1}–u_{cau50} and lower arm SM capacitor voltages u_{cal1}–u_{cal50} in phase A. Fig. 16(c) shows the arm currents i_{au} and i_{al} in phase A. Fig. 16(d) shows that the upper arm switching frequency $f_{\mathrm{sw\_}au}$ and lower arm switching frequency $f_{\mathrm{sw\_}al}$ in phase A are almost the same. Fig. 16(e) shows the upper arm power loss $P_{\mathrm{arm\_}au}$ and lower arm power loss $P_{\mathrm{arm\_}al}$ in phase A are almost the same.

B. Case II: SM Bypass in One Arm

Fig. 17 shows the performances of the MMC with 10% SM bypass in the upper arm of phase A, where the faulty SM_{46}–SM_{50} are bypassed. The proposed VSF-PLBC is enabled since 3 s. Fig. 17(a) shows i_a, i_b, and i_c. Fig. 17(b) shows the capacitor voltages u_{cau1}–u_{cau45} and u_{cal1}–u_{cal50} in phase A. Due to the SM bypass in the upper arm of phase A, the capacitor voltages u_{cau1}–u_{cau45} are higher than the capacitor voltages u_{cal1}–u_{cal50} in phase A. Fig. 17(c) shows the i_{au} and i_{al}. Fig. 17(d) shows the sampling frequency f_{s_au} and f_{s_al} in phase A. Fig. 17(e) shows the switching frequency $f_{\mathrm{sw\_}au}$ and $f_{\mathrm{sw\_}al}$ in phase A. Fig. 17(f) shows that $P_{\mathrm{arm\_}au}$ and $P_{\mathrm{arm\_}al}$ in phase A are unbalanced before 3 s because of SM bypass, where the maximum difference

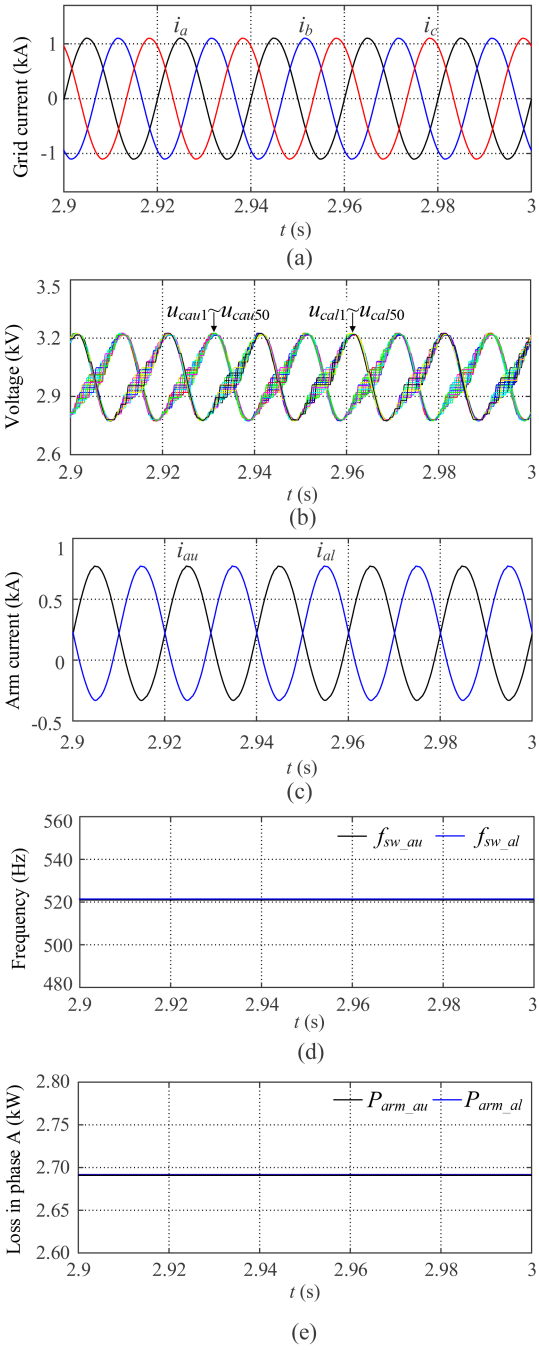

Fig. 16. (a) i_a, i_b, and i_c. (b) u_{cau1}–u_{cau50} and u_{cal1}–u_{cal50}. (c) i_{au} and i_{al}. (d) $f_{\mathrm{sw\_}au}$ and $f_{\mathrm{sw\_}al}$. (e) $P_{\mathrm{arm\_}au}$ and $P_{\mathrm{arm\_}al}$.

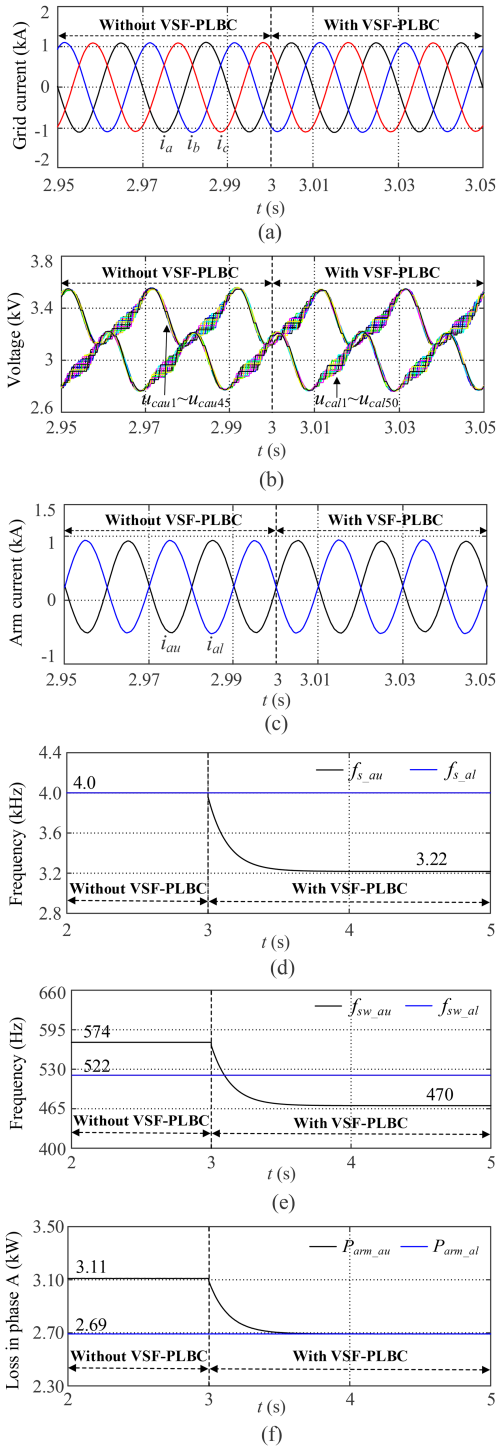

Fig. 17. (a) i_a, i_b, and i_c. (b) u_{cau1}–u_{cau45} and u_{cal1}–u_{cal50}. (c) i_{au} and i_{al}. (d) f_{s_au} and f_{s_al}. (e) $f_{\mathrm{sw\_}au}$ and $f_{\mathrm{sw\_}al}$. (f) $P_{\mathrm{arm\_}au}$ and $P_{\mathrm{arm\_}al}$.

is 0.42 kW. Since 3 s, the proposed control is enabled, and the power losses $P_{\mathrm{arm\_}au}$ and $P_{\mathrm{arm\_}al}$ become balanced.

C. Case III: SM Bypass in Arms of Different Phases

Fig. 18 shows the performances of the MMC with 10% SM bypass in the upper arm of phase A, where the faulty SM_{46}–SM_{50} are bypassed, and with 6% SM bypass in the upper arm of phase B, where the faulty SM_{48}–SM_{50} are bypassed. Here, the proposed VSF-PLBC is enabled since 3 s. Fig. 18(a) shows grid currents i_a, i_b, and i_c. Fig. 18(b) shows the upper arm SM capacitor voltages u_{cau1}–u_{cau45} in phase A, lower arm SM capacitor voltages u_{cal1}–u_{cal50} in phase A, and upper arm SM capacitor voltage u_{cbu1}–u_{cbu47} in phase B. Fig. 18(c) shows the arm currents i_{au} and i_{al} in phase A and i_{bu} in phase B. Fig. 18(d) shows the sampling frequency f_{s_au} and f_{s_al} in phase A and f_{s_bu} in phase B. Fig. 18(e) shows the switching frequency $f_{\mathrm{sw\_}au}$ and $f_{\mathrm{sw\_}al}$ in phase A and $f_{\mathrm{sw\_}bu}$ in phase B. Fig. 18(f)

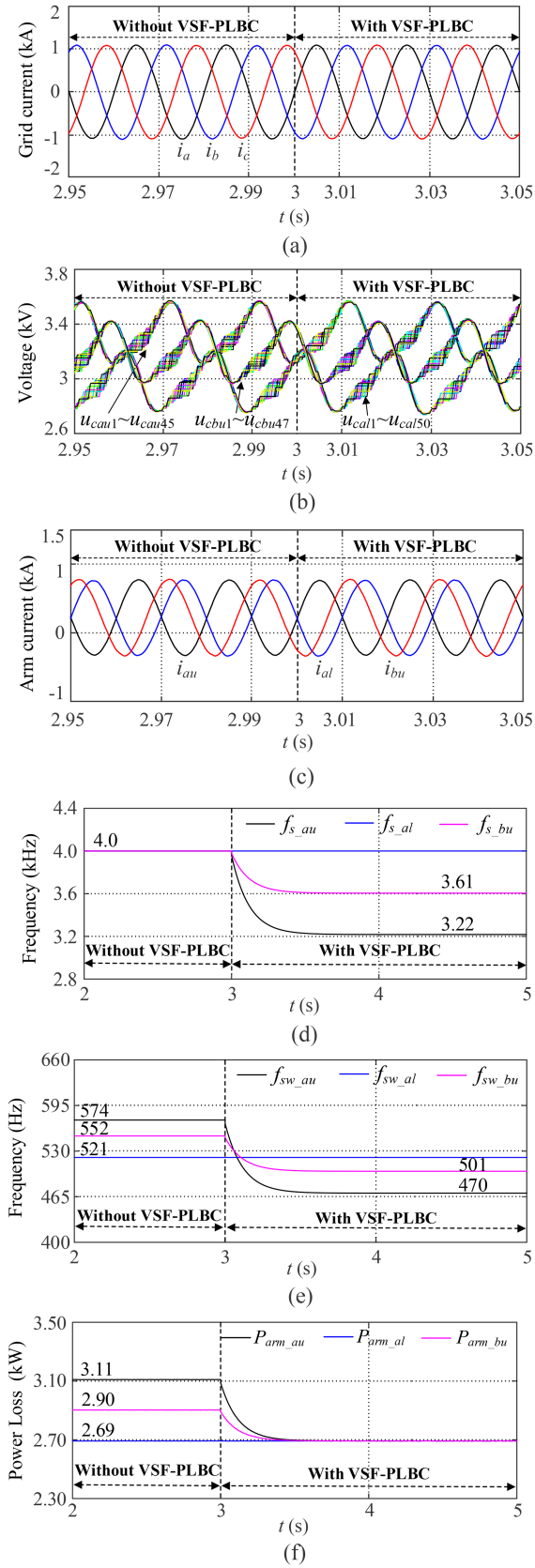

Fig. 18. (a) i_a, i_b, and i_c. (b) u_{cau1}–u_{cau45}, u_{cal1}–u_{cal50}, and u_{cbu1}–u_{cbu47}. (c) i_{au}, i_{al}, and i_{bu}. (d) f_{s_au}, f_{s_al}, and f_{s_bu}. (e) f_{sw_au}, f_{sw_al}, and f_{sw_bu}. (f) P_{arm_au}, P_{arm_al}, and P_{arm_bu}.

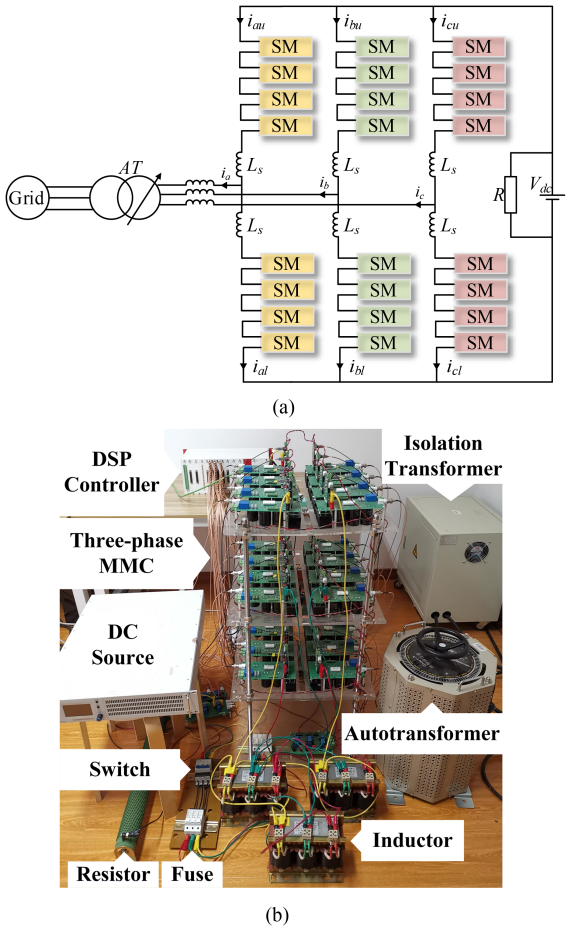

Fig. 19. (a) Experimental circuit. (b) Photograph of experimental platform.

shows that P_{arm_au} and P_{arm_al} in phase A and P_{arm_al} in phase B are unbalanced before 3 s because of SM bypass, where the differences are 0.42 and 0.21 kW. Since 3 s, the proposed VSF-PLBC is enabled, and the power losses P_{arm_au}, P_{arm_al}, and P_{arm_au} become balanced.

VII. Experimental Studies

Fig. 19(a) shows the three-phase MMC experimental circuit configuration, which is built in the laboratory to verify the proposed VSF-PLBC. Fig. 19(b) illustrates the experimental platform photo. The dc link of the MMC consists of a dc power supply and the load resistance. The grid side of the MMC adopts an autotransformer *AT* to connect to the grid. The SM uses FF75R12YT30 as the switch/diode. The digital signal process controller executes system control algorithm and transfers switching signals through optical fibre to the gate driver of each SM. The detailed experimental platform parameters are shown in Table IV.

A. Case I: Normal Situation

Fig. 20 shows the performances of the three-phase MMC under normal situation. Fig. 20(a) shows the upper arm output voltage u_{au} and lower arm output voltage v_{al}, the output current

TABLE IV
EXPERIMENTAL SYSTEM PARAMETERS

Parameter	Value
Rated Power (kW)	1
DC-link voltage V_{dc} (V)	200
Grid line-to-line Voltage (V)	82
Number of SM per arm N	4
SM capacitance (mF)	2.35
Arm inductance L_s (mH)	3
Filter inductance L_f (mH)	3
Proportional gain of PI controller	20
Integral gain of PI controller	330

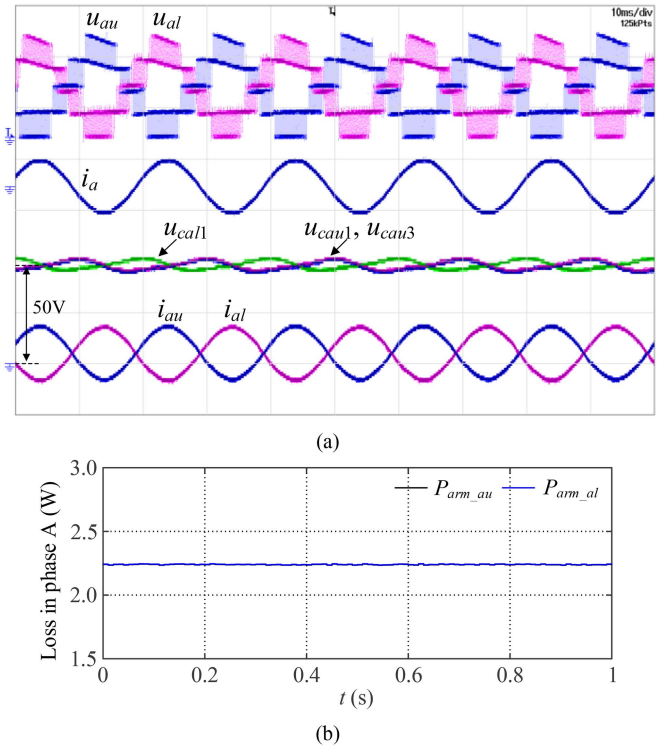

Fig. 20. (a) Experimental waveforms. u_{au} and u_{al} (100 V/div); i_a (20 A/div); u_{cau1}, u_{cau3}, and u_{cal1} (25 V/div); i_{au} and i_{al} (10 A/div). Time base is 10 ms/div. (b) P_{arm_au} and P_{arm_al}.

i_a in phase A, the upper arm SM capacitor voltages u_{cau1}, u_{cau3} and lower arm SM capacitor voltage u_{cal1} in phase A, the upper arm current i_{au}, and the lower arm current i_{al} in phase A. Fig. 20(b) shows that the power losses P_{arm_au} and P_{arm_al} in phase A are almost the same under normal situation.

B. Case II: SM Bypass

Fig. 21 shows the performances of the MMC with one SM bypass in the upper arm of phase A. Here, the proposed VSF-PLBC is enabled since 2.4 s. Fig. 21(a) shows the upper arm output voltage u_{au} and lower arm output voltage u_{al} in phase A, the output current i_a in phase A, the upper arm SM capacitor voltages u_{cau1}, u_{cau3} and the lower arm SM capacitor voltage u_{cal1} in phase A, the upper arm current i_{au}, and the lower arm current i_{al} in phase A.

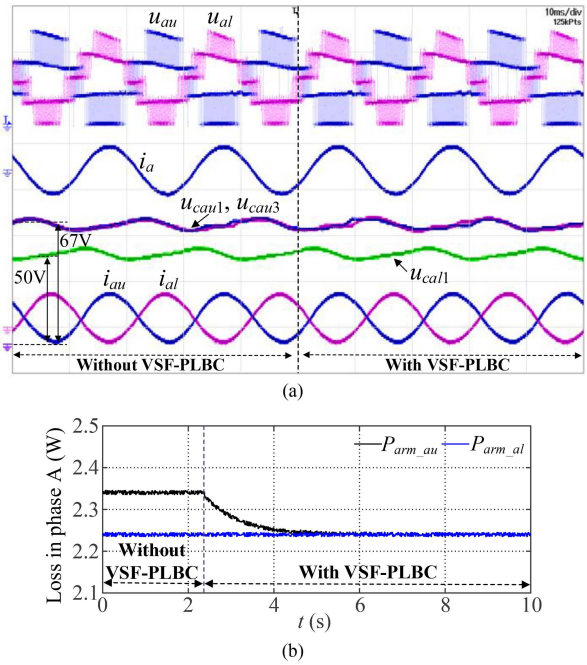

Fig. 21. (a) Experimental waveforms. u_{au} and u_{al} (100 V/div); i_a (20 A/div); u_{cau1}, u_{cau3}, and u_{cal1} (25 V/div); i_{au} and i_{al} (10 A/div). Time base is 10ms/div. (b) P_{arm_au} and P_{arm_al}.

In Fig. 21(a), the upper arm capacitor voltages u_{cau1}, u_{cau3} are higher than the lower arm capacitor voltage u_{cal1} owing to SM bypass in the upper arm of phase A. Fig. 21(b) shows that the power losses P_{arm_au} and P_{arm_al} in phase A are unbalanced without proposed VSF-PLBC, where the maximum difference is about 0.1 W. After proposed VSF-PLBC is enabled, the P_{arm_au} and P_{arm_al} in phase A become balanced.

VIII. CONCLUSION

In this article, the power loss distribution in the arms of three-phase MMC under SM bypass was analyzed in detail. The SM bypass would result in the unbalanced SM voltage and switching frequency among arms with different number of healthy SMs, and lead to unbalanced power loss distribution among the arms in three-phase MMC with SM bypass. A VSF-PLBC was proposed in this article to improve the performance of the MMC with SM bypass. Through the regulation of the sampling frequency for AISN in the arm of the MMC, the power losses among the arms of three-phase MMC can be kept balanced, which could significantly improve the reliability of the MMC under SM bypass. The simulation and experiment were conducted in the laboratory, and the simulation and experiment results verified the effectiveness of the proposed VSF-PLBC.

APPENDIX

In the BAN-based capacitor voltage-balancing control, as shown in Fig. 2, the total switching times N_{total} in one fundamental cycle can be approximately expressed as [19], [31]

$$N_{\mathrm{total}} = N_{\mathrm{BAN}} T_f f_s + N_e \tag{25}$$

where N_e is the extra switching times in one fundamental cycle produced by the nearest level modulation algorithm. Considering the SM bypass, the N_e can be approximately expressed as [19], [31]

$$N_e = \frac{V_{\rm dc}[(1+m)-(1-m)]}{2U_{cf}} = mN_n(1-\lambda). \tag{26}$$

Based on (25) and (26), the SM's average switching frequency $f_{\rm sw}$ can be obtained as [19], [31]

$$f_{\rm sw} = \frac{N_{\rm total}}{N_n(1-\lambda)T_f} = \frac{N_{\rm BAN}f_s}{N_n(1-\lambda)} + \frac{m}{T_f}. \tag{27}$$

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