The Enhanced Modular Multilevel Converter With DC Fault Blocking Capability

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***Abstract*—The large energy-storage requirement and lack of dc fault-tolerant capability are the major drawbacks of modular multilevel converters (MMC). To address these issues, alternate hybrid topologies have been developed, but these are all non-modular, and hence, MMC remains the most preferred topology for high-power applications. In this article, a new submodule (SM) structure is proposed that consists of five switches and a capacitor. Based on this SM, a novel enhanced modular multilevel converter (EMMC) is developed, which is fully modular, scalable, and requires fewer switches and capacitors. It also possesses the features of reduced energy-storage requirement and dc fault-tolerant capability. The structures and operating principles of proposed SM and EMMC topology are presented. The proposed topology is compared with state-of-the-art topologies in terms of the switch counts, SM capacitors, and isolated power-supplies requirements to highlight the main features of EMMC. The proposed EMMC is an effective and more efficient converter solution compared with the major existing high-power hybrid converters. Moreover, it has a fully modular structure. A 21-level, grid-connected EMMC simulation model is developed to validate its working principles and dc fault-tolerant capability. The working principles and dc fault-tolerant capability are further validated using a scaled-down five-level EMMC experimental prototype.**

***Index Terms*—DC fault-tolerant and energy-storage requirement, enhanced modular multilevel converter (EMMC), modular multilevel converter (MMC).**

I. Introduction

THE high voltage dc (HVdc) transmission systems are becoming a predominant means to process and transfer large power due to the penetration of new renewable sources and the economic aspects of HVdc transmission [1], [2], [3], [4], [5], [6], [7]. Presently, the modular multilevel converter (MMC) is considered as the most preferable voltage source converter solutions for the HVdc systems due to its modular and scalable structure, high efficiency, and excellent harmonic performance [2], [3], [4]. A submodule (SM) is the basic building block of the MMC. The half-bridge SM (HBSM), as shown in Fig. 1(a), is one of the popular structures due to its simple design, fewer components requirement, and higher efficiency. However, the HBSM-based MMC does not have the ability to block/limit the current in the event of a dc-side short-circuit fault. When such a fault occurs, the switches are blocked to avoid conduction of large currents. However, the antiparallel diodes of the switches in HBSMs continue to provide path for the fault current. Hence, the equivalent circuit of MMC during a dc fault can be represented, as shown in Fig. 1(b) [25]. The diodes in this figure represent the equivalent antiparallel diodes in each converter arm. It can be observed from this figure that the ac source feeds fault through the diodes, and hence, it cannot block/limit the current in the event of a dc-side short-circuit fault. The full-bridge SM [FBSM, shown in Fig. 1(c)] based MMC, named the hybrid MMC (HMMC1), can overcome this issue by using the negative voltage state of the FBSM. However, the FBSM requires double the number of switches as compared to the HBSM, which results in higher initial cost and losses. To reduce the switch count and also to have the dc fault-tolerant capability, some structural modifications are made to the HMMC1 by replacing 50% of FBSMs with the HBSMs [8], and the resulting configuration may be termed as HMMC2. Although HMMC2 requires fewer switches compared to HMMC1, but it still requires substantially large number of switches. The clamped-double SM [shown in Fig. 1(d)] (CDSM) based MMC discussed in [20] can further reduce the number of switches as compared to HMMC2 and also, it possesses the dc fault-tolerant capability. The double zero SM [shown in Fig. 1(e)] discussed in [21] uses an SiC device in series with its capacitor to enable two parallel conduction paths for the current during the zero state, thereby reducing the overall losses. Many other structures are also discussed in the literature with the aim to utilize fewer switches and achieve the dc fault-tolerant capability [22], [23]. However, most of these SMs lack in practical feasibility and have complex structure/control.

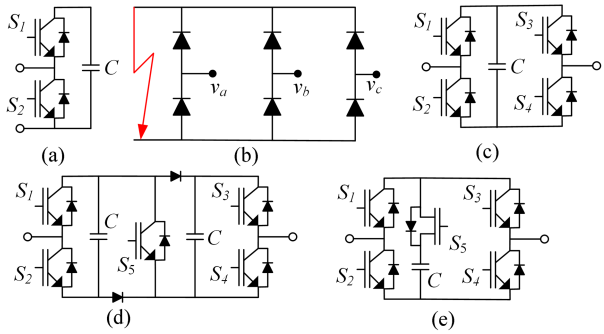

Fig. 1. (a) HBSM. (b) Equivalent circuit of MMC during dc-side fault. (c) FBSM. (d) CDSM. (e) Double zero SM.

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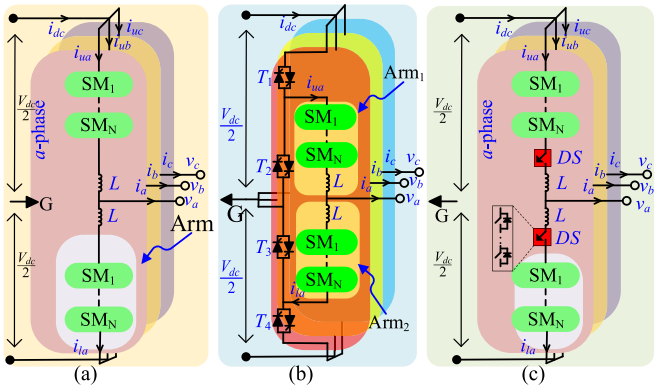

Fig. 2. Schematics of (a) three-phase modular multilevel converter, (b) three-phase MEMC, and (c) three-phase AAC.

To reduce the volume and cost of the converter and to embed the dc fault-tolerant capability, many hybrid multilevel converters are proposed in the literature [5], [6], [9], [10], [11], [12], [13], [14]. A family of such hybrid converters can be realized by combining a two- or three-level structures with the wave-shaping circuits (WSC) [9], [10], [11], [12], [13], [14]. The two- or three-level structures are constructed by a series connection of IGBT stacks, called "director switches" (DS), which operate at a low switching frequency. The WSC, which are constructed by the series connection of SMs, convert the two- or three-level voltage generated by the DS into a multistepped voltage waveform. The alternate-arm converter (AAC) is one of the first and most researched converter topologies in this category [9], [10]. The AAC consists of six arms, each of them is constructed by a WS and a DS, as shown in Fig. 2(c). During the positive half-cycle of the output voltage, the DS of the upper arm is turned ON and the WSC of the upper arm generates the desired multistepped output voltage waveform. Similarly, in the negative half-cycle of the output voltage, the DS of the lower arm is turned ON and the WSC of the lower arm generates the desired multistepped output voltage waveform. As the arms are operated alternatively, the AAC requires only 50% of SMs in each arm as compared to MMC [9], [10]. Furthermore, as the AAC uses FBSMs, the opposite polarity voltage generated by the FBSMs can be used to block the fault current in the event of a dc-side short-circuit fault. Hence, the overall footprint of AAC would be smaller compared to MMC and it also has the dc fault-tolerant capability [9]. However, as the entire output current flows only through one of the arms, the current rating requirement of semiconductors and capacitors is marginally higher in AAC in comparison with MMC. The hybrid two-level converter (H2LC) discussed in [12] is another such hybrid topology, which uses a two-level (2L) converter constructed by series connection of IGBTs, and a WSC on the ac side, which comprises series-connected FBSMs. Like AAC, the WSC of H2LC converts the 2L voltage into a multistepped voltage using the FBSMs. In H2LC too, the FBSMs carry entire output current, and hence, the current rating of devices in H2LC is also higher compared to MMC. The modular-embedded multilevel converter (MEMC) is discussed in [14], whose each phase-leg comprises a set of four switch valves constructed by series connection of thyristors or IGBTs and two arms constructed by series connection of SMs, as shown in Fig. 2(b). The phase-legs in MEMC are operated in such a way that at any time instant two out of the three phase-legs are always connected in series. As the entire dc-link voltage is shared by two phase-legs, for the same voltage rated devices and SM capacitors, the MEMC requires only 50% of SMs compared to MMC for the given dc-link voltage and output power.

The afore-discussed converter topologies aim to embed the dc fault-tolerant capability, reduce the number of devices and SM capacitors compared to MMC. However, none of these hybrid converter topologies are modular. As discussed earlier, they are developed by combining mainly two structures; one is composed of a series connection of SMs, while the other is realized by connecting several lower rated devices in series to act as a high voltage switch. Hence, the modularity is compromised in these converters. Furthermore, as these converters use the series connection of IGBTs, they pose additional challenges, such as synchronization of gate pulses, equal voltage sharing between the series-connected IGBTs, lower reliability, and isolated power supplies to each series-connected IGBT, among many others [5], [6], [15].

In this article, a new multilevel converter, named "enhanced modular multilevel converter" (EMMC), is proposed with an objective to have a fully modular structure while requiring fewer semiconductor devices and SM capacitors, and also, to have the dc fault-tolerant capability. Therefore, the proposed EMMC can overcome the issues highlighted in the discussion presented above in both MMC and the hybrid topologies. The proposed converter comprises two arms in each leg, which are constructed by a series connection of several identical SMs and an inductor. As the proposed converter is fully modular, the number of series-connected SMs can be scaled up or down based on the required voltage ranges.

A new SM structure is also proposed in this article, which results in fulfilling all the set objectives, i.e., fully modular structure, fewer components, and dc fault-tolerant capability. The proposed SM structure consists of five switches and a capacitor. This SM can generate four states, namely, insertion, bypassed, blocked, and open-circuit states. The first three states can be used to operate the SM as the FBSM and the open-circuit state can be used to disconnect the SM/arm from the conduction path. Using the open-circuit state of the proposed SM structure, the EMMC arms are operated to conduct alternatively. A detailed explanation of the converter, SM structure, and their operation is discussed in this article. It is shown that the proposed EMMC requires only half number of SMs as required in MMC for the same dc-link voltage and power. A 3-phase 21-level grid-connected EMMC simulation model is developed in PSCAD to validate its working principles. Furthermore, a five-level laboratory prototype of EMMC is constructed and tested in the lab to experimentally verify its working principles and the dc fault-tolerant capability.

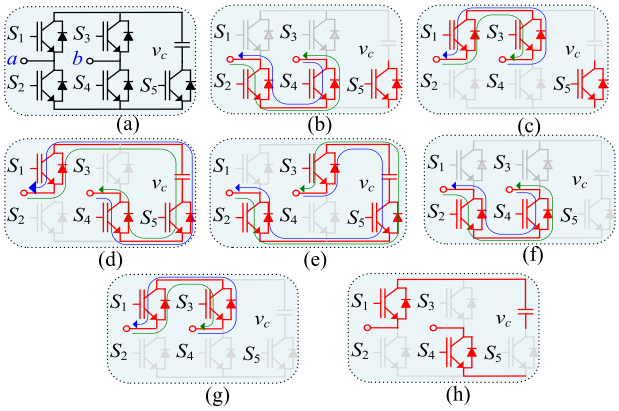

Fig. 3. (a) Circuit configuration of the proposed SM, (b), (c), (f), and (g) zero states, (d) positive state, (e) negative state, and (h) open-circuit state.

II. Proposed Submodule and Enhanced Modular Multilevel Converter Structures

In this section, first, the SM structure and its operating principle are explained and then the proposed EMMC structure and its operating principles are discussed.

A. Proposed Submodule Structure and Its Operation

The circuit configuration of the proposed SM structure is shown in Fig. 3(a). It can be observed that the proposed SM structure consists of a capacitor and five switches (S_1, S_2, S_3, S_4, and S_5), where S_1 is complimentary to S_2 and S_3 is complimentary to S_4. The terminals a and b are the ac output terminals and V_{ab} represents the output voltage of the SM. It can be seen from Fig. 3(b) and (c) that when both the upper switches (S_1 and S_3) or both the lower switches (S_2 and S_4) are turned ON, then V_{ab} is zero, which is termed as the "zero state." In this state, there is a conduction path for either current direction. Hence, the zero state can be achieved using multiple combinations of switches. Similarly, as can be observed from Fig. 3(d), when the switches S_1, S_4, and S_5 are turned ON, then V_{ab} is equal to the capacitor voltage and there is again a conduction path for either direction of the current. Hence, to achieve this "positive state" using the proposed SM, switches S_1, S_4, and S_5 should be turned ON. The proposed SM can also generate negative voltage by turning ON S_2, S_3, and S_5, as shown in Fig. 3(e).

It is clear from the above discussion that when S_5 is turned ON, then, the zero, positive, and negative voltage states can be realized based on the different combination of other switches. Now, when S_5 is turned OFF, it can be observed from Fig. 2(f) and (g) that when both the upper or lower switches are turned ON, then the SM is still in zero state. Therefore, using the proposed SM, the zero state can be realized using four different switching combinations. Finally, it can be observed from Fig. 2(h) that when S_1, S_4 are turned ON, then the SM works in the "open-circuit" state, and it does not let the current to flow. Therefore, the proposed SM can be operated to generate zero, positive, negative voltages, and also, it can operate in the open-circuit mode.

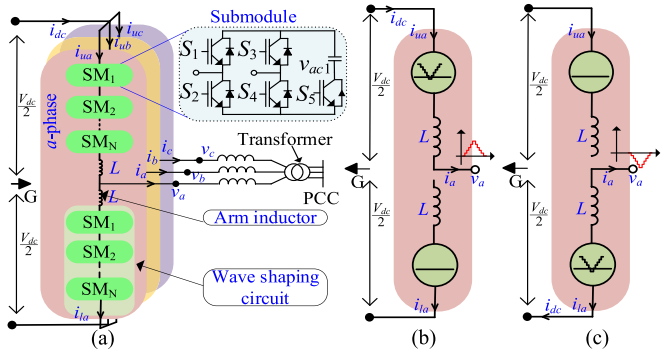

Fig. 4. (a) Three-phase EMMC schematic, single-phase equivalent circuit of EMMC during (b) positive and (c) negative half-cycle.

B. Proposed EMMC Topology and Operating Principles

The circuit configuration of the proposed three-phase EMMC is shown in Fig. 4(a). It can be seen that each phase-leg of EMMC comprises two identical arms, namely the upper and lower arms. Further, each EMMC arm is constructed by a series connection of multiple proposed SMs and an inductor. Based on the output voltage requirement, the state of each SM should be determined and operated accordingly.

In the proposed EMMC, all the three legs are identical, and hence, the a-phase leg is considered from this point onwards to explain the working principle of the converter. From Fig. 4, each EMMC arm has two terminals, namely the positive and negative terminals. The positive terminal of the upper arm is connected to the positive pole of the dc bus and the negative terminal of the lower arm is connected to the negative pole of the dc bus. Further, the negative terminal of the upper arm and the positive terminal of the lower arm are connected together to form the ac terminal of the leg, as shown in Fig. 4(a). As discussed earlier, the proposed SM can also be operated in the open-circuit state. Hence, using the proposed SM, the EMMC arms are operated in a way that the upper arm of a leg would be in conduction during the positive half-cycle of the output ac voltage and the lower arm would be in conduction during the negative half-cycle of the output ac voltage. Hence, during the positive half-cycle of the output voltage, the lower arm SMs are in the open-circuit mode and the desired multistepped output voltage is solely generated by the upper arm. The single-phase equivalent circuit of EMMC during the positive half-cycle of output ac voltage is shown in Fig. 4(b). From this figure, by applying KVL, the upper arm voltage can be expressed as

$$v_{ua} = \frac{V_{\rm dc}}{2} - v_a \qquad \text{for } v_a \geq 0 \tag{1}$$

where v_{ua} is the a-phase upper arm voltage, $V_{\rm dc}$ is the dc-link voltage, and v_a is the a-phase output ac voltage. Considering the zero crossing of v_a as the reference point, it can be expressed as

$$v_a = V_m \sin\omega t = \frac{mV_{\rm dc}}{2} \sin\omega t \tag{2}$$

where V_m is the ac-side voltage amplitude, m is the modulation index, which is defined as $V_m/(\frac{V_{\rm dc}}{2})$, and ω is the angular

frequency. Hence, the upper arm voltage is expressed as

$$v_{ua} = \frac{V_{\rm dc}}{2} - \frac{mV_{\rm dc}}{2}\sin\omega t \qquad \text{for } 0 \le \omega t \le \pi. \tag{3}$$

From Fig. 4(b), as the lower arm SMs are in the open-circuit state, during the positive half-cycle of the output ac voltage, the upper arm current can be expressed as

$$i_{ua} = I_m \sin(\omega t + \phi) \qquad \text{for } 0 \le \omega t \le \pi \tag{4}$$

where i_{ua} is the upper arm current, I_m and ϕ are the amplitude and power factor angle of the converter ac output current, respectively.

Similarly, during the negative half-cycle of v_a, the upper arm SMs operate in the open-circuit mode so that the desired multistepped ac output voltage is generated solely by the lower arm. The single-phase equivalent circuit of EMMC during the negative half-cycle of v_a is shown in Fig. 4(c). From this figure and (2), the lower arm voltage and current can be expressed as

$$v_{la} = \frac{V_{\rm dc}}{2} + \frac{mV_{\rm dc}}{2}\sin\omega t \qquad \text{for } \pi \le \omega t \le 2\pi \tag{5}$$

$$i_{la} = -I_m \sin(\omega t + \phi) \qquad \text{for } \pi \le \omega t \le 2\pi. \tag{6}$$

Therefore, it is clear from the above discussion that the upper arm shapes the output voltage during the positive half-cycle while the lower arm does the same during the negative half-cycle. The number of steps in the positive half-cycle of v_a is equal to the number of SMs in the upper arm (N_{ua}) and the number of steps in the negative half-cycle of v_a is equal to the number of SMs in the lower arm (N_{la}). To have symmetry, N_{ua} and N_{la} should be equal ($N_{ua} = N_{la} = N$). Therefore, the proposed EMMC with N SMs per arm can generate a maximum of $2N{+}1$ (including zero voltage level) levels in its ac output voltage. It can further be observed from (3) that when v_a is zero, the upper arm voltage is $V_{\rm dc}/2$ and when v_a assumes its peak value ($V_{\rm dc}/2$), the upper arm voltage is zero. Similarly, from (4), the lower arm voltage of EMMC varies between 0 and $V_{\rm dc}/2$. On the other hand, it is to be noted that the arm voltage in MMC varies between 0 and $V_{\rm dc}$. Therefore, for the same dc-link voltage and device voltage ratings, the proposed EMMC requires only half number of SMs as required in MMC.

C. Energy Balance

To generate fairly accurate output ac voltage, the SMs capacitor voltages should be balanced at their nominal voltage. To fulfil this objective, the net energy exchanged by the arm should be zero in each fundamental cycle of the output voltage/current. If the net energy exchanged is not zero, the SMs capacitor voltages would keep on increasing or decreasing based on the net gain or loss of the arm energy, respectively. In this section, an analysis of the net energy exchanged by an arm of the proposed converter is presented to examine whether the SMs capacitor voltages are balanced naturally or not.

From (4), (6), and Fig. 4, the entire output current flows through the upper arm during the positive half-cycle and it flows through the lower arm during the negative half-cycle of the output ac voltage. Therefore, the net energy exchanged by the upper arm can be expressed as

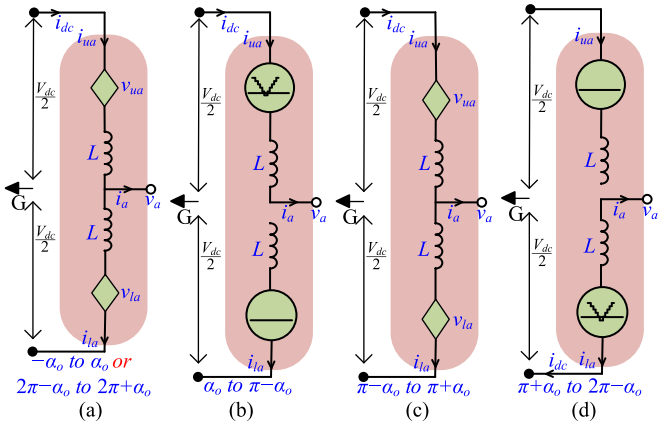

Fig. 5. Equivalent circuit of EMMC during (a), (c) overlap and (b), (d) nonoverlap periods.

$$\Delta E = \int_0^{2\pi} v_{ua} i_{ua} d\omega t \Rightarrow \Delta E = \int_0^{\pi} v_{ua} i_{ua}\, d\omega t$$
$$(\because\ i_{ua} = 0\ for\ \pi \le \omega t \le 2\pi). \tag{7}$$

Substituting the upper arm voltage and current expressions from Section II-B in (7) and expanding the integral, the net energy exchanged by the upper can be expressed as

$$\Delta E = V_{\rm dc}\cos\phi - \frac{mV_{\rm dc}}{4}\cos\phi\pi\ . \tag{8}$$

From (8), the conditions for which the net energy exchanged by the EMMC arm is zero can be expressed as

$$\cos\phi = 0; \qquad m = 4/\pi. \tag{9}$$

Therefore, the SMs capacitor voltages are naturally balanced only for the operating conditions as in (9). These operating conditions are termed as "sweet spots." However, for the applications such as HVdc, the converter should be able to operate satisfactorily for a wide range of operating points. Some of the other hybrid converters discussed earlier in Section I, such as AAC [9], H2LC [12], and parallel hybrid converter [15], also face the same issues of a restricted operating range. To address this issue in EMMC, the overlap technique, that was proposed earlier for AAC, is utilized, and extended for achieving the energy balancing in EMMC for a wide range of operating conditions. In this technique, for a small duration, termed as the "overlap period," both the upper and lower arms are kept in the conduction mode. During this overlap period, the common mode current flowing through the both the arms is controlled in such a way that the energy gained in the nonoverlap period is lost during the overlap period and vice versa. The equivalent circuits of EMMC during the overlap period, positive and negative half cycles of v_a are shown in Fig. 5(a) and (c), respectively It can be seen from Fig. 5(a) and (c) that both upper and lower arms are in conducting state during the overlap period. Hence, the leg and dc bus form a closed loop. Using this closed loop, the overlap control schemes regulate the current in upper and lower arms to a predetermined magnitude such that the net energy exchanged by the arms is zero in a fundamental cycle.

Therefore, from Fig. 5(a) and (b), the upper arm of EMMC conducts from $-\alpha_o$ to $\pi+\alpha_o$, where $\alpha_o=\omega t_d$ is the overlap angle in radians and t_d is the overlap period in section. Similarly, the lower arm conducts from $\pi-\alpha_o$ to $2\pi+\alpha_o$, as shown in Fig. 5(c) and (d). Therefore, the expressions of the upper and lower arms voltage are modified as

$$\begin{aligned}
v_{ua} &= \frac{V_{\rm dc}}{2} - V_m \sin\omega t \qquad \text{for} -\alpha_o \le \omega t \le \alpha_o \\
v_{ua} &= \frac{V_{\rm dc}}{2} - V_m \sin\omega t \qquad \text{for } \alpha_o \le \omega t \le \pi-\alpha_o \\
v_{ua} &= \frac{V_{\rm dc}}{2} - V_m \sin\omega t \qquad \text{for } \pi-\alpha_o \le \omega t \le \pi+\alpha_o \\
v_{ua} &= \text{ open circuit} \qquad\qquad \text{for } \pi+\alpha_o \le \omega t \le 2\pi-\alpha_o
\end{aligned} \tag{10}$$

$$\begin{aligned}
v_{la} &= \frac{V_{\rm dc}}{2} + V_m \sin\omega t \qquad \text{for} -\alpha_o \le \omega t \le \alpha_o \\
v_{la} &= \text{open circuit} \qquad\qquad \text{for } \alpha_o \le \omega t \le \pi-\alpha_o \\
v_{ua} &= \frac{V_{\rm dc}}{2} + V_m \sin\omega t \qquad \text{for } \pi-\alpha_o \le \omega t \le \pi+\alpha_o \\
v_{ua} &= \frac{V_{\rm dc}}{2} + V_m \sin\omega t \qquad \text{for } \pi+\alpha_o \le \omega t \le 2\pi-\alpha_o.
\end{aligned} \tag{11}$$

Similarly, the upper arm current can be expressed as

$$\begin{aligned}
i_{ua} &= i_{\rm bal} \qquad\qquad\quad \text{for} -\alpha_o \le \omega t \le \alpha_o \\
i_{ua} &= I_m \sin(\omega t+\phi) \qquad \text{for } \alpha_o \le \omega t \le \pi-\alpha_o \\
i_{ua} &= i_{\rm bal} \qquad\qquad\quad \text{for } \pi-\alpha_o \le \omega t \le \pi+\alpha_o \\
i_{ua} &= 0 \qquad\qquad\qquad \text{for } \pi+\alpha_o \le \omega t \le 2\pi-\alpha_o
\end{aligned} \tag{12}$$

where $i_{\rm bal}$ is the balancing current to be controlled during the overalp duration for making the net energy zero in EMMC. Now, the upper arm energy during the overlap (ΔE_O) and nonoverlap (ΔE_{NO}) periods can be expressed as

$$\Delta E_{NO} = \left(2\cos\alpha_o - \frac{m}{2}\sin\alpha_o - \frac{m}{2}\left(\frac{\omega T}{2}-2\alpha_o\right)\right) \times \frac{V_{\rm dc} I_m}{2\omega}\cos\phi \tag{13}$$

$$\Delta E_o = \frac{2V_{\rm dc} I_{\rm bal}\alpha_o}{\omega}. \tag{14}$$

To balance the SMs capacitor voltages, the sum of energy gained by them during the overlap and nonoverlap periods should be equal to zero. Therefore, based on the operating conditions, "t_d" is varied to achieve the voltage balancing in the EMMC.

D. Rating Requirements of S_5 in the Proposed SM

As discussed earlier in Section II-A, the proposed SM can be operated to generate either zero, positive, or negative voltages, and it can also operate in the open-circuit mode. The equivalent circuit of the proposed SM and the conduction paths during the respective operating modes are shown in Fig. 3. In Fig. 3, the conducting IGBTs are shown in red color, while the nonconducting switches are shown in gray color. It can be observed from Fig. 3 that the current flowing through all the IGBTs is the same as the arm current when the corresponding IGBT is turned ON, and zero when it is turned OFF. Hence, depending on the respective active and reactive power values that the converter needs to exchange with the grid/load, all switches would be experiencing peak value of arm current at different instants of their conduction. Therefore, the current rating requirement of all the IGBTs in the proposed SM is the same.

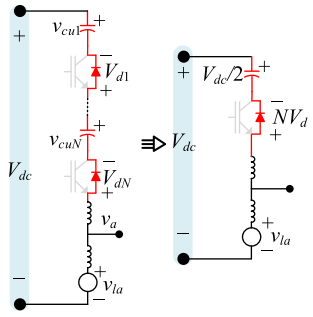

Fig. 6. Equivalent circuit of EMMC during the blocking mode.

The voltage rating requirement of an IGBT can be determined based on the maximum voltage that appears across it. The equivalent circuit of one of the EMMC legs, as shown in Fig. 6, is considered for analyzing the voltage rating requirement. This equivalent circuit corresponds to an operating mode when the upper arm in the EMMC phase-leg is in the open-circuit mode while the lower arm is in conduction mode. Since the device under consideration is S_5, the maximum voltage appearing across S_5 when it is in OFF state should be determined. It can be observed from Fig. 6 that S_5 is turned OFF during the open-circuit mode and, hence, this case is considered where the SMs in upper arm are in the open-circuit mode.

As the switches S_1 and S_4 are turned ON in this mode, each SM in the upper arm can be represented as a capacitor in series with the antiparallel diode of S_5, as shown in Fig. 6. Now, by replacing the capacitor with a series-connected diode in each SM of upper arm with a lumped capacitor and a diode, the equivalent circuit can be simplified to be as in Fig. 6(b). As N cascaded capacitors, each having a voltage of $V_{\rm dc}/2N$, are represented using a single capacitor, the voltage across the lumped capacitor can be expressed as $V_{\rm dc}/2$. Similarly, as N cascaded diodes are represented using a single diode, the voltage across this diode can be expressed as NV_d, where V_d is the voltage across each diode. Applying KVL, it can be expressed as

$$-V_{\rm dc} + \frac{V_{\rm dc}}{2} - NV_d + v_{la} = 0 \Rightarrow N\,V_d = v_{la} - \frac{V_{\rm dc}}{2}. \tag{15}$$

Substituting (5) into (15), the voltage across the diode can be expressed as

$$V_d = \frac{mV_{\rm dc}}{2N}\sin\omega t \qquad \text{where } \pi \le \omega t \le 2\pi. \tag{16}$$

Therefore, it is clear from (16) that the maximum blocking voltage requirement of S_5 is $V_{\rm dc}/2N$, which is the same as that of the other four switches. Hence, it can be concluded that the

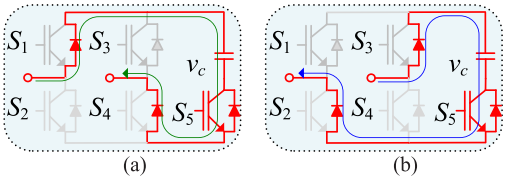

Fig. 7. Conduction path of (a) positive and (b) negative direction of current during the dc-side fault case.

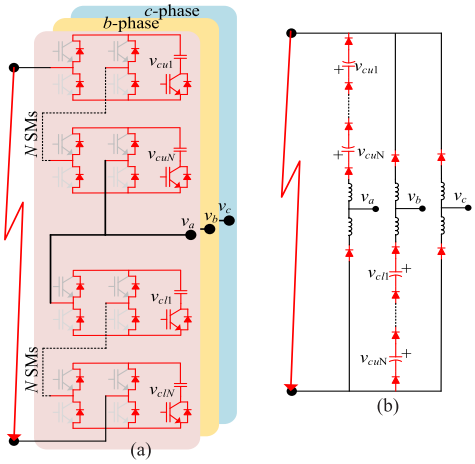

Fig. 8. (a) Equivalent circuit of EMMC. (b) Simplified equivalent circuit of EMMC during a dc-side short-circuit fault.

voltage rating requirement of all IGBTs in the proposed SM is the same and equal to $V_{\rm dc}/2N$.

E. DC Fault-Tolerant Capability

The proposed SM, having the negative voltage state, possesses the ability to block the fault current in the event of a dc-side short-circuit fault. The dc fault-tolerant capability can be achieved if the inserted capacitors by the SMs can oppose the fault current flow. The fault current flow can be opposed using the proposed SM by turning ON switch S_5 and turning OFF all the other switches. This is the blocking state of the proposed SM and its equivalent circuit during this state is shown in Fig. 7. It can be observed from Fig. 7(a) and (b) that irrespective of the current direction, the SMs capacitor voltage always opposes the current flow. The equivalent circuit of EMMC during the blocking state of the SMs is shown in Fig. 8(a). Based on the ac-side voltage polarity, at any time instant, the diode in one of three upper arms and one of three lower arms would be forward-biased. The equivalent circuit of EMMC when the diodes in upper arm of a-phase and lower arm of b-phase are forward-biased is shown in Fig. 8(b).

Now, applying KVL, the fault current expression can be derived as

$$\begin{aligned} 2L\,\tfrac{di_{\rm fault}}{dt} &= v_{ab} - \left(\sum_{i=1}^{N} v_{cui} + \sum_{j=1}^{N} v_{clj}\right) \\ 2L\,\tfrac{di_{\rm fault}}{dt} &= v_{ab} - V_{\rm dc}. \end{aligned} \tag{17}$$

Therefore, from (17) and Fig. 8(b), the line–line ac-side voltage drives the fault current and the sum of all the SMs capacitor voltages in upper arm of a-phase and lower arm of b-phase opposes the fault current. From (2), the peak value of the line–line ac-side voltage is $\sqrt{3}V_{\rm dc}/2$ and the sum of all the SMs capacitor voltages in upper arm of a-phase and lower arm of b-phase is $V_{\rm dc}$. Therefore, at any time instant, the opposing voltage is greater than the driving voltage. Hence, the fault current in EMMC ceases naturally when all the SMs are operated in the blocking state.

It is hence established that the proposed EMMC has the ability to oppose the dc fault current and it can protect from the large fault currents in the event of a dc-side short circuit.

TABLE I
COMPARISONS OF MMC, HMMC, AAC, AND EMMC

Parameter	MMC	HMMC2	HMMC1	AAC	EMMC
Number of SMs	12N	12N	12N	6N	6N
Number of capacitors	12N	12N	12N	6N	6N
Total switches	24N	36N	48N	30N	30N
Power supplies	24N	30N	36N	24N	18N
Dc-fault tolerant	No	Yes	Yes	Yes	Yes
Modularity	Fully	Fully	Fully	Partly	Fully
Peak value of arm current (max)	$\frac{3I_m}{4}$	$\frac{3I_m}{4}$	$\frac{3I_m}{4}$	I_m	I_m
RMS value of arm current (max)	$\frac{\sqrt{3}I_m}{4}$	$\frac{\sqrt{3}I_m}{4}$	$\frac{\sqrt{3}I_m}{4}$	$\frac{I_m}{2}$	$\frac{I_m}{2}$

Note: I_m is the peak valve of output current

III. COMPARATIVE ANALYSIS

To highlight its main features, the proposed EMMC is compared with the other major high-power converters, such as MMC, hybrid MMC (HMMC1 and HMMC2), and AAC in terms of device count, gate driver power supplies count, and efficiency. For this comparison analysis, it is considered that the number of output voltage levels in all converters is same and equal to $2N+1$ (where N is the number of SMs per arm in EMMC), and the voltage blocking capability of a single IGBT utilized in all the considered converters is equal to $V_{\rm dc}/2N$.

A. Device Count

For $2N+1$ ac-phase output voltage levels, the proposed EMMC requires N SMs per arm, MMC requires $2N$ SMs [1], [2], [3], AAC requires N SMs [9], and HMMC requires N HBSMs and N FBSMs per arm [7]. As discussed earlier, the arm voltage in EMMC can attain the maximum value of $V_{\rm dc}/2$, and hence, the average voltage of each SM capacitor would be equal to $V_{\rm dc}/2N$. It can be observed from Fig. 4 that the maximum voltage across the switches S_{1-5} in the proposed SM is equal to v_c, which is equal to $V_{\rm dc}/2N$. Therefore, the total number of switches required in a three-phase EMMC is $30N$ ($5N \times 2 \times 3$). Similarly, the number of switches required in MMC, HMMC, and AAC can be obtained to be as $24N$, $36N$, and $30N$, respectively, as listed in Table I.

It clear from the above discussion that the MMC requires fewer devices compared to the other high-power converters. However, the MMC using the HBSMs does not possess the dc fault-tolerant capability. On the other hand, the other three considered converters have the dc fault-tolerant capability, and

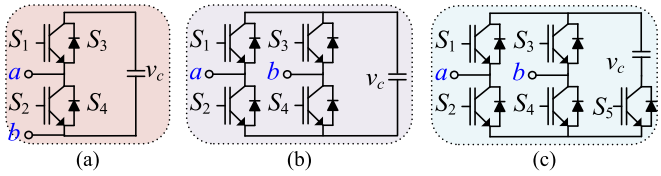

Fig. 9. Circuit schematics of (a) HBSM, (b) FBSM, and (c) proposed SM.

among these converters, the EMMC and AAC require fewer switches compared to the HMMC. However, as discussed earlier, the conventional AAC is not modular as it requires a series connection of switches to operate as the high voltage DSs. On the other hand, the EMMC is fully modular as it avoids the series connection of switches.

B. Gate Driver Power Supply

To turn ON the IGBT, a gate pulse with respect to its emitter is required. The IGBTs whose emitters are not connected to the same potential cannot be driven using the same power supply, and hence, an independent isolated power supply is required for each of such IGBTs. Therefore, the total number of isolated power supplies required to drive all the IGBTs is dependent on the number of unique connection points of the IGBT emitters. For example, an HBSM [shown in Fig. 9(a)] requires two isolated power supplies to drive the two switches. On the other hand, an FBSM requires only three isolated power supplies to drive four switches as the emitters of the lower IGBTs [S_2 and S_4 in Fig. 9(b)] are at the same potential in FBSM [19].

As discussed earlier, the proposed converter requires N number of the proposed SMs per arm for $2N+1$ phase output voltage levels. It can be observed from Fig. 9(c) that emitters of the switches S_2, S_4, and S_5 in the proposed SM are at the same potential, and hence, these three IGBTs can be driven using a single power supply. On the other hand, the emitter potentials of S_1 and S_3 are different, and hence, these switches require two isolated power supplies. Therefore, the proposed SM requires a total of three isolated power supplies to drive the five IGBTs. Hence, in an EMMC with N SMs per arm, the total number of isolated power supplies required is $18N$ ($3N \times 2 \times 3$). On the other hand, the MMC comprises $2N$ HBSMs in its each arm for $2N+1$ phase output voltage levels, and hence, it requires $24N$ isolated power supplies. Similarly, as the HMMC comprises N HBSMs and N FBSMs, it requires $30N$ isolated power supplies. The AAC consists of N FBSMs and N series-connected IGBTs (DS). As can be observed from the AAC schematic shown in Fig. 2, the emitter of each IGBT in the DS is at different potential, and hence, each IGBT requires a dedicated isolated power supply. Therefore, the total number of power supplies required in AAC is $24N$. For better understanding and clarity, these numbers are listed in Table I. It can be observed from the above discussion and Table I that the EMMC requires the least number of isolated power supplies to drive all IGBTs for the same dc link and ac output voltages. Hence, the overall cost and complexity of EMMC from the gate driver power supply point of view would be lower as compared to the other major converters.

TABLE II
SIMULATION PARAMETERS

Parameter	Values	Parameter	Values
dc-link voltage (V_{dc})	200 kV	Arm Inductance	0.5 mH
No. of SMs per arm	10	Grid voltage (L-L)	400 kV
SMs capacitance	2.5 mF	Transformer ratio	400/100
SMs capacitor voltage	10kV	Switching frequency	1 kHz

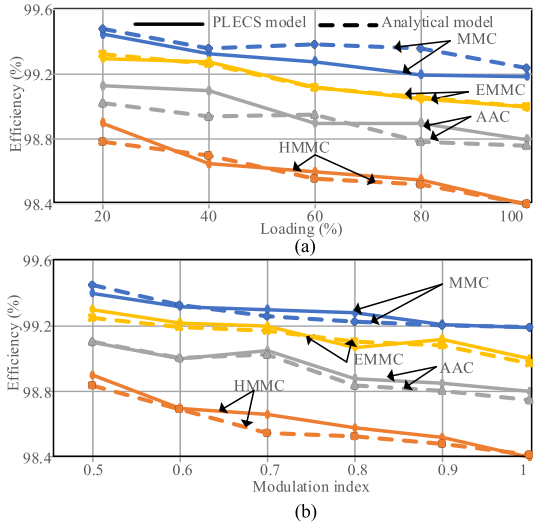

Fig. 10. Efficiency of MMC, HMMC2, AAC, and EMMC with respect to the varying values of (a) loading and (b) modulation index.

C. Efficiency

To highlight the advantages of the proposed EMMC, a detailed model of EMMC is developed in PLECS using the device characteristics of ABB made 6.5 kV, 1 kA IGBT (5SNA1000G650300, [24]). This model uses the same parameters as used in the simulation model, which is discussed in Section IV (listed in Table II). In this model, the devices are modeled in detail such that they all have the characteristics of a real-time device. The detailed models of devices are readily available in the form of packages from the devices manufacturers, which are imported into the PLECS to build the proposed EMMC. Now, this model calculates the device losses by considering the exact current flowing the devices when it is ON, the voltage across the switch and current through the switch when it is switching (ON or OFF), and the junction temperature and thermal conductivity. Similar models are also developed for the other converters under consideration and their corresponding efficiencies are obtained at different loading conditions and modulation indices. The obtained results are plotted in Fig. 10 (solid lines) for easy comparison. It can be observed from this figure that the efficiency of MMC is higher compared to all the other converters and EMMC stands second for the entire range of loading conditions. Furthermore, the converters efficiency drops as the loading increases due to the increased current through the semiconductors for larger loading.

To further justify the superiority of EMMC over the other major converters, an analytical model is developed to calculate the switching and conduction losses of the four converters under

consideration. This analytical model is based on the methodology discussed in [16]. In this analysis, similar to the PLECS model, the converter power rating is considered the same as that of the simulation model, which is discussed in Section IV (see Table II).

As discussed in [16], the conduction and switching losses of a semiconductor switch can be expressed as

$$P_{\text{cond}} = a_1\, i\,(t) + b_1 i^2\,(t)$$
$$E_{\text{sw}} = a_2\, i\,(t) + b_2 i^2\,(t) \tag{18}$$

where $i(t)$ is the instantaneous current flowing through the switch and a_1, a_2, b_1, and b_2 are coefficients derived from the datasheet. The same device characteristics, i.e., ABB made 6.5 kV, 1 kA IGBT (5SNA1000G650300, [24]), used in PLECS model are used in this analytical model as well. The coefficients (a_1, b_1) are obtained from the curve fitting of the I_C versus V_{CE} plots given in this IGBTs' datasheet and are obtained as $a_1 = 1.6577$ and $b_1 = 0.001425$. similarly, the coefficients are obtained from the curve fitting of the E versus I_C plots given in this IGBTs' datasheet and obtained as $a_2 = 0.01277$ and $b_2 = -\,7 \times 10^{-7}$. These values of a_1, a_2, b_1, and b_2 are used in (18) along with the corresponding expressions of $i(t)$ for the different converters under consideration to calculate the conduction and switching losses.

As can be observed from (18), the converter losses are dependent on the current. Hence, to determine the converter losses at different operating conditions, the relation between the rated current and the current at a given modulation index "m and "$k\%$" of loading can be obtained as

$$I_{m,k} = \frac{m \times k}{100}\, I_{\text{rated}} \tag{19}$$

where I_{rated} is the rated current. Now combining (18) and (19), the converter losses at different operating conditions can be obtained as

$$P_{\text{cond}(m,k)} = a_1\, \frac{m \times k}{100} i_{\text{rated}}\,(t) + b_1 \left(\frac{m \times k}{100}\right)^2 i^2_{\text{rated}}\,(t)$$
$$E_{\text{SW}(m,k)} = a_2\, \frac{m \times k}{100} m i_{\text{rated}}\,(t) + b_2 \left(\frac{m \times k}{100}\right)^2 i^2_{\text{rated}}\,(t)\,. \tag{20}$$

Using (20) and the considered operating condition, the converter losses of each converter under consideration are determined. The obtained loss values are used to determine the corresponding efficiency values of the considered converters, as plotted in Fig. 10 (dashed lines). It can be observed from Fig. 10(a) and (b) that the efficiency numbers obtained from analytical model are closely matching with that obtained from the PLECS model. Furthermore, as can be observed from (20), the conduction and switching losses are quadratically related to "m" and loading ("k"). Hence, as the values of k and/or m are increased, the losses are expected to increase, and therefore, the converter efficiency would be decreased. The same can be observed from Fig. 10(a) and (b).

It can further be noted that the efficiency of EMMC is superior to HMMC as the EMMC requires fewer switches than the HMMC. It can further be observed that although both the AAC and EMMC require the same number of switches, the efficiency of EMMC is higher than that of AAC. This is because, in AAC, irrespective of the SM state, two switches from each SM and all the switches in the DS carry current. Hence, the total number of switches in conduction would be $3N$ in each arm, which is equivalent to the conduction of three switches per SM. On the other hand, in the proposed SM, three switches conduct during the positive state ($+v_c$ output) and only two switches conduct during the zero state (zero output). Hence, the total number of switches carrying current in EMMC is always less than or equal to $3N$. Therefore, the overall losses in EMMC would be lower compared to that in AAC, which resulted in higher efficiency. Finally, as the MMC requires fewer semiconductor devices, its efficiency is higher than that of the EMMC. However, the MMC is not tolerant to dc faults.

D. Current Stress

The current stress of the IGBTs and the SM capacitors is one of the important converter design parameters. These current stresses depend on the peak and rms values of current flowing through the respective converter components. As the current through the devices and capacitors is the same as the arm current when they are inserted, their peak and rms values would be equal to those of the arm current values. As discussed in Section II-B, the EMMC arm current is equal to its output current when the corresponding arm is in conduction mode, and it is zero when it is in open-circuit mode. Therefore, the peak value of EMMC arm current is equal to its output current peak value. Using the arm current expression of EMMC in (4), the rms value of arm current can be obtained as half the peak value of output current, as listed in Table I.

The peak and rms values of currents through the devices of the other converters under consideration are similarly determined using their corresponding arm current expressions and are listed in Table I. It can be seen from Table I that the peak and rms values of device currents are lower in MMC and HMMC compared to that in AAC and EMMC. This is due to the current sharing between the arms in each phase leg of MMC and HMMC. Therefore, the proposed EMMC requires slightly higher current rated devices compared to MMC and HMMC.

It is clear from the above discussion that the proposed EMMC possesses all important features of MMC while being dc fault tolerant, and at the same time, it also requires fewer capacitors and switches compared to the HMMC. It produces the same number of output voltage levels by using only 50% of SMs to that required in MMC. Hence, it generates the same quality output voltages while using only half number of SMs as required in MMC. Furthermore, the EMMC requires fewer isolated dc power supplies and is more efficient compared to the conventional AAC and HMMC. Moreover, the proposed EMMC overcomes the major drawback of the conventional AAC, i.e., modularity. As the EMMC is modular in structure, the reliability of EMMC would be higher compared to all the other hybrid topologies existing in the literature for the targeted applications. Hence, the proposed converter can be a better candidate than the existing MMC, HMMC, and AAC topologies for high- and medium-voltage applications.

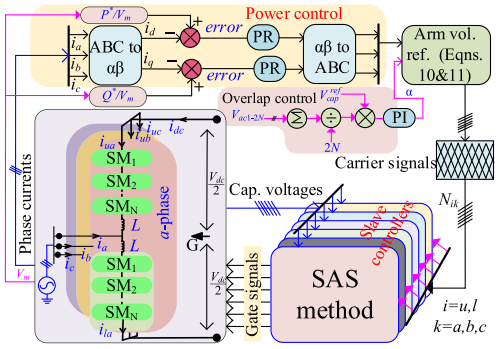

Fig. 11. Overall control block diagram of 21-level grid-connected EMMC.

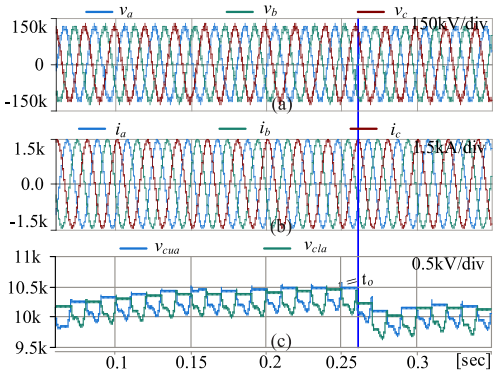

Fig. 12. Simulated waveforms of EMMC during the overlap controller test. (a) Three-phase converter output voltages. (b) Three-phase currents. (c) One SM capacitor voltage from each of a-phase upper and lower arms.

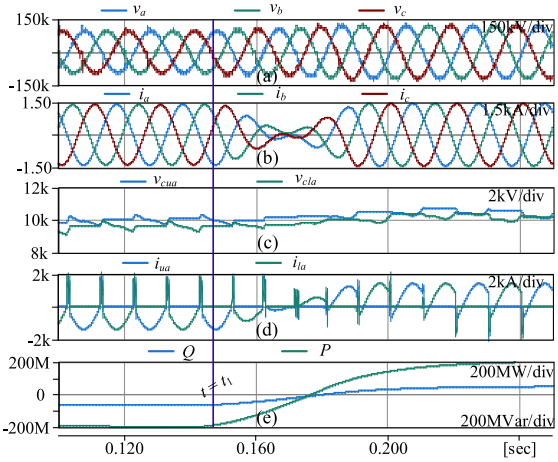

Fig. 13. Simulated waveforms of EMMC during power change test. (a) Three-phase output voltages. (b) Three-phase output currents. (c) One SM capacitor voltage from each of a-phase upper and lower arms. (d) Upper and lower arm currents in a-phase. (e) Active and reactive powers fed to grid.

IV. Validation of EMMC Using Simulation Studies

A 3-phase, 250 MVA, 21-level EMMC simulation model is developed in PSCAD to validate its working principles with the parameters listed in Table II. In this model, a voltage source of 200 kV is used to support the dc-link voltage. The overall system and control block diagram of the developed model is shown in Fig. 11. As illustrated in Fig. 11, the control architecture of EMMC can be divided into power control, overlap control, and voltage balancing control of SM capacitors. Based on the active and reactive power references, the power controller generates the three-phase output voltage reference signals for EMMC. As discussed in Section II-B, the net arm energy is not zero naturally in EMMC. Hence, an overlap controller is used to balance the SMs capacitor voltages. In this controller, the error between the actual and reference values of SMs capacitor voltages is passed through a PI controller, as shown in Fig. 11. The PI controller generates the overlap angle (α) such that by operating the converter in the overlapping mode for the duration equal to α/ω, the steady-state error is zero, i.e., SMs capacitor voltages are equal to the reference value. Using the overlap angle and reference output voltage signals, from (10) and (11), the reference arm voltage signals are determined. These arm voltage references are used along with the phase-shifted sinusoidal pulsewidth modulation technique [17] to determine the number of SMs to be inserted (insertion index, N_{ik}) in each EMMC arm. The insertion index value is communicated to the SMs capacitor voltage balance controller (SMVBC). Each arm of the EMMC comprises a dedicated SMVBC. The sorting and selecting method [18] is used to balance the SMs capacitor voltages in EMMC. All the SMs capacitors voltages' are sensed and communicated to SMVBC, where the SMs capacitor voltages are sorted based on their instantaneous values and the appropriate SMs are selected to be inserted based on the arm current direction and the insertion index.

In the first test, the developed simulation model is tested to validate the working of the overlap controller. In this test, the EMMC is initially operated without enabling the overlap controller. The active and reactive power references are set to -200 MW and -100 MVar, respectively. Some of the important parameters such as three-phase output voltage, SMs capacitor voltages, and output current are measured and plotted in Fig. 12. $V_{\rm dc}$ = 200 kV and each arm comprises ten SMs (N = 10), each SMs capacitor average voltage should be regulated to 10 kV ($V_{\rm dc}$/2N). However, as it can be observed from Fig. 12(c), where one of the SMs capacitor voltages from both the upper and lower arms of one phase-leg of EMMC are shown, these voltages continue to increase beyond 10 kV, which verifies that the capacitor voltages are not balanced since the overlap control is not activated. Therefore, as discussed earlier, a dedicated overlap controller is required to balance the SMs capacitor voltages in EMMC. To verify this, at $t = t_o$ in the simulation run, the overlap controller is enabled. It can be observed from Fig. 12(c) that as soon as the controller is enabled, the SMs capacitor voltages are brought back to be well regulated around 10 kV. These results verify that the proposed EMMC with the overlap control can balance the SMs capacitor voltages and generate a fairly good waveform at its ac terminals.

Now, in another test, to validate the working of EMMC for HV and MV applications, the system is initially operated at $P^* = -200$ MW and $Q^* = -100$ MVar, and after $t = t_1$, the P^* and Q^* values are linearly changed to 200 MW and 100 MVar, respectively. The corresponding results are shown in Fig. 13. It can be observed from Fig. 13(e) that, initially, the system is expectedly operating at $P = -200$ MW and $Q = -100$ MVar, and later, the system is operating at $P = 200$ MW and $Q = 100$ MVar. The power controller adjusts the magnitude of the three-phase

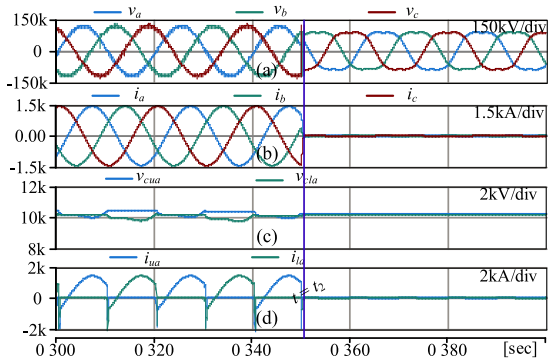

Fig. 14. Simulated waveforms of EMMC during the dc fault test. (a) Three-phase output voltages. (b) Three-phase output currents. (c) One SM capacitor voltage from each of a-phase upper and lower arms. (d) Upper and lower arm currents in a-phase.

converter output voltage, as shown in Fig. 13(a), to feed the required active and reactive powers to the grid. It can be seen that the transition following the change in references is smooth. One of the SMs capacitor voltages from both the upper and lower arms of one phase-leg of EMMC are shown in Fig. 13(c). In this test, the overlap controller is kept enabled, and hence, the SMs capacitor voltages shown in Fig. 13(c) are balanced. Further, it can be observed from Fig. 13(d) that during the overlap time, both the upper and lower arms are carrying the current. Therefore, it is clear from this test that the proposed converter can operate satisfactorily well during transient conditions, such as power reversal and power factor change. Hence, the proposed EMMC can find a wide range of applications in high and medium voltage.

As discussed earlier in Section II-D, the proposed converter possesses the dc fault-tolerant capability, and to investigate the same, the developed model is tested for a dc-side fault case. In this study, the converter is initially set to operate at $P* = 200$ MW and $Q* = 100$ MVar and at $t = t_2$, a dc-side short-circuit fault is created. As soon as the fault is detected, as discussed in Section II-D, all the SMs are operated in blocked state, i.e., the gate pulses to S_{1-4} in each SM are withdrawn and the gate pulse is given to S_5 of each SM. The obtained results are shown in Fig. 14. It can be observed from this figure that as soon as the "blocking state" of the SMs is activated following the fault detection, the converter output current [see Fig. 14(b)] and arm current [see Fig. 14(d)] fall to zero by the converter action of imposing the opposite polarity voltage of sufficient magnitude. This further confirms that the proposed EMMC blocks the fault current in the event of a dc-side fault.

It can be observed from Figs. 12–14 that the EMMC exhibits excellent performance in response to the power reversal and power factor change with minimum transient effects in the active and reactive powers, ac currents, and SMs capacitor voltages. Furthermore, the dc fault-tolerant capability of EMMC is also verified. Thus, the results confirm the effectiveness of the proposed converter and control for HVdc applications.

V. Experimental Verification of EMMC

A five-level scaled-down laboratory setup of EMMC is developed, as shown in Fig. 15, to further validate its working

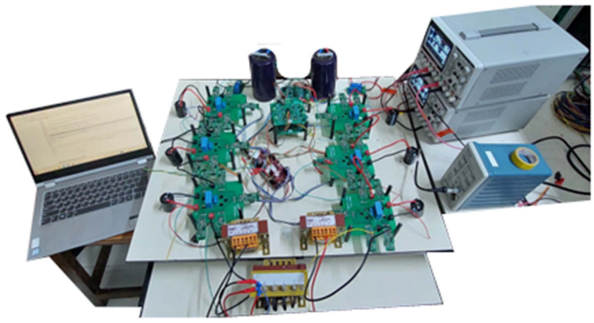

Fig. 15. Experimental setup of a five-level EMMC.

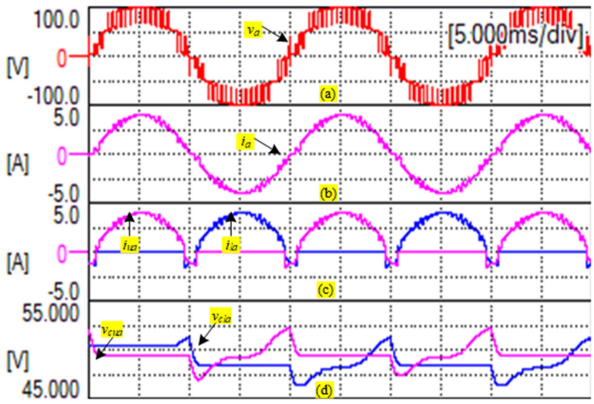

Fig. 16. Experimental waveforms of EMMC during an RL-load test. (a) Converter output voltage. (b) Output current. (c) Upper and lower arm currents in a-phase. (d) One SM capacitor voltage each from upper and lower arms.

principles. All the three control stages, i.e., the power control, overlap control, and SMVBC, are implemented using the TI-made digital signal processor (TMS320F28379D). A series of tests are conducted on the developed experimental setup to experimentally verify the efficacy of the proposed topology and its operating principles.

In the first test, the developed setup is connected to an RL load ($R = 30\ \Omega$ and $L = 10$ mH) and set to operate with unity modulation index value (m_i). Since $m_i = 1$ is not a sweet-spot condition for the EMMC, the overlap controller is enabled to balance the SMs capacitor voltages. Some of the important signals are recorded using the scope recorder (Yokogawa make DL850) and are plotted in Fig. 16. It can be observed from Fig. 16(a) that the converter output voltage is of desired five-level shape and the output current shown in Fig. 16(b) is nearly sinusoidal. As discussed earlier, the overlap controller is enabled to balance the SMs capacitor voltages in EMMC. Therefore, as can be observed from Fig. 16(c), during the overlap time at zero crossing of output voltage, both the upper and lower arms are carrying current. This has resulted in balanced SMs capacitor voltages at 50 V ($\frac{V_{dc}}{2N} = \frac{200}{2\times 2}$) as can be observed from Fig. 16(d).

To further show the dynamic performance of EMMC during the transients, the converter is initially operated at $m_i = 1$ and at $t = t_2$, the m_i value is changed from unity to 0.8. The corresponding results obtained from this test are shown in Fig. 17. It can be observed from Fig. 17(a) that the magnitude of the output voltage is decreased corresponding to the change in m_i

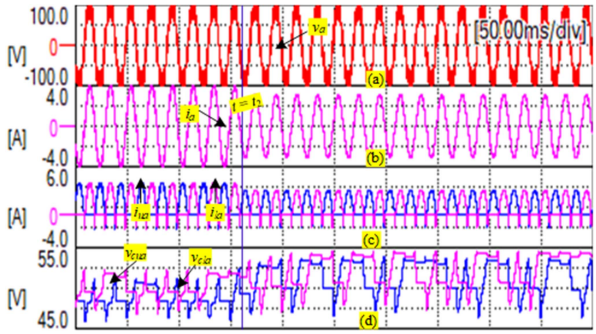

Fig. 17. Experimental waveforms of EMMC during modulation index change test. (a) Converter output voltage. (b) Output current. (c) Upper and lower arm currents in a-phase. (d) One SM capacitor voltage each from upper and lower arms.

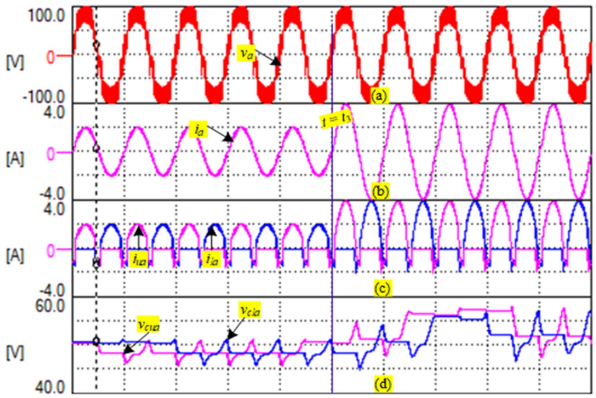

Fig. 18. Experimental waveforms of EMMC during load change test. (a) Converter output voltage. (b) Output current. (c) Upper and lower arm currents in a-phase. (d) One SM capacitor voltage each from upper and lower arms.

value and the transition is smooth. Similar to the earlier test, the overlap controller is activated to balance the SMs capacitor voltages as the operating point is not a sweet-spot condition. Hence, it can be seen from Fig. 17(c) that during the nonoverlap time, either the upper or lower arm is carrying the output current and during the overlap time, both the upper and lower arms carry current. Finally, it can be observed from Fig. 17(d) that the SMs capacitor voltages are varying between a specific window, which illustrates that the average value of these voltages is balanced, and this balancing is maintained even when the operating modulation index value is instantly changed. Further, the width of this window varies as the operating point is varied. This is expected as the SMs capacitor voltages ripple depends on the operating conditions [10]. Therefore, it can be concluded that the EMMC responds satisfactorily fast to the changes in m_i value and effectively regulate the SMs capacitor voltages to their reference.

In the next test, the system is initially set to operate at $m_i = 1$ with an RL load of $R = 50\ \Omega$ and $L = 10$ mH. After some time (at $t = t_3$), the load resistance is instantly changed from 50 Ω to 20 Ω. The corresponding results are shown in Fig. 18. It can be observed from this figure that the converter can operate satisfactorily well during the sudden change of load.

Finally, to validate the capability of the proposed EMMC to ride through the dc-side short-circuit faults, another experiment

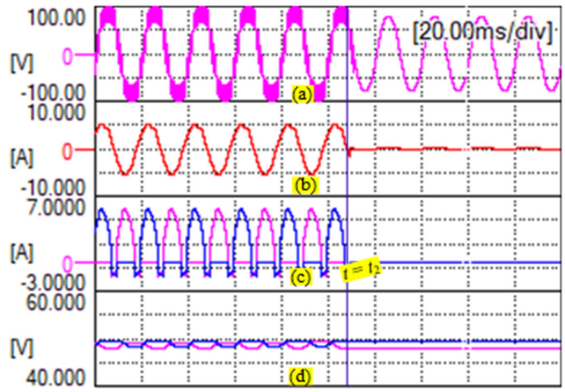

Fig. 19. Experimental waveforms of EMMC during the dc fault test. (a) Converter output voltage. (b) Output current. (c) Upper and lower arm currents in a-phase. (d) One SM capacitor voltage each from upper and lower arms.

is conducted. In this test, the system is initially set to operate in the grid-connected mode. Then, while the converter is exchanging the active and reactive powers with the grid corresponding to the set respective reference values, a dc-side short circuit is created at $t = t_2$ by connecting a 1 Ω resister across the converter dc-link terminals. Now, as discussed earlier in Section II-D, to limit the fault current, the converter is operated in the blocking mode by turning OFF S_1–S_4 switches and turning ON the S_5 switch of all the SMs. By performing this action following the fault occurrence, the corresponding measured results are shown in Fig. 19. It can be seen from Fig. 19(a) that following the fault occurrence at $t = t_2$, the converter is operated in the blocking mode, and hence, the voltage at converter output would be same as the grid voltage and the same can be inferred from Fig. 19(b). It can further be observed from Fig. 19(b) and (c) that the converter output current and arm currents have seized as soon as the converter is blocked following the dc-side fault detection. The results in Fig. 18 match with the simulation results presented in Fig. 13 and further validate the dc fault blocking capability of EMMC.

Therefore, it can be observed from Figs. 16 to 19 that the proposed EMMC generates the desired multilevel voltage waveform and can operate satisfactorily well during the transients and dc fault conditions. These results verify the effectiveness of the proposed EMMC topology and confirm its operating principles.

VI. Conclusion

This article proposes a new SM that consists of five switches and a capacitor. The proposed SM has the ability to produce three output voltage states (positive, negative, and zero voltage). Furthermore, an additional "open-circuit" state can also be realized using the proposed SM, which provides a unique operational feature and that is utilized to derive a novel converter topology in this article. The proposed modular converter topology in this article, which is based on the proposed SM structure, is named the "EMMC." The EMMC topology is fully modular and scalable in structure. It requires only half the number of SMs as used in MMC for the same dc-link voltage and voltage rating of IGBTs. Hence, it can have lower volume and initial cost compared to MMC. Furthermore, the EMMC is dc fault

tolerant as it can block the current in the event of a dc-side short-circuit fault to avoid feeding the fault from ac side. Moreover, it requires fewer isolated power supplies to drive the IGBTs compared to that required in MMC, HMMC, and AAC, which can further potentially reduce the converter cost. Therefore, the proposed EMMC offers a compact converter solution for high- and medium-voltage applications. The efficacy of the EMMC has been verified using PSCAD simulation studies and also on a scaled-down five-level experimental prototype of EMMC. Various case studies are performed to validate the working principle of EMMC under both steady-state and transient system conditions. The simulation and experimental results highlight the excellent performance of the proposed EMMC topology and its developed control and fault-tolerant capability.

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