Nonexcessive-ΔV and Low Complexity Model Predictive Control Based on Finite-State Machine for Three-Level Three-Phase Inverters

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***Abstract*—For three-level three-phase inverters, a novel finite-state machine-based model predictive control (FSM-MPC) is proposed. The state transition diagram of FSM is regarded as the operation guideline to avoid excessive voltage jumps (ΔV). No more than five voltage vectors (VVs) are selected as FSM-MPC's candidates VVs, based on the VV reference and the previous optimal VV. And the cost function is simplified in terms of time duration. Thus, evaluating a candidate VV requires a very low computation cost. Without losing control performance, the proposed FSM-MPC's execution time is decreased to 50% of the MPC algorithm, which enumerates all basic VVs to get global optimal VV and performance. Compared with the existing simplified algorithms, the proposed FSM-MPC makes current harmonics lower, and its average switching frequency is 33% less, which means much less switching loss. Furthermore, the proposed algorithm is robust when the electric-circuit parameters are mismatched in the control system. Experimental results are provided to validate the advantages of the proposed algorithm.**

***Index Terms*—Calculation burden, finite-state machine, model predictive control, three-level (3L) three-phase inverters, voltage jump (ΔV).**

I. Introduction

In RECENT years, multilevel voltage source inverters (VSIs) have attracted increasing attention, relying on new topologies to improve VSIs' performance. Compared with two-level VSIs, multilevel VSIs have advantages of high voltage operation capability, low switching losses, high efficiency, and low electromagnetic interference [1], [2]. Among them, three-level (3L) VSIs have been widely applied due to moderate levels and easy implementation.

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Optimization of control algorithms is crucial to improving VSIs' performance once the topology is fixed. The commonly employed controllers include proportional-integral (PI) control, proportional-resonant (PR) control, and deadbeat control [3], [4], [5], [6]. However, it is difficult for the PI controller to balance steady-state and transient performance. The performance of the PR controller decreases when the output frequency changes. For deadbeat control with modulator, its robustness and current control performance are highly dependent on system parameters [7], [8]. With the development of digital computing technology, more advanced control algorithms have been applied in recent years. Among them, finite control set model predictive control (FCS-MPC) has emerged as a promising control alternative due to its simple control structure, intuitive concept, and favorable dynamic performance. The basic concept of FCS-MPC is to iteratively evaluate all possible voltage vectors (VVs) by setting control objectives and designing cost functions.

One of the main challenges of FCS-MPC applied to 3L VSIs is the high computational burden. A common approach is to limit the search space. On the one hand, various methods are based on the VV reference ($\boldsymbol{v}^*$). In [9], [10], and [11], only several effective VVs adjacent to $\boldsymbol{v}^*$ are required. In [12], the VV closest to $\boldsymbol{v}^*$ is found based on the "S" factor in an algebraic way, which is directly regarded as the optimal VV. On the other hand, in [7], the iteration order is adjusted. Its first stage evaluates six virtual VVs; in the second optimization stage, VVs located around the optimal virtual VV are evaluated. Similarly, in [13], 13 VVs for outer predictive flux control and two switching states for inner predictive neutral point voltage (NPV) control are evaluated.

Unfortunately, the requirement of smooth switching leads to finite VV switching, and the above-mentioned algorithms do not consider finite VV switching. There are maybe no VV available for a simplified control set obtained by the above-mentioned algorithms, especially when the current/power reference changes dynamically.

To realize smooth switching, voltage jumps (ΔV) in phase and line-to-line voltages during VVs switching should not be greater than half of the dc side voltage [14], [15], [16], [17]. Excessive ΔV in phase voltage cannot utilize the advantages of 3L VSIs and may endanger the safe operation of inverter by causing a full dc voltage across one switch; excessive ΔV in line-to-line voltage increases the harmonic content of the output current, which is not friendly to the grid and increases the

burden on the filter [14], [15]. Considering this limitation, some intuitive methods have been proposed for a complete search space. In [15], an intermediate VV is inserted into two successive sectors with excessive ΔV, which is a trade-off. The work in [16] takes the allowable transitions between different VVs into account, but there still exists the possibility of excessive ΔV in line-to-line voltages. The work in [18] proposes switching tables to preselect feasible candidate VVs. But the switching tables are complicated, and the maximum number of candidate VVs reaches 13. In [19], the VVs that will cause excessive ΔV are ruled out from the control set. However, all candidate VVs may be excluded for a simplified control set. Besides, in [20], only the neighboring VVs of the optimal VV selected in the previous control cycle ($\boldsymbol{v}_L$) are evaluated, but no specific solution is given. Furthermore, the above-mentioned methods are not suitable for a limited search space.

To simultaneously model the finite control set and finite VV switching of 3L VSIs, the finite-state machine (FSM) could be employed. FSM is a mathematical model that describes the finite state of a system and the transfers among these states. And it is currently used in many fields, including power electronics [21], [22], [23]. Thus, this article proposes a low complexity FSM-MPC algorithm. The optimal VV that does not cause excessive ΔV is determined with low complexity, and the main contributions are listed as follows:

1) A novel FSM-MPC algorithm is applied to avoid excessive ΔV in phase and line-to-line voltages, which benefits the inverter's safe operation.
2) A straightforward geometric approach is proposed to guarantee no more than five candidates VV. And the cost function is further simplified based on time duration. Thus, the computational efficiency is significantly improved.
3) Control performance (including current harmonics and average switching frequency) of the proposed FSM-MPC algorithm is greatly improved, compared with the existing simplified algorithms.
4) The robustness of the proposed FSM-MPC algorithm is proved. It still performs well when the electric-circuit parameters are mismatched in the control system.

The remainder of this article is organized as follows. Section II summarizes the conventional predictive model of 3L VSIs and introduces the FSM model. Section III completely presents the proposed algorithm. Section IV provides the experimental results. Finally, Section V concludes this article.

II. System Modeling

A. Predictive Model of 3L VSIs

The topologies of 3L VSIs could be divided into neutral point clamped (NPC), flying capacitor, and cascade H-bridge. Without loss of generality, this article takes the 3L-NPC VSIs, for instance.

The topology of 3L-NPC VSIs is depicted in Fig. 1: each leg is composed of four switches and two clamped diodes; C_1 and C_2 are equivalent capacitors in dc-link. According to different switching combinations, each phase leg may output three states

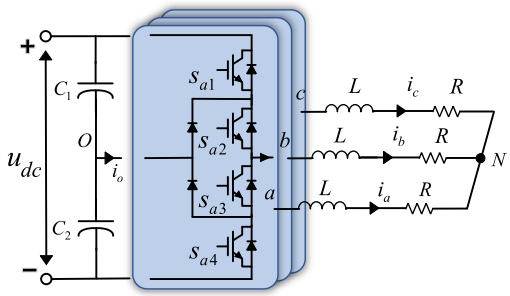

Fig. 1. Topology of 3L-NPC VSIs.

defined as follows:

$$S_z = \begin{cases} 1 & s_{z1} \text{ and } s_{z2} \text{ are on} \\ 0 & s_{z2} \text{ and } s_{z3} \text{ are on} \\ -1 & s_{z3} \text{ and } s_{z4} \text{ are on} \end{cases} \quad z = a, b, c. \tag{1}$$

Therefore, there are a total of $3^3 = 27$ switching states. These switching states generate 19 nonredundant and 8 redundant VVs in the abc frame.

The output voltage of each phase with respect to the load neutral point N is obtained as follows:

$$\begin{cases} u_{aN} = (2S_a - S_b - S_c) \times u_{dc}/6 \\ u_{bN} = (2S_b - S_c - S_a) \times u_{dc}/6 \\ u_{cN} = (2S_c - S_a - S_b) \times u_{dc}/6 \end{cases} \tag{2}$$

where u_{dc} represents dc-link voltage.

Taking the current direction in Fig. 1 as the positive direction, according to Kirchhoff's voltage law, the mathematical model of the ac side in the abc frame is expressed as follows:

$$L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + R\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} u_{aN} \\ u_{bN} \\ u_{cN} \end{bmatrix} \tag{3}$$

where i_a, i_b, and i_c represent phase currents, L refers to filter inductance, and R is the load.

Based on the Clark transformation, the mathematical model in the $\alpha\beta$ frame is derived as follows:

$$L\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + R\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \tag{4}$$

where i_α and i_β stand for the α-axis and β-axis components of the output current, respectively.

According to the forward-Euler approximation, (4) is discretized to predict the output current at $(k+1)$th instant as follows:

$$\begin{cases} i_\alpha^p(k+1) = i_\alpha(k) + (u_\alpha(k) - Ri_\alpha(k)) \times T_s/L \\ i_\beta^p(k+1) = i_\beta(k) + (u_\beta(k) - Ri_\beta(k)) \times T_s/L \end{cases} \tag{5}$$

where $i_\alpha(k)$ and $i_\beta(k)$ are α-axis and β-axis components of the output current sampled at the (k)th instant, respectively; $u_\alpha(k)$ and $u_\beta(k)$ are α-axis and β-axis components of the output VV, respectively; and T_s represents the sampling period.

In the operation of 3L VSIs, the direct cause of the unbalanced capacitor voltages is the current flowing through the neutral

point O. As depicted in Fig. 1, it is modeled as follows:

$$i_o = i_a(1 - |S_a|) + i_b(1 - |S_b|) + i_c(1 - |S_c|). \quad (6)$$

Assume $C_1 = C_2 = C$, the predictive difference of capacitor voltages at (k+1)th instant is obtained as follows:

$$\Delta u^p(k+1) = u_{c1}(k) - u_{c2}(k) + \frac{i_o(k)}{C} \times T_s \quad (7)$$

where $u_{c1}(k)$ and $u_{c2}(k)$ are the capacitor voltages sampled at the (k)th instant, respectively, and $i_o(k)$ is calculated by substituting the output VV into (6).

Taking model predictive current control (MPCC) as an example, to track current reference and balance capacitor voltages simultaneously, the cost function of the conventional MPCC is defined as follows [8], [24]:

$$g = (i^*_\alpha(k+1) - i^p_\alpha(k+1))^2 + \left(i^*_\beta(k+1) - i^p_\beta(k+1)\right)^2 + \lambda(\Delta u^p(k+1))^2 \quad (8)$$

where λ is the weighting factor, which sets the relative importance of the current control and NPV control; and $i^*_\alpha(k+1)$ and $i^*_\beta(k+1)$ represent α-axis and β-axis components of the output current reference at the (k+1)th instant, respectively.

B. Building and Simplification of FSM Model

There are 27 VVs, but the output VV cannot be switched at will. During VV switching, phase and line-to-line ΔV should not exceed $u_{dc}/2$. Examples are as follows:

1) Taking the switching from $(1, 0, 0)$ to $(-1, 0, 0)$ as an example, the phase voltage of phase A changes from $u_{dc}/2$ to $-u_{dc}/2$. It leads to the fact that 3L VSIs cannot reflect the advantages of topology, that is, reduced *dV/dt*. Besides, a single switch tube may withstand the dc side voltage and be damaged.
2) Taking the switching from $(1, 0, 0)$ to $(0, 1, 0)$ as an example, the line-to-line voltage between phases A and B changes from $u_{dc}/2$ to $-u_{dc}/2$. Excessive line-to-line ΔV increases the harmonics of the output current and is not friendly to the grid.

Therefore, not only the number of candidate VVs is limited, but also the VV switching. These two could be modeled by FSM. The current output VV of 3L VSIs represents its state. For any two VVs, if there is no excessive ΔV when switching between them, they are considered to be connected. Then, the state transition diagram of the FSM model is shown in Fig. 2(a). 27 VVs could be classified as zero, small, medium, and large VVs, denoted as circles with four different colors in Fig. 2. Besides, $(0, 0, 0)$ is selected as the only zero VV in Fig. 2(b), both $(1, 1, 1)$ and $(-1, -1, -1)$ are ruled out, the reasons are as follows:

1) These three VVs have the same effect in current control and NPV control.
2) Switching between $(0, 0, 0)$ and any small VVs will not cause excessive ΔV; but $(1, 1, 1)$ and $(-1, -1, -1)$ have no such guarantee.

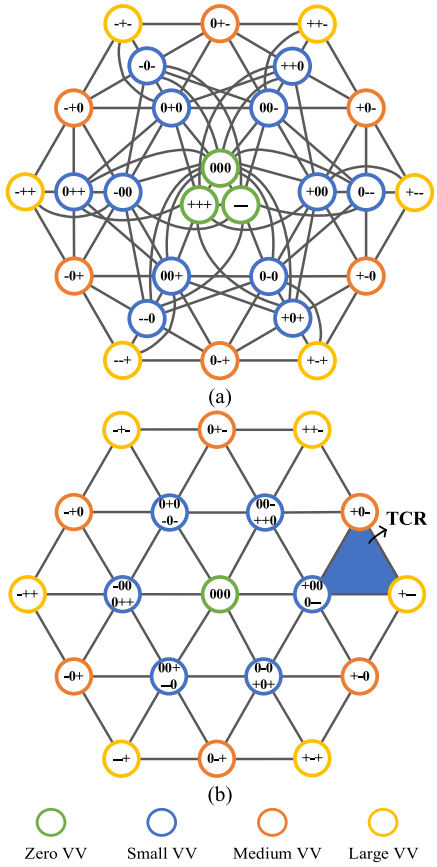

Fig. 2. State transition diagram of 3L VSIs FSM model. (a) Original diagram. (b) Proposed simplified diagram.

3) The common-mode voltage of $(0, 0, 0)$ is 0, and the others' are the largest of all VVs [11].

Next, to simplify the model, it is assumed that redundant VVs located at the same position in the space vector diagram are a unit. For any VV, as long as it is connected to anyone in a unit, it is regarded to be connected to the unit. Thus, Fig. 2(a) is simplified to Fig. 2(b), which is similar to the space vector diagram.

C. Analysis of Dead Zone Effect

To avoid short circuit of dc side capacitor, dead zone must be added during the VV switching. Therefore, it is necessary to analyze whether the dead zone will cause excessive ΔV, for VV switching that follows Fig. 2(a).

Take the output voltage of phase A switching from "+" level to "0" level as an example, s_{a3} cannot be turned ON immediately after s_{a1} is turned OFF, and dead zone needs to be set. As shown in Fig. 3, when $i_a > 0$, the output voltage of dead zone is "0" level; when $i_a < 0$, it is "+" level. Similarly, the output voltage of dead zone in other cases could be determined, as shown in Table I.

According to Table I, the output voltage of dead zone is the same as the output voltage before or after switching. Thus, dead zone does not affect the jump amplitude of phase voltage.

For any two phases, if the output voltages of dead zone are both the same as the voltage before or after switching, the line-to-line

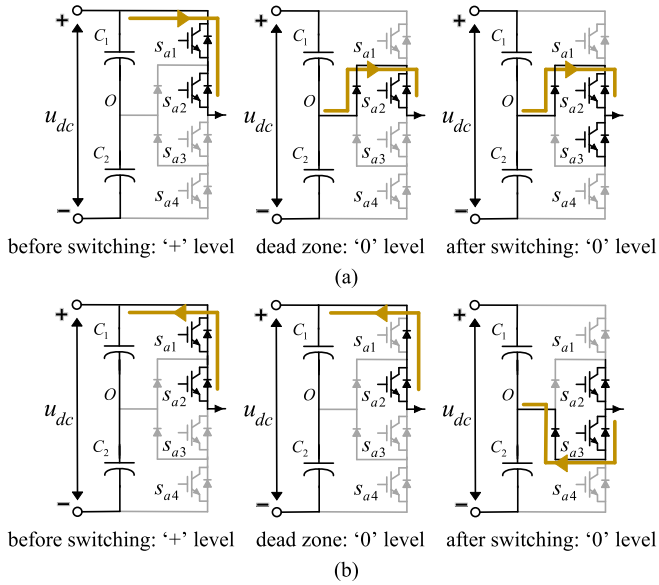

Fig. 3. Analysis of dead zone output voltage. (a) $i_a > 0$. (b) $i_a < 0$.

TABLE I
OUTPUT VOLTAGE OF DEAD ZONE

	$+\rightarrow 0$	$0\rightarrow +$	$-\rightarrow 0$	$0\rightarrow -$
$i_a > 0$	0	0	–	–
$i_a < 0$	+	+	0	0

ΔV is unaffected. And it is also possible that the dead zone output voltage of one phase is the same as the voltage before switching, and the voltage of the other phase is the same as after switching. That is, the output voltage of one phase changes first, and the other phase changes later. Obviously, this situation also does not introduce excessive ΔV of line-to-line voltage.

Therefore, if the VV switching follows Fig. 2(a), the dead zone does not introduce excessive ΔV.

III. PROPOSED FSM-MPC ALGORITHM

In this section, first, $\boldsymbol{v}^*$ is obtained. Then, without considering the ΔV, candidate VVs are preselected based on $\boldsymbol{v}^*$ in a normalized method. Next, this method is improved to preselect candidate VVs based on $\boldsymbol{v}^*$ and $\boldsymbol{v}_L$. Consequently, at least one candidate VV satisfies the FSM model and will not cause excessive ΔV. Furthermore, the cost function is further simplified.

A. Voltage Reference Calculation

It is assumed that under the effect of $\boldsymbol{v}^*$, the actual output current tracks the given value within one control cycle. $\boldsymbol{v}^*$ could be obtained by replacing $i_\alpha^p(k+1)$ and $i_\beta^p(k+1)$ with $i_\alpha^*(k+1)$ and $i_\beta^*(k+1)$ in (5), respectively, and making rearrangement of the equation [25], [26], [27]:

$$\begin{cases} u_\alpha^*(k) = Ri_\alpha(k) + (i_\alpha^*(k+1) - i_\alpha(k)) \times L/T_s \\ u_\beta^*(k) = Ri_\beta(k) + (i_\beta^*(k+1) - i_\beta(k)) \times L/T_s \end{cases} \tag{9}$$

where $u_\alpha^*(k)$ and $u_\beta^*(k)$ are the α-axis and β-axis components of $\boldsymbol{v}^*$, respectively.

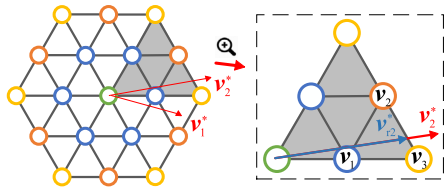

Fig. 4. Determination of TCR without considering excessive ΔV.

Substituting (5) and (9) into (8), it could be derived as follows:

$$\begin{aligned} &\left(i_\alpha^*(k+1) - i_\alpha^p(k+1)\right)^2 + \left(i_\beta^*(k+1) - i_\beta^p(k+1)\right)^2 \\ &= \frac{T_s^2}{L^2}\left[\left(u_\alpha^*(k) - u_\alpha(k)\right)^2 + \left(u_\beta^*(k) - u_\beta(k)\right)^2\right] = \frac{T_s^2}{L^2}\rho^2 \end{aligned} \tag{10}$$

where ρ represents the Euclidean distance between the VV selected and $\boldsymbol{v}^*$ in the $\alpha\beta$ frame.

Equation (10) indicates equivalence between ρ and the deviation of the predicted output current. So, (8) is rewritten as follows:

$$g = \rho^2 + \lambda(\Delta u^p(k+1))^2. \tag{11}$$

The work in [9], [10], [11], and [12] limits the search space to around $\boldsymbol{v}^*$ to reduce the number of candidate VVs. The reason is that current control is more important than NPV control in MPCC. Therefore, ρ^2 should take the most significant proportion in (11). Ideally, the VV closer to $\boldsymbol{v}^*$ is more likely to be optimal.

B. Determination of Candidate VVs Without Considering Excessive ΔV

To reduce the number of candidate VVs, triangle candidate area (TCR) is adopted to limit the search space. TCR belongs to the minor triangular areas, and an example is shown in Fig. 2(b). VVs located at the vertices of TCR are selected as candidates. By traversing all possible triangle areas, it could be found that the number of candidate VVs will not exceed 5.

If excessive ΔV is not considered, all triangles in Fig. 2(b) could be used as TCR. According to (11), TCR should be the triangle closest to $\boldsymbol{v}^*$ in Fig. 2(b). The location of $\boldsymbol{v}^*$ could be divided into two categories: within or outside the control region.

1) if $\boldsymbol{v}^*$ falls within the control region (e.g., $\boldsymbol{v}_1^*$ in Fig. 4), TCR is the triangle in which $\boldsymbol{v}^*$ is located. In the space vector diagram, any VV (including virtual VVs) could be synthesized by $(1, 0, 0)$ and $(0, 1, 0)$. Through (2) and Clark transformation, $(1, 0, 0)$ is converted to $(u_{dc}/3, 0)$ in the $\alpha\beta$ frame, and $(0, 1, 0)$ to $(-u_{dc}/6, \sqrt{3}u_{dc}/6)$. Then in the $\alpha\beta$ frame, any VV could be synthesized by $(u_{dc}/3, 0)$ and $(-u_{dc}/6, \sqrt{3}u_{dc}/6)$. $\boldsymbol{v}^*$ is expressed as follows:

$$\begin{aligned} \boldsymbol{v}^* = &\frac{3u_\alpha^* + \sqrt{3}u_\beta^*}{u_{dc}} \times \left(\frac{u_{dc}}{3}, 0\right) \\ &+ \frac{2\sqrt{3}u_\beta^*}{u_{dc}} \times \left(-\frac{u_{dc}}{6}, \frac{\sqrt{3}u_{dc}}{6}\right). \end{aligned} \tag{12}$$

TABLE II
CANDIDATE VVS AND TIME DURATIONS

	$e \geq f$	$e < f$
$\boldsymbol{v}_1$	$(x, y, 0)$	$(x, y, 0)$
$\boldsymbol{v}_2$	$(x+1, y, 0)$	$(x, y+1, 0)$
$\boldsymbol{v}_3$	$(x+1, y+1, 0)$	$(x+1, y+1, 0)$
t_1	$1-e$	$1-f$
t_2	$e-f$	$f-e$
t_3	f	e

In the *abc* frame, (12) is drawn as follows:

$$\begin{aligned}\boldsymbol{v}^* &= \frac{3u_\alpha^* + \sqrt{3}u_\beta^*}{u_{dc}} \times (1,0,0) + \frac{2\sqrt{3}u_\beta^*}{u_{dc}} \times (0,1,0) \\ &= (x,y,0) + (e,0,0) + (0,f,0) \end{aligned} \tag{13}$$

where x, y, e, and f, respectively, represent

$$x = \text{floor}\left(\frac{3u_\alpha^* + \sqrt{3}u_\beta^*}{u_{dc}}\right) e = \frac{3u_\alpha^* + \sqrt{3}u_\beta^*}{u_{dc}} - x$$

$$y = \text{floor}\left(\frac{2\sqrt{3}u_\beta^*}{u_{dc}}\right) f = \frac{2\sqrt{3}u_\beta^*}{u_{dc}} - y.$$

Suppose $\boldsymbol{v}_1, \boldsymbol{v}_2$, and $\boldsymbol{v}_3$ are at the vertices of TCR, $\boldsymbol{v}^*$ could be synthesized by these three VVs. Let time durations be t_1, t_2, and t_3, "volt-second balance" is drawn as follows:

$$\begin{cases} \boldsymbol{v}^* = (t_1 \quad t_2 \quad t_3)\,(\boldsymbol{v}_1 \quad \boldsymbol{v}_2 \quad \boldsymbol{v}_3)' \\ t_1 + t_2 + t_3 = 1 \end{cases}. \tag{14}$$

If $e \geq f$, (13) could be converted to the form of (14) as follows:

$$\begin{aligned}\boldsymbol{v}^* &= \begin{pmatrix} x & y & 0 \end{pmatrix} + \begin{pmatrix} e & 0 & 0 \end{pmatrix} + \begin{pmatrix} 0 & f & 0 \end{pmatrix} \\ &= \begin{pmatrix} 1-e & e-f & f \end{pmatrix} \begin{pmatrix} x & y & 0 \\ x+1 & y & 0 \\ x+1 & y+1 & 0 \end{pmatrix}. \end{aligned} \tag{15}$$

Otherwise, (13) is converted to

$$\begin{aligned}\boldsymbol{v}^* &= \begin{pmatrix} x & y & 0 \end{pmatrix} + \begin{pmatrix} e & 0 & 0 \end{pmatrix} + \begin{pmatrix} 0 & f & 0 \end{pmatrix} \\ &= \begin{pmatrix} 1-f & f-e & e \end{pmatrix} \begin{pmatrix} x & y & 0 \\ x & y+1 & 0 \\ x+1 & y+1 & 0 \end{pmatrix}. \end{aligned} \tag{16}$$

According to (15) and (16), $\boldsymbol{v}_1$, $\boldsymbol{v}_2$, $\boldsymbol{v}_3$, t_1, t_2, and t_3 are obtained as shown in Table II. For any $\boldsymbol{v}^*$, after getting x, y, e, and f through (13), it is straightforward to obtain $\boldsymbol{v}_1$, $\boldsymbol{v}_2$, $\boldsymbol{v}_3$, t_1, t_2, and t_3.

2) If conversely, $\boldsymbol{v}^*$ falls outside the control region. $\boldsymbol{v}^*$ is converted to its projection to the hexagon's frontier. An illustrative example is shown in Fig. 4, and $\boldsymbol{v}_2^*$ is converted to $\boldsymbol{v}_{r2}^*$. The TCR of $\boldsymbol{v}_2^*$ is the triangle in which $\boldsymbol{v}_{r2}^*$ is located. VVs $(\boldsymbol{v}_1, \boldsymbol{v}_2, \boldsymbol{v}_3)$ and their time duration (t_{r1}, t_{r2}, t_{r3}) corresponding to $\boldsymbol{v}_{r2}^*$ could be obtained by referring to Table II as follows:

$$\boldsymbol{v}_{r2}^* = t_{r1}\boldsymbol{v}_1 + t_{r2}\boldsymbol{v}_2 + t_{r3}\boldsymbol{v}_3. \tag{17}$$

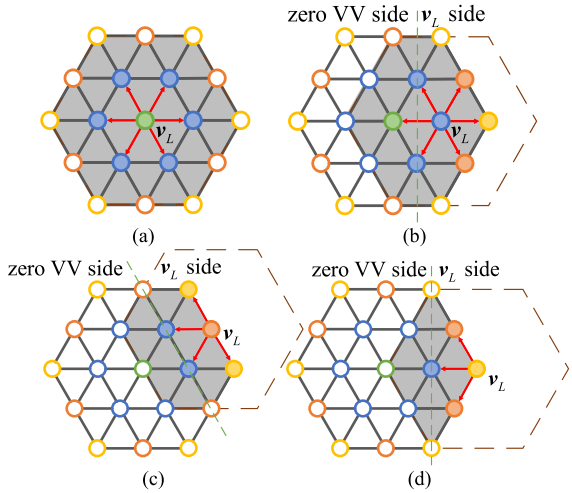

Fig. 5. Four subsets and the feasible domain of TCR. (a) Zero VV. (b) Small VV. (c) Medium VV. (d) Large VV.

Since $\boldsymbol{v}_{r2}^*$ is located at the hexagon's frontier, $\boldsymbol{v}_1$, $\boldsymbol{v}_2$, and $\boldsymbol{v}_3$ are small VV, medium VV, and large VV, respectively, as shown in Fig. 4. $\boldsymbol{v}_{r2}^*$ is on the connection between $\boldsymbol{v}_2$ and $\boldsymbol{v}_3$, thus t_{r1} is zero and the sum of t_{r2} and t_{r3} is 1. Plus, the modulus of $\boldsymbol{v}_3$ is twice as large as $\boldsymbol{v}_1$. Let the modulus of $\boldsymbol{v}_2^*$ be l, the modulus of $\boldsymbol{v}_{r2}^*$ be l_r, the time duration (t_1, t_2, t_3) of $\boldsymbol{v}_1$, $\boldsymbol{v}_2$, $\boldsymbol{v}_3$ in synthesizing $\boldsymbol{v}_2^*$ is obtained as follows:

$$\begin{aligned}\boldsymbol{v}_2^* &= \frac{l}{l_r}\boldsymbol{v}_{r2}^* \\ &= \frac{l}{l_r}(t_{r2}\boldsymbol{v}_2 + t_{r3}\boldsymbol{v}_3) \\ &= \frac{l}{l_r}(t_{r2}\boldsymbol{v}_2 + t_{r3}\boldsymbol{v}_3) + \left(\frac{l}{l_r} - 1\right)\boldsymbol{v}_3 + \left(2 - 2\frac{l}{l_r}\right)\boldsymbol{v}_1 \\ &= \left(2 - 2\frac{l}{l_r}\right)\boldsymbol{v}_1 + \frac{l}{l_r}t_{r2}\boldsymbol{v}_2 + \left(\frac{l}{l_r} + \frac{l}{l_r}t_{r3} - 1\right)\boldsymbol{v}_3. \end{aligned} \tag{18}$$

That is

$$t_1 = 2 - 2\frac{l}{l_r}\; t_2 = \frac{l}{l_r}t_{r2}\; t_3 = \frac{l}{l_r} + \frac{l}{l_r}t_{r3} - 1. \tag{19}$$

C. Determination of Candidate VVs Considering Excessive ΔV

Since switching from v_L to the optimal VV selected should not cause excessive ΔV, the optimal VV should be connected with $\boldsymbol{v}_L$, or be $\boldsymbol{v}_L$ in Fig. 2(a). If excessive ΔV is considered, not all triangles in Fig. 2(b) could be used as TCR. Therefore, the method proposed in the previous subsection needs improvement.

To determine the feasible domain of TCR, Fig. 2(b) is split into four subsets depending on the type of $\boldsymbol{v}_L$. Without loss of generality, $(0, 0, 0)$, $(1, 0, 0)$, $(1, 0, -1)$, and $(1, -1, -1)$ are taken as examples, as shown in Fig. 5. VVs located at the position of solid dots are connected with $\boldsymbol{v}_L$ in Fig. 2(b) or is $\boldsymbol{v}_L$. So at least one candidate VV satisfies the FSM model when TCR falls within the grey areas in Fig. 5. Otherwise, this inference is

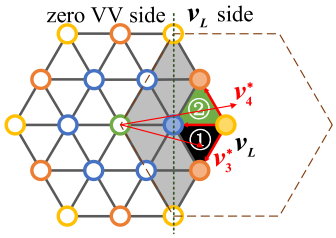

Fig. 6. Selection of TCR and candidate VVs ($||v^*|| \geq ||v^* - v_L||$).

false. That is, the grey area is the feasible domain of TCR. And TCR should be the triangle closest to v^* in its feasible domain. Besides, VVs in a unit in Fig. 2(b) will be selected as candidate VVs together. Among them, unfeasible candidate VVs are ruled out in the last step.

The feasible domain of TCR could be regarded as the overlap of the two hexagonal areas centered on zero VV and v_L. Thus, it is described regardless of the type of v_L. To determine candidate VVs, Fig. 5(b)–(d) are divided into two parts by the green line: v_L side and zero VV side. For Fig. 5(a), v_L is zero VV, so the whole feasible domain is considered as v_L side. Then, according to the position of v^*, it is divided into two categories:

1) If v^* is located in the v_L side ($||v^*|| \geq ||v^* - v_L||$), TCR is the triangle closest to v^* in the hexagonal area centered on zero VV. Therefore, v_1, v_2, v_3, t_1, t_2, and t_3 could be obtained by substituting v^* into the method proposed in the previous subsection.
   Taking Fig. 5(d) as an example, as shown in Fig. 6, the black triangle ① is the closest one to v_3^* in the feasible domain, and it is also the closest one to v_3^* in the hexagonal area centered on zero VV; similarly, the green triangle ② corresponds to v_4^*.
2) If v^* is located in the zero VV side ($||v^*|| < ||v^* - v_L||$), TCR is the triangle closest to v^* in the hexagonal area centered on v_L. By analyzing $v^* - v_L$ in this hexagonal area, v_1, v_2, v_3, t_1, t_2, and t_3 could be obtained.
   Taking Fig. 5(d) as an example, as shown in Fig. 7(a), the yellow triangle ③ is the closest one to v_5^* in the feasible domain, and it is also the closest one to v_5^* in the hexagonal area centered on v_L. To obtain candidate VVs, the analysis is as follows:
   First, v_5^* is converted to v_{s5}^* through $v_{s5}^* = v_5^* - v_L$.
   Then, Fig. 7(a) is split into Fig. 7(b) and (c). That is, two hexagonal areas centered on zero VV and v_L, respectively.
   Next, in Fig. 7(c), VVs (v_{s1}, v_{s2}, v_{s3}) located at the vertices of the black triangle ⑦ and their time durations (t_1, t_2, t_3) in synthesizing v_{s5}^* are obtained by substituting v_{s5}^* into the method proposed in the previous subsection.
   Finally, VVs (v_1, v_2, v_3) located at the vertices of the yellow triangle ⑨ in Fig. 7(c) could be obtained by adding v_L to v_{s1}, v_{s2}, v_{s3}. Since the yellow triangles (⑤ and ⑨) in Fig. 7(b) and (c) have the same position in their corresponding hexagons, v_1, v_2, and v_3 are the desired result. And the time durations of v_1, v_2, v_3 in synthesizing v_5^* is t_1, t_2, t_3, too. It is derived as follows:

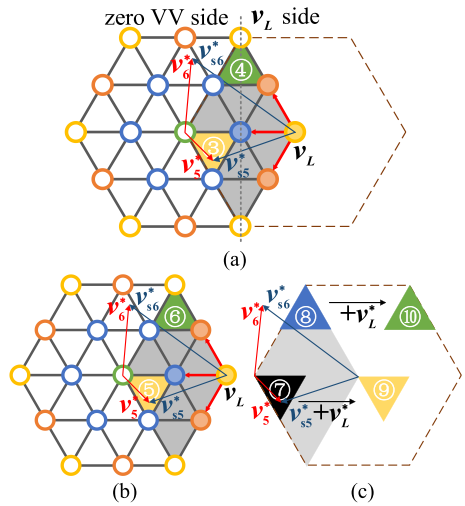

Fig. 7. Selection of TCR and candidate VVs ($||v^*|| < ||v^* - v_L||$).

$$\begin{aligned} v_5^* &= v_{s5}^* + v_L \\ &= v_{s1}t_1 + v_{s2}t_2 + v_{s3}t_3 + v_L \\ &= (v_{s1} + v_L)t_1 + (v_{s2} + v_L)t_2 + (v_{s3} + v_L)t_3 \\ &= v_1 t_1 + v_2 t_2 + v_3 t_3. \end{aligned} \tag{20}$$

Similarly, the blue triangle ⑧ and green triangle ⑩ in Fig. 7(c) correspond to v_6^*.

Besides, candidate VVs are obtained by adding or subtracting (1, 1, 1) to v_1, v_2, and v_3. Among them, candidate VVs which will cause excessive ΔV are ruled out to determine the final ones.

D. Cost Function in Terms of Time Duration

Although the cost function (11) dramatically reduces the calculation amount of one iteration, (11) could be further simplified in terms of time duration. Take v_1 as an example, the following derivation process is obtained according to (14):

$$\begin{aligned} (v^* - v_1)^2 &= [(v^* - v_1)(t_1 + t_2 + t_3)]^2 \\ &= [(v^* - v_1)\,t_1 + (v^* - v_1)(t_2 + t_3)]^2 \\ &= [-(v^* - v_2)\,t_2 - (v^* - v_3)\,t_3 \\ &\quad + (v^* - v_1)\,(t_2 + t_3)]^2 \\ &= [(v_2 - v_1)\,t_2 + (v_3 - v_1)\,t_3]^2 \\ &= \left(\frac{1}{3}u_{dc}\right)^2 t_2^2 + \left(\frac{1}{3}u_{dc}\right)^2 t_3^2 + \left(\frac{1}{3}u_{dc}\right)^2 t_2 t_3. \end{aligned} \tag{21}$$

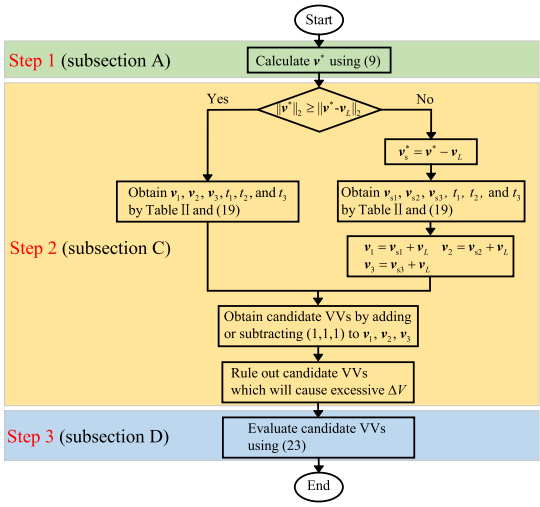

Fig. 8. Block diagram of the proposed FSM-MPC algorithm.

Since $(\boldsymbol{v}^* - \boldsymbol{v}_1)^2$ is positively correlated with t_2 and t_3 in (21), (21) is approximated as follows:

$$\begin{aligned}(\boldsymbol{v}^* - \boldsymbol{v}_1)^2 &= \left(\frac{1}{3}u_{dc}\right)^2 t_2^2 + \left(\frac{1}{3}u_{dc}\right)^2 t_3^2 + \left(\frac{1}{3}u_{dc}\right)^2 t_2 t_3 \\ &\approx \left(\frac{1}{3}u_{dc}\right)^2 t_2^2 + \left(\frac{1}{3}u_{dc}\right)^2 t_3^2 + 2 * \left(\frac{1}{3}u_{dc}\right)^2 t_2 t_3 \\ &= \left(\frac{1}{3}u_{dc}\right)^2 (t_2 + t_3)^2 \\ &= \left(\frac{1}{3}u_{dc}\right)^2 (1 - t_1)^2. \end{aligned} \tag{22}$$

According to (22), $(\boldsymbol{v}^* - \boldsymbol{v}_1)^2$ is positively correlated with $(1 - t_1)^2$. Similarly, this conclusion applies to $(\boldsymbol{v}^* - \boldsymbol{v}_2)^2$ and $(\boldsymbol{v}^* - \boldsymbol{v}_3)^2$. Thus, (11) could be further simplified to evaluate $\boldsymbol{v}_1, \boldsymbol{v}_2, \boldsymbol{v}_3$ as follows:

$$g = (1 - t)^2 + \lambda(\Delta u^p(k+1))^2. \tag{23}$$

t represents time duration, and it is easily obtained according to Table II and (19). Besides, redundant VVs at the same position have the same t. Compared with the conventional algorithm, which requires computing the current prediction model 27 times, it takes one time to get $\boldsymbol{v}^*$; compared with the simplified cost function (11), the calculation of t is considerably smaller than the Euclidean distance between VVs.

Based on the above-mentioned analysis, the control block diagram of the proposed FSM-MPC algorithm is shown in Fig. 8. And it could be divided into three steps:

Step 1 (subsection A): calculate the reference VV;
Step 2 (subsection C): determine candidate VVs considering excessive ΔV;
Step 3 (subsection D): evaluate candidate VVs using (23).

Remark 1: The proposed FSM-MPC algorithm applies to motor drives or grid-connected systems. The difference from the *R-L* plant analyzed in this article is the acquisition of $\boldsymbol{v}^*$ (i.e., the first step in Fig. 8), and the subsequent steps are the same.

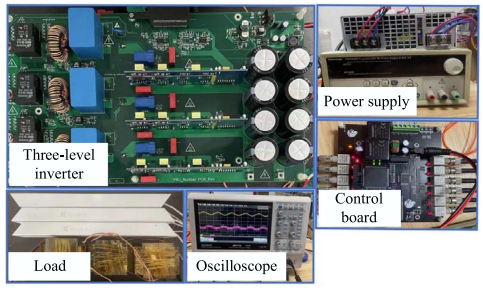

Fig. 9. Experimental platform of the 3L inverter.

TABLE III
EXPERIMENTAL PARAMETERS

Name	Description	Value
u_{dc}	Dc-link voltage	100 V
C	Dc-link capacitors	400 μF
L	Filter inductance	5 mH
R	Loads	10 Ω
T_s	Sampling period	100 us
t_d	Dead time	3 us

IV. EXPERIMENT RESULTS

To verify the feasibility and advantages of the proposed FSM-MPC algorithm, an experimental platform based on DSP (TMS320F28335) and field programmable gate array (FPGA) (XC6SLX9) is built, as shown in Fig. 9, and its key parameters are listed in Table III. DSP is used for deploying control algorithms, and FPGA is for PWM wave generation and sensor data acquisition.

The following four algorithms are applied to the platform for comparisons in this section:

Algorithm 1 (Algo 1): simplified algorithm proposed in [10].
Algorithm 2 (Algo 2): simplified algorithm proposed in [13].
Algorithm 3 (Algo 3): combined with the requirement of avoiding excessive ΔV, all 27 basic VVs are evaluated to get the optimal one. Thus, this enumeration approach guarantees the globally optimal result in the current control and NPV control.
Algorithm 4: the proposed FSM-MPC algorithm.

The cost function of the Algos 1–3 is (11); for the FSM-MPC algorithm, it is (23). The tuning of λ in the cost function depends on the fluctuation of NPV, and the two are positively correlated. Since there are no theoretical guidelines [7], λ is tuned by trial and error. Finally, λ in (11) is set to 0.15; in (23), λ is 0.01. As a result, the fluctuations of these four algorithms are reasonable and basically consistent.

For conciseness, the experimental test conditions are summarized in Table IV. I^* and f^* represent the amplitude reference and the frequency reference of inverter output currents, respectively.

TABLE IV
TEST CONDITIONS

Condition	I^*	f^*
Case 1	2 A	50 Hz
Case 2	4 A	50 Hz
Case 3	Step from 2 to 4A	50 Hz
Case 4	Step from 4 to 2A	50 Hz

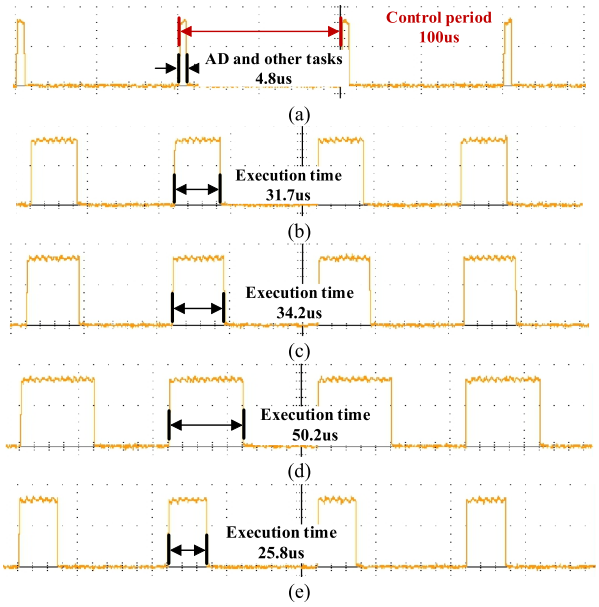

Fig. 10. Execution time. (a) AD and other tasks. (b) Algo 1. (c) Algo 2. (d) Algo 3. (e) Proposed FSM-MPC algorithm.

A. Execution Time

To compare the computational efficiency, an input/output (I/O) port of DSP is utilized to evaluate execution time. The voltage level of this I/O port is set to "1" when executing a specific program and "0" when this program is finished.

The control period is equal to the sampling period, which is 100 us, as shown in Fig. 10(a). As displayed in Fig. 10(b) and (c), the two existing simplified Algos 1 and 2 take 31.7 us and 34.2 us, respectively, since they simplify the control set. For Algo 3, evaluating 27 basic VV one by one takes a long time (50.2 us), as shown in Fig. 10(d). In contrast, the proposed FSM-MPC algorithm takes only 25.8 us, as shown in Fig. 10(e). The reason is that the cost function (23) proposed in this article greatly reduces the calculation amount, so the total execution time is smaller. Thus, the proposed FSM-MPC algorithm significantly improves computational efficiency.

B. Steady-State Experimental Evaluation

To compare the steady-state performance of these four algorithms, experiments are performed under Cases 1 and 2. Fig. 11 displays the experimental results, including the line-to-line voltage (u_{ab}), phase voltage (u_{aN}), dc-link upper capacitor voltage (u_{c1}), the output current of phase A (i_a), and the total harmonic distortion (THD) of i_a under Case 1. Fig. 12 shows the corresponding experimental waveforms under Case 2. To obtain frequency spectrums of i_a in Figs. 11 and 12, the waveform data in the oscilloscope is imported into MATLAB; then, the fast Fourier transform is performed in Simulink.

The following aspects are shown in Figs. 11 and 12.

1) For these four algorithms, the peak-to-peak voltages of u_{aN} and u_{ab} are u_{dc} and $2u_{dc}$, respectively, while the max voltages jumps are different.
2) Excessive ΔV in phase and line-to-line voltages (marked with red circles) appear with Algos 1 and 2. While for Algo 3 and the proposed FSM-MPC algorithm, excessive ΔV is avoided.
3) Compared to Algo 3 with selected optimal VV, the proposed FSM-MPC algorithm has almost the same control performance, and its execution time is only 50% of Algo 3. It means the proposed FSM-MPC algorithm is good and fast.
4) For the proposed FSM-MPC algorithm and Algo 3, the THD of i_a is lower than the other two algorithms. Thus, avoiding excessive ΔV is beneficial to the current control performance.
5) There is no apparent fluctuation in NPV, which means the proposed FSM-MPC has good capability in NPV control.

Besides, for these four algorithms, the average switching frequencies under Case 1 are 1450, 1441, 1035, and 1037 Hz, obtained by counting the pulses in the FPGA. It can also be confirmed in the zoomed view of Fig. 11: for Algo 3 and the proposed FSM-MPC algorithm, the number of changes in u_{aN} is about two-thirds of the other two algorithms. That is, Algo 3 and the proposed FSM-MPC algorithm make current control more effective at a relatively low average switching frequency. It also means low switching losses.

Furthermore, the *dq*-axes current is analyzed under Case 2. Since the above-mentioned experimental results of the Algos 1 and 2 are similar, only Algo 1 is analyzed experimentally. Similarly, for Algo 3 and the proposed FSM-MPC algorithm, the latter is selected. Fig. 13(a) shows the steady-state current of Algo 1 under Case 2, and the *dq*-axes current is obtained by importing the three-phase current into MATLAB. Similarly, Fig. 13(b) shows the experimental results of the proposed FSM-MPC algorithm. A comparison of Fig. 13(a) and (b) reveals that excessive ΔV causes larger fluctuation in *dq*-axes current, particularly in the *d*-axis current. And examples are shown in Fig. 13(a), marked with red boxes with dashed line. Thus, avoiding excessive ΔV results in better *dq*-axes current.

Finally, the system efficiency is analyzed. For Algo 1 and the proposed FSM-MPC algorithm, the experimental results of system efficiency under different output current are shown in Fig. 14. Among them, under Case 1, the system efficiency is 88.0% and 88.7%, respectively; under Case 2, it is 93.6% and 94.0%, respectively. Thus, compared with Algo 1, the proposed FSM-MPC algorithm has higher system efficiency.

C. Dynamic Experimental Evaluation

To study the dynamic response, experiments under Cases 3 and 4 are conducted. Figs. 15 and 16 show the results, including u_{ab}, u_{aN}, u_{c1} and i_a. When the current reference is suddenly stepped, excessive ΔV in phase and line-to-line voltages appear,

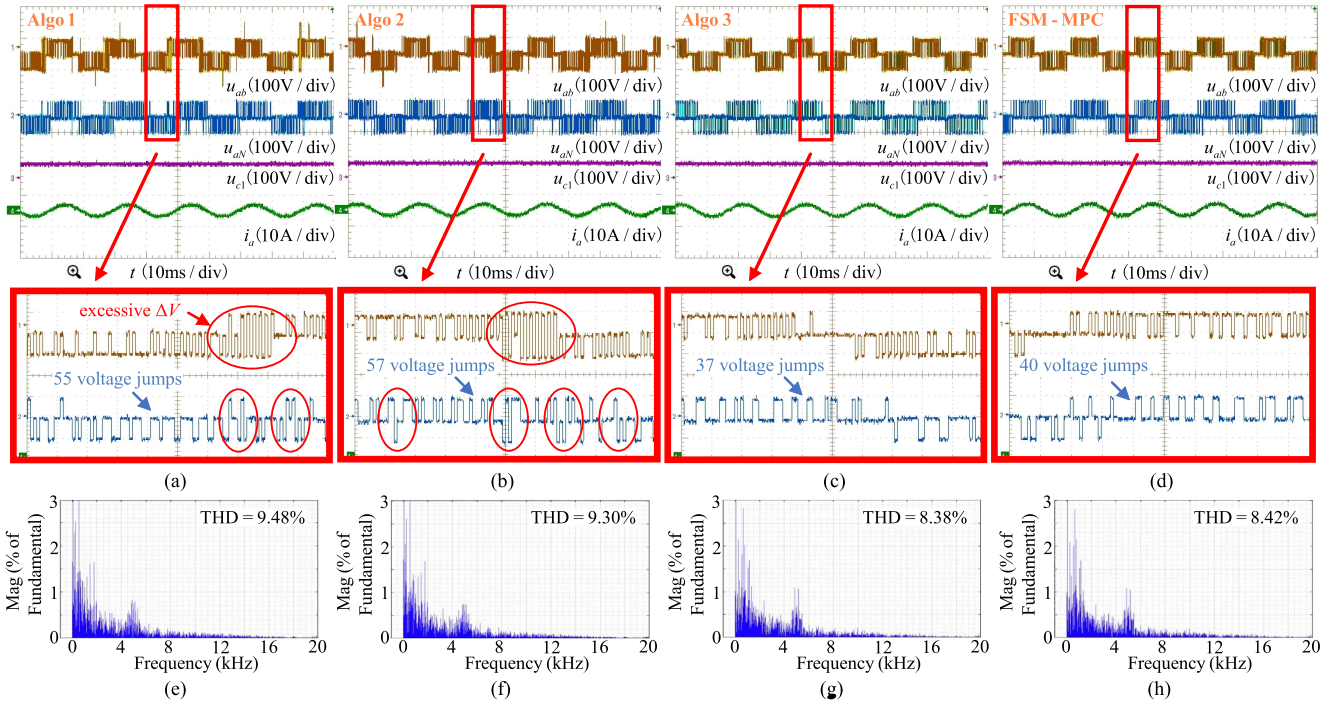

Fig. 11. Steady-state experimental results under Case 1. (a) and (e) for the Algo 1. (b) and (f) for the Algo 2. (c) and (g) for the Algo 3. (d) and (h) for the proposed FSM-MPC algorithm.

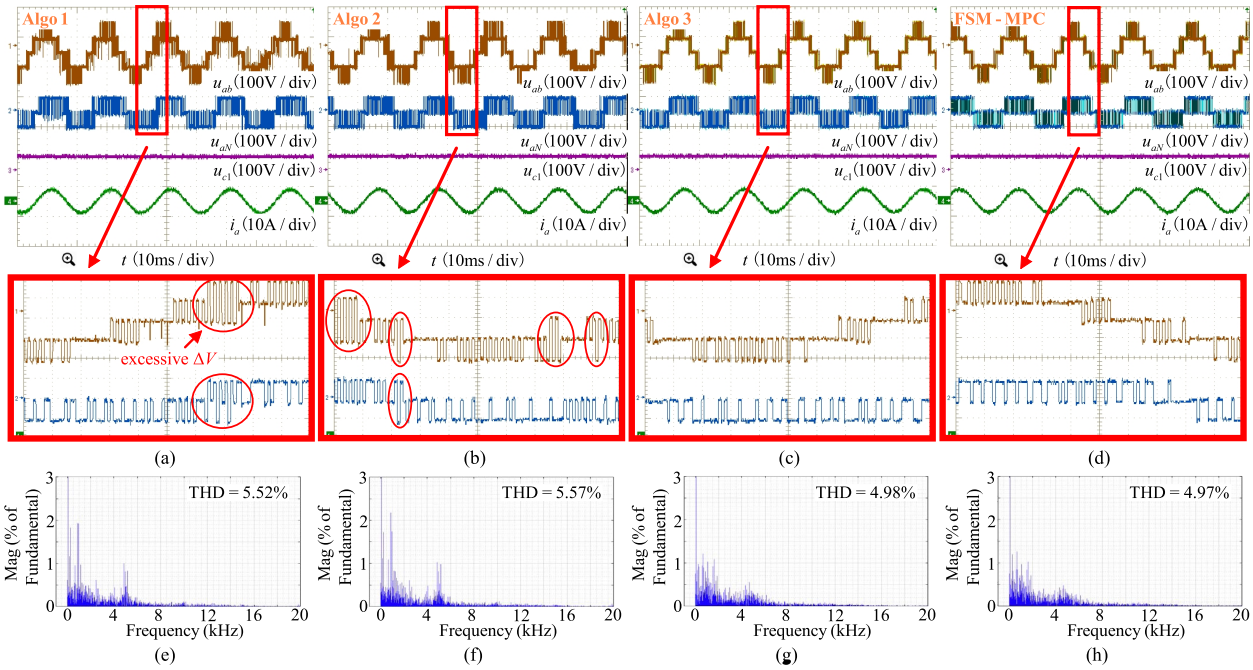

Fig. 12. Steady-state experimental results under Case 2. (a) and (e) for the Algo 1. (b) and (f) for the Algo 2. (c) and (g) for the Algo 3. (d) and (h) for the proposed FSM-MPC algorithm.

for Algos 1 and 2. In particular, the maximum ΔV of line-to-line voltage is up to 150 V. If the current reference changes more, it could theoretically be 200 V.

For Algo 3 and the proposed FSM-MPC algorithm, phase and line-to-line voltages change step by step (marked with blue circles). Besides, the waveforms of line-to-line voltage are similar, and the waveforms of phase voltage are different. The reason is that the NPV control affects the selection of redundant VVs. And redundant VVs at the same position in the space vector diagram result in different phase voltages and the same line-to-line voltages. That is, it is confirmed that the optimal VV selected by the proposed FSM-MPC algorithm is the same

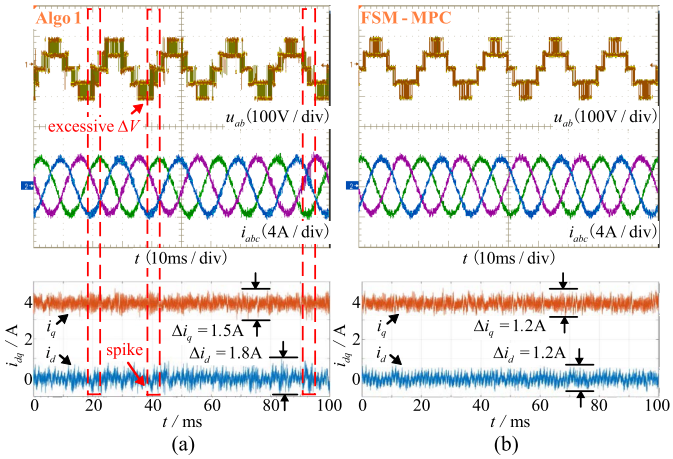

Fig. 13. *dq*-axes current under Case 2. (a) Algo 1. (b) Proposed FSM-MPC algorithm.

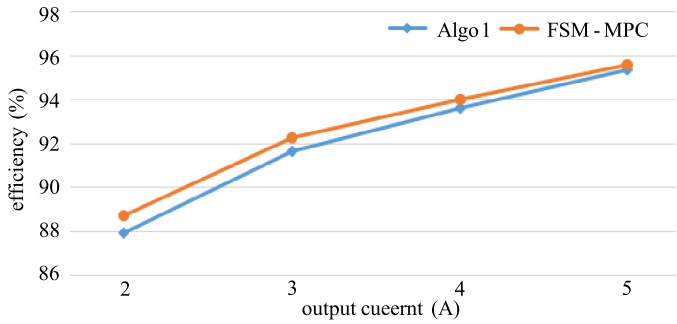

Fig. 14. System efficiency under different output current.

TABLE V
QUANTITATIVE COMPARISON OF PERFORMANCE

	Execution time	Max change in line-to-line voltage	Max change in phase voltage	THD		Average switching frequency	
				Case 1	Case 2	Case 1	Case 2
Algo 1	31.7 us	150 V	100 V	9.48%	5.52%	1450 Hz	1476 Hz
Algo 2	34.2 us	150 V	100 V	9.30%	5.57%	1441 Hz	1485 Hz
Algo 3	50.2 us	50 V	50 V	8.38%	4.98%	1035 Hz	1045 Hz
FSM-MPC	25.8 us	50 V	50 V	8.42%	4.97%	1037 Hz	1041 Hz

as Algo 3 in the $\alpha\beta$ frame, even though the number of candidate VVs is reduced.

Plus, for these four algorithms, output current responds within 1 ms with no significant change in NPV in Figs. 15 and 16. So, the proposed FSM-MPC algorithm is characterized by a good transient response.

In summary, the quantitative comparison of these four algorithms is shown in Table V.

D. NPV Control Performance Evaluation

To further test the capability of the proposed FSM-MPC algorithm in NPV control, first, unbalanced capacitor voltages are set by adding an offset (−50 V) to $\Delta u^p(k+1)$ in (23); then, the offset is removed. The experimental result is shown in Fig. 17. The output current is distorted when capacitor voltages are unbalanced. And capacitor voltages become balanced within 5 ms, which means the proposed FSM-MPC has good capability in NPV control.

TABLE VI
EXPERIMENTAL RESULTS OF ROBUST PERFORMANCE

	Algo 1	Algo 2	Algo 3	FSM-MPC
–	5.52%	5.57%	4.98%	4.97%
$L_m/L = 0.75$	6.35%	6.46%	5.73%	5.75%
$L_m/L = 0.5$	9.03%	8.87%	8.03%	8.01%
$R_m/R = 0.75$	5.71%	5.78%	5.12%	5.13%
$R_m/R = 0.5$	6.16%	6.12%	5.43%	5.40%

E. Robust Performance Evaluation

The predictive model as well as $\boldsymbol{v}^*$ highly depends on the exact parameters of the *R-L* filter model. In this test, the robust performance of these four algorithms is analyzed by changing the electric-circuit parameters in the control system (L_m and R_m) under Case 2. Table VI shows the THD of i_a, when L_m and R_m are set to half or three-quarters of L and R, respectively. When the parameter fluctuation occurs, for Algo 3 and the proposed FSM-MPC algorithm, the THD of i_a is still about the same and smaller than the other two algorithms. Thus, the effect of improving current control performance by avoiding excessive ΔV is robust.

Furthermore, compared with R, the mismatch of L has a greater impact on the control performance. For the proposed FSM-MPC algorithm, the main experimental results under Case 2 are shown in Fig. 18, when L is mismatched. There is no excessive ΔV in phase or line-to-line voltages. Thus, when parameter fluctuation occurs, the proposed FSM-MPC algorithm still works, avoiding excessive ΔV.

V. CONCLUSION

This article proposes a low complexity FSM-MPC algorithm for three-phase 3L inverters. The proposed algorithm is evaluated experimentally for a 3L VSI, compared with the enumeration method considering excessive ΔV and two existing simplified algorithms proposed in [10] and [13]. Based on the above-mentioned analysis, the main conclusions are drawn as follows:

1) The proposed FSM-MPC algorithm significantly improves computational efficiency, owing to the simplified control set and the cost function (23). Meanwhile, it should be pointed out that the optimal VV obtained in $\alpha\beta$ frame is the same as the enumeration method.
2) For the proposed FSM-MPC algorithm with a simplified control set, whether in the steady-state or the dynamic process, it is guaranteed that there is no excessive ΔV in phase and line-to-line voltages, which is a benefit for the security of inverter operation.
3) Compared with the existing simplified algorithms, the proposed FSM-MPC is more efficient. Avoiding excessive ΔV makes current harmonics smaller at a relatively low average switching frequency. Furthermore, the FSM-MPC algorithm is robust, when the electric-circuit parameters are mismatched in the control system.

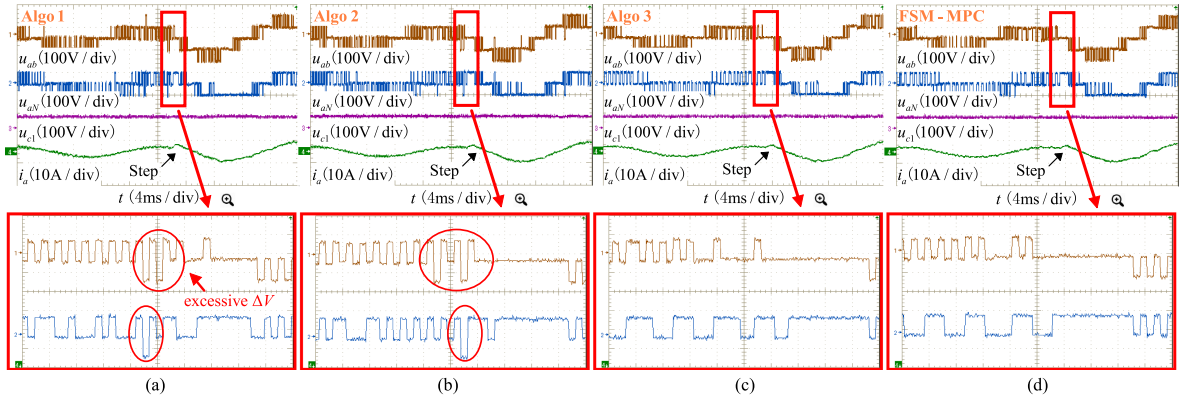

Fig. 15. Dynamic experimental results under Case 3. (a) Algo 1. (b) Algo 2. (c) Algo 3. (d) Proposed FSM-MPC algorithm.

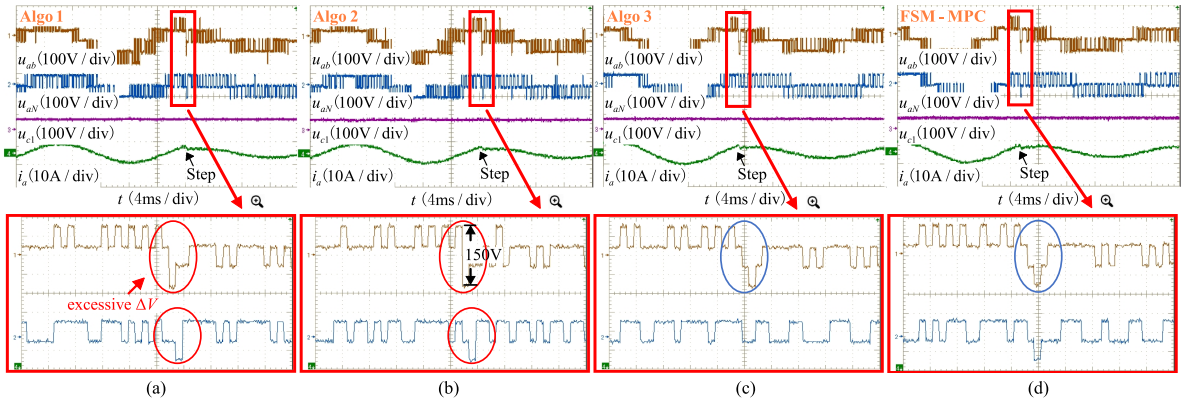

Fig. 16. Dynamic experimental results under Case 4. (a) Algo 1. (b) Algo 2. (c) Algo 3. (d) Proposed FSM-MPC algorithm.

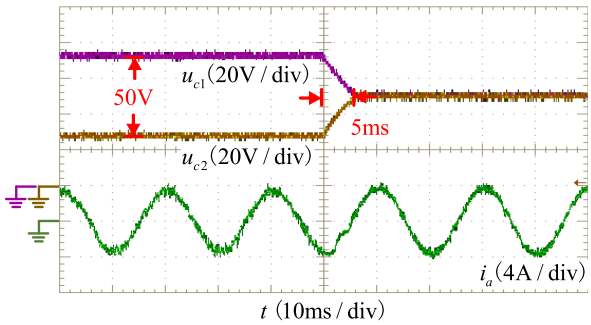

Fig. 17. Experimental result of NPV control.

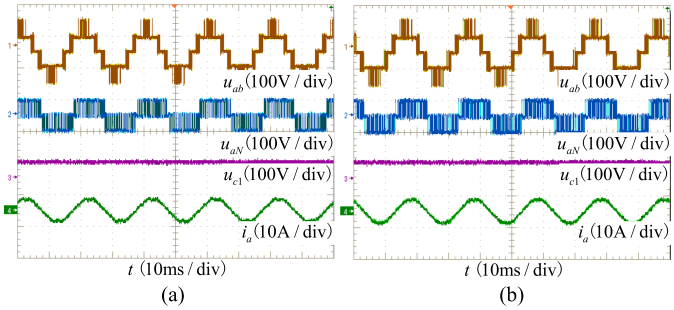

Fig. 18. Experimental results of L_m variation under Case 2. (a) $L_m/L = 0.5$. (b) $L_m/L = 0.75$.

4) The proposed FSM-MPC algorithm has good steady-state performance and fast dynamic response. Since the control period could increase with improved computational efficiency, the control performance could be further improved.

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