Modulation-Based DC-Bias Elimination of DAB Converter Under Second Harmonic

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***Abstract*—As a basic unit of solid-state transformer, the single-phase system composed of H-bridge and dual-active-bridge (DAB) is becoming an exciting topic for its high-efficiency, flexible power flow. However, the inherent second-harmonic power brings dc-link voltage ripple and phase shift oscillation, especially for the back-to-back systems with bilateral harmonics. In this article, the behavior of DAB's high-frequency link under second harmonic is modeled and described, revealing the inevitable dc-bias and current-stress increase. A modulation-based dc-bias eliminating strategy is presented, which uses two sawtooth carriers to generate a transitional period without any calculations. To reduce magnetic material's waste, a second-harmonic correction to transformer design is proposed. Moreover, the optimal inductance for single-phase shift with minimal current stress and full-range zero-voltage soft switching is obtained. These strategies enhance the ripple immunity of DAB, enabling the reduction of dc-link capacitance. Comprehensive simulations and experiments are performed to validate the accuracy and effectiveness of these optimizations.**

***Index Terms*—DC-bias, dual-active bridge (DAB), parameter optimization, second harmonic.**

I. Introduction

THE SOLID-STATE transformers based on dual-active bridge (DAB) converters have been widely used and studied in energy storage systems [1], railway traction and smart grid [2]. Compared with traditional line-frequency transformers, solid-state transformer (SSTs) reduce copper and iron consumption, enabling the output voltage regulation, flexible power flow, and power quality conditioning [3].

Fig. 1 shows a typical SST application in back-to-back system with input-series output-parallel structure, which can regulate the power flow between medium- and low-voltage grids [4], [5], [6]. Under neutral connection, the whole system can be decomposed into several independent single-phase sub-modules where the second-harmonic power occurs. As discussed in [7] and [8], this ripple power generates the second-harmonic voltage (SHV) in dc-link and distorts the output power quality. In conventional design, the bulky dc-link capacitors that account for more than 20% of system volume must be used to buffer this low-frequency fluctuation [9]. Some literatures proposed the fluctuating power control that transmits the second-harmonic power through DAB to the load [10], [11], [12], [13], [14]. With this approach, the dc-link capacitors just need to buffer the high-frequency switching ripple, and the capacitance requirement can be reduced a lot. However, the fluctuating power increases the current stress of high-frequency link dramatically [12], [13]. Due to the asynchronous second-harmonic power of each side, this method cannot be used in the back-to-back energy conversion. Hence, enhancing the ripple immunity of CHB and DAB to allow larger SHV in dc-link is a compromise to adopt smaller capacitors. The quantitative description and improvement of this immunity is presented in this article from the view of DAB's high-frequency link.

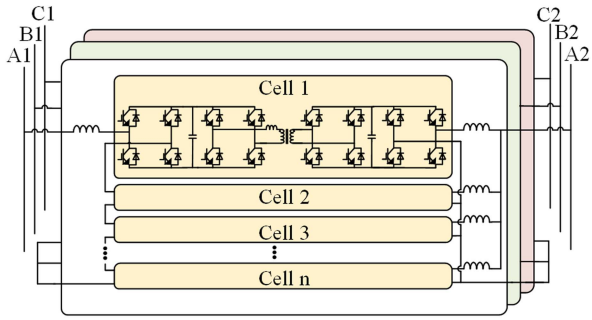

Fig. 1. Back-to-back system with input-series output-parallel structure.

One critical issue concerning DAB in practice is the dc-bias current caused by voltage-second imbalance. The dc bias in exciting inductor leads to the conservative design with low flux density for nanocrystalline-based transformers [15], giving rise to the waste of material. As for the auxiliary inductor, dc bias causes a sharp increase of current stress to semiconductors and windings during the transient process. Basically, the dc-bias current in DAB converter can be classified into three categories according to the imbalance's time scale: the steady-state dc-bias, the transient dc-bias and the periodic dc-bias. The steady-state dc-bias can be effectively suppressed by the symmetrical hardware design, including the power devices' selection and layout optimization [16]. Due to simplicity, the series-connected capacitor with transformer is a commonly used flux-balancing

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strategy, but it has drawbacks in cost, volume, efficiency and dynamic response especially for high-power applications [15], [29], [30]. Most literatures are focused on the transient dc-bias caused by dynamic process, including the dynamic optimization method [17], [18], [19], straightforward transient control [20], [21], piecewise linear transient phase-shift optimization [22], [23], [24], [25]. A common drawback of these methods is the time-consuming issue, requiring additional calculation during the transient. However, under periodic disturbance, this transient process persists in the whole operation. For example, SHV in dc-link is inevitably sampled and feedbacked into the DAB's phase shift, resulting in constantly updating transients that consume the computing resources continuously. To enhance the immunity to SHV, the behaviors of DAB's high-frequency link under second harmonic are modeled and described in this article, revealing the inevitable dc-bias issue. Furthermore, a novel updating strategy without additional calculation is proposed and tested to eliminate the dc-bias in the entire high-frequency link.

Apart from the dc-bias, the current stress optimization of DAB's high-frequency link has been studied in [13] and [14] under fluctuating power control. The second harmonic current shaping method based on feedforward compensation is proposed in [13] considering secondary-side SHV, but this method is complicated to implement. In [14], the third-order harmonic is injected into CHB's modulation waveform to reduce the peak-current stress of DAB's high-frequency link. But this method is limited by the maximum modulation index of CHB. What's more, [13], [14] are both focused on the fluctuating power control, and cannot be used in back-to-back system. In this article, a quantitative model of peak and RMS current stress is built to reveal the impact of SHV, based on which, the optimized design of the auxiliary inductor and high-frequency transformer is proposed.

The remainder of this article is organized as follows: Section II analyses the mechanism of voltage-loop controlled DAB and reveals the limited performance of second-harmonic notch filter due to the conflict between filtering effect and dynamic response. Sections III and IV build the quantitative model of the ripple current and dc-bias current in exciting and auxiliary inductor. Following that, the optimization to high-frequency link with smaller current stress and full-range zero-voltage soft switching (ZVS) is proposed. Section V presents the working principle of a novel modulation-based dc-bias eliminating strategy and the second-harmonic correction to transformer design. The experimental verification proceeds in Sections VI and VII. In Section VIII, a performance comparison of commonly used power decoupling methods is presented. The conclusion is summarized in Section IX.

II. Operation Principle and Ripple Quantization

A. Operation Principle

Due to the symmetrical structure of back-to-back system, one submodule is selected as the benchmark shown in Fig. 2. For DAB, the single phase-shift (SPS) modulation is commonly used to regulate the power flow by adjusting phase-shift angle between v_{AB} and v_{CD}. The steady-state working sequence is

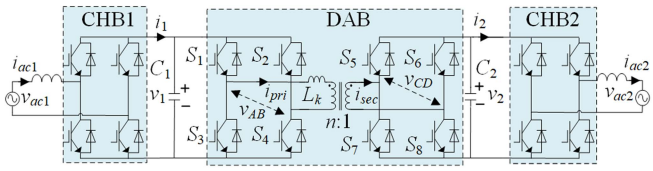


Fig. 2. Single-phase submodule of back-to-back system.

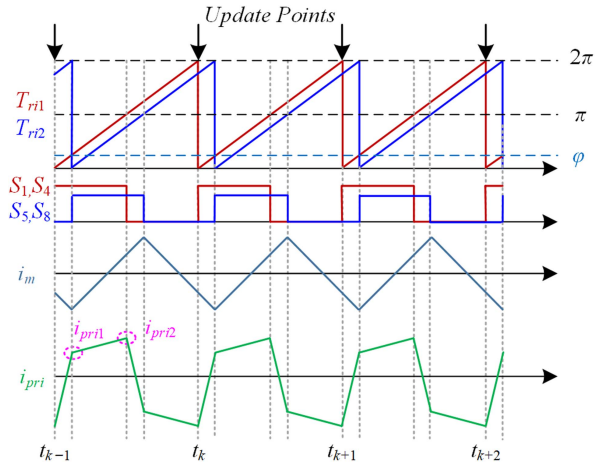


Fig. 3. Operating waveforms of DAB in steady-state.

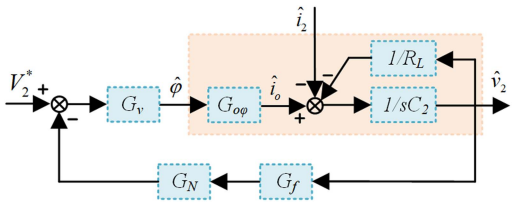


Fig. 4. DAB's voltage-loop control diagram.

shown in Fig. 3. T_{ri1} and T_{ri2} are the sawtooth carriers of the primary and secondary bridge, respectively. T_{ri1} is fixed as the time base. T_{ri2} moves according to the phase shift which updates at the update points. The output power of DAB is obtained as

$$P_{\text{out}} = \frac{nv_1v_2\varphi(\pi-\varphi)}{2\pi^2 f_s L_k} \tag{1}$$

i_{pri} is the current of auxiliary inductor. Assuming the transfer of current from the device to diode on turn-OFF is instantaneous [26], [27], the ZVS of the primary and secondary sides can be achieved under $i_{\text{pri1}} > 0$ and $i_{\text{pri2}} > 0$. Without loss of generality, the turns ratio n of the medium-frequency transformer is set as V_1/V_2 to get the maximum ZVS range. The exciting inductor is clamped by v_{CD}, so the exciting current i_m keeps the isosceles-triangle shape.

In system level, the dc-link voltage in primary side is regulated by CHB1, dc-link voltage in secondary side is regulated by DAB, and CHB2 is responsible for output power setting. Fig. 4 shows the voltage-loop control diagram of DAB. R_L is the equivalent DC load. i_2 represents the load disturbance including second-harmonic fluctuation. G_v is a PI regulator. $G_{o\varphi}$ is the transfer function from phase-shift angle φ to output current i_2. G_f is the low-pass filter that removes the switching noise and implements

anti-aliasing with cutoff frequency at f_L. G_N is a notch filter to damp the second harmonic with center frequency ω_n located at 2ω where ω is the grid's angular frequency

$$G_v = K_p + \frac{K_i}{s} \tag{2}$$

$$G_{o\varphi} = \frac{(\pi - 2\varphi)\, nV_2}{2\pi^2 f_s L_k} \tag{3}$$

$$G_N = \frac{s^2 + \omega_n^2}{s^2 + 2h\omega_n s + \omega_n^2} \tag{4}$$

$$G_f = \frac{1}{s/2\pi f_L + 1}. \tag{5}$$

B. Ripple Quantization

Setting the primary grid's phase angle as a reference, v_{ac1}, v_{ac2}, i_{ac1}, and i_{ac2} can be expressed as

$$\begin{cases} v_{ac1} = V_{m1} \sin(\omega t) \\ i_{ac1} = I_{m1} \sin(\omega t + \alpha) \end{cases}$$

$$\begin{cases} v_{ac2} = V_{m2} \sin(\omega t + \beta) \\ i_{ac2} = I_{m2} \sin(\omega t + \beta + \alpha). \end{cases} \tag{6}$$

Where V_{m1}, V_{m2} is the amplitude of gird voltage, β is the phase difference between two girds, and α is the power factor angle.

From above, the dc-link power can be obtained as:

$$\begin{cases} p_1 = [\cos\alpha - \cos(2\omega t + \alpha)]\, S \\ p_2 = [\cos\alpha - \cos(2\omega t + 2\beta + \alpha)]\, S \end{cases} \tag{7}$$

where $S = V_{m1}\, I_{m1}/2 = V_{m2}\, I_{m2}/2$ is the apparent power.

As seen, the second-harmonic power is generated on both sides, and related to the grid's phase angle. p_1-p_2 is the total power buffered by dc-link capacitors. In the applications of driving passive load, β can be regulated to zero to synchronize the second-harmonic power ($p_1 = p_2$), so the fluctuating power control effectively reduces the capacitance requirement. But in the back-to-back system, β is determined by the girds. The ripple power cannot counterbalance with each other, and may even be enhanced if $\beta \notin [-\pi/6, \pi/6] \cup [5\pi/6, 7\pi/6]$. Hence, controlling DAB to transmit only the dc power and buffering the ripple power by respective dc-link capacitors, is a compromise to reduce the SHV in back-to-back applications.

Assuming the allowable SHV ratio is δ on both sides, the dc-link capacitance is calculated as

$$\begin{cases} C_1 = \frac{S}{2\omega\delta V_1^2} \\ C_2 = \frac{S}{2\omega\delta V_2^2} \end{cases} \tag{8}$$

where $\delta = \Delta V_{2\omega j}/V_j$, $\Delta V_{2\omega j}$ is the SHV's amplitude.

From (7) and (8), the dc-link voltage is obtained as

$$\begin{cases} v_1 = V_1 - \delta V_1 \sin(2\omega t + \alpha) \\ v_2 = V_2 + \delta V_2 \sin(2\omega t + 2\beta + \alpha) \end{cases}. \tag{9}$$

The SHV becomes larger with smaller dc-link capacitance, which influences the normal operation of DAB. According to Fig. 4, SHV in dc-link is inevitably sampled and feedbacked into the DAB's control loop, contributing to the phase-shift oscillation. This voltage ripple should be filtered out by second-harmonic notch filter to achieve constant power transmission. From Fig. 4, the phase-shift angle can be expressed as

$$\varphi = \varphi_{dc} + \varphi_{2\omega} \cos(2\omega t + 2\beta + \alpha + \theta) \tag{10}$$

where

$$\begin{cases} \varphi_{\rm dc} = \frac{\pi}{2} - \frac{\pi}{2}\sqrt{1 - \frac{8 f_s L_k P_{\rm out}}{n V_1 V_2}} \\ \varphi_{2\omega} = \frac{S}{V_2}\left|\frac{G_N G_f G_v}{sC_2 + 1/R_L + G_N G_f G_v G_{o\varphi}}\right|_{s=j2\omega} \\ \theta = \arg\left(\frac{G_N G_f G_v}{sC_2 + 1/R_L + G_N G_f G_v G_{o\varphi}}\right)_{s=j2\omega} \end{cases}.$$

From above, the oscillation's amplitude $\varphi_{2\omega}$ is related to the notch filter's properties that are determined by the parameter h in (4). Fig. 5 shows the amplitude-frequency response of the notch filter under different h. As noted, increasing the value of h leads to a wider notch bandwidth and improved rejection of variations in the grid frequency.

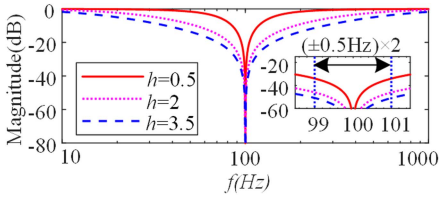


Fig. 5. Amplitude-frequency response of notch filter under different h.

TABLE I
SYSTEM PARAMETER VALUES

Parameter	*Meaning*	*Value*
S	rated power	500 VA
V_1, V_2	dc-link voltage	100 V
v_{ac}	output ac voltage	50 Vp
n	turns ratio	1:1
f_s	switching frequency	20 kHz
L_k	auxiliary inductor	50 μH
C_1, C_2	dc-link capacitor	800 uF

However, there exists a conflict between DAB's dynamic and G_N's filtering performance. Based on the main circuit parameters given in Table I., Fig. 6(a) shows the root locus of system's leading poles about h under different crossover frequencies. As seen, the insertion of notch filter threatens the system's stability. The crossover frequency must be reduced to keep enough stability margin and damping ratio. And the allowable notch bandwidth decreases as the crossover frequency increases. After considering the light load conditions, this filter effect must be further reduced as shown in Fig. 6(b). Hence, the filtering of second harmonic may not be sufficient in practice due to the requirement of dynamic response time and stability margin.

According to the grid-connected standards, the allowable variation of grid frequency is ±0.5-Hz [28]. If the parameter

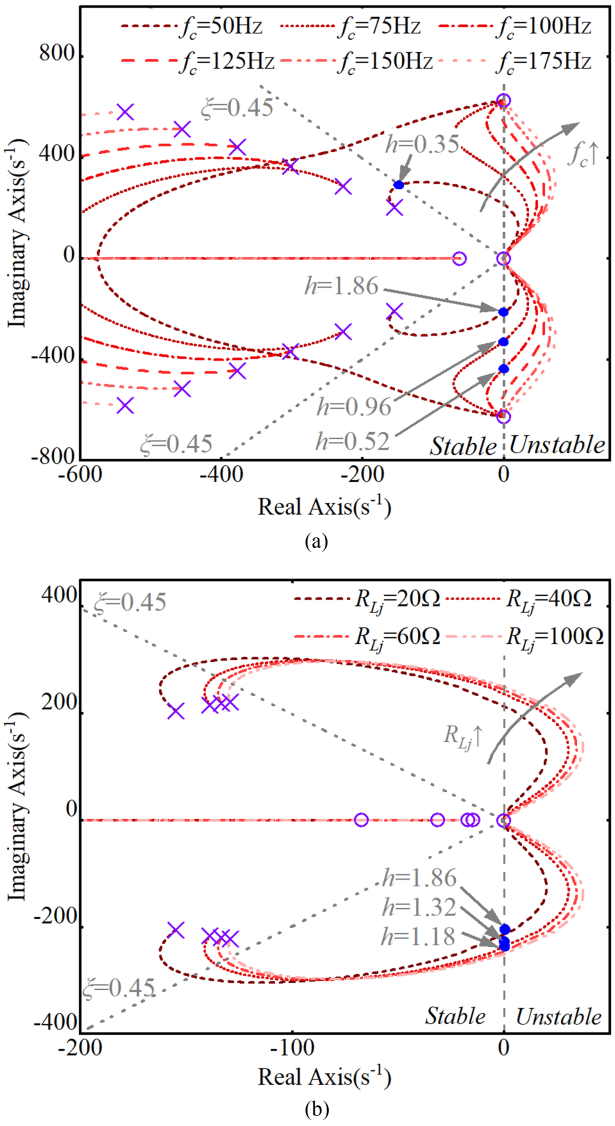


Fig. 6. Root locus of leading poles in DAB control loop with notch filter parameter h. (a) Under different cutoff frequency f_c. (b) Under different load R_{Lj}.

h is set to 0.35 with crossing frequency $f_c = 50$-Hz and damping ratio $\xi = 0.45$, the peak-to-peak value of phase-shift oscillation is 0.01, accounting for 2.8% of steady-state value. In practice, this filtering effect could be further weakened due to the spectral leakage during the discretization process. Therefore, the ripple in DAB's phase shift needs to be considered to get the system's exact performance under second harmonic.

III. Exciting Current Under DC-Link Voltage Ripple

The flux design of magnetic core is related to the maximum exciting current. Transient dc-bias of exciting current has been fully discussed and resolved by other literatures. But its behavior under second harmonic has never been elaborated. Hence, a detailed quantitative analysis of this issue is derived in this section.

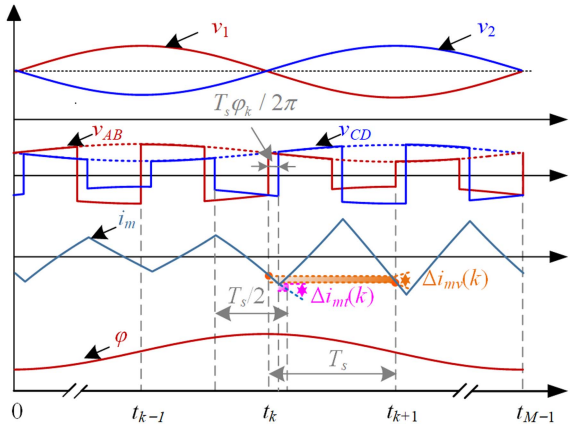


Fig. 7. Acting moments of different imbalance factors under second harmonic. DC-bias current caused by voltage-imbalance Δi_{mv}, DC-bias current caused by time-imbalance Δi_{mt}.

The exciting inductor in DAB is clamped by the midpoint voltage v_{CD} on the secondary side. Consequently, volt-second imbalance of v_{CD} is the root reason for exciting current's dc-bias. According to the different action moments, the imbalance factors can be divided into two categories: the voltage imbalance caused by the asymmetry amplitude of v_{CD}, and the time imbalance caused by the non-50% duty cycle of v_{CD}. More specifically, the amplitude of v_{CD} is modulated by the dc-link voltage v_2, so the positive and negative voltage is asymmetrical. As for the non-50% duty cycle, it is caused by the updating of the oscillating phase-shift angle. Hence, the voltage imbalance is in the time scale of the switching period, and the time imbalance happens only during updating process. Fig. 7 shows the dc-bias current Δi_{mv} and Δi_{mt} corresponding to these two imbalance factors. Due to the different acting moments, it is possible to decoupling the calculation of dc-bias caused by dc-link voltage and phase-shift oscillation. Ultimately, the total dc-bias can be accurately determined by summing these separate components.

A. Exciting Current Caused by Voltage Imbalance

From Fig. 7, v_{CD} is asymmetric due to the fluctuation of dc-link voltage. While the asymmetry may be negligible within one single switching period, the effect can accumulate over the course of a second-harmonic period, leading to an increased risk of flux saturation in the magnetic core [15].

According to Fig. 7, the dc-bias accumulation during the k_{th} switching period can be represented as

$$\Delta i_{mv}(k) = \int_{kT_s+T_s\varphi_k/2\pi+T_s/2}^{kT_s+T_s\varphi_k/2\pi} \frac{v_2}{L_m}dt - \int_{kT_s}^{kT_s+T_s\varphi_k/2\pi} \frac{v_2}{L_m}dt - \int_{kT_s+T_s\varphi_k/2\pi+T_s/2}^{(k+1)T_s} \frac{v_2}{L_m}dt. \quad (11)$$

Substituting (9) into (11), $\Delta i_{mv}(k)$ is obtained as a function of φ_k and k. After calculating the partial derivative, the maximum value about φ_k appears at $\varphi_k = 0$. Substituting $\varphi_k = 0$ into (11),

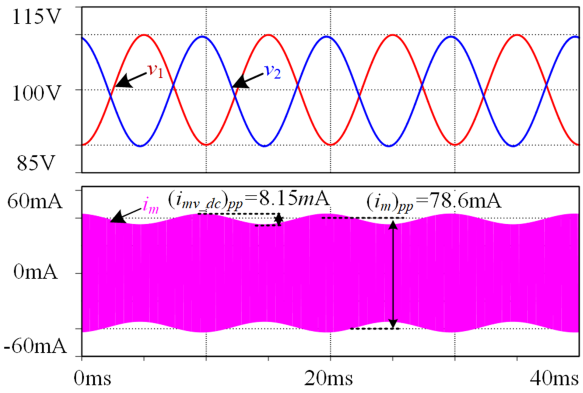


Fig. 8. Simulation waveforms of exciting current under SHV.

the total dc-bias exiting current until $k_{\rm th}$ is obtained as

$$i_{mv\_dc}(k) = \sum_{i=1}^{k} \Delta i_{mv}(i) = \frac{A_\omega S}{4\omega^2 L_m C_2 V_2} \sum_{i=1}^{k} \cos(2\omega T_s i + 2\beta + \alpha + \phi) \tag{12}$$

where

$$A_\omega = \sqrt{2\cos(2\omega T_s) - 8\cos(\omega T_s) + 6}.$$

From (12), the dc-bias caused by voltage imbalance is periodic. What really matters is the peak exciting current. To get this, the approximation shown in (13) is used. The ratio of maximum dc-bias to normal exciting current is obtained as

$$\sum_{i=0}^{M/2} \sin(2\omega T_s i) \approx \frac{\int_0^{\pi/2\omega} \sin(2\omega t)\, dt}{T_s} = \frac{1}{\omega T_s} \tag{13}$$

$$\kappa_m = \frac{(i_{mv\_dc})_{pp}}{(i_m)_{pp}} = \frac{A_\omega}{\omega^2 T_s^2}\delta \approx \delta. \tag{14}$$

As seen, the increasing proportion of exciting current is approximately equal to the SHV ratio, and the approximation error is smaller than 3.2% with $f_s/f_\omega > 10$. Hence, (14) provides a convenient guideline for the design margin of magnetic flux under second-harmonic conditions. Fig. 8 shows the simulation waveforms of exciting current under open-loop control. The increasing proportion (10.4%) meets well with the theoretical result (9.9%).

B. Exciting Current Caused by Phase-Shift Oscillation

The analysis in Section II indicates that phase-shift ripple exists even with the stable control loop. This ripple causes the small transients between switching periods. Fig. 9 shows the transient process in the high-frequency link of DAB under conventional updating strategy. In Fig. 9(a), the new phase-shift angle $\varphi+\Delta\varphi$ is received during t_{k-1}~t_k and updated to the comparison value at t_k. Then, the secondary-side carrier wave T_{ri2} is reset to zero when T_{ri1} intersects with $\varphi+\Delta\varphi$. Finally, the secondary-side PWM signals change synchronously at t_{k1}. While this updating

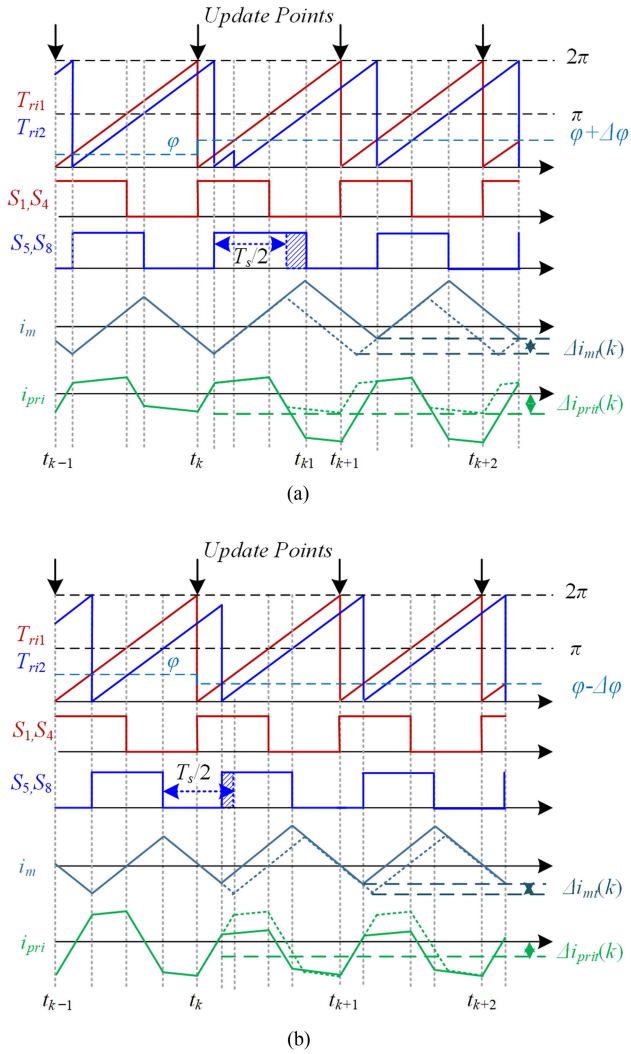


Fig. 9. Transient process of DAB's high frequency link under conventional updating strategy. (a) Phase shift increases from φ to $\varphi+\Delta\varphi$. (b) Phase shift decreases from φ to $\varphi-\Delta\varphi$.

mode is handy to implement with the pure modulation process, the dc-bias is inevitably generated in exciting current, which can be calculated as

$$\Delta i_{mt} = \frac{nV_2T_s}{2\pi L_m}|\Delta\varphi|. \tag{15}$$

The above equation is also applicable for the phase-shift decreasing case as shown in Fig. 9(b). Under transient processes such as the load step, this dc-bias gradually decreases to zero within several switching cycles due to the parasitic resistor. However, a nonnegligible dc-bias occurs if this small offset accumulates along phase-shift oscillation. Substituting (10) into (15), the total dc-bias in exiting current until $k_{\rm th}$ is calculated as

$$i_{mt\_dc}(k) = \frac{nV_2T_s\varphi_{2\omega}}{2\pi L_m} \sum_{i=1}^{k} \left| \begin{array}{l} \sin[2\omega k T_s + 2\beta + \alpha + \theta] \\ -\sin[2\omega(k-1)T_s + 2\beta + \alpha + \theta] \end{array} \right|. \tag{16}$$

In practice, this increasing dc-bias current generates the unbalanced voltage drop across the parasitic resistor. In cases where the margin of magnetic flux is sufficiently large, the dc-bias resulting from phase-shift updating and voltage drop from parasitic resistor may reach an equilibrium state, leading to a constant dc-bias throughout operation. However, this can increase the risk of flux saturation during transient process. If the flux margin is small, the transformer saturation occurs even under steady-state operation. Hence, the dc-bias elimination methods must be adopted in second-harmonic applications.

Obviously, this problem can be addressed using transient dc-bias eliminating strategies. Despite being effective for addressing occasional large transients, methods designed for this purpose often require additional calculations and may not be well-suited for persistent small transients. This is due to the fact that performing these complex calculations every switching cycle can be impractical and computationally expensive. To avoid this, a novel dc-bias eliminating strategy based on modulation is proposed in Section V.

IV. Inductor Current Under DC-Link Voltage Ripple

Unlike the exciting inductor, the auxiliary inductor is affected by the v_{AB} and v_{CD} simultaneously. Hence, the SHV on the primary and secondary sides should be both considered.

A. Inductor Current Caused by Voltage Imbalance

For simplicity, the phase-shift ripple is ignored here, so i_{pri1} and i_{pri2} shown in Fig. 3 can be represented as

$$\begin{cases} i_{\mathrm{pri1}} = \frac{(2\varphi_{\mathrm{dc}}-\pi)v_1+n\pi v_2}{4\pi L_k f_s} \\ i_{\mathrm{pri2}} = \frac{\pi v_1+n(2\varphi_{\mathrm{dc}}-\pi)v_2}{4\pi L_k f_s} \end{cases}. \tag{17}$$

Substituting (9) into (17), i_{pri1} and i_{pri2} are obtained as

$$\begin{cases} i_{\mathrm{pri1}} = I_{\mathrm{pridc}} + I_{\mathrm{pri}\omega}\sin(2\omega t+\alpha+\gamma_1) \\ i_{\mathrm{pri2}} = I_{\mathrm{pridc}} + I_{\mathrm{pri}\omega}\sin(2\omega t+\alpha+\gamma_2) \end{cases} \tag{18}$$

where

$$\begin{cases} I_{\mathrm{pridc}} = \frac{\varphi_{dc}V_1}{2\pi L_k f_s} \\ I_{\mathrm{pri}\omega} = \frac{\delta V_1}{4\pi L_k f_s}\sqrt{2\pi(\pi-2\varphi_{dc})(1+\cos 2\beta)+4\varphi_{\mathrm{dc}}^2} \\ \gamma_1 = \arctan\left(\frac{\pi\sin 2\beta}{\pi\cos 2\beta+\pi-2\varphi_{\mathrm{dc}}}\right) \\ \gamma_2 = \arctan\left(\frac{(2\varphi_{dc}-\pi)\sin 2\beta}{(2\varphi_{dc}-\pi)\cos 2\beta-\pi}\right) \end{cases}.$$

The peak-current stress can be represented by

$$I_{pk} = \max\left[i_{\mathrm{pri1}}, i_{\mathrm{pri2}}\right] = I_{\mathrm{pridc}} + I_{\mathrm{pri}\omega}. \tag{19}$$

According to (10), φ_{dc} can be represented by L_k and P_{out}, so I_{pk} is inherently determined by L_k, P_{out} and β. Fig. 10(a) shows the relationship curves between I_{pk} and L_k under different β. Because the voltage ratio deviates from 1, the peak-current stress increases with the larger SHV phase difference or smaller grid-phase difference β. Hence, the current stress should be designed under $\beta = 0$ to enables the full-range reliable operation.

To guarantee the ZVS on both sides, i_{pri1} and i_{pri2} should be larger than zero during the whole second-harmonic period.

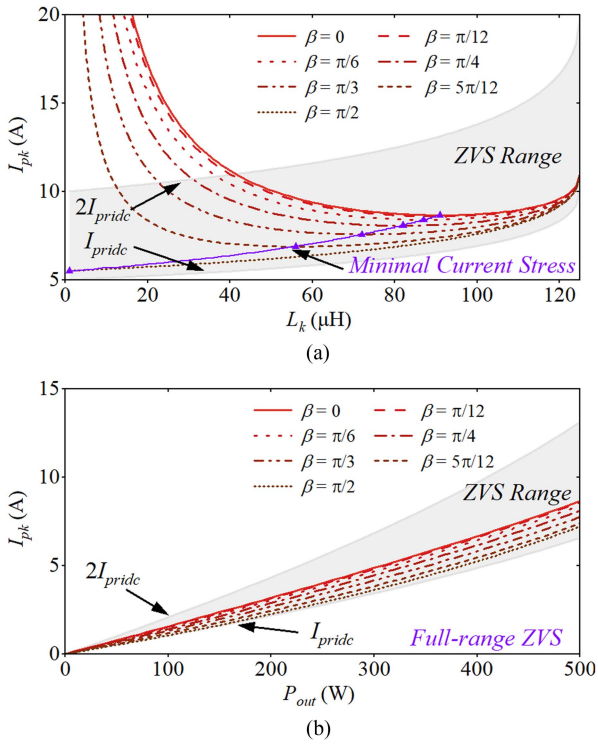


Fig. 10. Peak current stress I_{pk} under different auxiliary inductor L_k and output power P_{out}. (a) Under different auxiliary inductor L_k with rated P_{out}. (b) Under different output power P_{out} with optimal L_k.

According to (18), this requirement can be transformed into $I_{\mathrm{pridc}} < I_{pk} < 2I_{\mathrm{pridc}}$ which is shown in Fig. 10(a) with the grey shade. As seen, an optimal L_k can be selected with minimal current stress and full-range ZVS under the rated condition. Substituting the optimal L_k into (10), (18), (19), the relationship between the peak current and output power under different gird-phase β can be obtained and shown in Fig. 10(b). The ZVS is realized with full-range grid phase β and full-range output power P_{out}. The inherent reason is that the voltage unbalance between the input and output gets smaller and the voltage ratio V_1/nV_2 approaches one with output power decreasing.

Apart from the peak current stress, the RMS value is also enlarged by the second harmonic, which influences the design of the heatsink and transformer. Following the same method above, the RMS value of i_{pri} can be calculated. After some reasonable simplification, the increasing ratio is obtained as (20). This ratio gets larger as the second-harmonic phase difference increases, similar to the way in which peak-current stress also increases with this parameter. The final result is independent of operating conditions and widely applicable

$$\kappa_{\mathrm{rms}} = \frac{I_{\mathrm{pri}\omega\_\mathrm{rms}}}{I_{\mathrm{pridc\_rms}}} \approx \sqrt{1+\delta\sqrt{2-2\cos\beta}-1} \tag{20}$$

Under different grid-phase β, the simulation waveforms of inductor current with $L_k = 50$-uH are shown in Fig. 11(a). As seen, the current profile pulsates with the second harmonic and gets lower with β increasing. Fig. 11(b) shows the inductor current under different L_k with $\beta = 0$. The ZVS is lost with $L_k = 35$-uH, and the lowest peak current stress is obtained

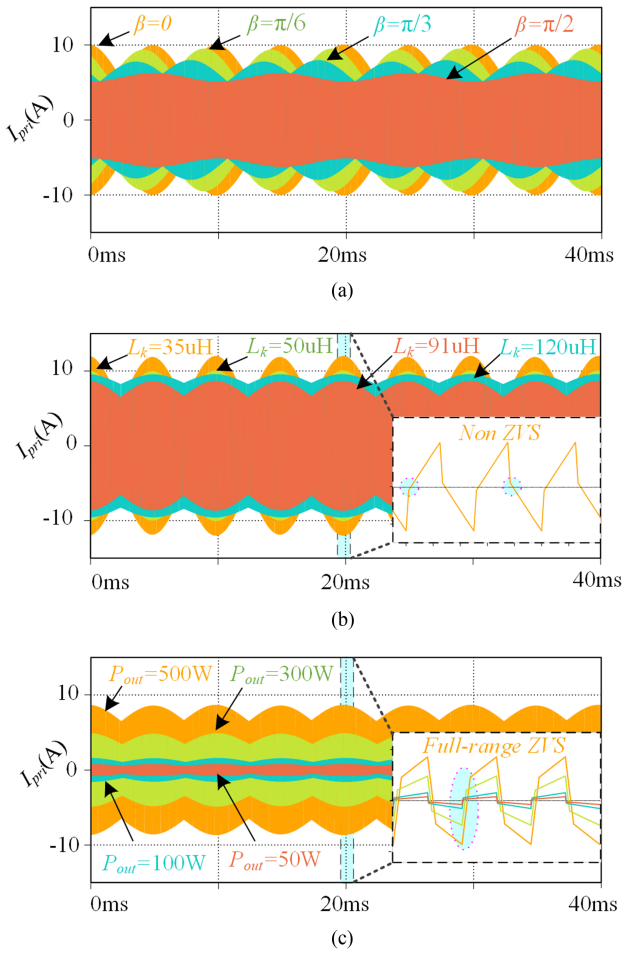


Fig. 11. Simulation waveforms of auxiliary inductor's current I_{pri} under different auxiliary inductor L_k, gird-phase β and output power P_{out}. (a) Under different β with $L_k = 50$ *uH* and rated P_{out}. (b) Under different L_k with $\beta = 0$ and rated P_{out}. (c) Under different P_{out} with $\beta = 0$ and optimal L_k.

with $L_k = 91$ uH, which coincides with the theoretical results. Under different output power, Fig. 11(c) shows the inductor current with $\beta = 0$ and optimal L_k, and the full-range ZVS is accomplished.

B. Inductor Current Caused by Phase-Shift Oscillation

Following the same analysis steps of exciting current, the dc-bias accumulation also occurs in auxiliary inductor's current under conventional updating strategy. Likewise, this dc-bias current is suppressed by parasitic resistor of main circuit. The unbalance from updating process and voltage drop finally reach equilibrium with a small dc-bias current. But the large dc-bias can be noticed during transient process shown in Fig. 9. Hence, this dc-bias is also necessary to be suppressed in practice.

V. Asynchronous Modulation Strategy and Second-Harmonic Correction to Transformer Design

From the above analysis, the phase-shift oscillation results in dc-bias issues, and the voltage imbalance brings current-stress rise, both of which influence the regular operation and design of DAB's high-frequency link. In this section, the asynchronous modulation strategy is proposed to eliminate the dc-bias, and the second-harmonic correction of the transformer is proposed to minimize the design margin and reduce material waste.

A. Asynchronous Modulation Strategy

To avoid the dc-bias caused by phase-shift oscillation, a novel phase-shift updating strategy completely based on modulation is proposed. The detailed working process of it is shown in Fig. 12. Compared with the traditional method in Fig. 9, two different sawtooth waves are applied to the secondary half-bridges respectively. The update points and operation for T_{ri2A} are the same as before: when T_{ri1} counts to φ or T_{ri2A} counts to 2π, the counter for T_{ri2A} is automatically cleared to zero. But T_{ri2B} is independent of T_{ri1} and only determined by T_{ri2A}: when T_{ri2A} counts to π or T_{ri2B} counts to 2π, the counter for T_{ri2B} is automatically cleared to zero. Through this process, the updating of S_6 and S_8 always lags behind S_5 and S_7 by half a switching cycle, so it is referred to as the asynchronous modulation strategy.

The generated zero voltage level in v_{CD} eliminates the dc-bias in the exciting and auxiliary inductor currents. This strategy retains the modulation-based advantage of conventional method while eliminating dc-bias in the whole high-frequency link. Taking the phase-shift decrease for instance, the demonstration for dc-bias elimination is shown as follows.

From Fig. 12(a), the zero-voltage interval between $[t_{k1}, t_{k2}]$ is

$$\Delta t_{\text{zero}} = \frac{\Delta\varphi}{2\pi} T_s. \tag{21}$$

Hence, the exciting current variation during $[t_{k-1,1}, t_{k1}]$ and $[t_{k2}, t_{k4}]$ can be calculated as

$$\Delta i_{m1} = \Delta i_{m2} = \frac{nV_2}{L_m}\left(\frac{T_s}{2} - \Delta t_{\text{zero}}\right). \tag{22}$$

After t_{k4}, the duty cycle of v_{CD} is fixed as 50%. Hence, no dc-bias in exciting current is generated during the transient process.

For auxiliary inductor current, the slope between $[t_k, t_{k1}]$, $[t_{k1}, t_{k2}]$ and $[t_{k2}, t_{k3}]$ can be respectively expressed as

$$\frac{di_{\text{pri}}(t)}{dt} = \begin{cases} \frac{V_1+nV_2}{L_k} & t \in [t_k, t_{k1}] \\ \frac{V_1}{L_k} & t \in [t_{k1}, t_{k2}] \\ \frac{V_1-nV_2}{L_k} & t \in [t_{k2}, t_{k3}] \end{cases}. \tag{23}$$

According to (17) and (23), i_{pri} in t_{k3} is calculated as

$$i_{\text{pri}}(t_{k3}) = i_{\text{pri2}}(\varphi_k). \tag{24}$$

Hence, after the transient process between $[t_{k1}, t_{k3}]$, the high-frequency link of DAB enters into a new steady state without dc-bias. The same conclusion can be obtained for the load-increase and power-reverse conditions similarly.

In the above analysis, the deadtime to prevent shoot-through of bridge-arm was not taken into account. Applying the analytical methodology proposed by Zhao et al. [22], [31], its impact on the proposed modulation can be inferred. Specifically, the elimination of the dc-bias is feasible during the phase-shift

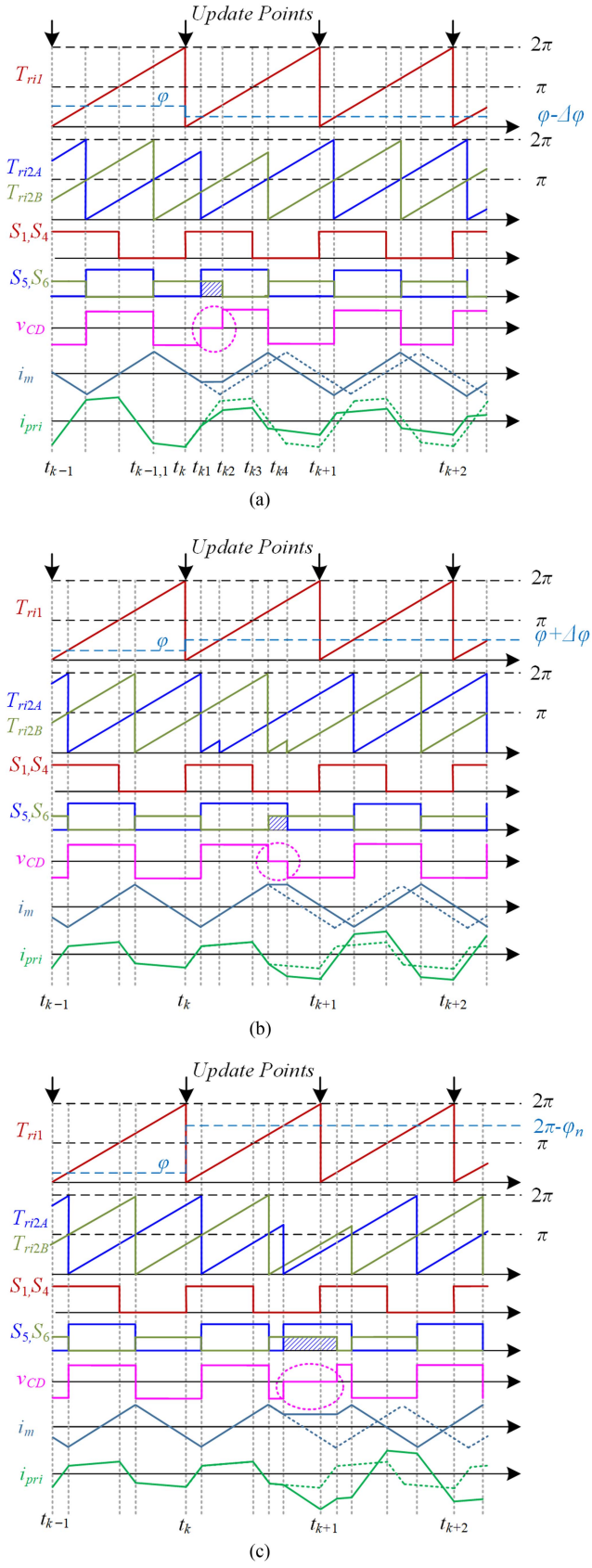


Fig. 12. Transient process of DAB's high frequency link under proposed asynchronous updating strategy. (a) Phase shift decreases from φ to $\varphi-\Delta\varphi$. (b) Phase shift increases from φ to $\varphi+\Delta\varphi$. (c) Phase shift inverts from φ to $-\varphi_n$.

TABLE II
SECOND-HARMONIC CORRECTION TO DAB'S TRANSFORMER DESIGN

Formula under DC	*Formula under SHV*
$N_2=\frac{V_2}{4f_sB_{sat}A_e},N_1=nN_2$	$N_2=\frac{V_2}{4f_sB_{sat}\frac{A_e}{1+\delta}},N_1=nN_2$
$k_wA_w=I_{Lrdc\_rms}\frac{N_1+nN_2}{j}$	$k_wA_w=\sqrt{1+2\delta}I_{Lrdc\_rms}\frac{N_1+nN_2}{j}$
$A_p=A_wA_e=I_{Lrdc\_rms}\frac{V_1+nV_2}{4k_wf_sB_{sat}}$	$A_p=A_wA_e=(1+\delta)\sqrt{1+2\delta}I_{Lrdc\_rms}\frac{V_1+nV_2}{4k_wf_sB_{sat}}$

increase, decrease, and positive-to-negative reversal. However, residual dc-bias is observed in $i_{\rm pri}$ during negative-to-positive reversal. To avoid this effect, the deadtime compensation can be adopted [22], but it is not necessary because this small residual dc-bias can be well suppressed by parasitic resistor of main circuit.

Compared with the method in [24] and [25], the zero-voltage level is similarly employed to eliminate the dc-bias with the equal settling time. However, with the proposed updating strategy, the elimination is automatically executed during the modulation process, without requiring any additional calculations. As a result, the off-load to the digital processor can be realized even under the varying phase-shift angle. Furthermore, the proposed strategy can be directly implemented by analog circuits to enhance the system's reliability.

B. Second-Harmonic Correction to Transformer Design

Under the proposed updating strategy, the dc-bias issue caused by phase-shift oscillation is well solved. But the current-stress increase caused by voltage imbalance challenges the traditional design methods. From Fig. 10, the peak current under $\beta=0$ increases to approximately 1.3 times the dc operation, so it is imperative to take into account the second-harmonic effect when selecting the power semiconductor. As for the high-frequency transformer, special consideration is also necessary, but more complex, as both the exciting current and inductor current need to be considered.

To reduce the material's waste caused by arbitrary design margin, a second-harmonic correction to transformer design is shown in Table II. $B_{\rm sat}$ is the saturation flux density in the range of 1.0-T $\sim$ 1.1-T for the nanocrystalline core; j is the current density; k_w is the filling coefficient of the magnetic core. Two factors contribute to the increase in size of the magnetic core: First, the ripple of the exciting current results in a higher flux density, leading to a larger cross-sectional area of the magnetic core. This is quantitatively assessed by (14). Second, the increase of RMS current necessitates a bigger window area for the primary and secondary windings, which is quantitatively evaluated by (20). The overall result is the larger requirement for the AP value of magnetic core as shown in the last row of Table II. As seen, only a correction coefficient about SHV ratio $(1+\delta)\sqrt{1+2\delta}$

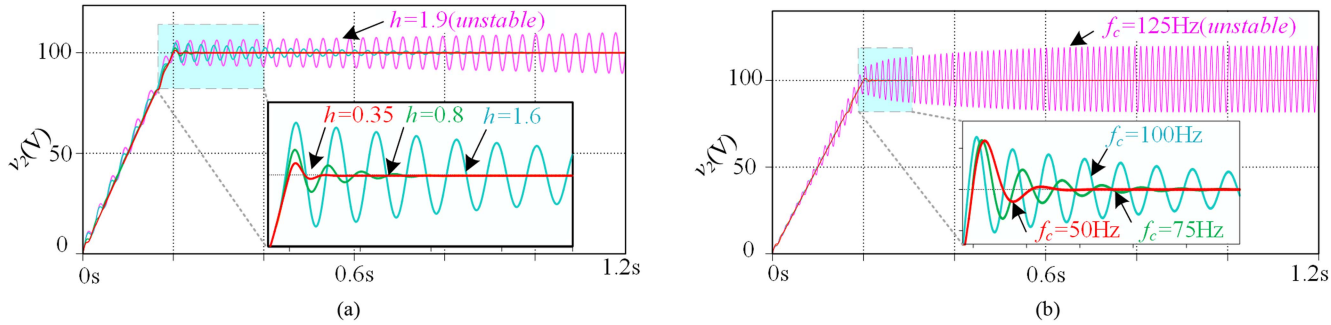


Fig. 13. Simulation waveforms of start-up process. (a) Under different notch filter parameters h with $f_c = 50$ Hz. (b) Under different cutoff frequency f_c with $h = 0.35$.

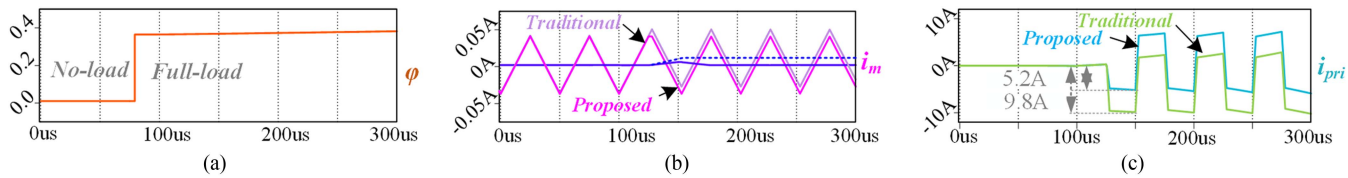


Fig. 14. Simulation waveforms of 0% $\sim$ +100% load-transient process under traditional and proposed updating strategy. (a) Phase-shift angle φ. (b) Exciting current i_m. (c) Auxiliary inductor current i_{pri}.

is added to the traditional formula, and the results are easy to implement.

Under conventional design, the practical flux density is usually set as half of the saturated flux density for enough design margin. From the above analysis, the actual required second-harmonic design margin is

$$\frac{1}{(1+\delta)\sqrt{1+2\delta}} = 0.806. \tag{25}$$

Hence, about 30% of magnetic flux swing is wasted in conventional design theory. And this waste is more serious with smaller dc-link SHV ratio. Undoubtedly, some other issues need to be concerned in the selection of practical flux density, such as overload ratio and heat dissipation. However, it is essential to perform these calculations using the corrected formula, rather than relying on the dc formula. By adopting this correction, the traditional design of DAB's transformer can be made less arbitrary under second harmonic conditions.

VI. Numerical Verification

To verify the effectiveness of proposed optimization methods, numerical simulations are carried out by the PLECS software with system parameters given in Table I. The verification about the L_k optimal selection has been provided in Fig. 11. Hence, the dc-bias issue concerning control and updating strategy is demonstrated here.

As analyzed in Section II, the control bandwidth is limited after second-harmonic notch filter is added to the voltage feedback path. To illustrate the impact to dynamic response, the simulation of two mutual-driving DABs is tested here. Fig. 13(a) shows the start-up waveforms of output voltage v_2 under different notch filter parameters h. As seen, with the increase of h, the overshoot and setting time become larger. The system becomes unstable after h changes from 1.6 to 1.9, which coincides with the theoretical critical value 1.86 in Fig. 6. Fig. 13(b) shows the start-up waveforms under different cutoff frequencies f_c. Similarly, the system's cutoff frequency must be reduced to keep enough stability margin under the notch filter. Therefore, it can be concluded that great second-harmonic filtering sacrifices dynamic response performance.

The transient process of DAB under traditional and proposed updating strategy is shown in Fig. 14 with $\varphi = 0$ to 0.35. The blue lines represent the dc-bias of the exciting current. During this transient, the dc-bias occurs both in the exciting current and the inductor's current under the traditional updating strategy. The current sharp in i_{pri} is almost 90% higher than the proposed method, which increases the risk of semiconductor failure. This issue can be avoided under proposed method due to the automatic generation of the zero-voltage period in the midpoint voltage. The same problem can be found in the load-decrease process, but the current sharp would not occur. For the power-reverse condition, the proposed method still works. The transient waveforms from $\varphi = 0.35$ to -0.35 and -0.35 to 0.35 are shown in Figs. 15 and 16. As seen, the proposed updating method decreases the current sharp by 30% and 60% separately with no dc-bias.

To verify the validity under second-harmonic conditions, the back-to-back system in Fig. 2 is tested with $f_c = 50$ Hz, $h = 0.35$. Fig. 17 shows the waveforms of P, v_1, v_2, φ, i_m, i_{pri}, v_{CD} under traditional and proposed updating strategy with parasitic resistor $R_p = 0.02\ \Omega$. There is ramp change of output power from 500 to -500 W in 0.4 s. These waveforms confirm stable operation even in transient process. The phase shift in Fig. 17(c) oscillates as predicted in Section II. Due to the ignorance of spectral leakage and v_1's SHV during analysis, the ripple content (5.6%) is

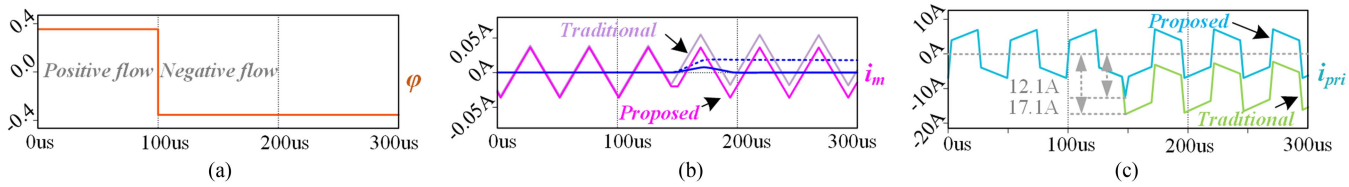


Fig. 15. Simulation waveforms of $+100\% \sim -100\%$ load-process under traditional and proposed updating strategy. (a) Phase-shift angle φ. (b) Exciting current i_m. (c) Auxiliary inductor's current i_{pri}.

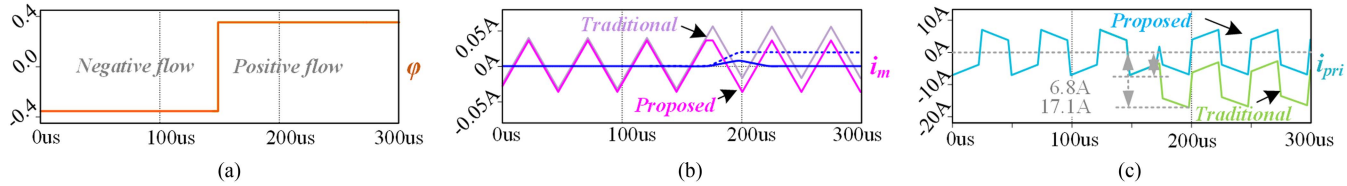


Fig. 16. Simulation waveforms of $-100\% \sim +100\%$ load-process under traditional and proposed updating strategy. (a) Phase-shift angle φ. (b) Exciting current i_m. (c) Auxiliary inductor's current i_{pri}.

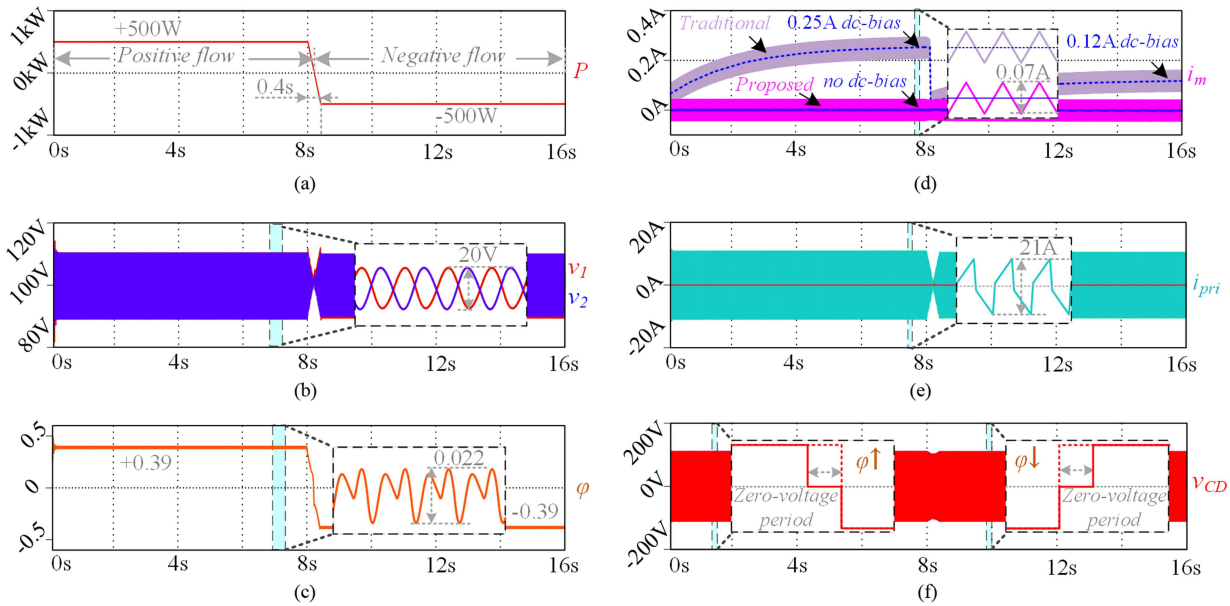
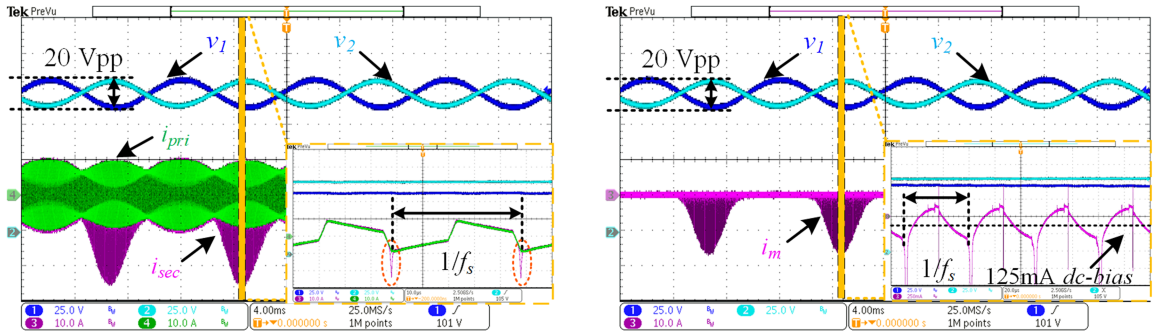


Fig. 17. Simulation waveforms of power-reverse process under traditional and proposed updating strategy. (a) Average power P. (b) DC-link voltage v_1, v_2. (c) Phase-shift angle φ. (d) Exciting current i_m. (e) Auxiliary inductor current i_{pri}. (f) Secondary-side midpoint voltage v_{CD}.

more serious than theoretical result (2.8%). Fig. 17(d) shows the exciting current under different power-flow directions. The dc-bias under traditional updating strategy accumulates after start-up and reaches the equilibrium state at 0.25 A, which increases the magnetic flux saturation risk in practice. If the direction of power flow is negative, the final value of dc bias is 0.12 A. In contrast, thanks to the transient zero-voltage levels shown in Fig. 17(f), the dc-bias under proposed updating strategy stays at zero regardless of power-flow direction. Hence, the peak exciting current is only 0.04 A, and requirement for magnetic core can be reduced a lot. The current of auxiliary inductor is shown in Fig. 17(e). Due to the damping effect of parasitic resistor, dc-bias in i_{pri} is hard to notice. But for the application where a sinusoidal phase-shift is required [10], [11], [12], [13], [14], the influence of updating process would be enlarged, causing larger dc-bias in i_{pri} under the traditional updating strategy.

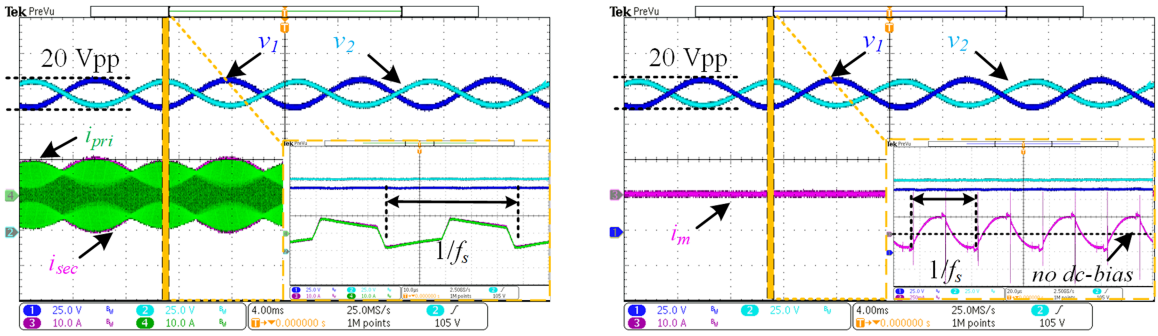
VII. Experimental Results

Experiments with parameters provided in Table I. are performed in the laboratory to further validate the effectiveness of the proposed dc-bias eliminating strategy and high-frequency link optimization theory. The DAB circuit used eight power MOSFETs (IPP076N15N5AKSA1) as the switching devices with drain-source on-state resistance $R_{\mathrm{DS(on)}} = 5.9\ \mathrm{m}\Omega$. To show the dc-bias effect caused by the conventional updating strategy, a magnetic core (KMN644020) with a larger AP value than the result in Table II is selected. Even so, the flux



(a) (b)

Fig. 18. Experiment steady-state waveforms under traditional updating strategy with $\beta = 0°$. (a) Primary-side and secondary-side DC-link voltage v_1 and v_2, primary-side and secondary-side current $i_{\rm pri}$ and $i_{\rm sec}$. (b) Primary-side and secondary-side DC-link voltage v_1 and v_2, exciting current i_m.



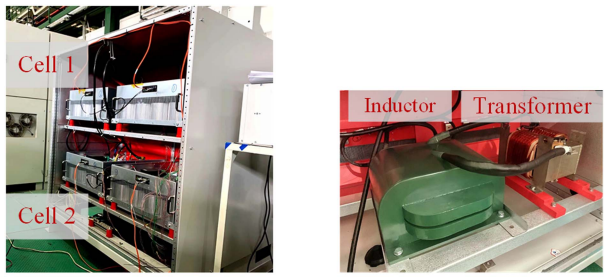
(a) (b)

Fig. 19. Experiment steady-state waveforms under proposed updating strategy with $\beta = 0°$. (a) Primary-side and secondary-side DC-link voltage v_1 and v_2, primary-side and secondary-side current $i_{\rm pri}$ and $i_{\rm sec}$. (b) Primary-side and secondary-side DC-link voltage v_1 and v_2, exciting current i_m.

saturation still occurs under the conventional updating strategy. The transformer magnetizing current is obtained by measuring the current difference between the primary 23-turn winding and the secondary 23-turn winding using a current probe.

A. *Steady-State Under Second-Harmonic Operation*

Figs. 18 and 19 show the steady-state waveforms with $\beta = 0°$ under the traditional and proposed updating strategy. From Fig. 18(b), a dc-bias about 125 mA occurs in the exciting current causing magnetic flux saturation. The exciting current surge is completely provided by the secondary-side current because the exciting inductor is clamped by the secondary-side voltage v_{CD}. Hence, the remarkable current peak is observed in the secondary-side current shown in Fig. 18(a), which sharply increases the risk of device damage. From the time scale of the second harmonic, this saturation only occurs in the positive half cycle of SHV on the secondary side. The reason is that the exciting current fluctuation is smaller in negative half cycle, and the peak exciting current is lower under same steady-state dc-bias. Hence, the saturation is not as severe as in the positive half cycle. From the time scale of switching period, this saturation only occurs around the action moment of v_{CD} from negative to positive. This is because the exciting current reaches its negative peak after half-switching-period negative clamping plus the original negative dc-bias. As in the simulation results, the dc-bias in the



(a) (b)

Fig. 20. Experiment setup of practical 185-kW back-to-back system with two mutual-driving cells. (a) Experiment platform. (b) Auxiliary inductor and high-frequency transformer in DAB.

auxiliary inductor is not apparent due to the significant damping effect of parasitic resistor. Fig. 19 is obtained using the proposed updating strategy based on the implementation in Fig. 12. Due to the modulation-based character, no additional calculation is added to the traditional control loop when applying the proposed method. No dc bias occurs in exciting current, and flux saturation is also avoided.

Furthermore, the steady-state experiment is also tested in a practical 185-kW back-to-back system with two mutual-driving cells shown in Fig. 20. As the results in the scale-down experiment, the magnetic saturation also occurs under the traditional

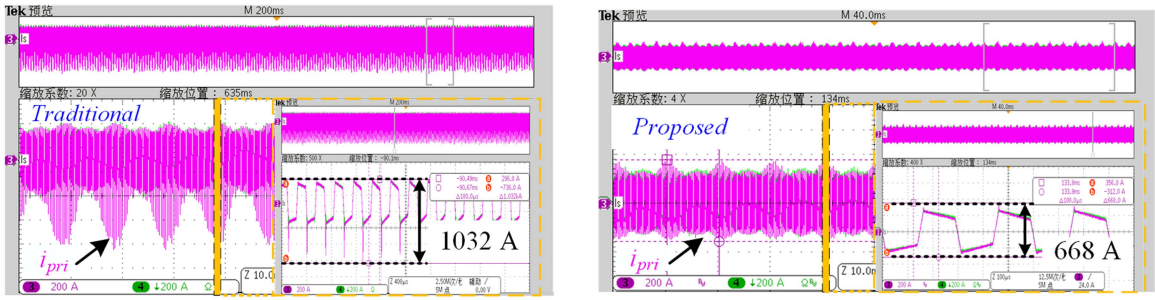


Fig. 21. Experiment steady-state waveforms in practical 185-kW back-to-back system with $\beta = 0°$. (a) Exciting current i_m under traditional updating strategy. (b) Exciting current i_m under proposed updating strategy.

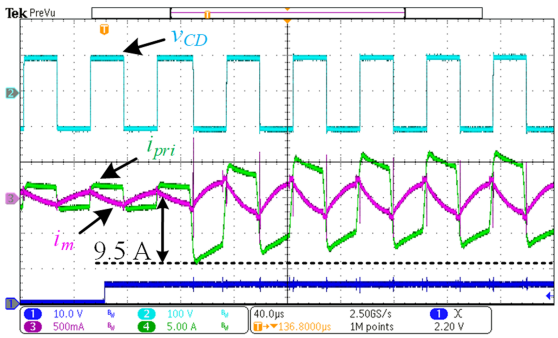


Fig. 22. Experiment transient response to a step change in phase-shift angle reference under traditional updating strategy. Secondary-side midpoint voltage v_{CD}, primary-side current i_{pri}, and exciting current i_m.

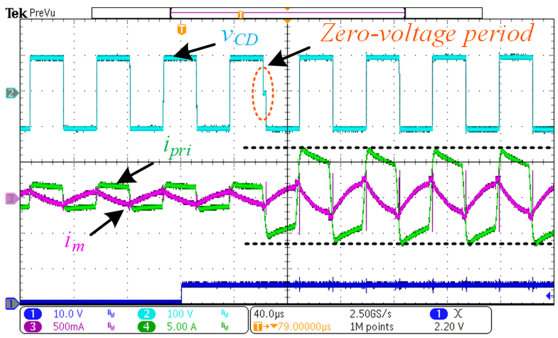


Fig. 23. Experiment transient response to a step change in phase-shift angle reference under proposed updating strategy. Secondary-side midpoint voltage v_{CD}, primary-side current i_{pri}, and exciting current i_m.

updating strategy. The secondary-side peak current reaches 1.032 kA, shown in Fig. 21. Under the proposed method, the current stress reduces to 668 A with no dc-bias. Hence, the comparison of the results has proved the validity of dc-bias accumulation under second harmonic and the effectiveness of proposed updating strategy.

B. Transient Response to a Step Change in Phase Shift

Figs. 22 and 23 show the transient waveforms when the transferred power increases from 200 to 500 W by a step change in phase-shift reference under traditional and proposed updating strategy. Two dc-power sources are connected in parallel with the primary and secondary dc-link and regulate dc-link voltage at 100-V independent of the change in phase-shift angle. A sharp increase in the primary side current can be observed in Fig. 22, which is about 1.39 times of the steady-state value. Due to parasitic resistor, this dc-bias current reduces to zero after five switching periods. Under the proposed modulation-based updating strategy, a small zero-voltage period is generated during the modulation process and inserted into the midpoint voltage v_{CD} changing the slope of i_{pri}. As a result, no sharp increase or dc-bias occurs in the inductor current. The phase-shift increase and reverse conditions also match the process in Fig. 12 and are not shown here for the sake of brevity. Hence, the proposed updating strategy is still valid to deal with the dc-bias in transient process with no additional calculation.

C. Current Stress Under Second-Harmonic Operation

In back-to-back applications, the SHV's phase difference between primary and secondary dc-link is determined by grid phase β. Consequently, as shown in Fig. 10, the peak current under bilateral second harmonic is related to β. Fig. 24 shows the steady-state waveforms under the proposed modulation strategy with different β and $L_k = 50$ uH. The peak current increases with β decreasing, and reaches its maximum under $\beta = 0°$, which coincides with the theoretical analysis. Hence, the parameters optimization should also be carried out under $\beta = 0°$ to reduce the peak current value. Fig. 25 shows the steady-state waveforms under different L_k. As seen, the peak current gets its minimum under $L_k = 91$ uH and is consistent with the theoretical prediction shown in Fig. 10.

VIII. Discussion

The high-frequency link optimization of DAB is provided in this article to minimize the effect of second-harmonic power, including the peak-current stress, high-frequency transformer design and dc-bias elimination. Except for the dc-link capacitor buffering, there exist some other second-harmonic power-decoupling methods, such as fluctuating power control [10], [11], [12], [13], [14] and auxiliary circuit [32], [33], [34], [35]. A comprehensive comparison is meaningful to the practical application of SST. It is qualitatively conducted in Fig. 26.

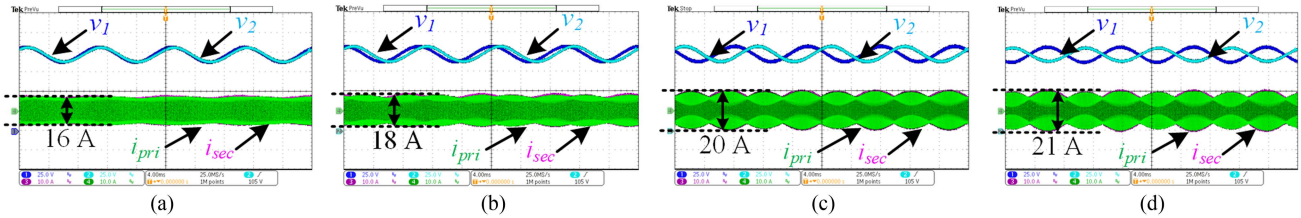


Fig. 24. Experiment steady-state waveforms under proposed updating strategy with different β and $L_k = 50$ uH. primary-side and secondary-side DC-link voltage v_1 and v_2, primary-side and secondary-side current $i_{\rm pri}$ and $i_{\rm sec}$. (a) $\beta = 90°$. (b) $\beta = 60°$. (c) $\beta = 30°$. (d) $\beta = 0°$.

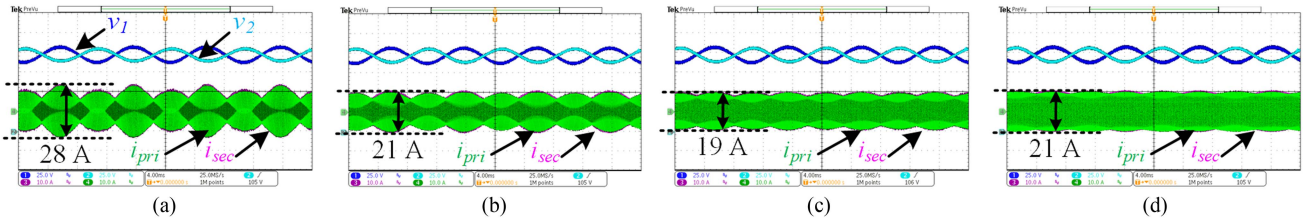


Fig. 25. Experiment steady-state waveforms under proposed updating strategy with different L_k and $\beta = 0°$. Primary-side and secondary-side DC-link voltage v_1 and v_2, primary-side and secondary-side current $i_{\rm pri}$ and $i_{\rm sec}$. (a) $L_k = 35$ uH. (b) $L_k = 50$ uH. (c) $L_k = 91$ uH. (d) $L_k = 108$ uH.

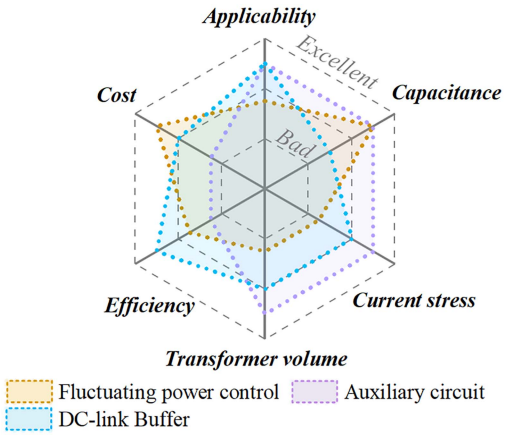


Fig. 26. Performance comparison among common power decoupling methods.

The fluctuating power control can eliminate dc-link SHV through the ripple power transmission, but burdens the power loss, current stress and transformer's capacity. In contrast, the dc-link buffer method compensates the ripple power by dc-link capacitors and only the dc power is transferred by DAB. But as shown in Fig. 10, the peak current is still 1.3 times larger than pure dc operation even with the proposed optimal inductance. As for the auxiliary circuit, this pure dc operation can be achieved with two power decoupling circuits at the rated power level, which increases the cost, power loss and volume of the high-power system.

IX. Conclusion

In this article, the behavior of DAB's high-frequency link under bilateral second harmonics is theoretically analyzed. Firstly, the compromise between the performance of 2ω notch filter and stability of control system is revealed, indicating the non-negligible phase-shift oscillation in steady state. Consequently, the updating transient exists during the whole operation. Based on that, the accumulating dc-bias issue is first demonstrated and quantitatively modeled. The dc-bias eliminating method must be executed at each switching cycle in back-to-back system. An asynchronous updating strategy based on modulation process is proposed to achieve this. Compared with other dc-bias eliminating methods, the transitional zero-level period is automatically generated and inserted without any calculation, which is more suitable to be continuously executed in second-harmonic applications.

Furthermore, based on the peak current modeling of the auxiliary inductor, the optimal selection of inductance with minimal current stress and full-range ZVS is obtained under SPS. For the high-frequency transformer, a second-harmonic correction is proposed to achieve high flux density with the ungapped nanocrystalline core.

Simulation and experimental results are provided on a scale-down 500-W prototype and a practical 185-kW prototype. The experimental results show that the proposed updating strategy can eliminate the flux saturation caused by the dc-bias current and keeps excellent dynamic response.

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