

Fast-Response Variable Frequency DC–DC Converters Using Switching Cycle Event-Driven Digital Control

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Abstract—This article investigates a new method to model and control variable-frequency power converters in a switching-synchronized sampled-state space for cycle-by-cycle digital control. There are a number of significant benefits in comparison to other methods, including fast dynamic performance together with ease of design and implementation. Theoretical results are presented and verified through hardware and simulations of a current-mode buck converter with constant ON-time and a current-mode boost converter with constant OFF-time. Dynamic voltage scaling for microprocessors and LiDAR are among the applications that can benefit.

Index Terms—Constant-on-time, current-mode, cycle-by-cycle digital control, dynamic voltage scaling (DVS), event-driven control, light detection and ranging (LiDAR), nonuniform sampling, sampled-data model, switching-synchronized, switching-synchronized sampled-state space (5s), variable frequency dc–dc converters.

I. INTRODUCTION

EFFICIENCY is achieved by power converters that provide the exact energy at the exact time. For example, in an electronic system whose power demand fluctuates rapidly, dynamic voltage scaling (DVS) is a crucial and widely used technique to optimize energy efficiency. However, traditional controllers are generally not able to provide both high-speed dynamic response and programmable flexibility at the same time, for example, analog controllers lack the flexibility in speedily tuning controller parameters for varying output voltage levels. Among these, constant-frequency dc–dc converters cannot be controlled cycle-by-cycle in a simple way over a wide voltage conversion

ratio. Even existing variable frequency power converters with digital controllers have extraordinary complexities in architecture, hardware, algorithms, or sensitivities to parameter variations. A new digital control framework is needed to overcome these pervasive limitations.

There are a number of loads that are dynamically demanding. Processors require higher voltages during intensive tasks [1]. Memories are able to work at a lower voltage supply when read/write bandwidth is less [2]. Wireless network modules choose working voltages based on communication channel conditions and packet throughput [3]. Light detection and ranging (LiDAR) can dynamically adjust the transmitter power to support efficient operation [4]. DVS for these kinds of electronic loads can tremendously reduce the world’s annual electrical power consumption [2], [5] and significantly extend the battery life of portable devices [6].

Recent literature suggests that to optimize a system’s energy efficiency, DVS voltage regulators should switch among a large number of voltage levels and within a sizable voltage range [1], [7]. A settling time of the order of 10 μ s or shorter is the goal for DVS for processor voltage regulator modules [8]. For example, a 10 μ s response for DVS reduces the power consumption of an embedded processor by 46.3% [8], [9], [10] compared to not using DVS.

Automatic power control of LiDAR is a technology where the power consumption of laser transmitters is dynamically adjusted to improve the LiDAR sensors’ detection accuracy and thermal management [4], [11], [12]. A boost converter is a good candidate for supplying the needed high voltage to LiDAR transmitters, as illustrated in Fig. 1. A high-performance boost LiDAR power supply needs a large control bandwidth to adjust the voltage level within 10 μ s [12] over a wide output voltage range and good load disturbance rejection to handle the instantaneous power consumption. The dynamics of power converters vary with operating point [13]. Real-time tuning including scheduled gain approaches [4] can easily be realized on a digital controller to ensure consistently good dynamic performance, in contrast to a single analog compensation network.

Digital control allows programmable flexibility for changes in electrical dynamics with different operating points from adaptive voltage step tracking. In comparison, a dc–dc converter with an analog controller is typically built with fixed compensation; therefore, good performance cannot be always reached over a wide range of voltage and load [14]. Among controller designs,

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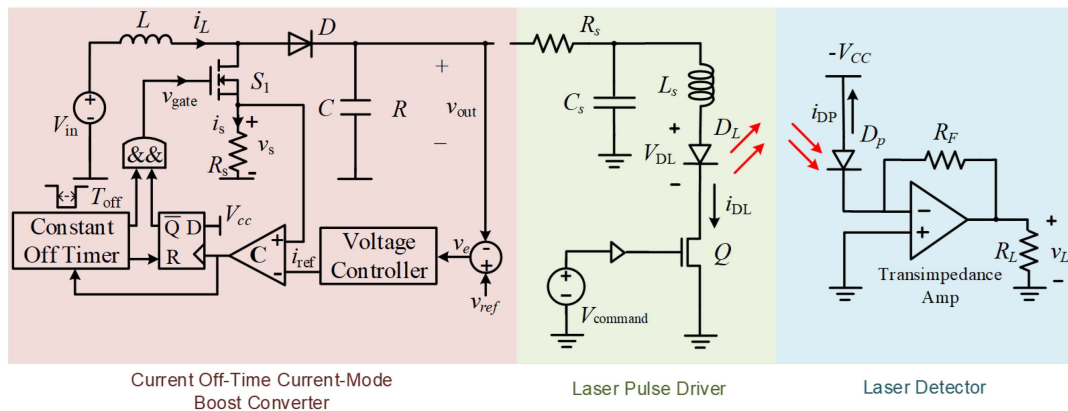


Fig. 1. Schematics of the constant OFF-time current-mode boost power supply and LiDAR transceiver system.

current-mode dc-dc converters are faster and more easily compensated than voltage-mode because current-mode converters are first-order systems [13]. In particular, variable frequency constant ON(OFF)-time operation of dc-dc converters does not need the additional complication of slope compensation [15] while ensuring *settling* to the inductor current setpoint for all operating points [16], [17]. Dc-dc converters for DVS should be digitally controlled, current-mode, and variable frequency constant ON (OFF)-time.

A typical approach to high-speed digital control is to oversample the output voltage so that the switching ripple is not aliased by the analog-to-digital converter (ADC). In variable frequency converters, higher cost and power consumption is incurred because of oversampling the highest possible switching frequency [18]. Not only does this impact the ADC, but also any subsequent digital signal processing.

The main contribution of this article is to provide a modeling and control framework for a cycle-by-cycle, event-driven controller where the output voltage sampling is synchronized to the variable switching cycle; it is worth noting that this minimizes the sampling rate. We will show that previous models including averaging and describing functions are not adequate for controller design and determining stability margin.

This article verifies the theoretical results through hardware with a current-mode buck converter with a constant ON-time and a current-mode boost voltage converter with a constant OFF-time (COT-CM) with a peak switching frequency of 3 MHz.

This rest of this article is organized as follows.

- 1) Section I introduces this article.
- 2) Section II discusses the modeling in a switching-synchronized sampled-state space.
- 3) Section III explains the switching-synchronized sampled-state space control concepts for dc-dc converters.
- 4) Section IV compares the modeling accuracy of 5S to previously known modeling methods.
- 5) Section V investigates the digital controller design in 5S.
- 6) Section VI exhibits the hardware implementations and experimental results.
- 7) Section VII concludes this article.

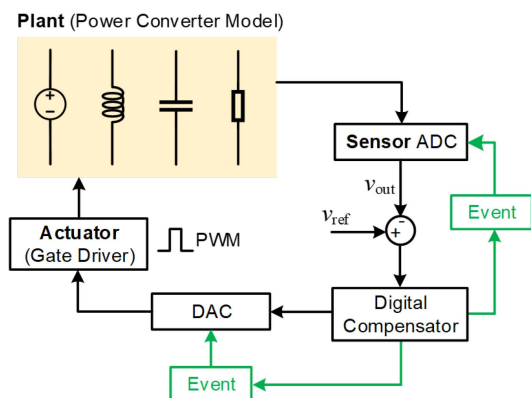


Fig. 2. Switching-synchronized control framework for power converters.

II. MODELING IN A SWITCHING-SYNCHRONIZED SAMPLED-STATE SPACE

A common approach to the design of digital controllers for power converters is based on the framework of physical time. The switched-system is converted to a time-invariant system through averaging, which is then transformed to the s -domain to design a controller. Bilinear transforms are used to convert this controller to the z -domain [18], [19]. Averaging strategies are more complicated for variable switching-frequency converters because intervals for cycle-averages are nonuniform and other methods are often used [20]; the dynamic response of these converters is ultimately limited by the longest switching period, which can happen during a transient.

This work provides a new framework to perform digital control on variable frequency power converters with faster dynamics without the computation, algorithmic, and hardware complexity in prevailing approaches. In comparison to the traditional periodic sampling and control framework, our new digital control framework shown in Fig. 2 includes a series of nonperiodic sampling and control actions that are triggered by events instead of clocks.

Unlike the traditional discrete-time state space, which uses periodic sampling or interpolation to obtain a uniform correspondence to a continuous-time (CT) state space, our control framework relies on a new state space called *switching-synchronized sampled-state space* (5S) [21], [22]. In [21] and [22], the derivations use an invariant inductor-current ramp, which is valid for small output voltage steps. This article advances the theory for large output voltage steps, which is a significant update. This section mathematically proves that the dynamics in 5S can fully reconstruct the physical circuit dynamics in the time domain, specifically no information is lost and there is a bijective mapping between 5S and CT state space. This work also mathematically proves that a controller designed in the time domain is equivalent to a controller designed in 5S, under settling time and overshoot constraints, design optimization in 5S is equivalent to optimization in the time domain.

Both direct digital design and controller implementation can be performed in 5S. Because no approximate state-space transformation is needed, unlike other methods, cycle-by-cycle digital control is precise. Also, because the z -transform can still be employed, power-converter models can be derived as simple linear, low-order systems, in contrast to more complicated plant models from the CT-derived s -domain. Familiar classical control methods for direct-digital design of controllers can be used. Because sampling is only as fast as the *local* switching frequency, both the burden on the ADC and the digital hardware for computation is alleviated. The naturally synchronized switch also allows sampling to be chosen to avoid switching transients.

In general, the switching-synchronized sampled-state space is a type of Poincare map [23]; similar strategies have been adopted in other areas of control theory [24], [25], [26], [27], [28]. In 5S, the capacitor voltage and inductor current trajectories are mapped from continuous physical time to sampled state space trajectories using a nonuniform, event-driven sampling function $S(t)$

$$S(t) : \{v(t), i(t)\} \mapsto \{v[n], i[n]\}. \quad (1)$$

The 5S state-space equations are not derived directly from the discretization of CT state-space equations of a power converter as is typically performed, e.g., [13], but rather as difference equations directly from the state trajectories at every switching interval; for example, for the familiar hard-switched converters, the inductor currents are ramps [21]. These difference equations are, in general, nonlinear. This method of derivation ensures that the relationship between capacitor charge and inductor volt-seconds is preserved, even in the sampled state space. No type of averaging is employed. This section shows rigorous mathematical proof that Lyapunov stability in the 5S sampled-data domain necessarily means stability in the continuous physical time domain.

Linearization is performed as the last step directly in the 5S sampled-state space. The linearized difference equations in the 5S sampled state space can be transformed to the z -domain to obtain transfer functions. Because $S(t)$ is nonuniform (i.e., in general, the sequence of sampling times $\{t[n], t[n+1], \dots\}$ are such that $t[n+1] - t[n] \neq T_s$ for any n), conclusions from the

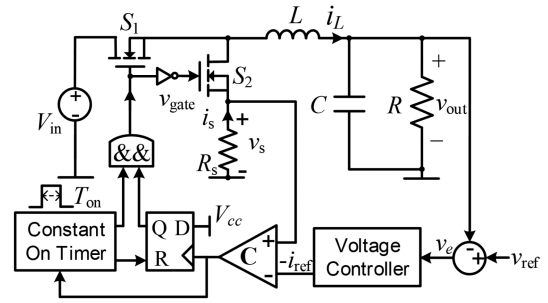


Fig. 3. Circuit diagram of a digitally controlled constant ON-time current-mode buck converter.

more familiar Nyquist sampling are not valid; therefore

$$z \neq e^{sT_s} \quad (2)$$

where T_s is required to be a constant sampling period, which means that there is no valid s -domain equivalent or transformation. Section IV demonstrates that the switching period and hence sampling period varies significantly even during small-signal voltage step responses, which furthers the assertion of (2).

This article shows in Sections II and V that 5S z -domain transfer functions are low order and straightforward to use in controller design. A number of classical tools can be used to ensure small-signal stability, stability margins, and transient performance, including root locus and Nyquist plots.

This work shows through rigorous mathematical proof that the worst-case overshoot in the continuous physical domain can be calculated as a linear proportion of the overshoot in the 5S sampled domain. This article also shows that the worst-case settling time in the continuous physical domain can be calculated from the number of cycles for settling and overshoot in the 5S sampled domain. This means that two of the most important transient performance metrics for the control of power converters can be optimized and traded off purely in the 5S sampled domain.

A. Operation of the COT-CM Buck Converter

A COT-CM buck converter is illustrated in Fig. 3. The annotated waveforms for inductor current and capacitor voltage are shown in Fig. 4. The valley current, enforced by a controller at the instance $t_v[n]$, is denoted at the n th switching cycle as $i_v[n]$ with the peak occurring at $t_p[n]$. The valley-current controller can be realized by a comparator and a digital-to-analog converter (DAC). The inductor current through S_2 , converted to a voltage with a current-sense resistor, is compared to the reference value from the DAC, which is updated every cycle. If the valley current falls below the command, S_2 turns OFF and S_1 turns ON. Because the valley-current settles in one cycle for a constant ON-time controller, i.e., deadbeat, the command, and actuation of current can be considered simultaneous.¹ The output voltage

¹a) *Deadbeat* refers to single-cycle settling for the current-control loop. b) *Command* is analogous terminology to *setpoint* and *reference*. c) *Actuation* in this case refers to actively turning the power switch on when the inductor current falls below the comparator threshold.

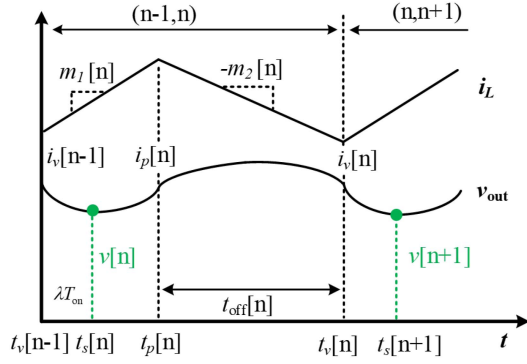


Fig. 4. Inductor current and capacitor voltage waveforms of a constant ON-time current-mode buck converter.

is sampled at every time instant $t_s[n]$ and is denoted for the n th cycle as $v[n]$. The ADC acquires and converts the output voltage during the ON-time of S_1 . The sampling time instant of the ADC is parameterized by λ , specifically $t_s[n] = t_v[n-1] + \lambda T_{\text{on}}$, $\lambda \in (0, 1)$.

The ordering of the indices for the sequences $\{i_v[n]\}$ and $\{v[n]\}$ in Fig. 4 is determined by circuit topology and causality. The reasoning is as follows. The output voltage that is sampled in the time domain immediately after $i_v[n-1]$ cannot be indexed as $v[n-1]$ because of the implication of a nonexistent direct feed-forward path from current to voltage in the circuit. This same output voltage also cannot be indexed as $v[n+1]$ because causality dictates that $v[n+1]$ cannot be updated ahead of $i_v[n]$. Only the unique ordering for the indices in Fig. 4 remains. In other words, in this particular example, because the inductor current feeds the charge on the output capacitor, in the sampled data space, an update to the output capacitor voltage must occur after the inductor current from the prior interval is known.

A stabilizing voltage controller [29] uses the error between the output voltage sample and reference to adjust the command for the valley-current. The voltage controller can be realized digitally with a field-programmable gate array (FPGA). In this 5S framework, all sampling and control actions are driven by events rather than time. The turn-ON event for S_1 is determined by the valley-current detection event and the turn-OFF event by the timeout event for the ON-time timer. Because of this, the events are not in general periodically nor uniformly distributed in the physical time domain.

B. Usual Power Electronics Assertions for COT-CM Buck Converters

The COT-CM buck converters satisfy the following properties:

- 1) the ON-time T_{on} of S_1 is constant;
- 2) OFF-time $t_{\text{off}}[n]$ of S_1 is determined by valley-current (the minimum inductor current every switching cycle), $0 < t_{\text{off}}[n] < +\infty$;
- 3) output voltage v_{out} has small ripple so the inductor waveform can be well-approximated as a linear ramp;

- 4) the inductor current is piecewise linear with the slopes of the rising and falling current ramps denoted as m_1 and $-m_2$, respectively;
- 5) input voltage $V_{\text{in}} > 0$ is constant;
- 6) output capacitor voltage denoted by $v(t) > 0$.

C. Modeling of the Buck Converters in 5S

This section begins by analyzing the more general problem of a linear-ramp current source with intercept i_0 and slope m charging a parallel resistor R and capacitor C whose initial voltage is v_0 . The solution of capacitor voltage $v(t)$ is

$$v(t) = \frac{1}{C} \int_0^t (i_0 + m\tau) e^{-\frac{t-\tau}{RC}} d\tau + v_0 e^{-\frac{t}{RC}}. \quad (3)$$

One can approximate this voltage, which can be representative of the output of a power converter, by a quadratic using a Taylor series approximation with an error that is small for $T_{\text{on}} \ll RC$

$$v(t) = v_0 + t \left(\frac{i_0}{C} - \frac{v_0}{RC} \right) + t^2 \frac{m}{2C}. \quad (4)$$

From this perspective, a practical current-mode buck converter with constant on-time can be represented as a time-piecewise-linear current source charging the output of an RC filter, with the rising slope m_1 and falling slope m_2 can be expressed as

$$m_1 = \frac{V_{\text{in}} - v_{\text{out}}[n]}{L}; m_2 = \frac{v_{\text{out}}[n]}{L}. \quad (5)$$

The inductor current ramp can then be written as

$$i_p[n] = i_v[n-1] + m_1 T_{\text{on}} \quad (6)$$

$$i_v[n] = i_p[n] - m_2 t_{\text{off}}[n] \quad (7)$$

where $t_{\text{off}}[n]$ is implicitly controlled by the valley-current command.

In the time interval $(t_s[n], t_p[n])$, one can treat the inductor current $i_v[n-1] + m_1 t$ as a ramp that charges the output RC filter. Given capacitor voltage $v[n]$ at time instance $t_s[n]$, the capacitor voltage $v(t_p[n])$ at time instance $t_p[n]$ can be obtained by substituting $v(t)$ and v_0 in (4) by $v(t_p[n])$ and $v[n]$, respectively

$$v(t_p[n]) = v[n] + (1 - \lambda) T_{\text{on}} \left(\frac{i_v[n-1]}{C} - \frac{v[n]}{RC} \right) + (1 - \lambda)^2 T_{\text{on}}^2 \frac{m_1}{2C}. \quad (8)$$

Equation (8) yields

$$v(t_p[n]) = \left(1 - \frac{(1 - \lambda) T_{\text{on}}}{RC} \right) v[n] + \frac{(1 - \lambda)^2 m_1 T_{\text{on}}^2}{2C} + \frac{(1 - \lambda) T_{\text{on}} i_v[n-1]}{C}. \quad (9)$$

In the time interval $(t_p[n], t_v[n])$, given capacitor voltage $v(t_p[n])$, one can express the capacitor voltage $v(t_v[n])$ by

$$v(t_v[n]) = \left(1 - \frac{t_{\text{off}}[n]}{RC} \right) v(t_p[n]) - \frac{m_2 t_{\text{off}}^2[n]}{2C} + \frac{t_{\text{off}}[n] i_p[n]}{C}. \quad (10)$$

In the time interval $(t_p[n], t_s[n+1])$, given capacitor voltage $v(t_v[n])$, one can express the capacitor voltage $v[n+1]$ by

$$v[n+1] = \left(1 - \frac{\lambda T_{\text{on}}}{RC}\right) v(t_v[n]) + \frac{\lambda^2 m_1 T_{\text{on}}^2}{2C} + \frac{\lambda T_{\text{on}} i_v[n]}{C}. \quad (11)$$

Equations (9)–(11) between $v[n+1]$, $v[n]$, $i_v[n-1]$, and $i_v[n]$ reveal a nonlinear relationship between the valley current sequence and the voltage sequence. A small perturbation to this curve leads to the linearization about the operating point

$$\tilde{v}[n+1] = \gamma_v \tilde{v}[n] + \gamma_i \tilde{i}_v[n] + \gamma_{im1} \tilde{i}_v[n-1]. \quad (12)$$

By denoting $\hat{\tau}_1 = RC/T_{\text{on}}$, $\hat{\tau}_2 = LT_{\text{on}}/R$, and $M_r = (V_{\text{in}} - V_{\text{out}})/V_{\text{out}}$, the coefficients γ_v , γ_i , and γ_{im1} can be parameterized by

$$\begin{aligned} \gamma_v &= 1 - (1 + M_r) \hat{\tau}_1^{-1} - \frac{1 + M_r}{2} \hat{\tau}_1^{-1} \hat{\tau}_2^{-1} \\ \gamma_i &= R \left(\lambda + \frac{M_r}{2} \right) \hat{\tau}_1^{-1} \\ \gamma_{im1} &= R \left(1 - \lambda + \frac{M_r}{2} \right) \hat{\tau}_1^{-1}. \end{aligned}$$

In 5S, the power converter can be modeled as a low-order difference equation. Although 5S is obtained from a nonperiodic sampling process, the z -transform can always be performed on any linearized difference equation within a region of convergence irrespective of the underlying sampling. The z -transform on linear difference equation (12) leads to the z -domain expression of the plant

$$\frac{\hat{v}(z)}{\hat{i}_v(z)} = g_1 \frac{(1 - b_1 z^{-1}) z^{-1}}{1 - a_1 z^{-1}} \quad (13)$$

where

$$\begin{aligned} a_1 &= 1 - (1 + M_r) \hat{\tau}_1^{-1} - \frac{1 + M_r}{2} \hat{\tau}_1^{-1} \hat{\tau}_2^{-1} \\ g_1 &= R \left(\lambda + \frac{M_r}{2} \right) \hat{\tau}_1^{-1}, \quad b_1 = -\frac{1 - \lambda + M_r/2}{\lambda + M_r/2} \\ M_r &= \frac{V_{\text{in}} - V_{\text{out}}}{V_{\text{out}}}, \quad \hat{\tau}_1 = \frac{RC}{T_{\text{on}}}, \quad \hat{\tau}_2 = \frac{L/R}{T_{\text{on}}}. \end{aligned} \quad (14)$$

The z -domain transfer function gives insights to controller design because it reveals the direct relationship between circuit parameters and 5S dynamics. The slow open loop pole of the power converter plant located at a_1 corresponds to the output RC filter time constant. The fast open loop pole located at the origin (i.e., z^{-1}) corresponds to the one-cycle delay between when the inductor valley current is known and when the output capacitor voltage is updated. The slow pole in the transfer function indicates the amount of time scale separation between the switch ON-time and the time constant of the output low-pass filter. Together the fast pole and zero describe the delay between measurement and actuation; the zero represents the delay being less than one sample period. This zero varies with λT_{on} , which is the delay time from the valley-current time to the voltage-sampling time. The pole $z = 0$ corresponds to one switching cycle delay, which reflects the causality of the original

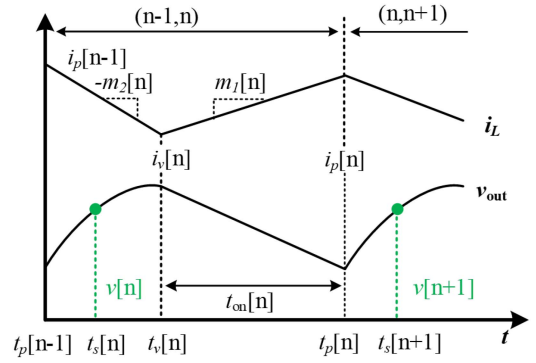


Fig. 5. Inductor current and capacitor voltage waveforms for COT-CM boost converter.

physical system. In the circuit, there is no direct feed-forward from the inductor current to the capacitor voltage, which means that the sampled voltage for the current cycle is determined by the current from the previous cycle.

D. Operation of COT-CM Boost Converters

The current-mode boost converter with constant OFF-time is illustrated in Fig. 1. The term “constant OFF-time” indicates that the turn-OFF time T_{off} of switch S_1 is predetermined and kept constant. The inductor current settles in one cycle after the peak current command is updated. The turn-ON time of S_1 is implicitly determined by the peak-current command $i_p[n]$ at $t_p[n]$ ($n > 0$). The sampling of v_{out} and control algorithms are conducted cycle-by-cycle during the OFF-time because the OFF-time is constant even during transients. $v[n]$ and $i_p[n]$ are not at the same physical time although their indices are same. The peak-current controller uses an analog comparator to determine when the inductor current crosses a threshold that is determined by the DAC reference, which is updated every cycle. Fig. 5 shows the current and the voltage of inductor L and capacitor C , respectively.

The acquisition and the conversion of the output voltage occurs when S_1 is turned-OFF. A fixed parameter λ quantifies the sampling time $t_s[n]$, namely, $t_s[n] = t_p[n-1] + \lambda T_{\text{off}}$, $\lambda \in (0, 1)$. The peak inductor current during each switching cycle is represented by $i_p[n]$, while the $v[n]$ sequence and the $i_p[n]$ sequence do not correspond to the same physical times. In this discretization, all the measurements and the switching are event-triggered instead of clock-triggered. The peak-current detection signal triggers the turn-OFF event of S_1 , and the OFF-time timer drives the turn-ON event.

E. Usual Power Electronics Assertions for Boost Converters

The constant-OFF-time current-mode boost converters satisfy the following properties:

- 1) the OFF-time T_{off} of S_1 is constant;
- 2) ON-time $t_{\text{on}}[n]$ of S_1 is determined by the peak-current (the maximum commanded inductor current every switching cycle), $0 < t_{\text{on}}[n] < +\infty$;

- 3) output voltage v_{out} has small ripple so the inductor waveform can be well-approximated as a linear ramp;
- 4) input voltage $V_{\text{in}} > 0$ is constant;
- 5) the circuit is in continuous-conduction-mode (CCM);
- 6) output capacitor voltage denoted by $v(t) > 0$.

F. Modeling of Boost Converters in 5S

By performing a similar procedure to Section II-C, which is derived in [4], the z -domain model of the boost converter is

$$\frac{\tilde{v}(z)}{\tilde{i}_p(z)} = g_1 \frac{(1 - b_1 z^{-1}) z^{-1}}{1 - a_1 z^{-1}} \quad (15)$$

which is parameterized by

$$a_1 = 1 - 2(\hat{\tau}_1^{-1} + \hat{\tau}_3^{-1}) - \frac{\lambda^2 + (1 - \lambda)^2}{2} \hat{\tau}_1^{-1} \hat{\tau}_2^{-1} \quad (16)$$

$$d_1 = (\lambda \hat{\tau}_1^{-1} + \frac{\lambda^2}{2} \hat{\tau}_1^{-1} \hat{\tau}_2^{-1} - 1)(\hat{\tau}_1^{-1} + \hat{\tau}_3^{-1}) - \left(1 + (1 - \lambda)\hat{\tau}_1^{-1} - 2(\hat{\tau}_1^{-1} + \hat{\tau}_3^{-1}) - \frac{\lambda^2}{2} \hat{\tau}_1^{-1} \hat{\tau}_2^{-1}\right) \times (1 - \lambda)\hat{\tau}_1^{-1} \hat{\tau}_2^{-1}, \quad (17)$$

$$d_2 = \left(\lambda \hat{\tau}_1^{-1} + \frac{\lambda^2}{2} \hat{\tau}_1^{-1} \hat{\tau}_2^{-1} - 1\right) (\hat{\tau}_1^{-1} + \hat{\tau}_3^{-1}) + \lambda \hat{\tau}_1^{-1} \hat{\tau}_2^{-1} \quad (18)$$

$$g_1 = \left(\lambda \hat{\tau}_1^{-1} - \left(1 - \lambda \hat{\tau}_1^{-1} - \frac{\lambda^2}{2} \hat{\tau}_1^{-1} \hat{\tau}_2^{-1}\right) \frac{\hat{\tau}_1^{-1} + \hat{\tau}_3^{-1}}{\hat{\tau}_2^{-1}}\right) R \quad (19)$$

$$b_1 = \frac{d_1}{d_2}. \quad (20)$$

The definitions of $\hat{\tau}_1$, $\hat{\tau}_2$, and $\hat{\tau}_3$ are

$$\hat{\tau}_1 = \frac{RC}{T_{\text{off}}}, \quad \hat{\tau}_2 = \frac{L/R}{T_{\text{off}}}, \quad \hat{\tau}_3 = \frac{RC}{T_{\text{on}}} \quad (21)$$

where T_{off} is the constant OFF-time, T_{on} is the ON-time, and $T = T_{\text{off}} + T_{\text{on}}$.

For example given $\lambda = 0$, which means that the voltage sampling occurs at the inductor current peak, the parameters can be simplified to

$$a_1 = 1 - \frac{2T}{RC} - \frac{T_{\text{off}}^2}{2LC} \quad (22)$$

$$g_1 = -\frac{T}{T_{\text{off}}} \frac{L}{RC} \quad (23)$$

$$b_1 = 1 + \frac{T_{\text{off}}^2 R}{T} \frac{R}{L} - \left(1 + \frac{T_{\text{on}}}{T}\right) \frac{T_{\text{off}}^2}{LC}. \quad (24)$$

In practice, the voltage sampling is performed after the switching transients have died down (i.e., $\lambda > 0$), to reduce the interference that corrupts the voltage measurement.

Note that the 5S transfer function has one zero and two poles, while the traditional s -domain current-mode boost converter model in [30] shows only one zero and one pole. All poles are inside the unit disk, so the open loop system in 5S is stable.

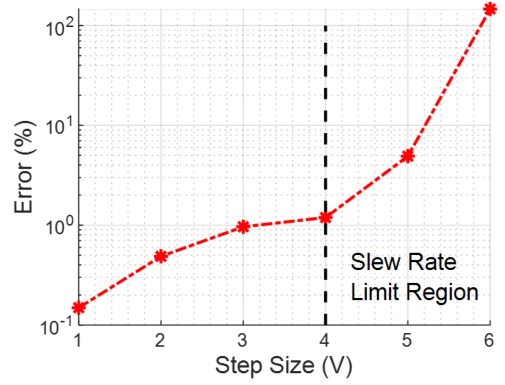


Fig. 6. Worst-case voltage error between the model and simulation under different voltage-step sizes at the initial output voltage of 40 V.

The fast pole is from the single-cycle delay between measurement and actuation, which is the causality requirement of the discretized system. The slow pole is from the output RC -filter of the boost converter, which corresponds with the traditional s -domain model. The zero in the 5S model is analogous to the right-half-plane (RHP) zero of the averaged-state-space boost converter model. One difference between the 5S model and the averaged state-space model is that this zero is not only determined by the circuit parameters and operating point, but also influenced by the sampling delay.

The theoretical voltage step response matches the simulation, which is shown in Figs. 20 and 21 in Section VI-C. The single-step voltage error $e[n]$ between the model and simulation is defined by

$$e[n] \triangleq \frac{(V_{\text{sim}}[n] - V_{\text{model}}[n])}{V_{\text{stepsize}}} \times 100\%. \quad (25)$$

Fig. 6 compares the worst-case voltage error between the small-signal model in (15) and switched-circuit simulation under different output-voltage step sizes at the initial output voltage 40 V. The reason for the increasing error in the region where the inductor current is slew-rate limited is due to the fact that slew-rate limiting is a large signal behavior and small-signal models like (15) are no longer valid. The inductor current cannot increase faster than the cycle-by-cycle inductor ramp despite the controller demanding it. The worst-case error e_w between the model and simulation is defined by

$$e_w \triangleq \max_n |e[n]|. \quad (26)$$

One can observe that the worst-case error is small (below 1%) if the voltage-step size is within 4 V. The error rises quickly when the step size, λ is above 4 V because of large-signal effects; for example, the inductor-current slew rate limit starts to dominate the dynamics. For this COT-CM boost converter, the first significant large-signal behavior which designers face is that the minimum ON-time is reached; hence, the actuator is saturated and the peak inductor current no longer matches the current command.

III. SWITCHING-SYNCHRONIZED SAMPLED-STATE SPACE CONTROL CONCEPTS FOR DC–DC CONVERTERS

In this section, we show that the *5S* model of dc–dc converters agrees with the switched state-space model [30] concerning the stability and transient performance. However, the controller synthesis problem for *5S* models is much easier than that for a switched state-space model because the former is a pure discrete system, while the latter is a hybrid system [31]. In *5S*, small-signal controller design is straightforward because conventional digital controller design tools (e.g., root locus and Nyquist plots) can be used even though *5S* represents something different from the conventional.

A. Stability

Stability is the minimum requirement for a closed-loop controlled system. Trajectories in *5S* contain less information than the physical trajectories. Because of the discretization, the information about the system dynamics between the adjacent sampled data are lost. Because of the nonuniform sampled data, the information about physical time is lost as well. However, by utilizing the restrictions on the trajectories in Section II-B, the stability relationship is preserved. This article mathematically proves that stability in *5S* enforces stability in physical time.

Stability means the capacitor voltage and inductor current waveforms converge to a periodic trajectory in the phase plane. The following procedure results in a mathematical proof. The detailed proof can be found in Theorem 1 in Appendix A. Given a constant ON(OFF)-time dc–dc converter system, this proof first shows that a point in the state space of *5S* is equivalent to a specific voltage and current magnitude in the CT domain by constructing an invertible reconstruction mapping; the variable switching period can be similarly reconstructed. For a stable system in *5S*, the proof shows that both the capacitor voltage and inductor current trajectories are bounded. Using the usual assertions (1), (3), (4) in Section II-B, the proof shows that the switching period is also bounded. Within this bounded switching period, the reconstruction mapping yields a proof that both capacitor voltage and inductor current converge to a periodic waveform. The proof finally confirms that the switching period converges and that there are no subharmonics in this periodic waveform. This periodic steady state is referred to as a *synchronously asymptotically stable least-harmonics (SASL) equilibrium*. The rigorous definition of SASL can be found in Definition 7 in Appendix A.

The stability criterion in *5S* is identical to the classical discrete-time system stability theory. From root locus or Nyquist [32] stability criteria, one can provide a sufficient and necessary condition for a compensated discrete linear system: all closed-loop poles are inside the open unit disk.

B. Transient Response

The transient performance of a controlled system is usually characterized by the response to a step input [33]. For constant ON(OFF)-time dc–dc converters, this article analyzes the output voltage step response with a focus on settling time

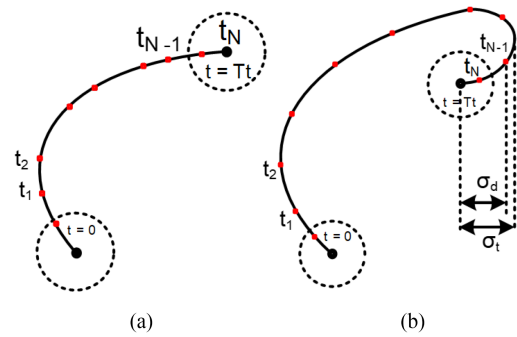


Fig. 7. Conceptual phase plane trajectories of converging from one setpoint to another illustrate *5S* discretization in physical time. (a) Optimizing the transient settling cycles is equivalent to optimizing the transient settling time, i.e., fewest *5S* cycles correspond to shortest settling time. (b) Overshoot in continuous physical time can be bounded from above from the overshoot in *5S* using information about the trajectories.

and overshoot because they are among the two most important transient performance criteria for power converter designers. This section shows that the transient performance in *5S* maps to the physical time. Given a closed-loop constant ON(OFF)-time dc–dc converter system with a reference output voltage step command $V_{e1} \rightarrow V_{e2}$, the *settling time* T_t is the transition time from one steady state to another and the *settling cycles* N_t is the number of turn-ON instants from one steady state to another. The *overshoot* for the sampled output-voltage, peak inductor current, and output voltage is given by

$$\sigma_d^v = \frac{\max_n v[n] - V_{e2}}{V_{e2} - V_{e1}} \quad (27)$$

$$\sigma_d^i = \frac{\max_n i[n] - I_{e2}}{I_{e2} - I_{e1}} \quad (28)$$

$$\sigma_t^v = \frac{\max_t v(t) - V_{e2}}{V_{e2} - V_{e1}} \quad (29)$$

Because of the nonuniform sampling, the settling steps and settling time are not proportional as illustrated in Fig. 7(a). This work proves that the optimization on the *settling steps* in the *5S* representation is equivalent to the optimization on the worst-case *settling time* in the physical state space. The detailed proof can be found in Theorem 2 in Appendix B. Through the volt-second relationship of the inductor current together with the capacitor charge, the proof constructs the relationship between the settling time, switching cycles, transient voltage waveforms, and steady-state current waveforms. The *5S* voltage overshoot in (27) and (29) bounds the worst-case transient voltage waveforms. Finally, the proof confirms that the settling time can be bounded from above by a linear function of settling steps. By optimizing the settling steps, the worst-case settling time is also optimized.

Because of the discretization, the overshoot in *5S* is smaller than that in CT as illustrated in Fig. 7(b). The mathematical proof confirms that the *overshoot* in the physical time is bounded from above by a linear function of the *overshoot* in *5S*. The detailed proof can be found in Theorem 3 in Appendix B. Through the charge of the output capacitor, this article constructs the

relationship between the maximum voltage in $5S$, the maximum voltage in CT , transient voltage waveforms, and transient current waveforms. The inductor current overshoot in (28) bounds the transient inductor current. Finally, the proof confirms that the overshoot in physical time can be bounded from above by a linear function of the overshoot in $5S$. In this way, the overshoot in physical time can be safely constrained by imposing the constraints on overshoot in $5S$.

A result of the $5S$ theory is the calculation of the worst-case voltage in the physical time domain from a voltage step using the peak overshoot of the step response of the $5S$ z -domain transfer function. The discrete $5S$ overshoot is going to be less than or equal to the physical CT overshoot because sampling during the inductor current peak/valley event does not necessarily coincide with the peak CT voltage. Because the inductor current is the mechanism by which charge is added to the output capacitor, the largest possible voltage ripple (i.e., upper bound) can be calculated from the largest inductor current during the transient; this is shown in (58) and (59) for a boost converter.

Therefore, the digital controller design in the time domain can be conveniently converted to a controller design in $5S$. In other words, this work transforms a complicated hybrid² optimization problem to a pure discrete-domain optimization problem, which is much easier to design.

IV. COMPARISON OF PREVIOUS MODELING METHODS TO $5S$

The modeling performance of $5S$ is compared to two previously known modeling efforts: averaging [13], [18], [30] and describing function methods [20]. In the first method, averaging and then linearization are first performed in the CT domain of the power converter state space equations. Sampling is then performed as the final step on these linearized averaged equations. It is worth noting that the averaging window is required to be larger than the largest switching period of a variable frequency converter. The describing function method is a small-signal model that uses a succession of approximations that rely on approximating the inductor valley current by its fundamental sinusoid.

In summary, the steps for the describing function (DF) method include the following:

- 1) performing a small-signal perturbation on the inductor valley current;
- 2) restricting the inductor valley current perturbation so that the switching frequency perturbation is small-signal and the spectrum of the perturbation contains only multiples of the switching frequency;
- 3) for a particular valley current command, approximating the resulting inductor current by its fundamental frequency sinusoid;
- 4) deriving the mapping between the valley current command to the inductor current amplitude and phase;
- 5) using a Pade approximation to make the transfer function between valley current command to the resulting approximate inductor current a rational transfer function;

²Combined continuous-time states and discrete-time states [34].

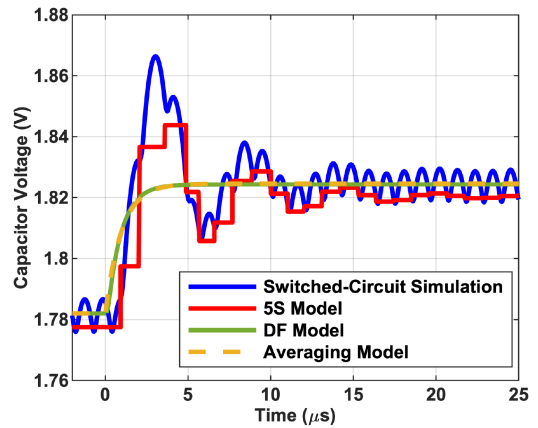


Fig. 8. Comparison of small-signal step responses for various models versus switched-circuit simulation.

TABLE I
COMPARISON OF MODELING METHODS

Performance metric	Avg. ^a model [13]	DF ^b method [20]	$5S$ ^c	SC ^d Sim
Rise time (μs)	1.81	1.81	0.856	0.768
Gain margin	∞	25.9 dB	3.7 dB	N/A
Phase margin	91.3°	84.5°	26.5°	N/A
Trans. stability margin (Ringing cycles)	0	0	4	4

^a Averaging model

^b Describing function-based method

^c Switching-synchronized sampled-state space

^d Switched-circuit simulation

- 6) using an averaging model to derive the transfer function from the approximated inductor current to the output voltage.

A switched-circuit simulation of a buck converter ($L = 100$ nH) was performed with the event-driven controller in Fig. 2 in closed loop with a proportional controller ($K = 200$). A comparison of the step responses of the $5S$, DF, and averaging models with identical proportional controller gain is shown in Fig. 8. When comparing to a switched-circuit simulation with identical proportional gain, $5S$ more accurately models the step response. In Table I, a comparison of the phase margin from Nyquist plots shows that $5S$ gives a more accurate stability margin; this is evidenced by the agreement in the ringing cycles between $5S$ and the switched-circuit simulation.

An important discrepancy between the switched-circuit simulation and the assumptions in both averaging and DF is the typically wide variation in switching period despite a small-signal

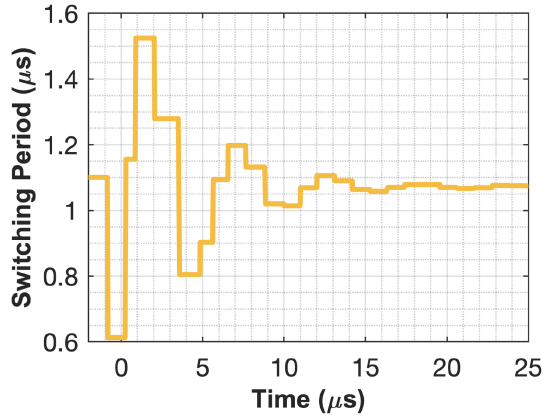


Fig. 9. Switching period significantly varies even for a small-signal step response in a switched-circuit simulation.

output voltage step. This is demonstrated when the switching period is plotted versus time in Fig. 9 for the switched-circuit simulation in Fig. 8. The 5S framework does not require the switching period variation to be small.

From Section II, the sampling period is synchronized with the switching period. Because the switching period varies significantly during a small-signal transient, approximating the sampling period by its steady-state value is inaccurate. In 5S, Ω is an abstract topological frequency rather than a true physical frequency whose transform is related to time; hence, any variation in the switching period is valid. It is worth noting that any transformation from the 5S z -domain to an s -domain that corresponds to a physical frequency (e.g., $s = j2\pi f$, where f is a physical frequency in Hz) is not possible.

V. DIGITAL CONTROLLER DESIGN IN 5S

A. Digital Controller Design for a COT-CM Boost Converter

The open-loop converter plant for a COT-CM boost converter does not have a transient response that is fast enough to perform DVS for LiDAR because the output RC -filter results in a slow pole. This shortcoming motivates us to develop a systematic compensation method.

Previous sections of this article have shown that performance-optimized digital controller design in the time domain can be equivalently converted to a performance-optimized controller design in 5S. Controller design problems in 5S can be solved by classical control methods. Root locus or Nyquist plots can be used for direct-digital design of the controller because the plant is modeled as a z -domain transfer function [32].

Any traditional discrete-time controller can be transformed to 5S using an event-driven sampler and actuator, which are updated synchronously with switching actions. This section illustrates a design example of a boost converter performing a voltage step task. The root-locus method is shown in Fig. 10. In the compensator, the first pole $p_k = 1$ (integrator) is placed to force the steady-state voltage error to be zero. Also, a zero z_k as well as an appropriate gain k speeds up the transient

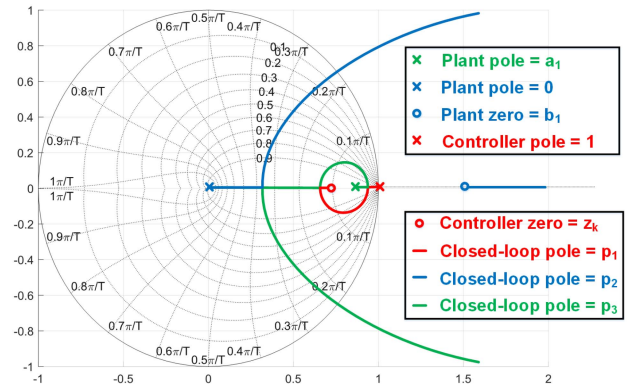


Fig. 10. Root-locus method for digital controller design in 5S of a COT-CM boost converter.

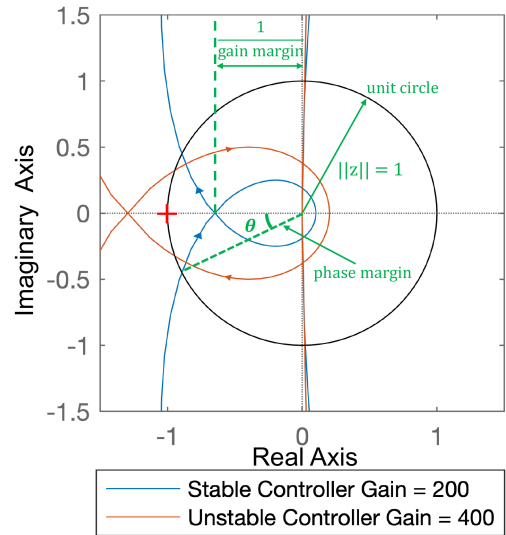


Fig. 11. Nyquist Plot for a buck converter using proportional control shows stable and unstable contours. Gain and phase margin are determined using conventional methods [35].

response. The resulting *switching-synchronized* proportional-integral (S^2PI) compensator can be expressed as

$$K(z) = k \frac{1 - z_k z^{-1}}{1 - p_k z^{-1}}. \quad (30)$$

A zero z_k in the neighborhood of the slow open-loop pole a_1 provides additional compensation. The perceived optimal way is to achieve pole-zero cancellation; however, this cancellation is never perfect in practice because of the uncertainty of a_1 . z_k to the left of the poles $z = a_1$ and $z = 1$ provides better robust performance. From root locus rules, z_k is the destination of the root locus leaving a_1 . The resulting closed-loop pole p_1 stays on the real axis and in the neighborhood of z_k . At high gain, the settling is determined by the zero z_k .

A conventional Nyquist plot is also applicable in 5S as illustrated in Fig. 11. Stable and unstable controller are shown

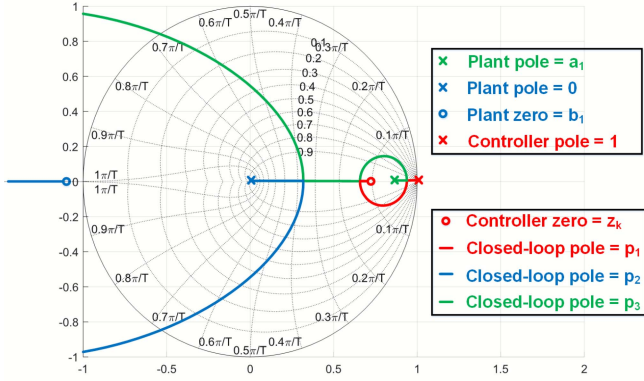


Fig. 12. Closed-loop root-locus of PI-compensated constant ON-time current-mode buck converter.

for a proportional controller with different gains. The standard method for determining gain and phase margins are illustrated [35]. Gain margin and phase margin are the appropriate stability margins for closed-loop small-signal controller design in $5S$.

B. Digital Controller Design for a COT-CM Buck Converter

Similarly, in a current-mode buck converter with constant ON-time, the z -domain transfer function is a second-order system with one fast pole and one slow pole. For the controller, a pole at $z = 1$ for zero steady-state error with a zero for a proportional-integral (PI) controller is all that is needed.

This section shows a controller design example here for a current-mode buck converter with constant ON-time with the hardware prototype specifications chosen with the goal of minimizing settling time with no overshoot. The uses the $5S$ framework with the equivalent goal of minimizing the number of cycles for settling under a zero overshoot constraint. The plant model is $0.0023(1 + 1.4390z^{-1})z^{-1}/(1 - 0.9739z^{-1})$ with a controller pole at $a = 1$ for zero steady-state error, zero at $b = 0.9750$, and gain of 50. The root locus is illustrated in Fig. 12, where it is apparent that the closed-loop dynamics are dominated by a complex-conjugate pole pair. The next section verifies the discrete-time step later with the hardware.

VI. HARDWARE, EXPERIMENTAL, AND SIMULATION RESULTS

A. Digital Controller Hardware

The digital controller hardware was implemented in a Xilinx Spartan 6 FPGA for the buck converter and Artix 7 FPGA for the boost converter. The FPGA uses synchronous logic to run the digital controller, ADCs, and DACs. Events can be asynchronous and external to the FPGA, such as when the inductor current crosses the comparator reference. The controller is event-based which means actions are still triggered by the internal FPGA synchronous clock; however, for an asynchronous event, the FPGA clock cycle which is closest to the time of the event synchronously clocks the trigger of the logic branch. Events can also be synchronous and internal; for example, the timeout of a fixed

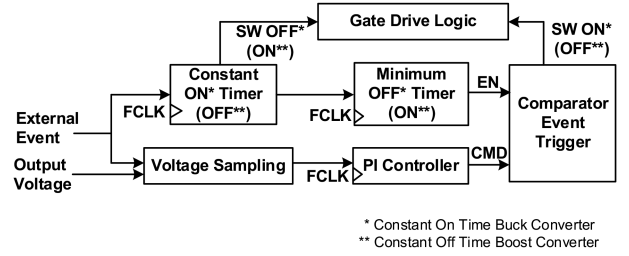


Fig. 13. Control stream of the power converters.

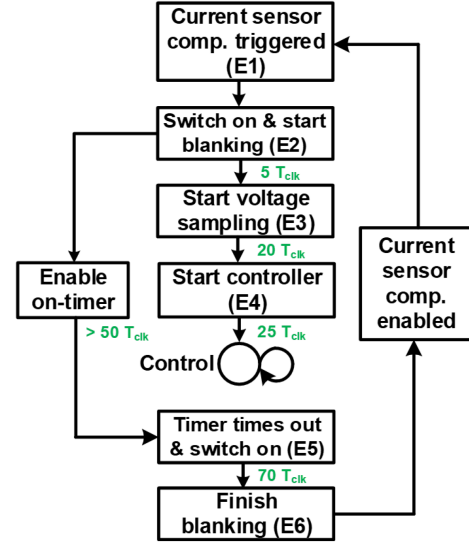


Fig. 14. Switching-synchronized sampling and control flowchart of a COT-CM buck converter.

ON-time hardware timer within the FPGA. The transfers of data to and from the DAC and ADC are performed by divided-down FPGA clocks that are synchronized to the FPGA internal clock; it is worth noting that the divided-down clocks are much faster than the event rates. The FPGA clocking, event paths, and logic modules are illustrated in Fig. 13. The comparator event (an external event) is triggered when the inductor current crosses the comparator threshold which is determined by the DAC. This event determines the valley current for the buck converter by turning the power switch ON or the peak current for the boost by turning the power switch OFF. The comparator event also starts the ON/OFF-timer for the buck or boost, respectively. Another event is triggered when the ON/OFF-timer completes, turning the power switch OFF for the buck converter or ON for the boost converter.

For the buck converter controller in Fig. 14, (E1) corresponds to the instance when the valley inductor current crosses the comparator threshold and corresponds to $i_v[n]$ in Fig. 4. The comparator output is blanked for an interval of time so it does not retrigger events from switching transients and the power switch is turned ON in (E2) after a logic delay. After 5 FPGA clock cycles (one cycle = 5 ns), the ADC samples the output voltage in (E3) which takes approximately 20 FPGA clock cycles. The controller then processes the data and performs calculations in

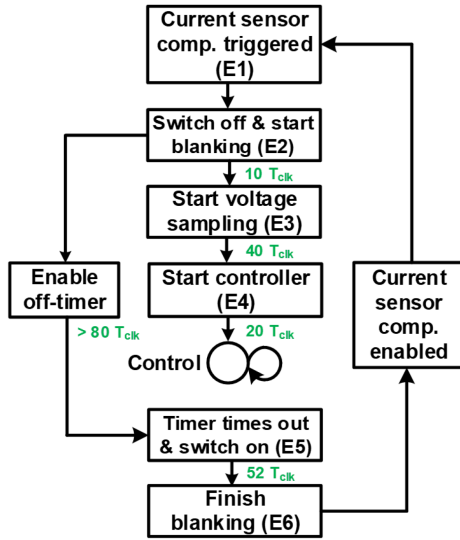


Fig. 15. Switching-synchronized sampling and control flowchart of a COT-CM boost converter.

(E4), which takes 25 FPGA clock cycles. It is worth noting that (E3) and (E4) occur while the comparator output blanking is enabled during the ON-time. When the ON-time timer completes in (E5), the power switch turns OFF, which corresponds to $i_v[n]$ in Fig. 4. After the switching transient, which is at most 70 FPGA clock cycles, blanking is disabled in (E6), after which the current-sense comparator output is reenabled.

For the boost converter controller in Fig. 15, (E1) corresponds to the instance when the peak inductor current crosses the comparator threshold and corresponds to $i_p[n]$ in Fig. 5. The comparator output is blanked for an interval of time so it does not retrigger events from switching transients and the power switch is turned OFF in (E2) after a logic delay. After 10 FPGA clock cycles (one cycle = 2.5 ns), the ADC samples the output voltage in (E3) which takes approximately 40 FPGA clock cycles. The controller then processes the data and performs calculations in (E4), which takes 20 FPGA clock cycles. It is worth noting that (E3) and (E4) occur while the comparator output blanking is enabled during the OFF-time. When the OFF-time timer completes in (E5), the power switch turns ON, which corresponds to $i_v[n]$ in Fig. 5. After the switching transient, which is at most 52 FPGA clock cycles, blanking is disabled in (E6), after which current-sense comparator output is reenabled.

B. Buck Converter for VRM Applications

We designed and built a current-mode buck converter with constant ON-time that is controlled by a 5S digital controller, which is a prototype for dynamic voltage scaling and is shown in Fig. 16. The 1.8 V output was selected based on the power requirements for a typical microprocessor [36]. The power level was chosen to be 20 W based on the thermal design power (TDP) value [37]. The switching frequency was chosen to be 1.67 MHz to demonstrate high-speed cycle-by-cycle digital control, which can be challenging. Other circuit parameters are reported in Table II. The control algorithm follows the flowchart in Fig. 14.

TABLE II
DESIGN PARAMETERS OF THE COT-CM BUCK CONVERTER PROTOTYPE

Param.	Values	Param.	Values
V_{in}	8 V	L	200 nH
V_{out}	1.8 V	Power	20 W
T_{on}	250 ns	R_s	10 m Ω
C	200 μ F	Peak f_{sw}	1.67 MHz
FPGA	Spartan-6	ADC	LTC2378-16
MOSFET	IRF6620	DAC	MAX5184
Diode	B520	Diff. Op-Amp	LT1994

TABLE III
DESIGN PARAMETERS OF THE COT-CM BOOST CONVERTER PROTOTYPE

Param.	Values	Param.	Values
V_{in}	12 V	L	6.8 μ H
V_{out}	40 V	Power	16 W
T_{off}	200 ns	R_s	100 m Ω
C	1 μ F	Peak f_{sw}	3 MHz
FPGA	Artix-7	ADC	LTC2378-16
MOSFET	GS61004B	DAC	MAX5184
Diode	STPS1H100A	Diff. Op-Amp	LT1994

The prototype performs well for fast transient response in both small-signal reference step and large-signal reference step. A small-signal step of 50 mV shows a rise time as fast as 5 μ s with no overshoot in Fig. 17.

Theory, simulation, and experiment show good agreement in Fig. 17. A possible reason for the small discrepancy between theory and experiment might be attributed to our model assumption of a lossless circuit with real losses causing deviations in the duty ratio and switching frequency from the ideal. This result with only a small discrepancy is a verification of theory with experiment. It is worth noting that a large-signal 0.5 V reference step to a 1.8 V setpoint was demonstrated to be stable despite inductor slew rate limiting. The large-signal response in Fig. 18 shows a rise time as fast as 8 μ s with less than 3% overshoot.

C. Boost Converters for LiDAR Applications

A current-mode boost converter was designed and built with constant OFF-time that is controlled by a 5S digital controller. Our COT-CM boost regulator includes an analog peak-current-control circuit and digital voltage-control loop as shown in Fig. 1. The prototype shown in Fig. 19 was constructed with the parameters in Table III and controlled by an Artix-7 FPGA from Xilinx with a 400 MHz system clock. The control algorithm follows the flowchart in Fig. 15. One control cycle consists of approximately 80 FPGA clock cycles which determines the 200 ns constant OFF-time. The 12 V input is a common voltage

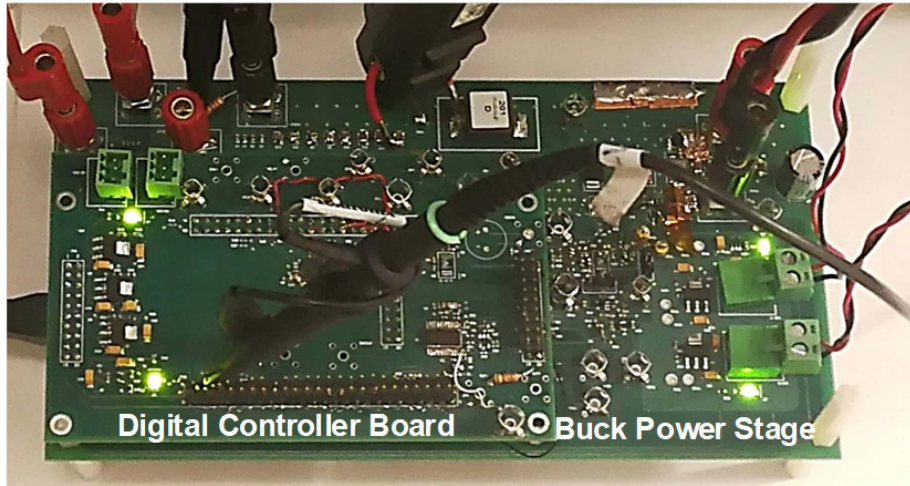


Fig. 16. Constant ON-time current-mode buck converter prototype and digital control hardware.

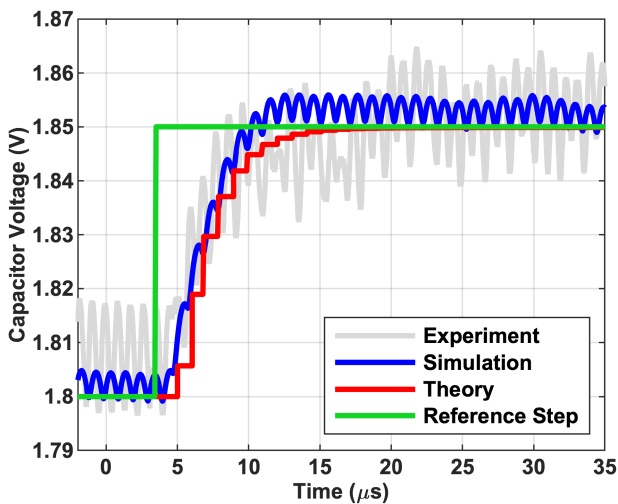


Fig. 17. Small-signal output capacitor voltage response of a COT-CM buck converter for a reference voltage step.

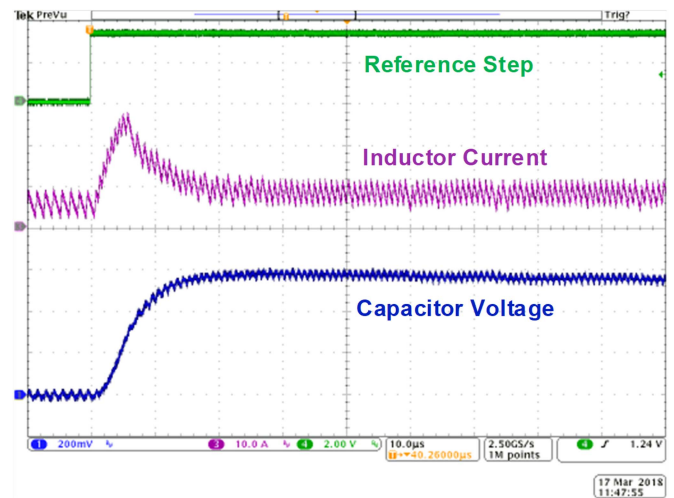


Fig. 18. Large-signal output voltage/inductor current response of a COT-CM buck converter in reference voltage step.

level in a vehicle. The output voltage was selected to be 40 V based on the laser driver solution in [38]. The power level was set to be 16 W based on a commercial product [12]. The peak switching frequency is 3 MHz because LiDAR transmitters need to be more compact and portable [12] with high switching frequency largely shrinking the size and weight.

Theory, simulation, and experiment show good agreement in Figs. 20 and 21. The theoretical current is offset from the experimental data by 10%. This deviation is a result of the assumption in the theory that the converter is lossless; the prototype is instead 90% efficient. The theoretical voltage matches the experimental data in steady state because of the integrator in the controller. The actual voltage ripple is approximately 200 mV in Fig. 21.

The practical DVS task for LiDAR involves voltage steps over a wide range of setpoints. Over these laser driver operating points, a fixed controller that is stable and has no overshoot at high voltage conversion ratio will be slow at low output

voltage. To maintain transient performance throughout each of the operating points' transitions, a different controller design is used for each transition. It is worth noting that the LiDAR transmitter can be modeled as a small-signal resistive load at each operating point. The controller design is parameterized by a family of linear controllers that can be easily stored as a lookup table in the ROM of the FPGA.

Our digital implementation makes it straightforward to adapt the controller gains; this is an important advantage over analog controllers.

The experimental large-signal staircase voltage steps from 20 V \rightarrow 25 V \rightarrow 30 V \rightarrow 35 V \rightarrow 40 V shown in Fig. 22 emulate a practical dynamic laser pulse peak power corresponding to 60 W \rightarrow 80 W \rightarrow 100 W \rightarrow 115 W \rightarrow 125 W. Each voltage step exhibits a rise time of approximately 5 μ s with small overshoot, which satisfies the dynamic performance requirements for state-of-the-art LiDAR transmitter systems. A load step from 16 to

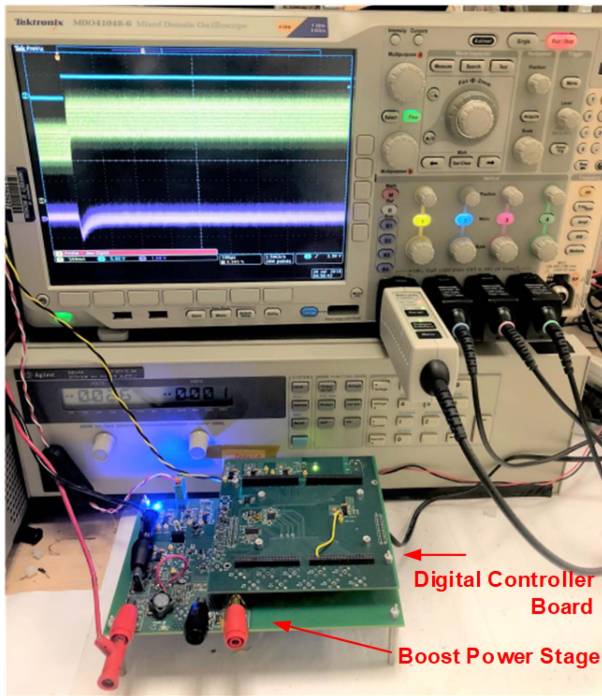


Fig. 19. Constant OFF-time current-mode boost converter prototype and digital control hardware under test.

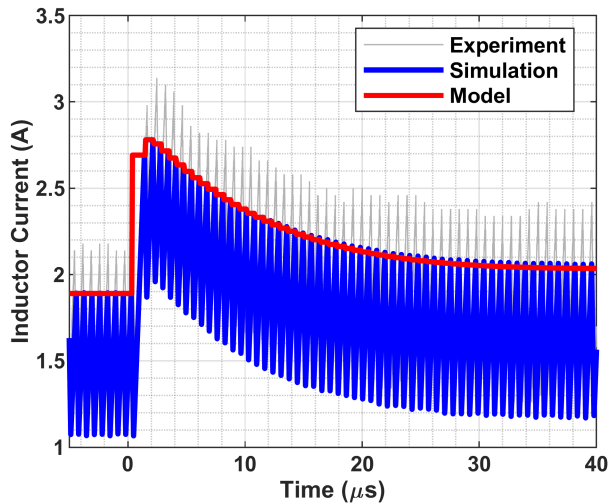


Fig. 20. Comparison of the inductor current i_L waveform of a COT-CM boost converter between the theory, simulation, and experiment for an output voltage step response.

22.4 W at 40 V output voltage shown in Fig. 23 emulates a laser pulser repetition rate step from 700 kHz to 1 MHz. Under a large load disturbance, the maximum voltage deviation is 1 V, which is within the 5% capacitor bank discharge limit [38].

D. Effect of Output Capacitance and Loading

The effects of different output capacitance and load on the voltage step response are demonstrated in simulation for the buck converter in Fig. 24 and the boost converter in Fig. 25.

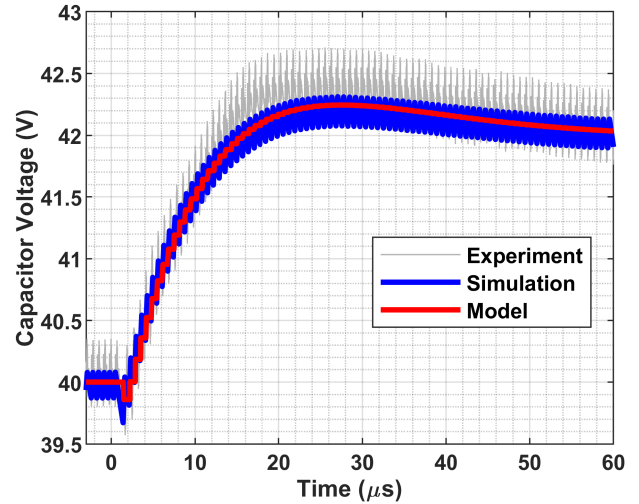


Fig. 21. Comparison of the capacitor voltage v_c waveform of a COT-CM boost converter between the theory, simulation, and experiment for an output voltage step response.

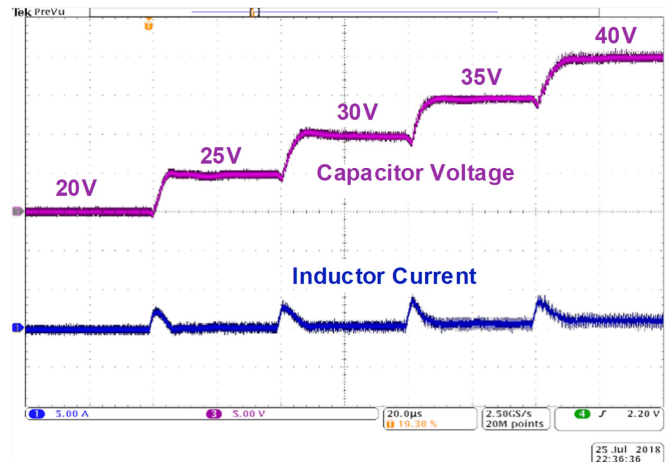


Fig. 22. Dynamic laser pulse voltage scaling.

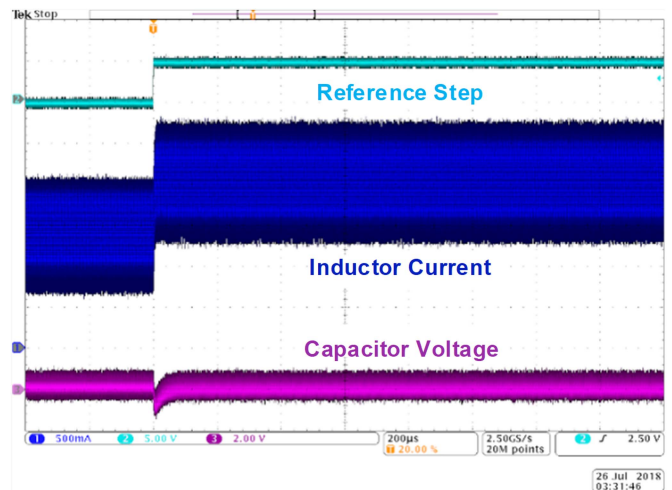


Fig. 23. Laser pulse repetition rate step.

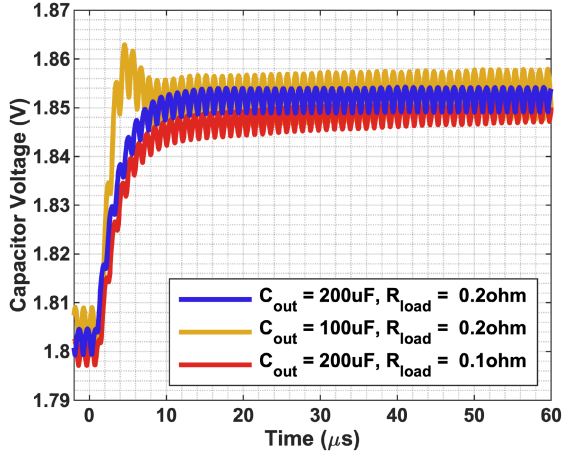


Fig. 24. Step response for buck converter over output capacitance and load using switched circuit simulation.

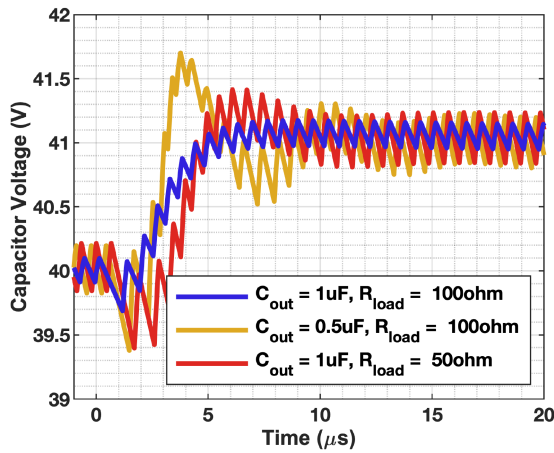


Fig. 25. Step response for boost converter over output capacitance and load using switched circuit simulation.

Output capacitance is typically chosen to satisfy a particular output voltage ripple requirement or to provide holdup while the control system catches up [39]. Additionally, output capacitance may be constrained by the stability requirements of the current control loop [40]. The input voltage, nominal output voltage, constant ON and OFF times, and inductance are identical to the hardware and can be found in Tables II and III, for the buck and boost converters, respectively.

It is worth noting that the controllers in these simulations are identical to those in hardware and kept the same over output capacitance and load in Figs. 24 and 25. In both the buck and the boost, the output capacitance and load resistance values affect the pole location from the output filter. In the boost converter, the zero is predominantly affected by the output load resistance and inductor value.

One can observe a long tail settling in the buck converter when the capacitance and load are varied significantly. In practice, the controller design is typically modified so it is appropriate for the output capacitance and satisfies a specification for the load range.

VII. CONCLUSION

This article presented a new model and design methodology for performing switching cycle event-driven digital control on variable-frequency dc-dc converters. We demonstrated an accurate model for a dc-dc converter plant in a nonperiodic sampled state space. We illustrated a method for designing a switching-synchronized controller for a given plant. Closed-loop system performance from an analytical model is verified through simulations and experiments. Dynamic voltage scaling as an application for dc-dc converters using a switching-synchronized controller can largely improve the energy efficiency of processors, memories, communications circuits, and LiDAR power supplies, among others, by responding to the varying energy demand at high speed and a very flexible way.

APPENDIX A STABILITY

Definition 1: Σ is a class of boost converters with the following properties:

- 1) the OFF-time T_{off} of S_1 is constant;
- 2) ON-time $t_{\text{on}}[n]$ of S_1 is determined by the peak-current (the maximum commanded inductor current every switching cycle), $0 < t_{\text{on}}[n] < +\infty$;
- 3) output voltage v_{out} has small ripple so the inductor waveform can be well-approximated as a linear ramp;
- 4) input voltage $V_{\text{in}} > 0$ is constant;
- 5) the circuit is in CCM;
- 6) output capacitor voltage denoted by $v(t) > 0$.

Definition 2: \mathcal{S} is the set of systems with class Σ plants, and controller K with noise-free output voltage measurement and peak-current actuation.

Definition 3: Given any system $\mathcal{S}_1 \in \mathcal{S}$, under the switching-synchronized discrete state-space representation, V is a class of *discrete state trajectories*, which includes a sequence of vectors $\{\mathbf{u}[n]\}$ with $\mathbf{u}[n-1] = [v[n] \quad i_p[n-1]]^T$. $v[n]$ is the output voltage that is sampled at $t_s[n] = t_p[n-1] + \lambda T_{\text{off}}$, where $t_p[n-1]$ is the n th turn-OFF time of S_1 , as in Fig. 5. $i_p[n]$ is the peak current after n switching cycle, as in Figs. 1 and 5.

The *discrete state trajectory* is defined in [21].

Definition 4: Given any system $\mathcal{S}_1 \in \mathcal{S}$, W is a class of CT state trajectories that a vector-valued function evolving through time $\mathbf{x}(t) = [v_{\text{out}}(t) \quad i_L(t)]^T$. $v_{\text{out}}(t)$ is the output voltage and $i_L(t)$ is the inductor current as in Fig. 1. Without loss of generality and because of causality, we denote the starting time of $\mathbf{x}(t)$ as the time $t_0 \triangleq t_p[n=0]$ of the first inductor current peak.

Given a system $\mathcal{S}_1 \in \mathcal{S}$ with all the parameters and initial states determined, class V and class W trajectories are denoted as $\{\mathbf{u}[n]\}$ and $\mathbf{x}(t)$, respectively, there must exist more than one mapping that transforms $\{\mathbf{u}[n]\}$ to $\mathbf{x}(t)$. To examine the relationship between $\{\mathbf{u}[n]\}$ and $\mathbf{x}(t)$, we only need to construct one of these mappings. A boost converter operating in CCM can be modeled as a switched-affine time-invariant system. In what follows, $s \in \{0, 1\}$ as a super/subscript indicates the state of the

switch: $s = 0$ represents S_1 is OFF and $s = 1$ represents S_1 is ON, as in Fig. 1.

The state transition matrix Φ_s and the offset vector Γ_s are defined as follows. During the time interval $[t_p[n], t_p[n] + T_{\text{off}}]$ ($n \geq 0$)

$$\begin{aligned} \mathbf{x}(t) &= \begin{bmatrix} x_1(t_p[n]) + \alpha_1(t - t_p[n]) - \frac{m_2[n]}{2C}(t - t_p[n])^2 \\ x_2(t_p[n]) - m_2[n](t - t_p[n]) \end{bmatrix} \\ &= \Phi_0(t, t_p[n]) \mathbf{x}(t_p[n]) + \Gamma_0(t, t_p[n]) \end{aligned} \quad (31)$$

where $\alpha_1 = x_2(t_p[n])/C - x_1(t_p[n])/RC$

$$\Phi_0(t_2, t_1) \triangleq \begin{bmatrix} 1 - \frac{t_2-t_1}{RC} - \frac{(t_2-t_1)^2}{2LC} & \frac{t_2-t_1}{C} \\ -\frac{(t_2-t_1)}{2L} & 1 \end{bmatrix},$$

$$\Gamma_0(t_2, t_1) \triangleq \begin{bmatrix} \frac{V_{\text{in}}}{2LC}(t_2 - t_1)^2 \\ \frac{V_{\text{in}}}{2L}(t_2 - t_1) \end{bmatrix}.$$

During the time interval $[t_p[n] + T_{\text{off}}, t_p[n+1]]$

$$\begin{aligned} \mathbf{x}(t) &= \begin{bmatrix} x_1(t_p[n] + T_{\text{off}})(1 - (t - t_p[n] - T_{\text{off}})/RC) \\ x_2(t_p[n] + T_{\text{off}}) + m_1(t - t_p[n] - T_{\text{off}}) \end{bmatrix} \\ &= \Phi_1(t, t_p[n] + T_{\text{off}}) \mathbf{x}(t_p[n] + T_{\text{off}}) + \Gamma_1(t, t_p[n] + T_{\text{off}}) \end{aligned} \quad (32)$$

where

$$\Phi_1(t_2, t_1) \triangleq \begin{bmatrix} 1 - \frac{t_2-t_1}{RC} & 0 \\ 0 & 1 \end{bmatrix}, \Gamma_1(t_2, t_1) \triangleq \begin{bmatrix} 0 \\ \frac{V_{\text{in}}}{L}(t_2 - t_1) \end{bmatrix}.$$

We observe that $\Phi_s(t_2, t_1) = \Phi_s(t_2 - t_1, 0)$ and $\Gamma_s(t_2, t_1) = \Gamma_s(t_2 - t_1, 0)$. We can write Φ_s and Γ_s by

$$\Phi_s = \begin{bmatrix} \phi_{vv}^s & \phi_{vi}^s \\ \phi_{iv}^s & \phi_{ii}^s \end{bmatrix}, \quad \Gamma_s = \begin{bmatrix} \gamma_{gv}^s \\ \gamma_{gi}^s \end{bmatrix}.$$

From (31), the state at the sampling time t_s in the $(n+1)$ th switching cycle is

$$\mathbf{x}(t_s[n+1]) = \Phi_0(\lambda T_{\text{off}}, 0) \mathbf{x}(t_p[n]) + \Gamma_0(\lambda T_{\text{off}}, 0). \quad (33)$$

In defining $v(t_s[n])$ as the output voltage at the sampling time instant in the n th interval and $v[n]$ as the sampled output voltage at $t_s[n]$, $v(t_s[n+1]) = v[n+1]$. Similarly, $i(t_p[n]) = i_p[n]$ from Definition 3.

From (33), the state at the $(n+1)$ th turn-OFF time instant is

$$\mathbf{x}(t_p[n]) = \mathbf{B} \mathbf{u}[n] + \mathbf{C} \quad (34)$$

where

$$\mathbf{B} \triangleq \begin{bmatrix} \frac{1}{\phi_{vv}^0(\lambda T_{\text{off}}, 0)} & -\frac{\phi_{vi}^0(\lambda T_{\text{off}}, 0)}{\phi_{vv}^0(\lambda T_{\text{off}}, 0)} \\ 0 & 1 \end{bmatrix}, \quad \mathbf{C} \triangleq \begin{bmatrix} -\frac{\gamma_{gv}^0(\lambda T_{\text{off}}, 0)}{\phi_{vv}^0(\lambda T_{\text{off}}, 0)} \\ 0 \end{bmatrix}.$$

Because $\phi_{vv}(t, 0) \neq 0$ for all $t > 0$ from property 3 of class Σ power converters, \mathbf{B} is an invertible matrix.

Any CT state during the OFF-time of the $(n+1)$ th switching cycle is determined by (31) and (34). The state at the $(n+1)$ th turn-ON time instant of S_1 can be reconstructed by

$$\mathbf{x}(t_p[n] + T_{\text{off}}) = \Phi_0(T_{\text{off}}, 0) \mathbf{x}(t_p[n]) + \Gamma_0(T_{\text{off}}, 0). \quad (35)$$

Based on property 5 and property 6 of class Σ power converters, $t_{\text{on}}[n+1]$ can be expressed as

$$\begin{aligned} t_{\text{on}}[n+1] &= (i_p[n+1] - i_p[n] + m_2 T_{\text{off}})/m_1 \\ &= \mathbf{E} \mathbf{u}[n+1] + \mathbf{F} \mathbf{u}[n] + T_{\text{off}} \end{aligned} \quad (36)$$

where

$$\mathbf{E} = \begin{bmatrix} 0 & L/V_{\text{in}} \end{bmatrix}, \quad \mathbf{F} = \begin{bmatrix} T_{\text{off}}/V_{\text{in}} & -L/V_{\text{in}} \end{bmatrix}. \quad (37)$$

Any CT state during the ON-time of the $(n+1)$ th switching cycle can be determined from (32), (35), and (36). A mapping \mathbf{A} from $\{\mathbf{u}[n]\}$ to $\mathbf{x}(t)$ can be explicitly constructed as

$$\begin{aligned} \mathbf{A}: \quad (a) \quad & t_{\text{on}}[n+1] = \mathbf{E} \mathbf{u}[n+1] + \mathbf{F} \mathbf{u}[n] + T_{\text{off}}. \\ (b) \quad & \mathbf{x} \left(\tau + \sum_{j=1}^n (T_{\text{off}} + t_{\text{on}}[j]) + t_0 \right) \\ &= \begin{cases} \Phi_0(\tau, 0) \mathbf{B} \mathbf{u}[n] + \Phi_0(\tau, 0) \mathbf{C} + \Gamma_0(\tau, 0) & 0 < \tau \leq T_{\text{off}} \\ \Phi_1(\tau, T_{\text{off}}) \Phi_0(T_{\text{off}}, 0) (\mathbf{B} \mathbf{u}[n] + \mathbf{C}) \\ + \Phi_1(\tau, T_{\text{off}}) \Gamma_0(T_{\text{off}}, 0) + \Gamma_1(\tau, T_{\text{off}}) & T_{\text{off}} < \tau \leq T_{\text{off}} + t_{\text{on}}[n+1]. \end{cases} \end{aligned} \quad (38)$$

To simplify (38)-(b), we define functions \mathbf{D}_{n+1} from $\mathbf{u}[n] \times \tau$ to $x(t)$ as

$$\begin{aligned} \mathbf{D}_{n+1}(\mathbf{u}[n], \tau) &= \mathbf{x} \left(\tau + \sum_{j=1}^n (T_{\text{off}} + t_{\text{on}}[j]) + t_0 \right) \\ & \quad 0 < \tau \leq t_{\text{on}}[n+1]. \end{aligned} \quad (39)$$

We can now show that mapping \mathbf{A} preserves stability. This result is consequential because in $5S$, classical discrete-domain design methods can be applied to controller design.

Definition 5: From [41], the distance from a point \mathbf{x} to a nonempty set γ is

$$\mathbf{dist}(\mathbf{x}, \gamma) \triangleq \inf\{ \|\mathbf{x} - \mathbf{y}\|_2 \mid \mathbf{x} \in \mathbb{R}^n, \mathbf{y} \in \gamma \subseteq \mathbb{R}^n \}.$$

Definition 6: For a system $S_1 \in \mathcal{S}$, a CT state trajectory $\mathbf{x}_e(t)$ is a *least harmonics equilibrium* if there exists a period $T > 0$ such that $\mathbf{x}_e(t+T) = \mathbf{x}_e(t)$ for all $t \geq 0$ and there is only one current peak during the period T .³

Definition 7: $\mathbf{x}_e(t)$ is an equilibrium of system $S_1 \in \mathcal{S}$. Assume $\mathbf{x}_e(t)$ is perturbed at t_b and the perturbed trajectory is $\mathbf{x}(t)$. $t_1 \geq t_b$ and $t_2 \geq t_b$ occur at the current peaks of $\mathbf{x}(t)$ and $\mathbf{x}_e(t)$, respectively. $\mathbf{x}_e(t)$ is a *synchronously asymptotically stable least harmonics equilibrium* of S if there exists a $\delta > 0$ such that if $\|\mathbf{x}(t_1) - \mathbf{x}_e(t_2)\|_2 < \delta$, then $\lim_{t \rightarrow +\infty} \mathbf{dist}(\mathbf{x}, \mathbf{x}_e(t)) = 0$.

Theorem 1: For a system $S_1 \in \mathcal{S}$, if a discrete state in a switching-synchronized sampled-state space representation \mathbf{u}_e is an asymptotically stable equilibrium in the sense of Lyapunov

³In this article, unless specially mentioned, the equilibrium means least harmonics equilibrium.

(ISL) and if we construct a sequence $\{\mathbf{u}_e[n]\}$ with $\mathbf{u}_e[n] = \mathbf{u}_e = [V_e, I_e]$, $\forall n \geq 0$, then the corresponding CT state trajectory $\mathbf{x}_e(t) \triangleq \mathbf{A}(\{\mathbf{u}_e[n]\})$ is a stable equilibrium in the sense of Definition 7.

Proof: We denote the induced 2-norm [42] for matrix \mathbf{Z} by $\|\mathbf{Z}\|_M \triangleq \sup_{\mathbf{x} \neq \mathbf{0}} \frac{\|\mathbf{Z}\mathbf{x}\|_2}{\|\mathbf{x}\|_2}$.

1) We show $\mathbf{x}_e(t)$ is an equilibrium. From (36), $t_{\text{on}}^e \triangleq ((v_e - V_{\text{in}})/V_{\text{in}})T_{\text{off}} = t_{\text{on}}[n+1]$ for all $n \geq 0$. Let $T = t_{\text{on}}^e + T_{\text{off}}$. From (38) and (39), given any $n \geq 0$

$$\begin{aligned} \mathbf{x}_e(\tau + nT + t_0) &= \mathbf{D}_{n+1}(\mathbf{u}[n], \tau) \\ &= \mathbf{D}_1(\mathbf{u}[0] = \mathbf{u}_e, \tau) = \mathbf{x}_e(\tau + t_0) \end{aligned} \quad (40)$$

where $0 < \tau \leq T$. Therefore, $\mathbf{x}(t+T) = \mathbf{x}(t)$, $\forall t \geq t_0$, where t_0 is from Definition 4. Because there is only one peak current during each T period, $\mathbf{x}_e(t)$ is an equilibrium.

2) We show that $\mathbf{x}_e(t)$ is an asymptotically stable equilibrium. Because \mathbf{u}_e is an asymptotically stable equilibrium ISL, $\exists \delta_1 > 0$ such that if $\|\mathbf{u}[0] - \mathbf{u}_e\|_2 < \delta_1$, then $\lim_{n \rightarrow +\infty} \mathbf{u}[n] = \mathbf{u}_e$, where $\{\mathbf{u}[n]\}$ is the corresponding class V trajectory after the perturbation. The corresponding class W trajectory is $\mathbf{x}(t) = \mathbf{A}(\{\mathbf{u}[n]\})$. For any perturbation on $\mathbf{x}_e(t)$ at $t = t_b$, $t_1 = t_p[0] \geq t_b$ at a current peak of $x(t)$ and $t_2 = t_p^e[0] \geq t^b$ at a current peak of $x_e(t)$ are both at discrete state space points.

$$\begin{aligned} \|\mathbf{x}(t_1) - \mathbf{x}_e(t_2)\|_2 \\ = \|\mathbf{B}(\mathbf{u}[0] - \mathbf{u}_e)\|_2 \leq \|\mathbf{B}\|_M \|\delta_1\|_2. \end{aligned} \quad (41)$$

We show that if $x(t_1)$ lies in the δ_2 neighborhood of $x_e(t)$ where $\delta_2 = \|\mathbf{B}\|_M \|\delta_1\|_2$, then given any $\epsilon_1 > 0$, there exists a $t_c > \max\{t_1, t_2\}$ such that $\text{dist}(\mathbf{x}, \mathbf{x}_e(t)) \leq \epsilon_1$ for all $t \geq t_c$.

Because every entry of $\Phi_1(t, 0)$, $\Phi_1'(t, 0)$ and $\Gamma_1'(t, 0)$ are continuous functions of t , from [42, Th. 2.5.4], $\|\Phi_1(t, 0)\|_M$, $\|\Phi_1'(t, 0)\|_M$, and $\|\Gamma_1'(t, 0)\|_2$ are continuous functions of t .

From the Weierstrass theorem in [42], in the closed interval $[0, 2t_{\text{on}}^e]$, there exists M_1, L_1 , and L_2 such that

$$\begin{aligned} \|\Phi_1(t, 0)\|_M &\leq M_1, \quad \|\Phi_1'(t, 0)\|_M \leq L_1, \\ \|\Gamma_1'(t, 0)\|_2 &\leq L_2. \end{aligned} \quad (42)$$

Given any $\epsilon_1 > 0$, $\exists N_1 \quad \forall n \geq N_1$ such that

$$\|\mathbf{u}[n] - \mathbf{u}_e\|_2 \leq \min \left\{ \frac{\epsilon_1}{2M_1 \|\Phi_0(T_{\text{off}}, 0)\mathbf{B}\|_M}, \frac{V_{\text{in}}}{2L + T_{\text{off}}} t_{\text{on}}^e, \frac{m_1 \epsilon_1}{2L_1(a_0 + a_1 + a_2) + L_2} \right\} \quad (43)$$

where $a_0 = \|\Phi_0(T_{\text{off}}, 0)\mathbf{B}\|_M (\|\mathbf{u}_e\|_2 + \delta_1)$, $a_1 = \|\Phi_0(T_{\text{off}}, 0)\mathbf{C}\|_2$ and $a_2 = \|\Gamma_0(T_{\text{off}}, 0)\|_2$.

Given any $t > \sum_{j=1}^{N_1} (T_{\text{off}} + t_{\text{on}}[j])$, there exists $N_2 \geq N_1$ such that $\sum_{j=1}^{N_2} (T_{\text{off}} + t_{\text{on}}[j]) < t \leq \sum_{j=1}^{N_2+1} (T_{\text{off}} + t_{\text{on}}[j])$. Let $\tau = t - \sum_{j=1}^{N_2} (T_{\text{off}} + t_{\text{on}}[j])$ and then $0 < \tau \leq T_{\text{off}} + t_{\text{on}}[N_2 + 1]$.

$t_{\text{on}}[N_2 + 1]$ is bounded in the closed interval $[0, 2t_{\text{on}}^e]$ because

$$\left| t_{\text{on}}[N_2 + 1] - t_{\text{on}}^e \right|$$

$$\begin{aligned} &\leq \left| \frac{i_p[N_2 + 1] - i_p[N_2]}{m_1} \right| + \left| \left(\frac{v_{\text{out}}[N_2] - V_e}{m_1 L} \right) T_{\text{off}} \right| \\ &\leq \frac{L}{V_{\text{in}}} \|\mathbf{u}[N_2 + 1] - \mathbf{u}_e\|_2 + \frac{L}{V_{\text{in}}} \|\mathbf{u}[N_2] - \mathbf{u}_e\|_2 \\ &\quad + \frac{T_{\text{off}}}{V_{\text{in}}} \|\mathbf{u}[N_2] - \mathbf{u}_e\|_2 \leq t_{\text{on}}^e. \end{aligned} \quad (44)$$

If $\tau \leq T$, then

$$\begin{aligned} \text{dist}(\mathbf{x}, \mathbf{x}_e(t)) &\leq \|\Phi_1(\tau, T_{\text{off}})\Phi_0(T_{\text{off}}, 0)\mathbf{B}(\mathbf{u}[N_2] - \mathbf{u}_e)\|_2 \\ &\leq M_1 \|\Phi_0(T_{\text{off}}, 0)\mathbf{B}\|_M \|\mathbf{u}[N_2] - \mathbf{u}_e\|_2 < \epsilon_1. \end{aligned} \quad (45)$$

If $\tau > T$, then

$$\begin{aligned} \text{dist}(\mathbf{x}, \mathbf{x}_e(t)) &\leq \|\Phi_1(T, T_{\text{off}})\Phi_0(T_{\text{off}}, 0)\mathbf{B}(\mathbf{u}[N_2] - \mathbf{u}_e) \\ &\quad + (\Phi_1(\tau, T_{\text{off}}) - \Phi_1(T, T_{\text{off}}))\Phi_0(T_{\text{off}}, 0)(\mathbf{B}\mathbf{u}[N_2] + \mathbf{C}) \\ &\quad + (\Phi_1(\tau, T_{\text{off}}) - \Phi_1(T, T_{\text{off}}))\Gamma_0(T_{\text{off}}, 0) \\ &\quad + \Gamma_1(\tau, T_{\text{off}}) - \Gamma_1(T, T_{\text{off}})\|_2. \end{aligned} \quad (46)$$

From the mean value theorem in [43]

$$\begin{aligned} \|\Phi_1(\tau, T_{\text{off}}) - \Phi_1(T, T_{\text{off}})\|_M &\leq L_1|\tau - T| \\ \|\Gamma_1(\tau, T_{\text{off}}) - \Gamma_1(T, T_{\text{off}})\|_2 &\leq L_2|\tau - T|. \end{aligned} \quad (47)$$

From (46) and (47)

$$\begin{aligned} \text{dist}(\mathbf{x}, \mathbf{x}_e(t)) &\leq M_1 \|\Phi_0(T_{\text{off}}, 0)\mathbf{B}\|_M \|\mathbf{u}[N_2] - \mathbf{u}_e\|_2 \\ &\quad + (\tau - T)L_1 \|\Phi_0(T_{\text{off}}, 0)\mathbf{B}\|_M (\|\mathbf{u}_e\|_2 + \delta_1) \\ &\quad + (\tau - T)L_1 \|\Phi_0(T_{\text{off}}, 0)\mathbf{C}\|_2 \\ &\quad + (\tau - T)L_1 \|\Gamma_0(T_{\text{off}}, 0)\|_2 + (\tau - T)L_2 \leq \epsilon_1. \end{aligned} \quad (48)$$

Hence, we proved that for any $\epsilon_1 > 0$, there exists a $t_c = \sum_{j=1}^{N_1} (T_{\text{off}} + t_{\text{on}}[j])$ such that $\text{dist}(\mathbf{x}, \mathbf{x}_e(t)) \leq \epsilon_1$ for all $t \geq t_c$. This implies $\lim_{t \rightarrow +\infty} \text{dist}(\mathbf{x}, \mathbf{x}_e(t)) = 0$.

In all, we proved that for $\mathbf{x}_e(t)$, $\exists \delta_2$, such that if the perturbation on $\mathbf{x}_e(t)$ at t_b results in $\|\mathbf{x}(t_1) - \mathbf{x}(t_2)\|_2 < \delta_2$, then $\lim_{t \rightarrow +\infty} \text{dist}(\mathbf{x}, \mathbf{x}_e(t)) = 0$.

From Definition 7, the CT state trajectory $\mathbf{x}_e(t)$ is an asymptotically stable least harmonics equilibrium of \mathcal{S} . ■

The stability criterion in 5S is identical to the classical discrete-time system stability theory. From root locus or Nyquist [32] stability criteria, we can provide a sufficient and necessary condition for a compensated discrete linear system: all closed-loop poles are inside the open unit disk.

APPENDIX B TRANSIENT RESPONSE

Because of the nonuniform sampling, the settling steps and settling time are not proportional as illustrated in Fig. 7(a). We mathematically proved that the optimization on the settling steps in the 5S representation is equivalent to the optimization on the worst-case settling time in the physical state space.

Theorem 2: Given a system $\mathcal{S}_1 \in \mathcal{S}$ and \mathbf{u}_e is an asymptotically stable equilibrium ISL. Given a system $\mathcal{S}_1 \in \mathcal{S}$ in the reference output voltage step command $V_{e1} \rightarrow V_{e2}$, the settling

time T_t is bounded by the following functions of the settling cycles N_t :

$$T_t \leq \rho N_t + \gamma \quad (49)$$

where

$$\rho(\sigma_d^v) = \frac{V_{e1}}{V_{in}} T_{off} + \frac{V_{e2} - V_{e1}}{V_{in}} T_{off} \sigma_d^v \quad (50)$$

$$\gamma = \frac{L}{V_{in}} (I_{e2} - I_{e1}). \quad (51)$$

Proof: Assume $\mathbf{u}_e = [V_e \quad I_e]$ and the initial state is $\mathbf{u}[0] = [V_0, I_0]$

$$T_t = \sum_{k=0}^{N_t-1} (T_{off} + t_{on}[k+1]). \quad (52)$$

Based on property 5 and property 6 of a class Σ power converters

$$\frac{V_{in}}{L} t_{on}[n] - \frac{v[n] - V_{in}}{L} T_{off} = i_p[n] - i_p[n-1]. \quad (53)$$

Summing up both sides of (53) for $n = 1$ to $n = N_t$ results in

$$\frac{V_{in}}{L} (T_t - N_t T_{off}) - \frac{\sum_{k=1}^{N_t} v[k] - N_t V_{in}}{L} T_{off} = I_{e2} - I_{e1}. \quad (54)$$

From (27)

$$\sum_{k=1}^{N_t} v[k] \leq N_t V_{e1} + \sigma_d^v N_t (V_{e2} - V_{e1}). \quad (55)$$

Substituting (55) into (54) yields

$$\begin{aligned} T_t &\leq \frac{L}{V_{in}} (I_{e2} - I_{e1}) + T_{off} N_s + \frac{V_{e1} - V_{in}}{V_{in}} T_{off} N_s \\ &\quad + \sigma_d^v \frac{V_{e2} - V_{e1}}{V_{in}} T_{off} N_s \\ &= \left(\frac{V_{e1}}{V_{in}} T_{off} + \frac{V_{e2} - V_{e1}}{V_{in}} T_{off} \sigma_d^v \right) N_s + \frac{L}{V_{in}} (I_{e2} - I_{e1}). \end{aligned} \quad (56)$$

Because of the discretization, the overshoot in 5S is smaller than that in CT as illustrated in Fig. 7(b). We mathematically proved that the *overshoot* in the physical time is bounded from the top by a linear function of the *overshoot* in 5S.

Theorem 3: Given a system $\mathcal{S}_1 \in \mathcal{S}$ in a reference output voltage step command $V_{e1} \rightarrow V_{e2}$, the overshoot in CT σ_t^v is bounded by the following functions of the overshoot in 5S σ_d^v :

$$\sigma_t^v \leq (1 - (1 - \lambda)\alpha)\sigma_d^v + (1 - \lambda)\alpha\sigma_d^i \quad (57)$$

where $\alpha = T_{off}/RC$.

Proof: From (27) and (29), $\sigma_d^v \leq \sigma_t^v$. We want to bound σ_t^v from above. Let $t_m = \operatorname{argmax} v(t)$, $N = \operatorname{argmax} v[n]$, and $K = \operatorname{argmax} i_p[n]$. Assume t_m is in the M th switching cycle. Let $\tau = t - t_p[M-1]$ and $\alpha_c = (1 - \lambda)T_{off}/RC$. In time interval $0 < \tau \leq T_{off}$, the capacitor voltage $v(\tau)$ increases with τ . The charging current is the difference between charge injected by the current source and charge drained by the load. During the

interval $T_{off} < \tau \leq T_{off} + t_{on}[M]$, the capacitor is discharging to the load; therefore, the capacitor voltage $v(\tau)$ decreases with τ . Let $i_c(t)$ be capacitor current, then the maximum $v(t)$ is bounded by

$$\begin{aligned} v(t_m) &= v[M] + \int_{\lambda T_{off}}^{T_{off}} \frac{i_c(\tau)}{C} d\tau \\ &\leq v[M] + \int_{\lambda T_{off}}^{T_{off}} \frac{1}{C} \left(i_L(\tau) - \frac{v[M]}{R} \right) d\tau \\ &\leq (1 - \alpha_c) v[N] + \frac{1}{C} \int_{\lambda T_{off}}^{T_{off}} i_L(\tau) d\tau \\ &\leq (1 - \alpha_c) v[N] + (i_p[K] - I_{e1})\alpha_c R + I_{e1}\alpha_c R. \end{aligned} \quad (58)$$

From (28)

$$i_p[K] - I_{e1} = (\sigma_d^i + 1)(I_{e2} - I_{e1}) = (\sigma_d^i + 1) \frac{V_{e2} - V_{e1}}{R} \quad (59)$$

$$V_{e1} = I_{e1} R. \quad (60)$$

Substitute (59) and (60) into (58) yields

$$\begin{aligned} v(t_m) - V_{e1} &\leq (1 - \alpha_c) (v[N] - V_{e1}) + (\sigma_d^i + 1)(V_{e2} - V_{e1})\alpha_c. \end{aligned} \quad (61)$$

Substitute (27) and (29) into (61)

$$\sigma_t^v \leq (1 - \alpha_c)\sigma_d^v + \alpha_c\sigma_d^i. \quad (62)$$

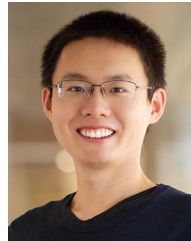
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