# Difference Between the PWM and Standard DC Power Cycling Tests Based on the Finite-Element Simulation

Luhong Xie, Lixin Wu, Erping Deng, *Member, IEEE*, Ying Zhang, Yushan Zhao, and Yongzhang Huang

***Abstract*—Pulsewidth modulation (PWM) power cycling, which has complex control strategies and high testing costs, received a lot of attention in recent years because the test conditions are closer to the application of power modules than standard DC power cycling. Therefore, the root difference of the failure modes and lifetime of insulated gate bipolar transistor power modules between DC and PWM power cycling is the concern in this article, based on the finite-element simulation. For stimulating the PWM power cycling with high accuracy and fast speed, an improved PWM (IPWM) power cycling is proposed and verified by a simple model. Then, an electrothermomechanical coupled model of a single chip is established for comparison. It mainly focuses on the current distribution, temperature distribution, and stress distribution. The current distribution comparison results show no difference, while a higher temperature gradient is shown in PWM power cycling due to the additional switching losses. However, the stress distribution results show chip solder layer is still the main failure mechanism both in DC and IPWM power cycling. Therefore, a conclusion can be obtained that there is no difference in failure mechanism and lifetime between DC and PWM power cycling. And the same bond wire failure and similar lifetime of DC and PWM power cycling tests further verify this conclusion.**

***Index Terms*—DC power cycling, electrothermal coupled model, insulated gate bipolar transistor (IGBT) power modules, pulsewidth modulation (PWM) power cycling.**

## I. Introduction

As THE core component of power conversion equipment and driver equipment, power modules like insulated gate bipolar transistors (IGBTs) are widely used in the driver system of new energy power conversion, rail traffic, and electric vehicles. Due to the poor working conditions, the failure of IGBTs is the main reason for the failure of the entire conversion system [1]. Therefore, it is crucial to improve the reliability of IGBT power modules. In this case, IGBT manufacturers and users need to comprehensively understand the failure mechanisms of IGBT power modules with accelerated aging tests and make improvements to their packaging structure [2].

Under this motivation, DC power cycling test (DC PCT) was first proposed by [3] many decades before. International Electrotechnical Commission (IEC) standard (IEC 60749-34:2010) [4] and European Center for Power Electronics standard (AQG324: 2018) [5] specify the test principles of DC PCT, which belongs to the accelerated aging experiments. IGBT power modules are always conducted and loaded with periodic current to generate a cyclic temperature, which accelerates the aging of the module. However, in real applications, pulsewidth modulation (PWM) is generally used to control the gate of the IGBT to control its switching state [6]. In this case, the IGBT module is actively switched by itself, therefore not only conduction losses but also switching losses are generated during switching process. Besides, blocking voltage will load on IGBT module when the module is switched OFF as a high-voltage source is normally used in real applications, which is not the case in the standard DC PCT as current source is normally used.

The PWM PCT was therefore proposed in [7] whose testing conditions are closer to the real application conditions and get considerable attention in recent years [8]. However, whether PWM PCT is more suitable to assess the reliability of the module than DC PCT is still a controversial issue. Many researchers have done the corresponding studies to compare DC and PWM PCT with the experience results [9], [10], [11]. As the switching behavior is the main difference, the static parameters like threshold voltage $V_{\mathrm{GEth}}$ and gate-emitter leakage current $I_{\mathrm{GES}}$ or dynamic performances like switching-ON and switching-OFF waveforms are measured during the PWM PCT based on IGBTs in literature [12], the slight differences of the parameters prove that the gate oxide layer is not affected. Similar works have been done for SiC MOSFET in the PFC converter in literature [13], and a significant decrease in $V_{\mathrm{GEth}}$ was observed. But in DC PCT, the threshold voltage of SiC MOSFET showed a continuously increasing trend [14], [15]. The change of the $V_{\mathrm{GEth}}$ means the aging of the gate oxide of SiC MOSFET due to the presence of gate oxide traps, which would directly affect the thermal stress, thereby accelerating package degradation. Therefore, the comparison between DC and PWM PCT of SiC devices needs to be discussed

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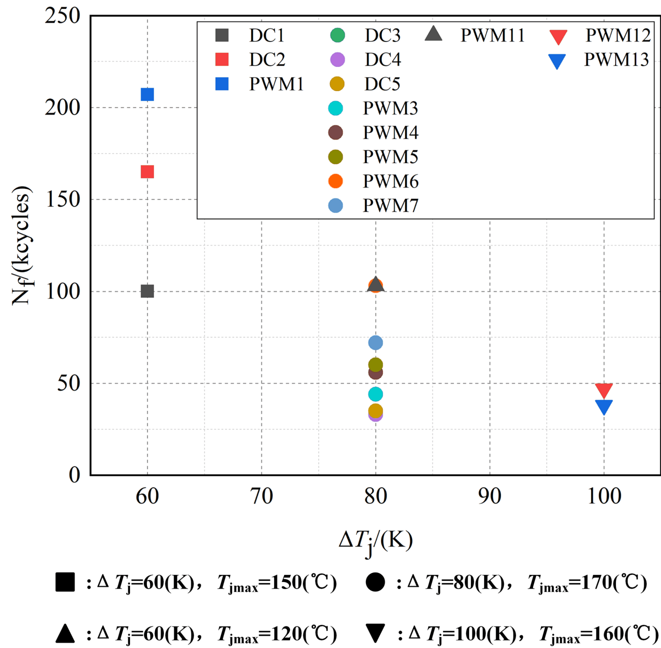


Fig. 1. Lifetime of the power modules in DC and PWM power cycling with different test conditions [9].

separately, which is not covered in this article but summarized in literature [16].

For IGBT power modules, our previous article has systematically compared and summarized the differences between DC and PWM PCTs in literature [17] from four aspects with published literatures: the test principles, junction temperature measurement methods, failure mechanisms, and lifetime. It was found that there has no influence on the failure modes, and even on the power cycling lifetime as shown in Fig. 1. The data presented in Fig. 1 are all extracted from literature [9]. It can be concluded that under the same test conditions, the lifetimes of DC power cycling are slightly lower than that of PWM power cycling. They can be considered almost the same if the difference of the junction temperature measurement is considered. In DC power cycling, $V_{\mathrm{CE}}(T)$ [18] method is used, which measures the average junction temperature of the chip surface. While the thermocouple is used in PWM power cycling which measures the maximum temperature of the chip surface at a point. Therefore, the real junction temperature in PWM power cycling is lower than that of DC power cycling, resulting in the lifetime of PWM is higher than DC power cycling.

Above all, it can be deemed that there is not much difference in terms of failure mechanisms and lifetime when comparing the power modules tested under DC PCT and PWM PCT. The experiment results of DC PCT and PWM PCT also verified this conclusion, which is shown in Section VI in detail. Furthermore, $V_{\mathrm{CE}}(T)$ method is used to measure the junction temperature in both DC and PWM PCT by different control strategies, avoiding the error due to the different measurement methods. But the differences in test principles are considerable between DC PCT and PWM PCT, mainly reflected in three aspects: the switching state, the source of the power losses, and the high voltage, which are summarized in Section II. The modules tested in DC PCT and PWM PCT are subjected to so great different test conditions but acted with the same performance. To understand this confusing phenomenon comprehensively, this article is devoted to explaining the failure mechanism of power modules under different PCTs from the perspective of finite-element (FE) simulation which has not been studied.

In the first, the test principles of standard DC PCT and normal PWM PCT are introduced to master the fundamental differences between them, which provides the references of the boundary condition settings in FE simulation for getting closer to the real test conditions. Then, a single chip model is established in Section III with eight-paralleled bond wires. On account of the great difficulties of PWM power cycling simulation, an IPWM (improved PWM) power cycling is therefore proposed in Section IV, which effectively reduces calculation memory and shortens simulation time while the PWM power cycling is equivalent. Its effectiveness is verified at the same time. In Section V, the differences in the current distribution of the paralleled bond wires and the temperature distribution of the chip surface between the two power cycling methods are analyzed by FE simulation, which can reflect the different thermal characteristics between DC and PWM power cycling while experiences cannot. And the thermal stress distribution visually shows the weak point of the module under different power cycling. Finally, standard DC PCT and PWM PCT, which have an improved test circuit for better using $V_{\mathrm{CE}}(T)$ method to measure junction temperature, are carried out with the same test temperature conditions of $\Delta T_j \approx 90$ K, $T_{j\max} \approx 150$ °C based on discrete devices with TO247 package. The results show that all device under test (DUTs) fail with bond wire and their lifetimes are close, which is consistent with the conclusion in the introduction.

## II. Test Principles and Differences

### A. DC Power Cycling Test

Fig. 2(a) shows the basic test circuit of DC PCT [19] and Fig. 2(b) shows the waveform diagram of currents and temperatures (junction temperature and heatsink temperature). During DC PCT, the IGBT module under test is mounted on a heatsink with a positive voltage in the gate to make the IGBT always be conducted. The IGBT module is heated up by a DC constant current, When the chip reaches the desired maximum junction temperature $T_{j\max}$, the load current $I_{\mathrm{load}}$ is switched OFF, controlled by switch $S$, then the chip is cooled down to the minimum junction temperature $T_{j\min}$ with an external cooling system. The load current will be switched ON again and the cycle is repeated. In the test circuit, there is another current source that provides measurement current to measure the junction temperature using the $V_{\mathrm{CE}}(T)$ method [18]. Generally, the measurement current $I_m$ should be small enough with $I_m \approx 0.001 * I_{\mathrm{load}}$ to create negligible power losses, and large enough to establish a stable voltage drop. A total of 100 mA is used in this article in DC PCT as well as in PWM PCT.

As the test IGBT module is always conducted during the power cycling and the load current is controlled by auxiliary switch $S$, the waveform of the current is a typical periodic pulse

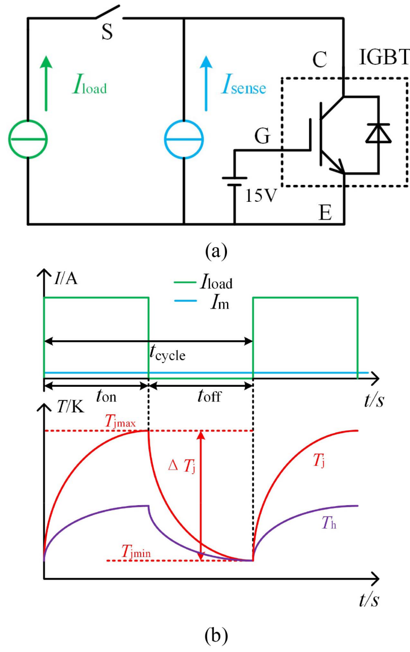


Fig. 2. Schematic diagram of DC power cycling test. (a) Structure of the test circuit. (b) Waveform of current and temperature.

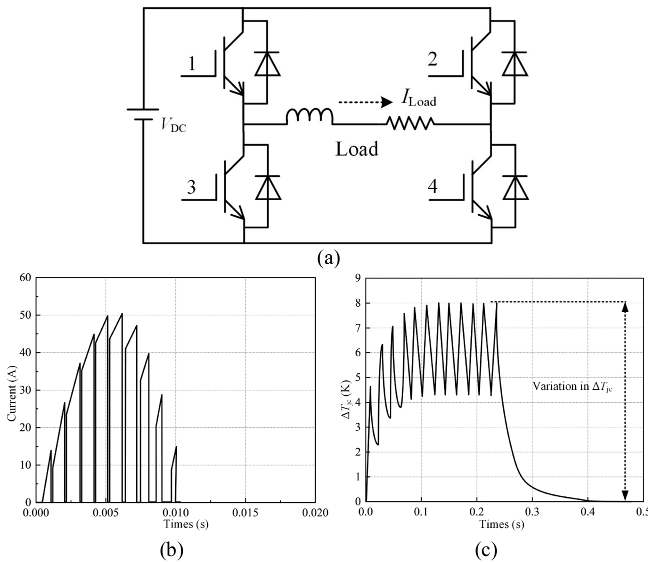


Fig. 3. Normal schematic diagram of PWM PCT. (a) Structure of the test circuit. (b) Waveform of current for one 20 ms load current cycle. (c) Waveform of temperature swing for $t_{\mathrm{ON}} = t_{\mathrm{OFF}} = 240$ ms [22].

wave. The losses are therefore generated during the conduction state. No high voltage is applied as the DUT is not actively switched and also no switching losses either.

## B. PWM Power Cycling Test

As PWM PCT refers to the actual application circuit, there are many circuit topologies based on different application occasions [7], [20], [21]. Take the normally used PWM PCT test circuit shown in Fig. 3(a) [22] as an example to analyze some typical

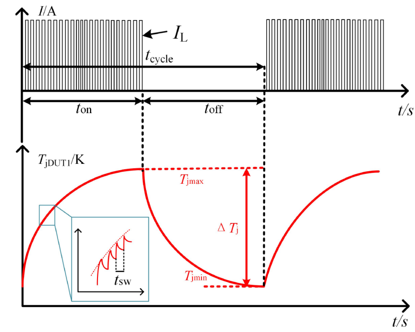


Fig. 4. Waveform of the current injected into the PWM power cycling simulation and the obtained temperature profiles.

features, which are used as a reference for the input of the simulation. This circuit is a typical two-phase full-bridge inverter circuit with a resistive-inductive load. The PWM wave is used as the IGBT gate driver signal, which is obtained by the PWM method detailed described in [23]. Fig. 3(b) and (c), respectively, show the current waveform in one switching cycle and the temperature waveform in one output cycle [22]. It can be seen that the current waveform of normal PWM power cycling is more complex than that of DC power cycling. And the junction temperature rises in a sawtooth waveform. That means DUTs will suffer several small temperature swings during the heating time, which may have an influence on the failure mechanism and lifetime of DUTs. In order to obtain the same junction temperature in FE simulation, a series of current pulses with PWM waveform with switching frequency $f_{\mathrm{sw}}$ during the heating time $t_{\mathrm{ON}}$ are applied in the electrothermo coupling model, as shown in Fig. 4. Noting that the current waveform is different with the normal PWM PCT, which is used especially in this article to obtained the same temperature profile, considering that temperature is the most important factor affecting the lifetime of DUTs [24].

As the DUTs are actively switched, the switching losses are thereby generated during the switch between the ON and OFF states. Therefore, in PWM power cycling, the switching losses should also be considered in simulation as additional power losses.

Besides, a reduction of thermal resistance of IGBT power modules is another one worth noting due to the application of high frequency, which will lower the junction temperature. Therefore, the test setting parameters of PWM PCT should be adjusted first to ensure the expected test temperature can be reached.

To sum up, the differences between DC and PWM PCTs can be summarized as follows:

1) The DUTs have different switch states. The DUTs are always conducted during DC PCT while that of PWM PCT are switched ON and OFF following the PWM signal. Different switching states result in different current forms and power losses.
2) The DUTs have different power losses. In DC PCT, there are only conduction losses because the DUTs have no

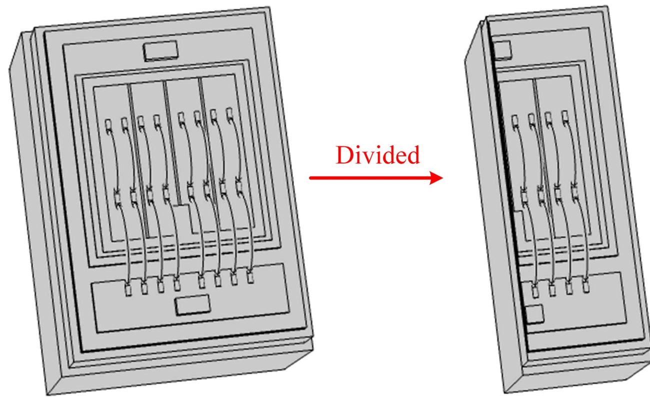


Fig. 5. Single-chip model.

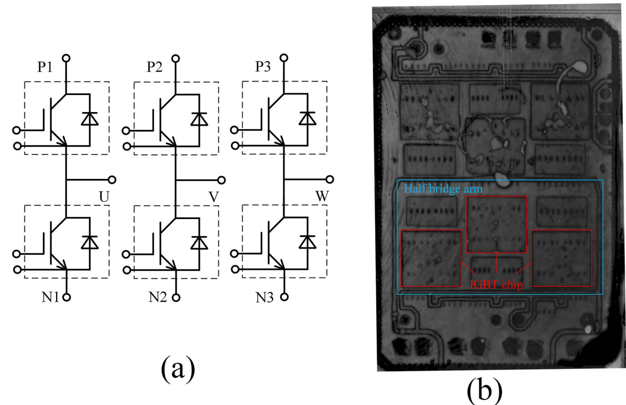


Fig. 6. 750 V/600 A IGBT power module. (a) Internal equivalent circuit of the reference module. (b) SAM picture of one of the phase bridges.

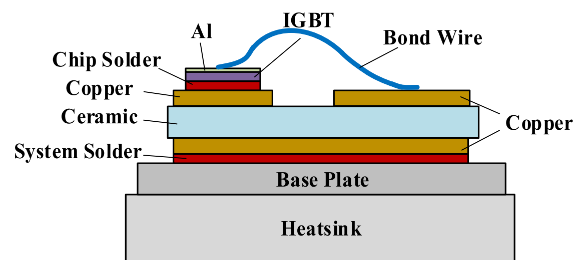


Fig. 7. Cross-sectional view of the single chip model.

switching behavior, whereas the DUTs have both switching losses and conduction losses in PWM PCT, and the switching losses can be easily controlled with the switching frequency $f_{\text{sw}}$.

3) The DUTs are subject to the high voltage or not. DUTs should withstand the high voltage when switched OFF in PWM PCT, which is not the case in DC PCT.

As for the influence of the high voltage, it is always been studied in high-voltage high humidity high temperature reverse bias [25] test, which mainly focuses on the reliability of the chip, especially the terminal area. In addition, it has also been found that high voltage will cause the moving of ions in the package and result in partial discharges [26]. Therefore, the insulation reliability of the package also needs to be considered in high-voltage applications of the power modules. Four nonstandard tests are summarized in literature [27] to investigate the insulation reliability of the package under huge electrical stress, and a novel approach is proposed to assess the high-voltage slope *dV/dt*, which is common in PWM-based applications. However, packaging degradation due to high voltage is uncommon in PCTs. Furthermore, the experiment results of PWM PCT indicate no other failure mechanisms that occur which may be caused by high voltage, except bond wire failure in this article. Therefore, the difference in the high voltage between the DC PCT and PWM PCT is not considered in this article.

TABLE I
MATERIAL AND GEOMETRIC PARAMETERS OF EACH LAYER

| Item | Material | Thickness(mm) |
|---|---|---|
| Bond wire | Aluminum | 0.3 |
| Metallization layer | Aluminum | 0.005 |
| IGBT chip | Silicon | 0.07 |
| Chip solder | 60Sn40Pb | 0.1 |
| Copper up | Copper | 0.3 |
| Ceramic | Al2O3 | 0.381 |
| Copper down | Copper | 0.3 |
| System solder | 60Sn40Pb | 0.1 |
| Base plate | Copper | 3 |
| Heatsink | Aluminum | 10 |

## III. Finite-Element Simulation

### A. Finite-Element Model

As shown in Fig. 5, a single chip model, simplified from a 750 V/600 A IGBT full-bridge module, is established. The internal equivalent circuit of the 750 V/600 A IGBT power module is shown in Fig. 6(a), which is used in electric vehicles especially. The SAM picture of one of the phase bridges is shown in Fig. 6(b). Therefore, the rated current and voltage of the single chip model can be obtained, as well as geometric parameters. The simplified model contains one IGBT chip and eight bond wires with diameter of 300 $\mu$m. The spacing of each bond wire is 1 mm. Between the bond wire and IGBT chip surface, there is an aluminum metallization layer with thickness of 5 $\mu$m. Below the chip, there are chip solder layer, direct bond copper, system solder layer, substrate, and heatsink. In order to facilitate the setting of boundary conditions, two small rectangular copper are added on the upper copper board as collector terminals and emitter terminals. Fig. 7 shows the cross-sectional view of the single-chip model, and the material and geometric parameters of each layer structure are given in Table I. In addition, this model is a symmetrical structure. In order to reduce the calculation memory and increase the calculation speed, the model is divided along the central longitudinal axis, and only the right part of the geometry is retained.

After the model is built, the overall model is divided into a number of small elements by meshing. Fig. 8 shows the FE

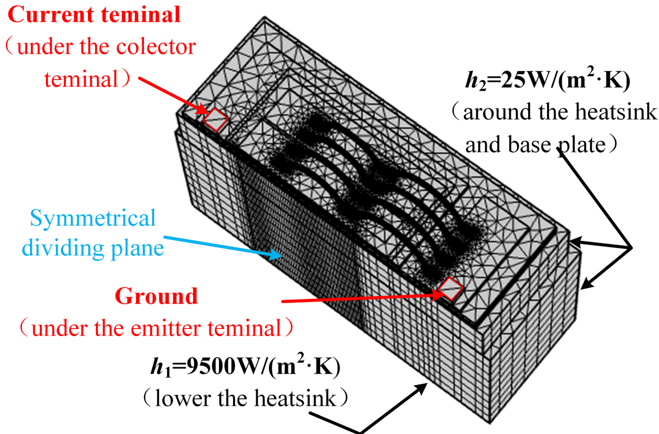


Fig. 8. Finite-element model with half-symmetric layout.

model after meshing. For making the solution more accurate, a finer mesh is made on the bond wire and chip area, and a sweep operation from top to bottom is used to make the simulation closer to the actual thermal dissipation path.

## B. Settings of Electrothermo Coupling Field

The electric field and thermal field are set at the same time and coupled by the Joule heating multiphysics interface to simulate the real power cycling process of the module. As each half-bridge arm of the reference module is composed of three IGBT chips in parallel, the rated current of one chip is only 1/3 of the module.

In the electric field, the current source is applied to the upper surface of the collector terminal in the form of surface current density with $J = 200/2$ (A/mm$^2$), where 200 A is the load current amplitude and 2 mm$^2$ is the area of the upper surface of the collector terminal, while the upper surface of the emitter terminal is set as the ground. The active area of the IGBT chip is considered the heat region and its electrical conductivity is obtained from the measured I-V characteristic, which considers the dependence of temperature. In the thermal field, the heat convection coefficient on the bottom of the heatsink is set to simulate water cooling heat dissipation: $h_1 = 9500$ W/(m$^2$·K); the heat convection coefficient around the heatsink and the substrate are set to simulate the convection heat transfer between the module and the air: $h_2 = 25$ W/(m$^2$·K); the ambient temperature is set with 30°C.

Fig. 9 shows the current waveform applied in simulations. Fig. 9(a) is the periodic rectangular pulse waveform used in DC power cycling with $t_{\text{cycle}} = 0.2$ s and $t_{\text{ON}} = 0.1$ s, while Fig. 9(b) is the PWM waveform used in PWM simulation with $f_{\text{out}} = 5$ Hz and $f_{\text{sw}} = 1$ kHz. In the PWM, the PWM wave is obtained by comparing the amplitude of the sine wave and the triangular wave used as the fundamental wave and the carrier wave [28], respectively. Based on this principle, the sinusoidal wave Sin with frequency $f_{\text{out}}$ and the triangular wave Trian with frequency $f_{\text{sw}}$ are set and then compared as follows: when Sin $\geq$ Trian, output 1; when Sin $<$ Trian, output 0.

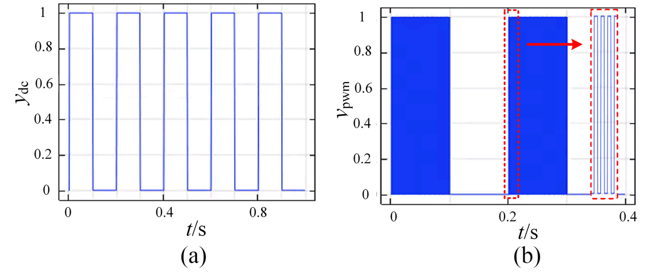


Fig. 9. Current waveform used in FE simulation. (a) Rectangular pulse wave used in DC power cycling. (b) PWM wave used in PWM power cycling.

TABLE II
ANAND PARAMETERS OF THE VISCOPLASTIC MATERIAL MODEL [30]

| Parameters | Value | Description |
|---|---|---|
| $A$(1/s) | 1.4283E8 | pre-exponential factor |
| $Q/R$(K) | 10413.3 | Q: activation energy, R: universal gas constant |
| $\xi$ | 1.472 | stress multiplier |
| $m$ | 0.141446 | strain rate sensitivity of stress |
| $s_0$(MPa) | 20.2976 | coefficient for deformation resistance saturation value |
| $s_{\text{init}}$(MPa) | 1.0665 | initial value of deformation resistance |
| $h_0$(MPa) | 5023.9 | hardening/softening constant |
| $a$ | 1.120371 | strain rate sensitivity of hardening or softening |
| $n$ | 0.032472 | strain rate sensitivity of saturation (deformation resistance) value |

In PWM power cycling, the module is always switching ON and OFF by controlling its gate, so the switching losses $P_{\text{sw}}$ produced during the switching process should be considered. This article uses the losses calculation software Melcosim [29] of Mitsubishi to calculate the switching losses of the half-bridge arm of the module in different switching frequencies. By substituting the data extracted from the module datasheet, the switching losses $P_{\text{sw}}$ could be obtained in different switching frequencies. When the switching frequency $f_{\text{sw}}$ is 1 kHz, the switching loss $P_{\text{sw}}$ is 21.06 W. And when the switching frequency reaches 10 kHz, the switching losses are almost close to the conduction losses. As three chips are paralleled in the referenced power module, $P_{\text{sw}}/3$ is applied as the additional body heat source to the chip active area to simulate the switching losses making the simulation results closer to the actual PWM PCT.

## C. Settings of Mechanical Field

As the temperature results have been obtained, the thermal expansion multiphysics field is used to couple the temperature results to calculate the thermal stress of the model. The materials of all modules use linear elastic material model, except for the bond wire and solder layer. It should be noted that the aluminum bond wire and aluminum metallization layer use the viscoelastic material model, while the solder layers use the viscoplastic material model to stimulate their nonlinear material behavior. And the Anand parameters of the viscoplastic material model are listed in Table II [30].

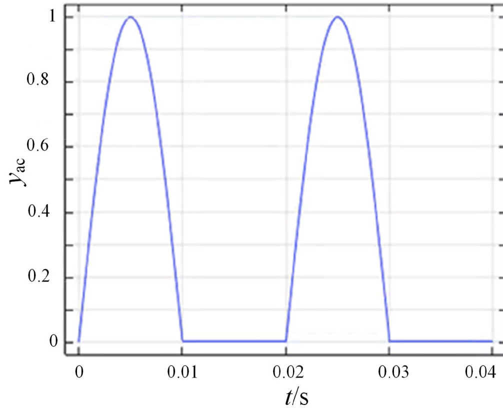


Fig. 10. Sin waveform used in AC power cycling.

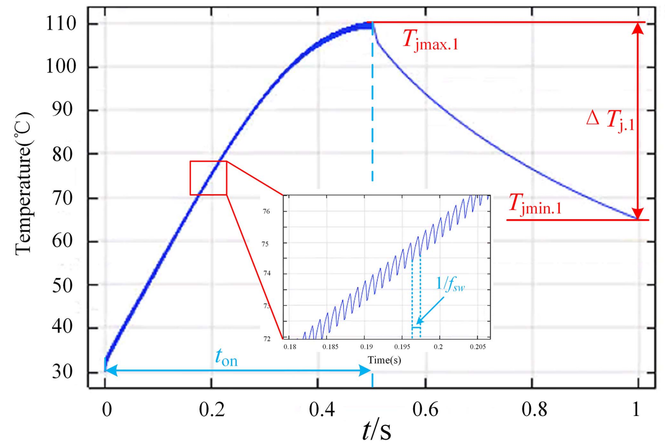


Fig. 11. Temperature result of the first cycle of the PWM power cycling with the conditions in $f_{sw} = 1$ kHz, $t_{ON} = 0.5$ s.

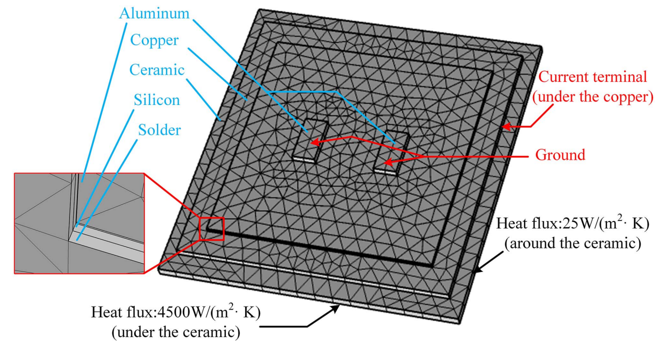


Fig. 12. Simple simulation model and its boundary condition settings.

Besides, fixed constraints must be set on the bottom of the heatsink based on actual application conditions. And the central section needs to be symmetrical, the same as the thermo field.

## IV. IPWM Power Cycling

### A. Equivalent Methods

To obtain the correct result, the calculation step of the PWM power cycling simulation must be small than the switching period. Otherwise, the switching process in PWM power cycling will be lost. Generally, the calculation step is set as step = $1/f_{sw}/10$, and the simulation step in the PWM power cycling is in the range of $10^{-4}$–$10^{-5}$, while the $f_{sw}$ is ranging from 1 to 10 kHz. Such a small step requires a very long simulation time, especially when the thermal constant of the module needs tens of seconds. For example, it takes about 80 h to solve only one cycle with $t_{cycle} = 0.2$ s and $f_{sw} = 1$ kHz in a Dell server with two processors of Gold 5218 CPU and 128G running memory. For the simulation model in this article, the thermal time constant of 24 s is needed to get a stable simulation result. Therefore, 9600 h is required to simulate a PWM power cycling with $t_{cycle} = 0.2$ s and $f_{sw} = 1$ kHz. Obviously, it is impractical to directly perform PWM power cycle simulation.

This article proposes an IPWM power cycling that can shorten the simulation time and reduce calculation memory without losing accuracy while equivalent the normal PWM power cycling. The fundamental principle is to make the temperature swing $\Delta T_j$ and the maximum temperature $T_{jmax}$ of the equivalent power cycling simulation the same as the corresponding PWM power cycling, as the temperature is the main factor causing the failure of the module. The average junction temperature of the chip surface is extracted as the junction temperature in simulations in this article because a large number of experiments and theories prove that the average temperature of the chip surface is closest to the junction temperature measured by $V_{CE}$(T) method [31]. The equivalent steps are described as follows.

According to the area equivalent theorem [32], a sine wave can be used to replace a series of PWM waves. So a sine wave of the load current with the same amplitude and $f_{out}$ is used in power cycling to equivalent PWM wave. Fig. 10 shows a sine wave with $f_{out} = 50$ Hz. However, there is a certain deviation in the temperature results for two different excitations. To reduce the deviation, taking the junction temperature swing $\Delta T_{j.1}$ and maximum junction temperature $T_{jmax.1}$ of the first output cycle of the PWM power cycling as the benchmark as shown in Fig. 11, the current $I$ and ambient temperature $T_a$ are adjusted to make the $\Delta T_{j.1}$ and $T_{jmax.1}$ close to those of the PWM power cycling. When the difference value of the $\Delta T_{j.1}$ and $T_{jmax.1}$ between them are less than 1 °C, it can be considered that this power cycling can be equivalent to the PWM power cycling, which is called IPWM power cycling.

### B. Verification of the Equivalent Method

To verify the effectiveness of the equivalent method, the temperature swing $\Delta T_j$ and the maximum temperature $T_{jmax}$ when the simulation is stable between the IPWM power cycling and corresponding PWM power cycling should be compared.

In this case, a simple model is established and its boundary condition settings are shown in Fig. 12. Then, four simulation setups with various combinations of simulation conditions ($t_{ON}$, $f_{sw}$, $I$) and results are performed as shown in Table III. The temperature swing $\Delta T_j$ and the maximum temperature $T_{jmax}$ are extracted as Fig. 13 shows when the simulation reaches a stable state.

TABLE III
SIMULATION CONDITIONS AND RESULTS OF THE VERIFIED SIMPLE MODEL

| Group | $t_{on}$ (s) | $f_{sw}$ (kHz) | PWM power cycling | | | | | | IPWM power cycling | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Type | $I$(A) | $T_a$(°C) | $\Delta T_j$(K) | $T_{jmax}$(°C) | $t_s$(h) | Type | $I$(A) | $T_a$(°C) | $\Delta T_j$(K) | $T_{jmax}$(°C) | $t_s$(h) |
| 1 | 0.1 | 1 | PWM1 | 180 | 30 | **20.12** | **125.05** | 13.5 | IPWM1 | 200.54 | 39.67 | **20.11** | **125.31** | 0.5 |
| 2 | 0.5 | 1 | PWM2 | 160 | 30 | **54.82** | **125.98** | 15.5 | IPWM2 | 174.55 | 36.24 | **54.55** | **126.03** | 0.5 |
| 3 | 0.5 | 1 | PWM3 | 180 | 30 | **69.39** | **149.24** | 15.5 | IPWM3 | 196.66 | 37.78 | **69.03** | **149.36** | 0.5 |
| 4 | 0.5 | 3 | PWM4 | 180 | 30 | **69.12** | **160.41** | 40.5 | IPWM4 | 196.69 | 37.37 | **68.83** | **160.53** | 0.6 |

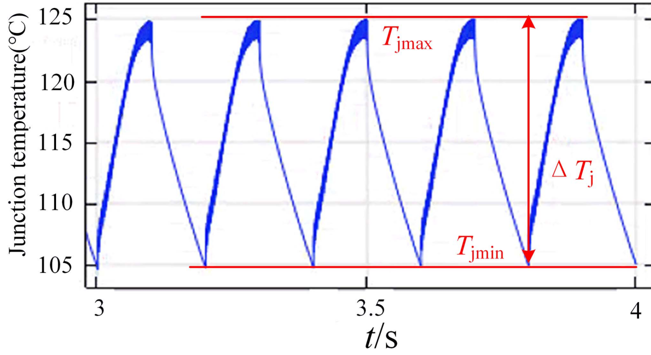


Fig. 13. Temperature result after PWM power cycling simulation is stabilized with the conditions in $f_{\mathrm{sw}} = 1$ kHz and $t_{\mathrm{ON}} = 0.1$ s.

From Table III, it can be seen that $\Delta T_j$ and $T_{j\max}$ of the IPWM power cycling, which are adjusted by the equivalent method, are close to the corresponding PWM power cycling within 0.4 °C, reaching the equivalent principles. Therefore, the equivalent method proposed in this article is effective. So IPWM power cycling can be regarded as the corresponding PWM power cycling. Noting that the calculation time reduces hugely in IPWM power cycling.

## V. SIMULATION RESULTS AND DISCUSSION

For effective comparison, the control variates method is applied to set the simulation groups, as shown in Table IV. Group1 is DC power cycling with load current $I_L$ is 200 A, but the heating time $t_{\mathrm{ON}}$ is 0.1 and 1 s, respectively. In order to explore the influence of switching frequency $f_{\mathrm{sw}}$ on the junction temperature in PWM power cycling, Group 2 with four IPWM power cycling is set, which is equivalent to the PWM power cycling with load current $I_L = 200$ A, the same as DC power cycling. Furthermore, the heating time $t_{\mathrm{ON}}$ of IPWM1 and IPWM 2 is 0.1 s, which is the same as dc1 but with a different switching frequency. Therefore, comparing dc1 with IPWM1 and IPWM2 can easily obtain the effects of the switching frequency on junction temperature. As well as comparing dc2 with IPWM3 and IPWM4. And the effects of the heating time $t_{\mathrm{ON}}$ can also be investigated in Group1 or Group2. To distinguish the difference in the temperature distribution which may be caused by switching losses between DC and PWM power cycling, the junction temperature swing $\Delta T_j$ and maximum junction temperature $T_{j\max}$ should be controlled the same for $\Delta T_j$ and $T_{j\max}$ have an influence on the temperature distribution. So $t_{\mathrm{ON}}$ and $I_{\mathrm{load}}$ of DC power cycling are adjusted in Group3 to reach the same $\Delta T_j$ and $T_{j\max}$ with corresponding IPWM power cycling in Group2.

TABLE IV
SIMULATION CONDITIONS AND RESULTS OF THE SINGLE-CHIP MODEL

| Group | Types | $t_{on}$ /(s) | $f_{sw}$ /(kHz) | $I_{load}$ /(A) | $T_a$ /(°C) | $\Delta T_j$ /(K) | $T_{jmax}$ /(°C) |
|---|---|---|---|---|---|---|---|
| Group 1 | DC1 | 0.1 | / | 200 | 30 | 49.24 | 147.78 |
| | DC2 | 1 | / | 200 | 30 | 79.93 | 164.13 |
| Group 2 | IPWM1 | 0.1 | 1 | 205.91 | 33.09 | 35.57 | 112.79 |
| | IPWM2 | 0.1 | 5 | 206.03 | 31.57 | 36.40 | 150.07 |
| | IPWM3 | 1 | 1 | 188.70 | 35.89 | 56.49 | 125.06 |
| | IPWM4 | 1 | 5 | 195.61 | 34.12 | 63.75 | 169.78 |
| Group 3 | DC3 | 0.1 | / | 173 | 26 | 35.99 | 112.70 |
| | DC4 | 0.1 | / | 171 | 61 | 36.22 | 147.61 |
| | DC5 | 1 | / | 170 | 30 | 55.97 | 124.88 |
| | DC6 | 1 | / | 180 | 60 | 65.59 | 169.70 |

Table IV not only shows the simulation conditions but also the temperature results. Comparing the temperature between Group1 and Group2, some conclusions can be obtained as follows:

1) *The switching process of PWM power cycling will mitigate the $\Delta T_j$ comparing with DC power cycling with the same tON and $I_{load}$.*
   It can be seen that the $\Delta T_j$ of the IPWM power cycling are always smaller than that of DC power cycling, even the switching frequency reaches 5 kHz in IPWM2 and IPWM4. This is because the switching process in the PWM power cycling makes the actual heating time $t_{\mathrm{ON}}$ shorter than the DC power cycling and the reduction of the thermal resistance, so the total power losses are less than the DC power cycling. To confirm this, the power losses in the chip domain are integrated with the electromagnetic heat loss function. The results show that the power loss of dc2 is 131.89 W, while the power losses of IPWM3 and IPWM4 are 108.83 and 118.12 W, respectively. Obviously, lower power losses lead to lower temperature swing.
2) *The switching losses influence the maximum temperature $T_{jmax}$ significantly while there is only a slight influence on temperature swing $\Delta T_j$, especially when tON is small.*

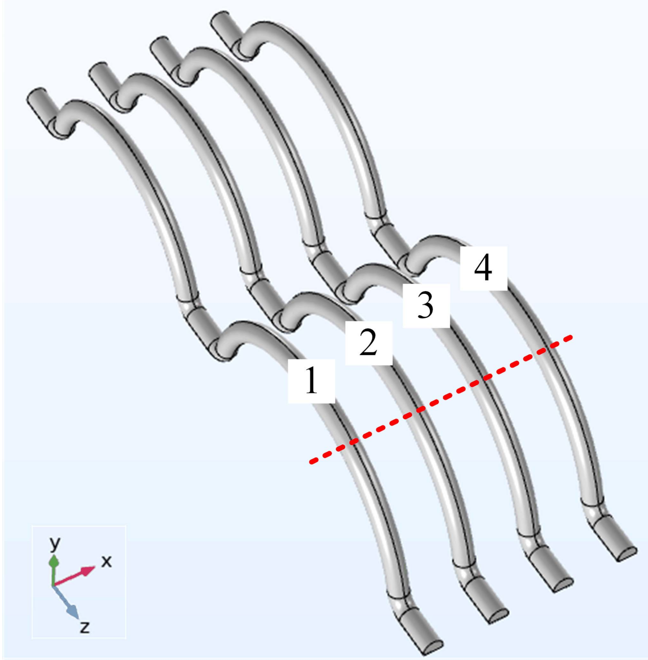


Fig. 14. Section at the highest point of the bond wire.

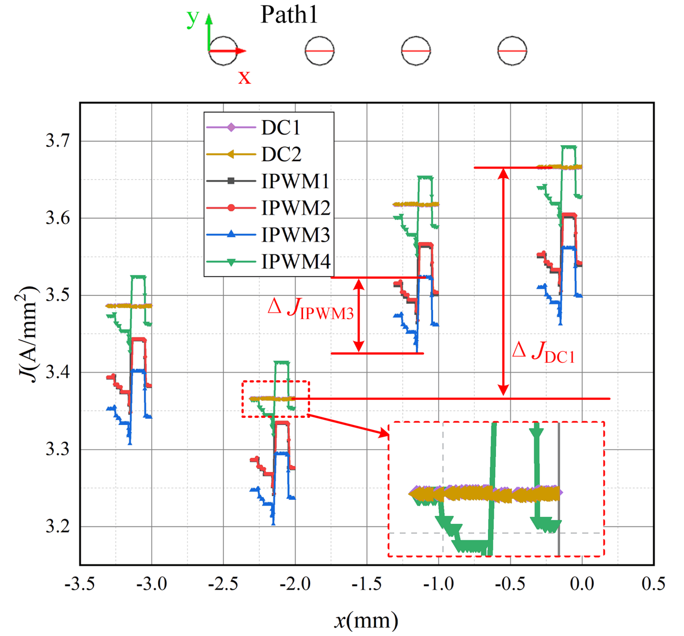


Fig. 15. Value of the current density along path 1 in the section of the bond wire.

Comparing IPWM1 and IPWM2 whose $t_{ON}$ both are 0.1 s, the $\Delta T_j$ of IPWM2 with switching frequency is 5 kHz is only higher than that of IPWM1 with 0.83 °C. However, when $t_{ON}$ is increased to 1 s, at the same switching frequency, the $\Delta T_j$ of IPWM4 is 7.26 °C higher than that of IPWM3 with switching frequency is 1 kHz. Different from $\Delta T_j$, $T_{j\max}$ is increased significantly with increasing the switching frequency regardless of the $t_{ON}$. Therefore, the conclusion can be obtained that $T_{j\max}$ is more sensitive to switching frequency than $\Delta T_j$.

In other words, IPWM power cycling is more difficult to get the high $\Delta T_j$ than DC power cycling as $t_{ON}$ and $I_{\text{load}}$ are the same. But a high $T_{j\max}$ is easy to be obtained by increasing the switch frequency $f_{\text{sw}}$.

### A. Current Distribution

This part analyzes the current distribution from the electrical perspective. The main purpose is to explore the differences in the current distribution between DC and PWM power cycling, especially the wire bond. Because the phenomenon of the "skin effect" or "proximity effect" [33] always occurs in parallel wires with varying currents, leading to heat congregation on the bond wire.

Therefore, the cross-section of the highest loop of the bond wire is taken as shown in Fig. 14, and the bond wires are successively numbered 1, 2, 3, and 4 along the positive direction of the $x$-axis.

Fig. 15 shows the current density modulus along path 1 in the bond wire cross-section. In DC power cycling, the current density modulus data points of dc1 and dc2 are almost overlapped, which means the current density along path 1 is the same as long as the load current is the same in DC power cycling. In IPWM power cycling, the current distribution with different frequencies is consistent, as Fig. 15 shows. There is no indication that there has a phenomenon of "skin effect" or "proximity effect" where the current density is concentrated on the surface or a certain side surface.

From Fig. 15, the difference between the maximum value and the minimum value of the current density modulus of a single bond wire can be extracted. Taking bond wire 3 of IPWM3 as an example, the difference $\Delta J_{\text{IPWM3}}$ is $9 \times 10^6$ (A/mm$^2$). Assuming that the current density on the wire bond is uniformly distributed with the maximum and minimum values, respectively, the current difference can be obtained as follows:

$$\Delta I_{\text{IPWM3}} = \Delta J_{\text{IPWM3}} \cdot \pi r^2 = 9 \times 10^6 \cdot \pi \cdot \left(0.15 \times 10^{-3}\right)^2 = 0.6359\,(\text{A}). \quad (1)$$

$r$ is the bond wire radius with 150 $\mu$m. As the rated current of each bond wire is 25 A, the difference with 0.6359 A is so small that the inhomogeneous current density distribution on the bond wire caused by the changing of the current amplitude in the IPWM power cycling can be ignored.

In addition, whether in DC power cycling or IPWM power cycling, the basic distribution phenomenon of the current density modulus on the bond wire is the same: the current density of the bond wire 4 is the largest, followed by 3 and 1, and the current density of the bond wire 2 is the smallest. That is because the material of the bond wire is aluminum whose resistivity has a positive temperature coefficient. The lower temperature of the edge bond wire, the smaller resistance it has. Therefore, bond wire 4 gets more current than 2 and 3, and bond wire 1 should get the minimal current. However, bond wire 1 is in the shortest path of current flow, most of the current will flow through bond wire 1. So bond wire 1 gets more current than 2 even the temperature of bond wire 1 is higher.

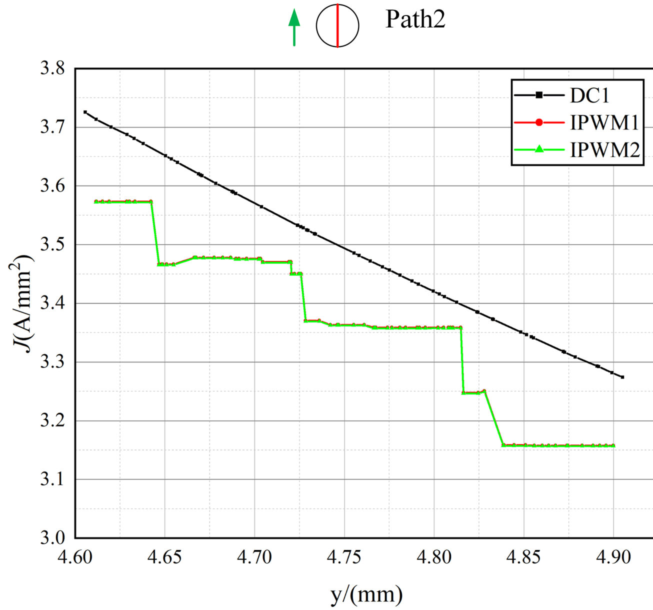


Fig. 16. Value of the current density modulus along path 2 in the section of the first bond wire.

As for the current difference between the bond wires, from Fig. 15, the current density modulus difference between wire bond 2 and wire bond 4 of dc1 power cycling $\Delta J_{\mathrm{dc1}}$ is $3 \times 10^7$ (A/mm$^2$). Assuming the current density on the bond wire is evenly distributed with the current density on path 1, the current difference between wire bond 2 and wire bond 4 can be obtained as follows:

$$\Delta I_{\mathrm{dc1}} = \Delta J_{\mathrm{dc1}} \cdot \pi r^2 = 2.1195\,(\mathrm{A}). \tag{2}$$

Considering that the resistance of the bond wire is about 6–15 mΩ [21], the power loss difference of the wire bond is $\Delta P = I^2 * R = 0.0674$ W, so it can be considered that the influence of the current difference between the four bond wires can be ignored.

Fig. 16 shows the current density along Path 2 on the bond wire1 section. The curve of IPWM1 almost coincides with IPWM2 even though the switching frequency of IPWM2 is higher than that of IPWM1. The current density of IPWM1 and IPWM2 on path 2 shows a downward trend but is not linear while that of dc1 decreases linearly as the $y$ increases. Therefore, it can be concluded that whether in DC or IPWM power cycling, the current is mainly concentrated on the lower surface at the cross-section at the highest loop of the bond wire. In other words, the current always tends to flow in the shortest path which can also be confirmed by Fig. 17, Which shows a longitudinal cross-sectional view of the bond wire1. The current density of point $F$ which locates on the shortest path of current is larger than that of point $C$.

In conclusion, there exist some differences between DC and IPWM power cycling in the current distribution of a bond wire. However, it is so small that could be ignored. As for the current distribution of the bond wires, the trend is exactly the same without current concentration, irrespective of DC power cycling or IPWM power cycling.

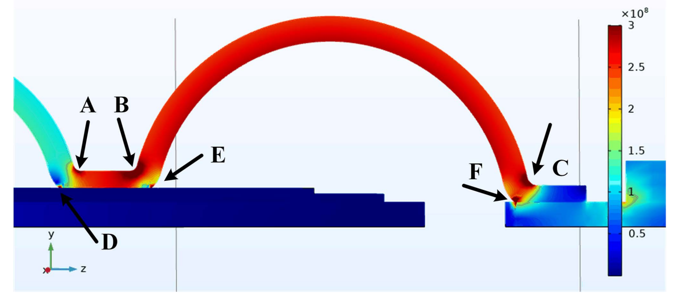


Fig. 17. Value of the current density in the longitudinal cross-section of the first bond wire.

### B. Temperature Distribution

Analysis of temperature distribution between DC and IPWM power cycling is the most crucial, as it is highly related to its reliability. The thermal stress caused by the mismatch of the coefficient of thermal expansion (CTE) of the materials of each layer under temperature swing results in the failure of the module [10]. So it is widely accepted that failure often happens in places where the material properties differ greatly and the temperature fluctuates greatly. Such as the chip surface and Al wire bond connection interface. Therefore, it is necessary to focus on the temperature distribution of the chip surface as well as the bond foot.

Furthermore, the temperature distribution is itself an accelerated factor for the failure mechanisms like bond wire lift-off, and cracks/voids in the die solder joint [34]. To make a reasonable and fair comparison, the temperature distribution of DC and IPWM power cycling should be under the same $\Delta T_j$ and $T_{j\max}$ to prevent the influence of the different $\Delta T_j$ and $T_{j\max}$. Therefore, the load currents of Group3 are adjusted so that it has a similar $\Delta T_j$ and $T_{j\max}$ as Group2. For the convenience of analysis, the simulation is subdivided into four small groups of a, b, c, and d, according to the different $\Delta T_j$ and $T_{j\max}$, as shown in Fig. 18.

Mirroring the model along the central axis of symmetry, the result of the complete model can be gained. Fig. 18 shows the result of the temperature distribution after mirroring the surface of the chip. It can be seen that although the $\Delta T_j$ and $T_{j\max}$ of DC and IPWM power cycling are close, the maximum temperatures and their positions on the chip surface are not the same. The temperature difference in the maximum temperature of the chip surface between them in group(d) is 5.09 °C, higher than the difference in group(c)is 2.5 °C. Compared with group(a) and group(b), the temperature difference of the group with higher switching frequency is also greater. Therefore, it can be concluded that with increasing the switching frequency, the temperature difference of the maximum temperature of the chip surface between DC and IPWM power cycling is greater, which is due to the extra switching losses in IPWM power cycling.

Besides that, the maximum temperature points always appear around the central bond wire in DC power cycling simulation, irrespective of the heating time ton. However, the maximum temperature points of IPWM power cycling mostly appear at the central region of the chip, except the IPWM3. That is because the switching loss of 1 KHz has little influence on the temperature distribution. Therefore, the conclusion can be obtained that as

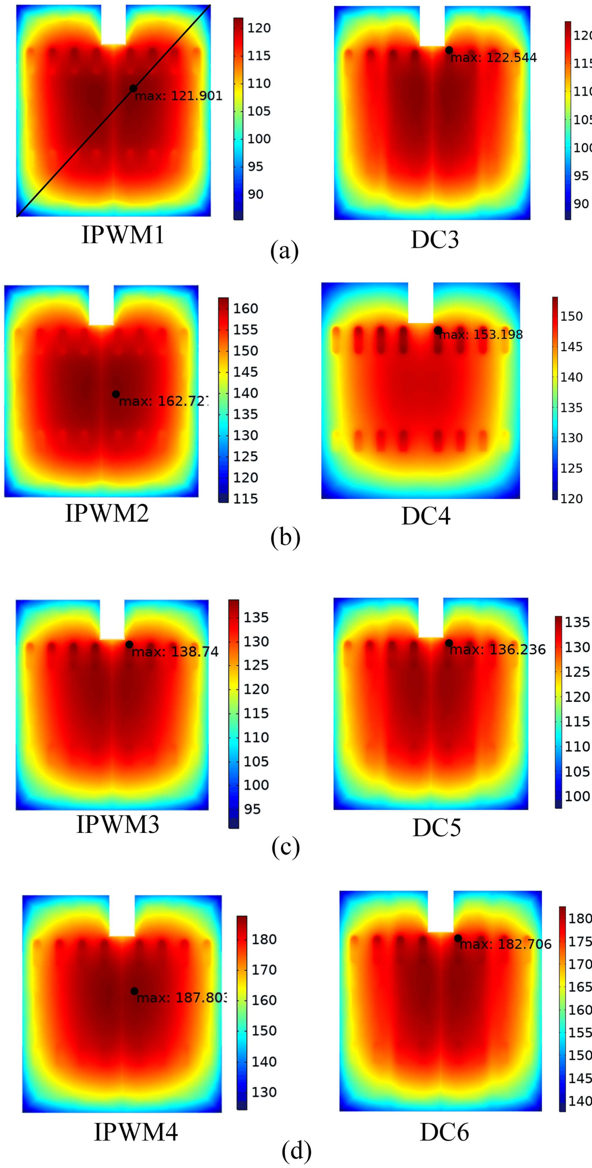


Fig. 18. Temperature results of the chip surface in the DC and IPWM power cycling.

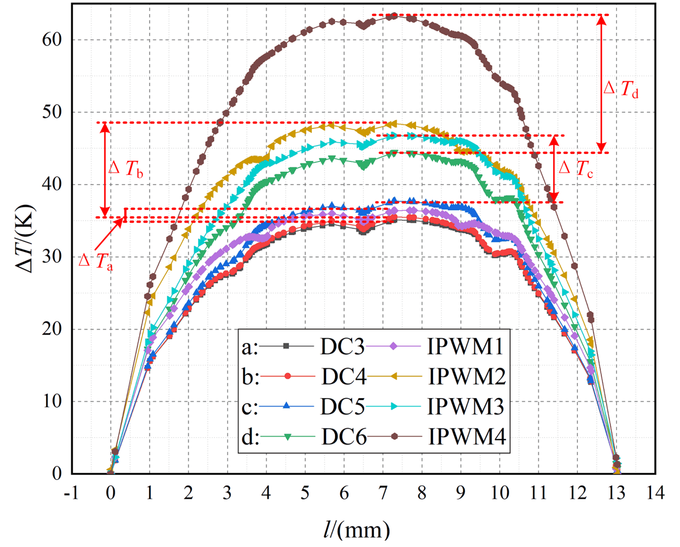


Fig. 19. Temperature distribution curves of the chip surface in DC and IPWM power cycling.

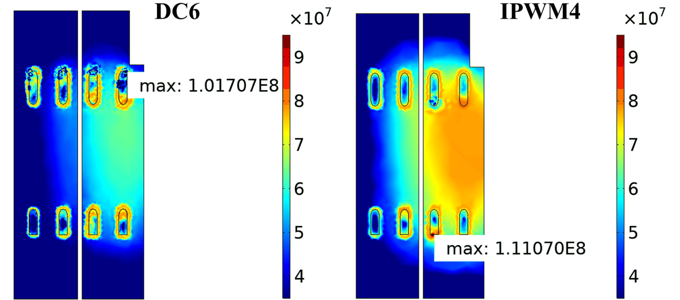


Fig. 20. Thermal stress distribution of the metallization layer in DC6 and IPWM4 power cycling.

the switching frequency increase, the temperature is more, and more concentrated in the center of the chip.

Fig. 19 shows the temperature extracted from the diagonal of the chip and subtracted from the minimum temperature on the diagonal. It is obvious that the curve of the IPWM power cycling is always higher than the DC power cycling in the same group (group a, b, c, d). The data shows that the maximum values on the temperature distribution curves of the IPWM1 and IPWM2 power cycling simulations are larger than the dc3 and dc4 power cycling with $\Delta T_a = 1.31$ K and $\Delta T_b = 12.9$ K, respectively, $t_{\rm ON}$ both are 0.1 s. When $t_{\rm ON}$ is 1 s, the maximum values on the temperature distribution curves of the IPWM3 and IPWM4 power cycling simulations are larger than the dc5 and dc6 power cycling with $\Delta T_c = 9.08$ K and $\Delta T_d = 18.63$ K, respectively.

It means that the lateral temperature distribution on the chip surface of the IPWM power cycling is more inhomogeneous than DC power cycling. However, the real temperature gradient may not be as large as shown above because of the thermal coupling from the other chips, which can be verified from the simulation results in literature [35].

### C. Thermal Stress Distribution

The module is subjected to thermal stress during power cycling, resulting from repeated expansion and contraction. Apparently, the failure mechanism of the module can be found more directly by thermal stress analysis. Note that the failure usually occurs on the bond wire and solder layer. Therefore, the stress distributions of the aluminum metallization layer surface and the solder layer surface which contains the chip solder layer and system solder layer are the main analytic objects.

Taking the stress distribution of group (d) (dc6 and IPWM4) as an example, which has the greatest difference in temperature distribution. Figs. 20 and 21 show the stress distribution of the aluminum metallization layer and chip solder layer separately when the junction temperature is maximum, and Fig. 22 shows the stress distribution of the system solder layer surface.

Obviously, the maximum thermal stress of IPWM4 power cycling is always higher than dc6 power cycling. That is because the temperature gradient of IPWM4 is higher than dc6. But the thermal stress difference is relatively small. Besides, as the temperature is more concentrated in the center, the stress of the center is higher by comparing the dc6 and IPWM4 in Fig. 20.

Fig. 21. Thermal stress distribution of the chip solder layer in DC6 and IPWM4 power cycling.

Fig. 22. Thermal stress distribution of the system solder layer in DC6 and IPWM4 power cycling.

But there is no doubt that the stress around the contact surface of the bond wire will be greater as there has the maximum CTE mismatch, and that is where the maximum stress appears, whether it is DC or IPWM power cycling.

In addition, it should be noted that the thermal stress on the chip solder layer surface is maximum, which means that the solder layer is mostly the failure position both in dc6 and IPWM 4 power cycling. And the maximum stress point appears at the joint edge of the solder layer and the silicon chip. This conclusion is consistent with the experimental conclusion [36].

Above all, due to the lateral temperature gradient of IPWM is larger than DC power cycling with the contribution of switching losses, the module is subjected to higher thermal stress, but with the same magnitude, and the failure locations are the same. As for the numerical difference, it may be smaller in practice, because in actual operation, the temperature distribution is more uniform due to the thermal coupling. Therefore, it can be concluded that as long as the temperature condition with $\Delta T_j$ and $T_{j\max}$ of the module is consistent, whether it is DC or IPWM power cycling, the failure mechanism and lifetime of the module can be considered the same.

## VI. Experimental Results

DC PCT is carried out on the three-phase DC power cycle test bench, which has been described in our previous article [37]. The PWM PCT bench is shown in Fig. 23. In order to obtain a similar temperature profile using the same junction temperature measurement method—$V_{\mathrm{CE}}(T)$ method, an improved and simplified control strategy and test circuit are used in this article, as shown in Fig. 24(a). The current amplitude is rated by the resistive load, but with a PWM waveform. That is because the gate signal with a PWM waveform is applied to the DUT, and a signal opposite to PWM is applied to the control switch 1 to make sure a current flow path when DUT is switched OFF. And control switch 2 is used to cutoff the load current flow path during the cooling time and ensure all the measurement current $I_m$ flow through the DUT, the sequence of the control is shown in Fig. 24(b). A discrete silicon device with one bond wire from Infineon is selected as the DUTs, and six devices for DC PCT while two devices for PWM PCT. Since the temperature is the most important factor affecting the lifetime, especially temperature swing $\Delta T_j$ and maximum temperature $T_{j\max}$. Therefore, the

Fig. 23. Test bench of PWM PCT.

Fig. 24. Test circuit of PWM PCT. (a) Test circuit topology. (b) Sequence of the control.

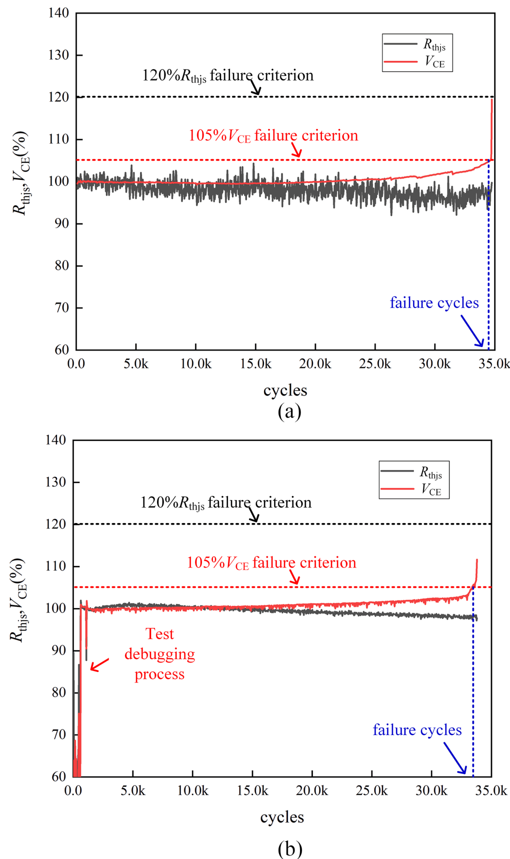


Fig. 25. Changing trends of $R_{\rm thjs}$ and $V_{\rm CE}$ during the PCTs. (a) DC PCT. (b) PWM PCT.

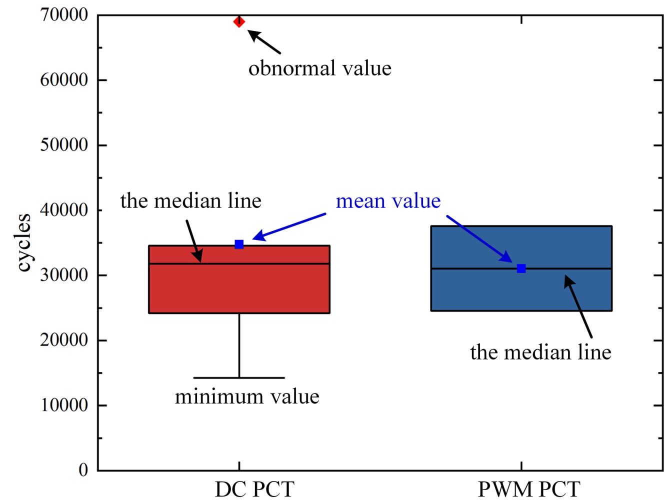


Fig. 26. Power cycling lifetime of DC PCT and PWM PCT.

test temperature conditions of DC and PWM power cycling are the same with $\Delta T_j \approx 90$K and $T_{j\max} \approx 150$ °C. Even the heating time $t_{\rm ON}$ is the same with 2 s. However, the actual heating time in PWM PCT is less than 2 s as the switch state. So the switching frequency $f_{\rm sw}$ is adjusted to increase the switching losses to achieve the same temperature condition. In this article, 10 kHz of the switching frequency is used. There is no doubt that the addition of inductor load will greatly increase the switching loss, but also bring the problem of oscillation, which affect the measurement. Therefore, only a resistance load is used in this test circuit.

As the standard failure criterion with 105% $V_{\rm CE}$ of the initial value and 120% $R_{\rm thjs}$ of the initial value applied in PCTs [4], which indicates the bond wire failure and solder layer degradation, respectively. Fig. 25 shows the changing trends of $V_{\rm CE}$ and $R_{\rm thjs}$ during DC PCT and PWM PCT. It can be seen that $R_{\rm thjs}$ decrease a little during the PCT because of the better contact of the silicon pad between DUTs and heatsink, while $V_{\rm CE}$ shows an exponential increase in the later period of PCT. And all DUTs fail with the rising of $V_{\rm CE}$. That means the bond wire is the failure point and no other failure mechanisms occur.

Since the control strategy of PWM PCT is more complex than DC PCT, some cycles are wasted at the beginning for debugging, which has a small impact on the lifetime. Even ignoring the number of cycles of the debugging process has no effect on the comparison results of the lifetime, as shown in Fig. 26. The lifetime distribution is almost the same, as well as the median line of the test lifetime data, indicating that there is no difference of lifetime between DC and PWM power cycling.

## VII. Conclusion

In this article, the principles of the DC PCT and PWM PCT are described in detail to obtain the fundamental difference between them and provide the reference for the boundary condition settings of the simulation model. After establishing the single-chip model, IPWM power cycling is proposed to equivalent the PWM power cycling considering the difficulties of the normal PWM power cycling simulation, which can effectively decrease calculation memory and shorten simulation time. And the equivalence of the IPWM power cycling is verified by the electrothermo simulation with a simple model.

The simulation results show that the switching process of the PWM power cycling will mitigate the $\Delta T_j$ compared with DC power cycling. And switching losses have a significant influence on $T_{j\max}$ while having little effect on $\Delta T_j$. Furthermore, the simulation results in current distribution, temperature distribution, and stress distribution between DC power cycling and IPWM power cycling are compared and analyzed. The conclusions from the simulation results can be drawn as follows:

1) There is no difference in the current distribution of the bond wire between the DC and PWM power cycling, which means the phenomenon of “skin effect” or “proximity effect” has not happened on the bond wire in IPWM power cycling. The current always tends to flow in the shortest path whether in DC power cycling or IPWM power cycling.
2) The switching loss in the IPWM power cycling causes the temperature to be concentrated in the center of the chip, resulting in the temperature distribution of the chip surface is more inhomogeneous than that in DC power cycling. But the temperature gradient will be smaller in the real module because of the thermal coupling from the other chips.

3) Chip solder layer is the place which has the greatest thermal stress, and the maximum stress points are all at the edge of the solder layer with the same magnitude. That means whether DC or IPWM power cycling, the edge of the chip solder layer will be the main failure region in a power module.

Finally, the experiments of DC PCT and PWM PCT are carried out. The same failure mode and the closer lifetime of DUTs, shown in Section VI, verify the conclusion that there is no difference between DC power cycling and PWM power cycling.

This article deeply analyses the difference between DC and PWM power cycling based on FE simulation. As no difference has been found indicating that DC power cycling is absolutely enough to assess the aging of the power module. But only the IGBT power devices is investigated, the influence of different power cycling method on SiC MOSFET devices needs further studying. And with the development of advanced chip or package technology, DC power cycling is more and more limited to testing the devices with low ON-resistance or low thermal resistance, therefore a novel DC power cycling is required, which is the focus of future article.

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